osmo-clock-gen - Feature #3758

design/build SI5351C based clock generator boards

01/12/2019 09:06 PM - laforge

Status:	Resolved	**Start date:**	01/12/2019
Priority:	Normal	**Due date:**	
Assignee:	laforge	**% Done:**	100%
Category:			
Target version:			

Description

Assuming most "serious" people playing with SDRs and/or measurement technology have a 10MHz source of some sort (GPS-DO, Rubidium, or "just" a calibated OCXO), the next problem is typically how to generate the paticularl frequency that is required by a given device. By far not all devices are able to deal with a 10MHz reference, including LimeSDR-mini, RTL-SDR, to name a few.

Jack Zimmerman has designed + released an OSHW Si5351C board at https://www.jackenhack.com/si5351c-i2c-frequency-clock-generator-breakout-board/ which looks quite promising. I'm currently trying to ge a PCBA from him so we can play with it.

Should this be doing what we want from it, I think the next step is to create a slightly extended version of the board, which

- includes a small microcontroller with some firmware to drive/initialize the Si5351
- provides a UART (3.3V on osmocom-style 2.5mm jack?) and/or USB to talk to it
- contains some non-volatile storage to store settings and be able to start up autonomously with a given configuration.

If we build a small batch of those boards, the per-board price will be low enough so one can simply have "one per required output frequency" and plug them in as needed, as opposed to using an expensive, large signal generator with UI (and possibly Fan, etc.).

History

#1 - 01/12/2019 09:12 PM - laforge

See also C_Band_LNB_Ext_Ref_Mod

#2 - 01/14/2019 01:47 PM - laforge

Some related ideas, in random order:

- use SAMD11 or SAMD21 microcontroller: Small, self-contained, no external clocks, UART+USB+I2C
- offer switchable 50 ohms termination on the clock input (jumper?)
- clock input on BNC, as is common for 10MHz?
- clock outputs on SMA? some on u.fl?
- separate/adjustable LDO for [some] clock outputs? They have individual supply pins...
- pAC coupling and resistive divider / biasing or even schmitt-trigger to ensure our symmetric clock input can safely feed into the CLKIN pin which is CMOS input...
- tvs diodes on all connectors
- overvoltage / reverse polarity protection

#3 - 01/14/2019 03:30 PM - laforge

- Subject changed from build SI5351C based clock generator boards to design/build SI5351C based clock generator boards

#4 - 01/16/2019 10:02 PM - laforge

- Checklist item [ ] TVS on all clocks and digital connectors added
Checklist item [ ] define pinout of TC-2030 for SWD added
Checklist item [ ] decide on DC input jack (like mpcie-breakout?) added
Checklist item [ ] ferritte bead between analog(clock) and digital(SAMD) supply? added
Checklist item [ ] overvoltage / reverse prolarity protection added

- Status changed from New to In Progress

- % Done changed from 0 to 10

Initial incomplete design pushed to http://git.osmocom.org/osmo-small-hardware/log/?h=laforge/clock-gen

- has ATSAMD11 in QFN20 package as main processor
  - USB on mini-B jack
  - UART on 2.5mm osmocom style jack
  - SWD on TagConnect TC-2030
- SN74LVC1G04 based self-biasing clock squarer for input side

#5 - 01/25/2019 12:46 PM - laforge

- Checklist item [x] TVS on all clocks and digital connectors set to Done
Checklist item [x] define pinout of TC-2030 for SWD set to Done
Checklist item [x] decide on DC input jack (like mpcie-breakout?) set to Done
Checklist item [x] overvoltage / reverse prolarity protection set to Done

- % Done changed from 10 to 80

#6 - 01/26/2019 11:34 AM - laforge

- Checklist item [ ] add i2c/spi on a header (maybe UEXT) added

#7 - 01/26/2019 06:17 PM - laforge

- Checklist item [ ] add M3 or M2.5 mounting holes (at least three) added
Checklist item [x] add i2c/spi on a header (maybe UEXT) set to Done

#8 - 01/27/2019 05:39 PM - laforge

- Checklist item [x] ferritte bead between analog(clock) and digital(SAMD) supply? set to Done
Checklist item [x] add M3 or M2.5 mounting holes (at least three) set to Done

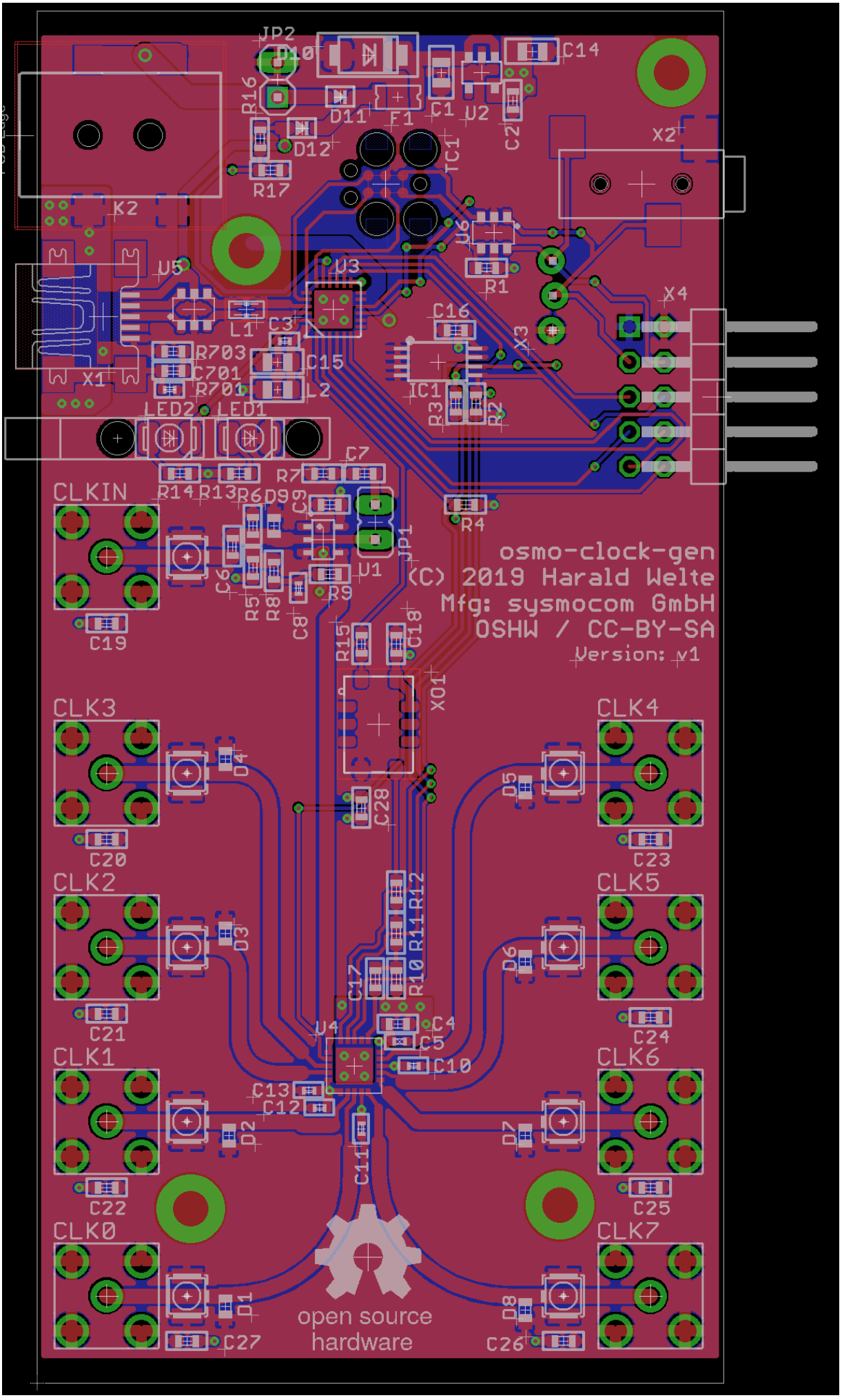
- File clock-generator.pdf added

- File clock-generator.brd.pdf added

- File osmo-clock-gen_eagle.png added

- % Done changed from 80 to 90

First version finished:


osmo-clock-gen
(C) 2019 Harald Welte
Mfg: sysmocom GmbH
OSHW / CC-BY-SA
Version: v1
CLKIN
CLK0
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
open source
hardware

#9 - 01/27/2019 05:55 PM - laforge

- Project changed from Misc Hardware Projects to osmo-clock-gen

#10 - 03/24/2019 10:37 AM - laforge

- Status changed from In Progress to Resolved

- % Done changed from 90 to 100

board v1 exist and is working according to horiz0n .

Files

clock-generator.pdf	132 KB	01/27/2019	laforge
clock-generator.brd.pdf	149 KB	01/27/2019	laforge
osmo-clock-gen_eagle.png	134 KB	01/27/2019	laforge