

Integrated Data Protocol Controller (IDPC)

SAB 79C401

ADVANCE INFORMATION

General Description

The SAB 79C401 Integrated Data Protocol Controller (IDPC) provides many of the essential building blocks for construction of a variety of communications systems. When combined with ROM, RAM, a microprocessor, and the appropriate physical layer transceiver, a complete ISDN, X.25, SNA, or similar system can be constructed.

The IDPC contains hardware and software support features for use in a single-processor environment (such as a terminal adaptor to an ISDN network) or a multi-processor application (such as a communication interface for a PC or integrated voice/data work station application). For multi-processor applications, the IDPC controls access to an external "shared" RAM which serves as a data buffer and communications area ("mailbox" concept). The IDPC arbitrates simultaneous requests for RAM access and supports an inter-processor interrupt scheme.

Functionally, the IDPC consists of four sections: Data Link Controller (DLC), Universal Synchronous/Asynchronous Receiver/Transmitter (USART), Dual-Port Memory Controller (DPMC), and Microprocessor Interface (MPI).

Data Link Controller (DLC)

The DLC is a high-speed, bit-oriented protocol processor that supports either multiplexed or non-multiplexed data transfer rates up to 2.048 Mbit/s.

The DLC provides full-duplex (simultaneous transmit and receive) data transfer between the chip's serial bus port and internal parallel bus. Through the use of a 32-byte receive FIFO, 16-byte transmit FIFO, and two external DMA channels, the DLC provides efficient movement of data to and from external memory and the serial bus port (network interface).

The DLC supports data transfers via DMA, interrupts, or polled I/O. The use of the FIFO buffers minimize interrupt latency and frequency of interrupts.

Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The IDPC contains a built-in USART for exchanging data between terminals and the ISDN network in applications where there is no host processor. The USART provides a superset of 8250 UART features and supports both synchronous and asynchronous serial communications. The USART is capable of full-duplex operation at speeds up to 56 bit/s using an internal programmable baud rate generator (or optional external clock sources).

The USART supports the following functions

- Program-selectable synchronous/asynchronous modes
- Software reset
- Line break recognition and generation
- Special character recognition
- Selectable stop bits (1-, 1.5-, or 2-stop bits)
- Full modem control handshake lines (RTS, CTS, DSR, and DTR)
- "Local Loopback" and "Stick Parity" test features

Dual-Port Memory Controller (DPMC)

The DPMC provides RAM access control and an inter-processor interrupt mechanism that permits two processors to share common RAM memory without the expense of dual-port RAM. These features are used in developing network interface applications for PCs and Integrated Voice/Data Workstations (IVDWs).

Microprocessor Interface (MPI)

The MPI consists of an 8-bit non-multiplexed data bus that allows the IDPC to function with a 12.5-MHz 80188 processor (or other similar microprocessor) with zero wait states.

Features**● Data Link Controller**

- Full featured bit-oriented communication controller supporting HDLC, SDLC, LAPB, LAPD, and DMI
- Data transfer rate: 2.048 Mbit/s
- 32-byte receive FIFO and 16-byte transmit FIFO with programmable thresholds and DMA handshakes
- Multiple (four plus broadcast) address recognition modes
- Multiplexed serial interface with up to thirty-one 8-bit channels or non-multiplexed serial interface
- Local and remote loopback modes
- Transparent mode
- 56 kbit/s mode

● USART

- Superset of Industry-Standard 8250 UART features
- 4-byte transmit/receive FIFOs
- Special character recognition (up to 128 programmable)
- Synchronous mode provides a transparent serial data path
- Local loopback mode

● Dual-Port Memory Controller

- Memory bus arbitrator provides dual-port access to standard low-cost static RAM
- Programmable inter-processor interrupts support RAM-based inter-processor mailbox

● Microprocessor Interface

- 8-bit non-multiplexed data bus
- Operates with 12.5-MHz 80188 processor with zero wait states

● General Features

- Compatible with PSB 79C30 DSC
- CMOS technology, single +5-V supply
- Power-down mode
- 68-pin PL-CC