High-Level Serial Communication Controller Extended (HSCX)

SAB 82525
SAB 82526
SAF 82525
SAF 82526

Preliminary Data

CMOS IC

Type	Ordering Code	Package
SAB 82525 N	Q67100-H8590 A401	PL-CC-44 (SMD)
SAB 82526 N	Q67100-H6111	PL-CC-44 (SMD)
SAF 82525 N	Q67100-H6057	PL-CC-44 (SMD)
SAF 82526 N	Q67100-H6129	PL-CC-44 (SMD)

The SAB 82525 is a High-Level Serial Communications Controller compatible to the SAB 82520 HSCC with extended features and functionality (HSCX).

The SAB 82526 is pin and software compatible to the SAB 82525, realizing one HDLC channel (channel B).

The HSCX has been designed to implement high-speed communication links using HDLC protocols and to reduce the hardware and software overhead needed for serial synchronous communications.

Due to its 8-bits demultiplexed adaptive bus interface it fits perfectly into every SIEMENS/ INTEL or Motorola 8- or 16-bit microcontroller or microprocessor system. The data throughput from/to system memory is optimized transfering blocks of data (usually 32 bytes) by means of DMA or interrupt request. Together with the storing capacity of up to 64 bytes in on- chip FIFO's, the serial interfaces are effectively decoupled from the system bus which drastically reduces the dynamic load and reaction time of the CPU.

The HSCX directly supports the X.25 LAP B, the ISDN LAP D, and SDLC (normal response mode) protocols and is capable of handling a large set of layer-2 protocol functions independently from the host processor.

Furthermore, the HSCX opens a wide area for applications which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications) by its programmable telecom-specific features.

The HSCX is fabricated using SIEMENS advanced ACMOS 3 technology and available in a PL-CC-44 pin package.

Features

Serial Interface

- Two independent full-duplex HDLC channels (SAB 82526: one channel)
  - On chip clock generation or external clock source
  - On chip DPLL for clock recovery for each channel
  - Two independent baudrategenerators (SAB 82526: one baudrate generator)
  - Independent time-slot assignment for each channel with programmable time-slot length (1 - 256 bit)
- Different modes of data encoding
- Modem control lines (RTS, CTS, CD)
- Support of bus configuration by collision resolution
- Programmable bit inversion
- Transparent receive/transmit of data bytes without HDLC framing
- Continuous transmission of 1 to 32 bytes possible
- Data rate up to 4 Mbit/s

Protocol Support

- Various types of protocol support depending on operating mode
  - Auto mode
  - Non auto mode
  - Transparent mode
- Handling of bit oriented functions in all modes
- Support of LAPB/LAPD/SDLC/HDLC protocol in auto mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable timeout and retry conditions
- Programmable maximum packet size checking

µP Interface

- 64 byte FIFO's per channel and direction
- Storage capacity of up to 17 short frames in receive direction
- Efficient transfer of data blocks from/to system memory by DMA or interrupt request
- 8-bit demultiplexed or multiplexed bus interface
- Intel or Motorola type MP interface

General

- Compatible to SAB 82520 (HSCC)
- Advanced CMOS technology
- Low power consumption: active 25 mW at 4 MHz
  standby 4 mW

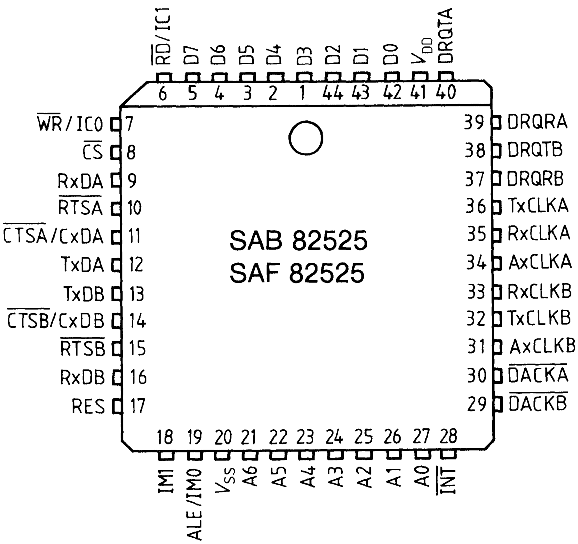
The data link controller handles all functions necessary to establish and maintain an HDLC data link, such as

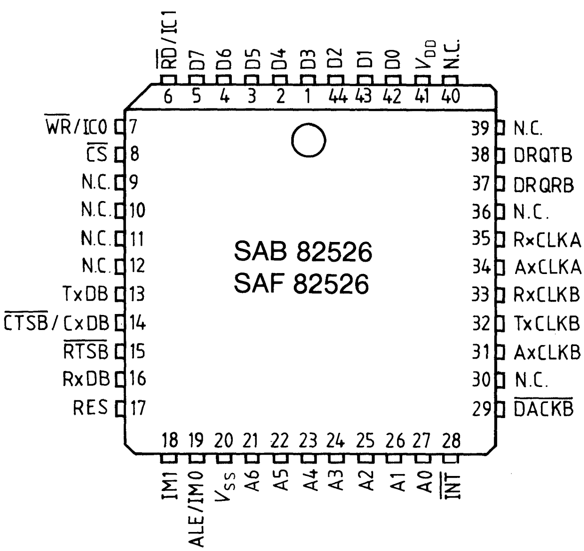
- Flag insertion and detection,
- Bit stuffing,
- CRC generation and checking,
- Address field recognition.

Associated with each serial channel is a set of independent command and status registers (SP-REG) and 64-byte deep FIFO's for transmit and receive direction.

DMA capability has been added to the HSCX by means of a 4-channel DMA interface (SAB 82525) with one DMA request line for each transmitter and receiver of both channels.

Pin Configurations
(top view)





Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
42 43 44 1 2 3 4 5	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Data Bus** The data bus lines are bidirectional threestate lines which interface with the system's data bus. These lines carry data and command/status to and from the HSCX.
6	$\overline{RD}$/IC1	I	**Read**, Intel bus mode, IM1 connected to low This signal indicates a read operation. When the HSCX is selected via CS the read signal enables the bus drivers to put data from an internal register adressed via A0-A6 on the data bus. When the HSCX is selected for DMA transfers via DACK, the RD signal enables the bus driver to put data from the respective receive FIFO on the data bus. Inputs to A0-A6 are ignored. **Input Control 1,** Motorola bus mode IM1 connected to high. If Motorola bus mode has been selected this pin serves either as E = Enable, active high (IM0 tied to low) or DS = Data Strobe, active low (IM0 tied to high) input (depending on the selection via IM0) to control read/write operations.
7	$\overline{WR}$/IC0	I	**Write**, Intel bus mode This signal indicates a write operation. When CS is active the HSCX loads an internal register with data provided via the data bus. When DACK is active for DMA transfers the HSCX loads data from the data bus on the top of the respective transmit FIFO. **Input Control** Motorola bus mode In Motorola bus mode, this pin serves as the R/W input to distinguish between read or write operations.
8	$\overline{CS}$	I	**Chip Select** A low signal selects the HSCX for a read/write operation.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
9 16	$\overline{\text{RXDA}}$ $\overline{\text{RXDB}}$	I	**Receive Data** (channel A/channel B) Serial data is received on these pins at standard TTL or CMOS levels.
10 15	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O	**Request to Send** (channel A/channel B) When the RTS bit in the mode register is set, the RTS signal goes low. When the RTS i reset, the signal goes high if the transmitter has finished and there is no further request for a transmission. In a bus configuration, this pin can be programmed via CCR2 to: – go low during the actual transmission of a frame shifted by one clock period, excluding collision bits – go low during the reception of a data frame – stay always high (RTS disabled).
11 14	$\overline{\text{CTSA}}$/ CXDA $\overline{\text{CTSB}}$/ CXDB	I	**Clear to Send** (channel A/channel B) A low on the CTS inputs enables the respective transmitter. Additionally, an interrupt may be issued if a state transition occurs at the CTS pin (programmable feature). If no "Clear To Send" function is required, the CTS inputs can be connected directly to GND. **Collision Data** (channel A/channel B) In a bus configuration, the external serial bus must be connected to the respective CxD pin for collision detection.
12 13	TXDA TXDB	O	**Transmit Data** (channel A/channel B) Transmit data is shifted out via these pins at standard TTL or CMOS levels. These pins can be programmed to work either as push-pull, or open drain outputs supporting bus configurations.
17	RES	I	**RESET** A high signal on this input forces the HSCX into the reset state. The HSCX is in power-up mode during reset and in power-down mode after reset. The minimum pulse width is 1.8 ms.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
18	IM 1	I	**Input Mode 1** Connecting this pin to either V_{SS} or V_{DD} the bus interface can be adapted to either SIEMENS/INTEL or Motorola environment. IM1 = LOW: Intel bus mode IM1 = HIGH: Motorola bus mode
19	ALE/IM0	I	**Address Latch Enable** (Intel bus mode) A high on this line indicates an address on the external address/data bus, which will select one of the HSCX's internal registers. The address is latched by the HSCX with the falling edge of ALE. This allows the HSCX to be directly connected to a CPU with multiplexed address/data bus compatible to SAB 82520 HSCC. The address input pins A0-A6 must be externally connected to the data bus pins (D0-D6 for 8-bit CPU's, D1-D7 for 16-bit CPU's, i.e. multiply all internal register addresses by 2). **Input Mode 0**, Motorola bus mode In Motorola Bus Mode, the level at this pin determines the function of the IC1 pin (see description of pin 6).
20	V_{SS}	I	**Ground** (0 V)
27 26 25 24 23 22 21	A0 A1 A2 A3 A4 A5 A6	I	**Address Bus** These inputs interface with seven bits of the system's address bus to select one of the internal registers for read or write. They are usually connected at A0-A6 in 8-bit systems or at A1-A7 in 16-bit systems.
28	$\overline{INT}$	O	**Interrupt Request** The signal is activated, when the HSCX requests an interrupt. The CPU may determine the particular source and cause of the interrupt by reading the HSCX's interrupt status registers. (ISTA, EXIR). $\overline{INT}$ is an open drain output, thus the interrupt requests outputs of several HSCX's can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull-up resistor.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
30 29	$\overline{\text{DACKA}}$ $\overline{\text{DACKB}}$	I	**DMA Acknowledge** (channel A/channel B) When low, this input signal from the DMA controller notifies the HSCX, that the requested DMA cycle controlled via DRQxx (pins 37-40) is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either read or write). Together with RD, if DMA has been requested from the receiver, or with WR, if DMA has been requested from the transmitter, this input works like $\overline{\text{CS}}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel. If DACKn is active, the input to pins A0-A6 is ignored and the FIFOs are implicitly selected. If the DACKn signals are not used, these pins must be connected to V_{DD}.
34 31	AxCLKA AxCLKB	I	**Alternative Clock** (channel A/channel B) These pins realize several input functions. Depending on the selected clock mode, they may supply either a – CD (= Carrier Detect) modem control or general purpose input. This pin can be programmed to functions as receiver enable if the "auto start" feature is selected (CAS bit in XBCH set). The state at this pin can be read from VSTR register, – or a receive strobe signal (clock mode 1) – or a frame synchronization signal in time-slot oriented operation mode (clock mode 5) – or, together with RxCLK, a crystal connection for the internal oscillator (clock mode 4, 6, 7, AxCLKA only).

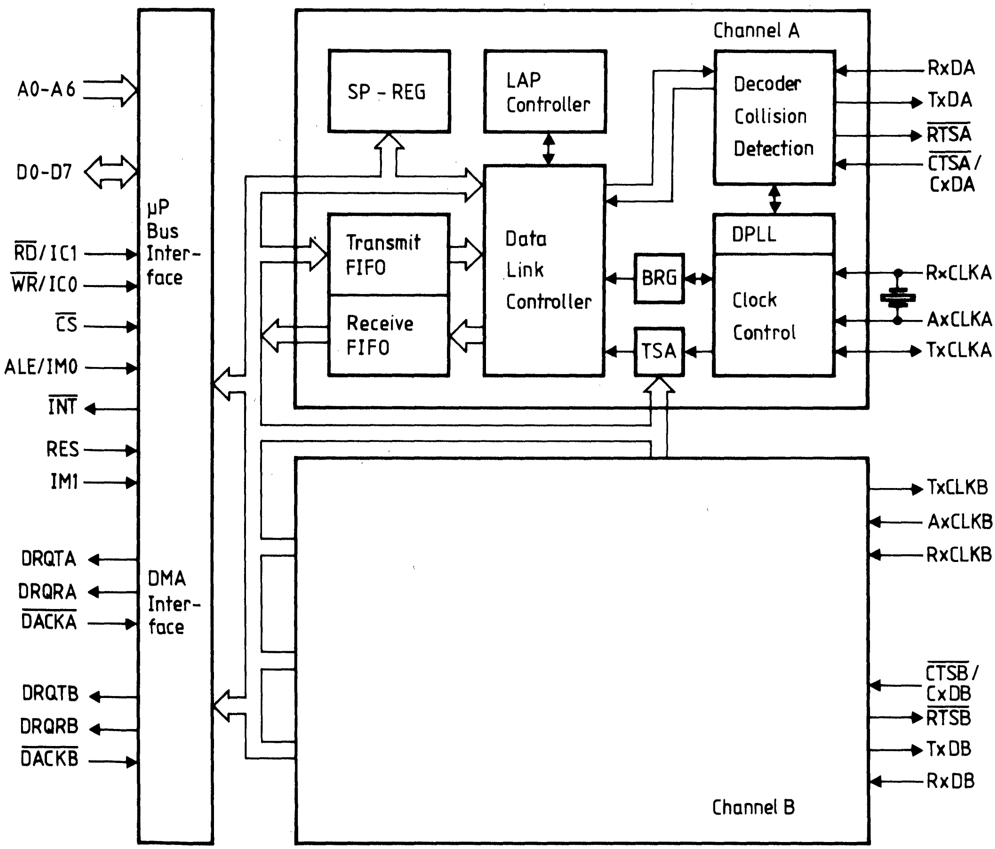
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
36 32	TxCLKA TxCLKB	I/O	**Transmit Clock** (channel A/channel B) The functions of these pins depend on the programmed clock mode, provided that the TSS bit in the CCR2 register is reset. Programmed as inputs (if the TIO bit in CCR2 is reset), they may supply either – the transmit clock for the respective channel (clock mode 0, 2, 6), – or a transmit strobe signal (clock mode 1). Programmed as outputs (if the TIO bit in CCR2 is set), the TxCLK pins supply either the – transmit clock of the respective channel which is generated either ● from the baud rate generator (clock mode 2, 6; TSS bit in CCR2 set), ● or from the DPLL circuit (clock mode 3, 7), ● or from the cristal oscillator (clock mode 4) – or a tristate control signal indicating the programmed transmit time slot (clock mode 5).
35 33	RxCLKA RxCLKB	I	**Receive Clock** (channel A/channel B) The functions of these pins also depend on the programmed clock mode. In each channel, RxCLK may supply either – the receive clock (clock mode 0) – or the receive and transmit clock (clock mode 1, 5) – or the clock for the baud rate generator (clock mode 2, 3), – or a crystal connection for the internal oscillator (clock mode 4, 6, 7, RxCLKA/B together with AxCLKA)
39 37	DRQRA DRQRB	O	**DMA Request Receiver** (channel A/channel B) The receiver of the HSCX requests a DMA data transfer by activating this line. The DRQRn remains high as long as the receive FIFO requires data transfers, thus always blocks of data (32, 16, 8 or 4 bytes) are transfered. DRQRn is deactivated immediately following the falling edge of the last read cycle.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
40 38	DRQTA DRQTB	O	**DMA Request Transmitter** (channel A/channel B) The transmitter of the HSCX requests a DMA data transfer by activating this line. The DRQTn remains high as long as the transmit FIFO requires data transfers. The amount of data bytes to be transfered from system memory to the HSCX (= byte count) must be written first to the XBCH, XBCL registers. Always blocks of data (n * 32 bytes + REST, n = 0,1,...) are transfered till the byte count is reached. DRQTn is deactivated immediately following the falling edge of the last $\overline{WR}$ cycle.
41	V_{DD}	I	Power +5 V power supply.

Block Diagram SAB 82525/SAB 82526



The HSCX SAB 82526 comprises one (channel B), the SAB 82525 two completely independent full-duplex HDLC channels (channel A and channel B), supporting various layer-1 functions by means of internal oscillator, Baud Rate Generator (BRG), Digital Phase Locked Loop (DPLL), and Time-Slot Assignment (TSA) circuits.

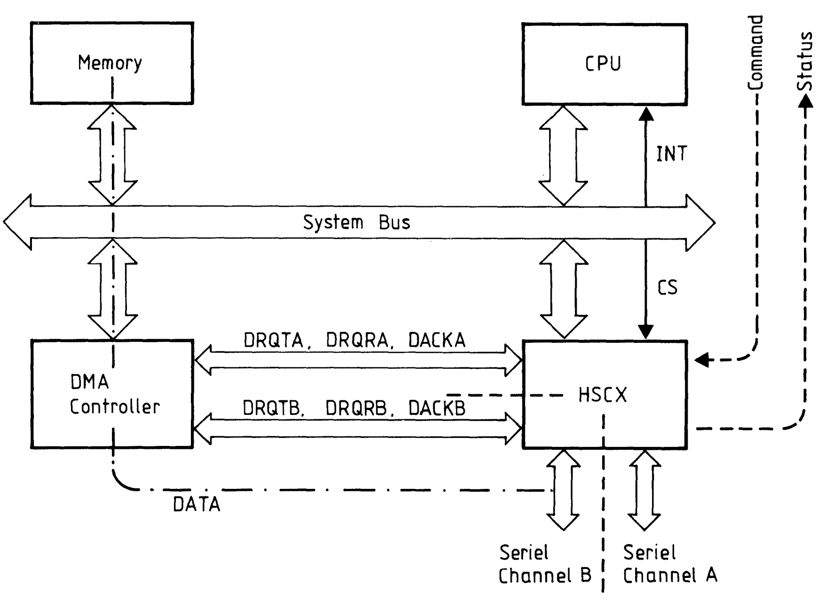
Furthermore, layer-2 functions are performed by an on-chip LAP (Link Access Procedure, e.g. LAP B or LAP D) controller.

System Integration

General Aspects

Figure 1 gives a general overview of the system integration of HSCX.

Figure 1
General System Integration of HSCX



The HSCX bus interface consists of an 8-bit bidirectional data bus (D0 – D7), seven address line inputs (A0 – A6), three control inputs ($\overline{RD}$/DS, $\overline{WR}$/R/W, $\overline{CS}$), one interrupt request output (INT) and a 4-channel DMA interface (DRQTA, DRQRA, DACKA, DRQTB, DRQRB, DACKB). Mode input pins (strapping options) allow the bus interface to be configured for either SIEMENS/INTEL or Motorola environment.

Generally, there are two types of transfers occuring via the system bus:

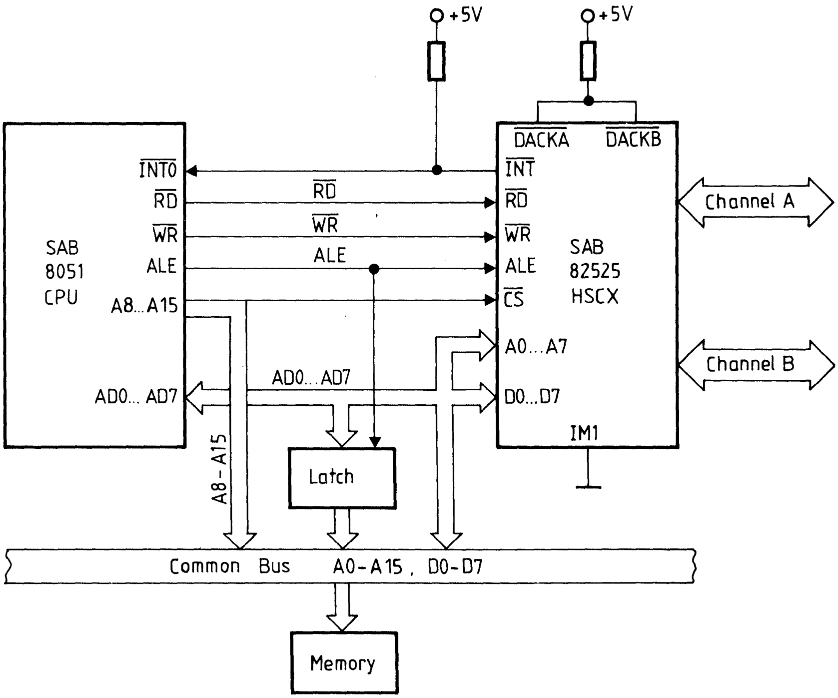
– command/status transfers, which are always controlled by the CPU. The CPU sets the operation mode (initialization), controls function sequences and gets status information by writing or reading the HSCX's registers (via $\overline{CS}$, $\overline{WR}$ or $\overline{RD}$, and register address via A0-A6).
– data transfers, which are effectively performed by DMA without CPU interaction using the HSCX's DMA interface (DMA Mode). Optionally, interrupt controlled data transfer can be done by the CPU (interrupt mode).

Specific Applications

HSCX with SAB 8051 Microcontroller

For cost-sensitive applications, the HSCX can be interfaced with a small SAB 8051 microcontroller system (without DMA support) very easily as shown in **figure 2.**

Figure 2
HSCX with 8051 CPU



Although the HSCX provides a demultiplexed bus interface, it can optionally be connected directly to the local multiplexed bus of SAB 8051 because of the internal address latch function (via ALE, compatibility to SAB 82520 HSCC).

The address lines A0 . . . A6 must be wired externally to the data lines D0 . . . D6 (direct connection) in this case.

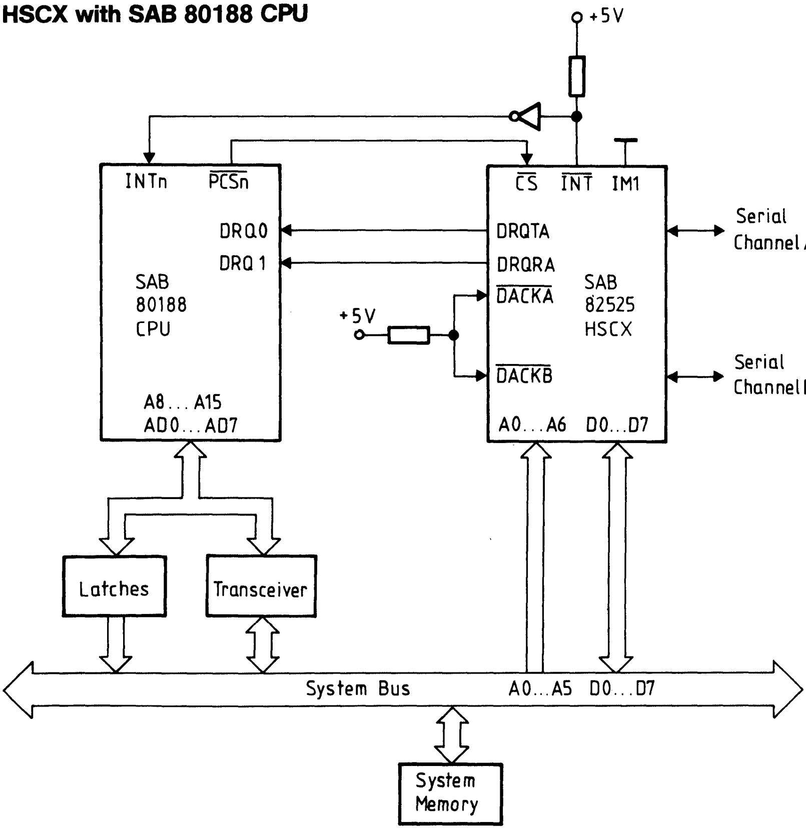
Intel bus mode is selected connecting IM1 pin to low (V_{SS}). Since data transfer is controlled by interrupt, the DMA acknowledge inputs (DACKA, DACKB) are connected to V_{DD} (+5 V).

HSCX with SAB 80188 Microprocessor

A system with minimized additional hardware expense can be with a SAB 80188 microprocessor as shown in **figure 3.**

Figure 3

HSCX with SAB 80188 CPU



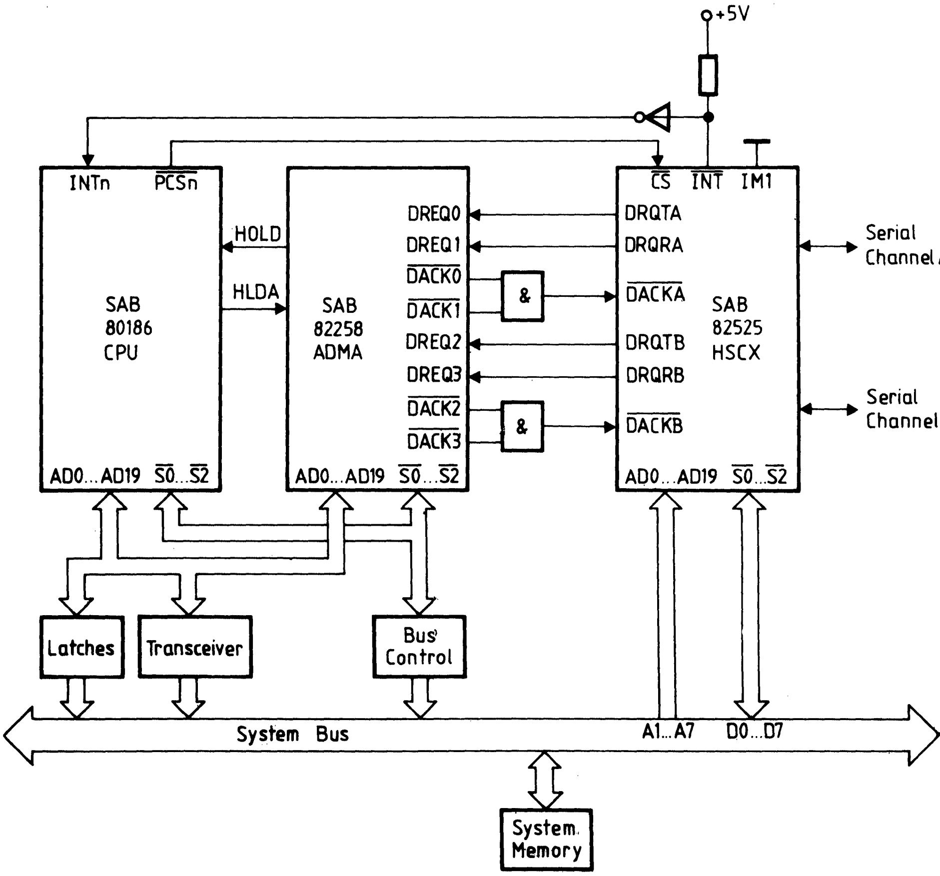
The HSCX is connected to the demultiplexed system bus. Data transfer for one serial channel can be done by the 2-channel on-chip DMA controller of the SAB 80188, the other channel is serviced by interrupt. Since the SAB 80188 does not provide DMA acknowledge outputs, data transfer from/to HSCX is controlled via CS, RD or WR address information (A0...A6) and the DACKA, DACKB inputs are not used.

This solution supports applications with a high speed data rate in one serial channel with minimum hardware expense making use of the on-chip peripheral functions of the SAB 80188 (chip select logic, interruptcontroller, DMA controller).

HSCX with SAB 80186 Microprocessor and SAB 82258 Advanced DMA Controller (ADMA)

In applications, where two high-speed channels are required, a 16-bit system with SAB 80186 CPU and SAB 82258 ADMA is suitable. This shown in **figure 4.**

Figure 4
HSCX with SAB 80186 CPU/SAB 82258 ADMA



The four selector channels of ADMA are used for serving the four DMA request sources of HSCX, allowing very high data rates at both the system bus and the serial channels.

Another big advantage of the ADMA is it's data chaining feature, providing an optimized memory management for receive and transmit data. Recording the HSCX, a linked chain of 32 byte deep buffers can be set up, which are subsequently filled with the contents of the HSCX's FIFOS during reception. Not used buffers can be saved and linked to another buffer chain reserved for the reception of the next frame.

As a result, it's not necessary to reserve a very large space in system memory, determined by the maximum frame length of every received frame.

In this example, the ADMA works directly at the CPU's local bus and shares the same bus interface logic (address latches, transceivers, bus controller) with the SAB 80186. Since one DMA acknowledge line is provided for each DMA request, two $\overline{\text{DACK}}$ outputs must be ANDed together for input to the HSCX.

The HSCX's data lines are connected to the lower half of the system data bus (D0...D7) and the address lines to A1...A7, thus (from the CPU's point of view) all internal register addresses must be multiplied by two (even register addresses only).

e.g. CMDR register: HSCX address 61_H < = > system address $C2_H$.

Functional Description

General

The HSCX distinguishes from other low level HDLC devices by its advanced characteristics. The most important are:

- Enlarged support of link configurations.

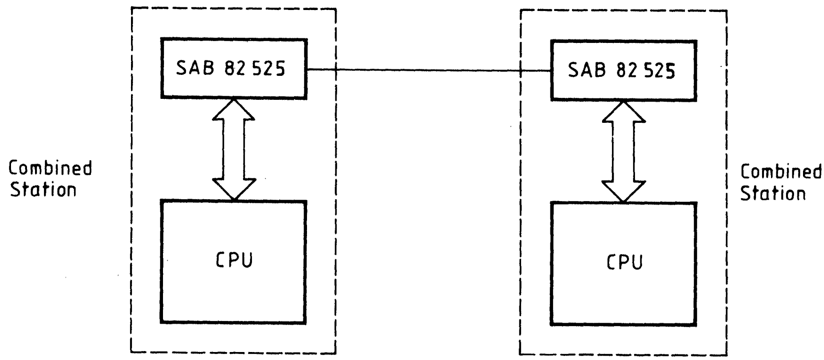
Beyond the point-to-point configurations, the HSCX directly enables point-to-multipoint or multimaster configurations without additional hardware or software expense.

In point-to-multipoint configurations, the HSCX can be used as a master as well as a slave station. Even when working as slave station, the HSCX can initiate the transmission of data at any time. An internal function block provides means of idle and collision detection and collision resolution, which are necessary if several stations start transmitting simultaneously.

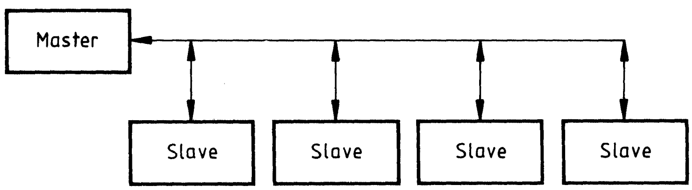
Thus also a multimaster configuration is possible.

Figure 5
Link Configuration

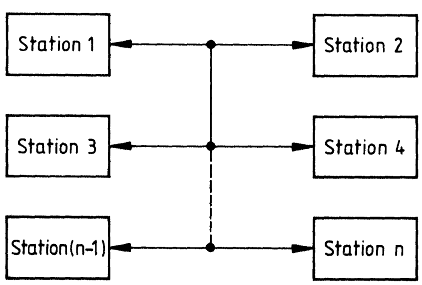
Point-to-Point Configuration



Point-to-Multipoint Configuration



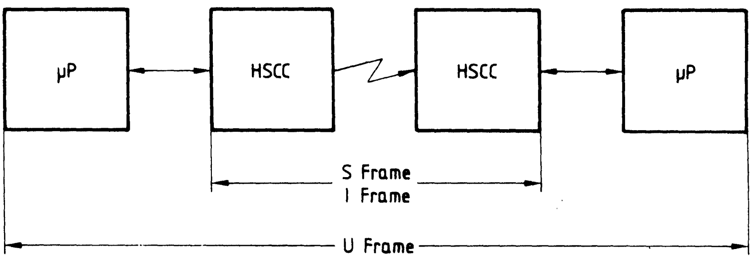
Multimaster Configuration



- Support of layer-2 functions by HSCX

Beside those bit-oriented functions usually supported with the HDLC protocol, such as bit stuffing, CRC check, flag and address recognition, the HSCX provides a high degree of procedural support. In a special operating mode (auto-mode), the HSCX processes the information transfer and the procedure handshaking (I-, and S-frames of HDLC protocol) autonomously. The only restriction is, that the window size (= number of outstanding unacknowledged frames) is limited to 1, which will be sufficient in most applications. The communication procedures are mainly processed between the communication controllers and not between the processors, thus the dynamic load of the CPU and the software expensive is largely reduced.

Figure 6
Procedural Support in Auto-Mode



The CPU is informed about the status of the procedure and has to manage the receive and transmit data mainly. In order to maintain cost effectiveness and flexibility, such functions as link setup/disconnection and error recovery in case of protocol errors (U frames of HDLC protocols) are not implemented in hardware and must be done by user's software.

- Telecomspecific features

In a special operating mode, the HSCX can transmit or receive data packets in one of up to 64 time slots of programmable width (clock mode 5). Furthermore, the HSCX can transmit or receive variable data portions within a defined window of one or more clock cycles, which has to be selected by an external strobe signal (clock mode 1). These features make the HSCX especially suitable for all applications using time division multiplex methods, such as time-slot oriented PCM systems, systems designed for packet switching, or in ISDN applications.

- FIFO buffers to efficient transfer of data packets.

A further speciality of HSCX are the FIFO buffers used for the temporary storage of data packets transfered between the serial communications interface and the parallel system bus. Also because of the overlapping input/output operation (dual- port behaviour), the maximum message length is not limited by the size of the buffer. Together with the DMA capability, the dynamic load of the CPU is drastically reduced by transfering the data packets block by block via direct memory access. The CPU only has to initiate the data transmission by the HSCX and determine the status in case of completely received frames, but is not involved in data transfers.

Operational Description

RESET

The HSCX is forced into the reset state if a high signal is input to the RES pin for a minimum period of 1.8 ms. During RESET, the HSCX is temporarily in the power-up mode, and a subset of the registers is initialized with defined values.

After RESET, the HSCX is in power down mode, and the following registers contain defined values:

Table 1
RESET Values

Register	RESET Value	Meaning
CCR1	00_H	– power down mode serial port configuration; pt-pt, NRZ coding, transmit data pins are open drain outputs – clock mode 0
CCR2	00_H	RTS pin normal function – CTS and RFS interrupts disabled no data inversion
MODE	00_H	auto mode 1 byte address field external timer mode – receivers inactive RTS output controlled by HSCX, timer resolution: k = 32.768, no testloop
STAR	48_H	XFIFO write enable receive line inactive no commands executing
ISTA EXIR	00_H	– no interrupts masked
CMDR	00_H	no commands
XBCH RBCH	00_H	– interrupt controlled data transfer (DMA disabled) – full-duplex LAPB/LAPD operation of LAP controller – carrier detect auto start of receiver disabled
XCCR RCCR	00_H	1-bit time slot

Detailed Register Description

Register Address Arrangement

Table 2
Layout of Register Addresses

ADDRESS Channel A	ADDRESS Channel B	REGISTER Read	REGISTER Write	
00 : 1F	40 : 5F	RFIFO	XFIFO	Receive/Transmit FIFO
20	60	ISTA	MASK	Interrupt STAtus/Mask
21	61	STAR	CMDR	STAtus/CoMnaD
22	62	MODE		MODE
23	63	TIMR		TIMer
24	64	EXIR	XAD1	EXtended Interrupt/Transmit ADdress 1
25	65	RBCL	XAD2	Receive Byte Count Low/Transmit ADdress 2
26	66	–	RAH1	Receive Address High 1
27	67	RSTA	RAH2	Receive STAtus/Rec. Addr. High 2
28	68	RAL1		Receive Address Low 1
29	69	RHCR	RAL2	Receive HDLC Control/Receive Addr. Low 2
2A	6A	–	XBCL	Transmit Byte Count Low
2B	6B	–	BGR	Baudrate Generator Register
2C	6C	CCR2		Channel Configuration Register 2
2D	6D	RBCH	XBCH	Reveive/Transmit Byte Count High
2E	6E	VSTR	RLCR	Version STatus/Receive frame Length Check
2F	6F	CCR1		Channel Configuration Register 1
30	70	–	TSAX	Time-Slot Assignment Transmit
31	71	–	TSAR	Time-Slot Assignment Receive
32	72	–	XCCR	Transmit Channel Capacity
33	73	–	RCCR	Receive Channel Capacity

Note: Channel A is not implemented in SAB 82526

Register Definitions

Receive FIFO (Read) RFIFO (00...1F/40...5F)

- Interrupt Controlled Data Transfer (Interrupt Mode)
  selected if DMA bit in XBCH is reset.

Up to 32 bytes of receive data can be read from the RFIFO following an RPF or an RME interrupt.

RPF Interrupt: Exactly 32 bytes to be read.
RMA Interrupt: Number of bytes to be determined by reading the RBCL, RBCH registers.

- DMA Controlled DataTransfer (DMA Mode)
  selected if DMA bit in XBCH

If the RFIFO contains 32 bytes, the HSCX autonomously requests a block data transfer by DMA activating the DRQR line as long as the start of the 32nd read cycle. This forces the DMA controller to continously perform bus cycles till 32 bytes are transfered from the HSCX to the system memory. (level triggered, demand transfer mode of DMA controller).

If the RFIFO contains less than 32 bytes (one short frame or the last of a long frame) the HSCX requests a block data transfer depending on the contents of the RFIFO according to the following table:

RFIFO Contents (Bytes)	DMA Request (Bytes)
(1) 2, 3	4
4–7	8
8–15	16
16–32	32

Additionally an RME interrupt is issued after the last byte has been transfered.

As a result, the DMA controller may transfer more bytes as actually valid in the current received frame. The valid byte count must therefore be determined reading the RBCH, RBCL registers following the RME interrupt.

Transmit FIFO (WRITE) XFIFO (00...1F/40...5F)

- Interrupt Mode
  selected if DMA bit in XBCH is reset.

Up to 32 bytes of transmit data can be written to the XFIFO following an XPR interrupt.

- DMA Mode
  selected if DMA bit in XBCH is set.

Prior to any data transfer, the actual byte count of the frame to be transmitted must be written to the XBCH, XBCL registers by the user.

If data transfer is then initiated via the CMDR register (command XTF or XIF), the HSCX autonomously requests the correct amount of block data transfers (n*32+REST, n=0,1, . . .).

Note: Addresses within the address space of the FIFO's are interpreted equally, i.e. the actual data byte can be accessed with any address within the valid scope.

Interrupt Status Register (READ)

	7							0	
IST A	REM	RPF	RSC	XPR	TIN	ICA	EXA	EXB	(20/60)

Value after RESET: 00_H

RME . . . Receive Message End

One message up to 32 bytes or the last part of a message greater then 32 bytes has been received and is now available in the RFIFO. The message is complete!
The actual message lengh can be determined reading the RBCH, RBCL registers.
Additional information is available in the RSTA register.

RPF . . . Receive Pool Full

A block of 32 bytes of a message is stored in the RFIFO. The message is not yet completed!
Note: This interrupt is only generated in interrupt Mode!

RSC . . . Receive Status Change (significant in auto mode only!)

A status change (receiver ready/receiver not ready) of the opposite station has been detected in auto mode. (i.e. the HSCX has received a RR/RNR supervisory frame according to the HDLC protocol.) The current status can be read from the STAR register (RRNR bit).

XPR . . . Transmit Pool Ready

A data block of up 32 bytes can be written to the transmit FIFO.

TIN . . .Timer Interrupt

The internal timer and repeat counter has been expired. (See also description of TIMR register!)

ICA . . . Interrupt of Channel A (Channel B only)

Indicates, that an interrupt is caused by channel A and the interrupt source(s) is (are) indicated in the ISTA register of channel A (i.e. at least one bit of the ISTA register of channel A is set).

EXA . . . Extended Interrupt of Channel A (Channel B only)

An interrupt is caused by channel B and source(s) is (are) indicated in the EXIR register of channel B.

Note: The ICA, EXA, and EXB bit are present in channel B only and point to the ISTA (CHA), EXIR (CHA), and EXIR (CHB) registers.

After the HSCX has requested an interrupt by turning its INT pin to low, the CPU must first read the ISTA register of channel B and check the state of these bits in order to determine which interrupt source(s) of which channel(s) has caused the interrupt. More than one interrupt source may be indicated by a single interrupt request.

After the respective register has been read, EXA, and EXB are reset. All other bits will be reset after reading ISTA. To prevent malfunctions, each bit is individually monitored and reset.

Mask Register (WRITE)

	7							0	
MASK	RME	RPF	RSC	XPR	TIN	ICA	EXA	EXB	(20/60)

Value after RESET: 00_H (all interrupts enabled)

Each interrupt source can be selectively masked by setting the respective bit in MASK (bit positions corresponding to ISTA register). Masked interrupts are not indicated when reading ISTA. Instead, they remain internally stored and will be indicated after the respective MASK bit is reset.

Note: In the event of an extended interrupt, no interrupt request will be generated with a masked EXA, EXB bit, although this bit is set in ISTA.

Extended Interrupt Register (READ)

Value after RESET: 00_H

	7							0	
EXIR	XMR	XDU EXE	PCE	RFO	CSC	RFS	0	0	(24/64)

XMR . . . Transmit Message Repeat

The transmission of the last message has to be repeated because
- the HSCX has received a negative acknowledgment in auto mode,
- or a collision has occured after sending the 32nd data byte of a message in a bus configuration.
- or CTS (transmission enable) has been withdrawn after sending the 32nd data byte of a message in point-to-point configuration.

XDU/EXE . . . Transmit Data Underrun/Extended Transmission End

The actual frame has been aborted with IDLE, because the XFIFO holds no further data, but the frame is not yet complete!
In extended transparent mode, this bit indicates the transmission-end condition.

Note: It is not possible to send transparent-, or I-frames when a XMR or XDU interrupt is indicated.

PCE . . . Protocol Error (significant in auto mode only!)

The HSCX has detected a protocol error, i.e. it has received
- an S-, or I-frame with incorrect N (R)
- an S-frame containing an I-field.

RFO . . . Receive Frame Overflow

One frame could not be stored due to occupied RFIFO (i.e. whole frame has been lost). This interrupt can be used for statistical purposes and indicates, that the CPU does not respond quickly enough to an incoming RPF, or RME interrupt.

CSC . . . Clear To send Status Change

Indicates, that a state transition has occured at the CTS pin. The actual state can be read from STAR register (CTS bit)
This interrupt must be enabled setting the CIE bit in CCR2.

RFS . . . Receive Frame Start

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after a valid address check in operation modes providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes.
After an RFS interrupt, the contents of
- RHCR
- RAL1
- RSTA – bit 3-0

are valid and can be read by the CPU.

This interrupt must be enabled setting the RIE bit in CCR2.

Status Register (READ)

Value after RESET: 48_H

	7							0	
STAR	XDOV	XFW	XRNR	RRNR	RLI	CEC	CTS	WFA	(21/61)

XDOV . . . Transmit Data Overflow

More than 32 bytes have been written to the XFIFO.

XFW . . . Transmit FIFO Write Enable

Data can be written to the XFIFO.

XRNR . . . Transmit RNR (significant in auto mode only!)

Indicates the status of the HSCX.

0 . . . receiver ready

1 . . . receiver not ready

RRNR . . . Received RNR (significant in auto mode only!)

Indicates the status of the remote station.

0 . . . receiver ready

1 . . . receiver not ready

RLI . . . Receive Line Inactive

Neither FLAGs as interframe time fill nor frames are received via the receive line.

Note: Significant in point-to-point configurations!

CEC . . . Command Executing

0 . . . no command is currently executed, the CMDR register can be written to.

1 . . . a command (written previously to CMDR) is currently executed, no further command can be temporarily written via CMDR register.

Note: CEC will be active at most 2.5 transmit clock periods. If the HSCX is in power down mode CEC will stay active.

CTS . . . Clear To Send State

If the CIE bit in CCR2 is set, this bit indicates the state of the CTS pin.

0 . . . CTS is inactive (high signal at CTS)

1 . . . CTS is active (low signal at CTS)

WFA . . . Waiting For Acknowledgement (significant in auto mode only).

Indicates the 'Waiting for Acknowledgement' status of HSCX.

Command Register (WRITE)

Value after RESET: 00_H

	7							0	
CMDR	RMC	RHR	RNR XREP	STI	XTF	XIF	XME	XRES	(21/61)

RMC . . . Receive Message Complete

Confirmation from CPU to HSCX, that the actual frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

Note: In DMA mode, this command is only issued once after a RME interrupt. The HSCX does not generate further DMA requests prior to the reception of this command.

RHR . . . Reset HDLC Receiver

All data in the RFIFO and the HDLC receiver deleted.

In auto mode, additionally the transmit and receive sequence number counters are reset.

RNR/XREP . . . Receiver Not Ready/Transmission Repeat

The function of this command depends on the selected operation mode (MDS1, MDS0, ADM bit in MODE):

- Auto mode: RNR

The status of the HSCX receiver is set. Determines, whether a received frame is acknowled via an RR, or RNR supervisory frame in auto mode.

0 . . . Receiver Ready (RR)

1 . . . Receiver Not Ready (RNR)

- Extended transparent mode 0,1: XREP

Together with XTF and XME set (write $2A_H$ to CMDR), the HSCX repeatedly transmits the contents of the XFIFO (1 . . . 32 bytes) without HDLC framing fully tranparent, i.e. without FLAG, CRC insertion, bit stuffing.

The cyclic transmission is stopped with an XRES command!

STI . . . Start Timer

The internal timer is started.

Note: The timer is stopped by rewriting the TIMR register after start.

XTF . . . Transmit Transparent Frame

● Interrupt mode

After having written up to 32 bytes the XFIFO, this command initiates the transmission of a transparent frame. An opening flag sequence is automatically added to the data by the HSCX.

● DMA mode

After having written the length of the frame to be transmitted to the XBCH, XBCL registers, this command initiates the data transfer form system memory to HSCX by DMA. Serial data transmission starts as soon as 32 bytes are stored in the XFIFO.

XIF . . . Transmit I-Frame (used in auto mode only!)

Initiates the transmission of an I-frame in auto mode. Additional to the opening flag sequence, the address and control field of the frame is automatically added by HSCX.

XME . . . Transmit Message End (used in interrupt mode only!)

Indicates, that the data block written last to the transmit FIFO completes the actual frame. The HSCX can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

In DMA mode, the end of the frame is determined by the transmit byte count in XBCH, XBCL!

XRES . . . Transmit Reset

The contents of the XFIFO is deleted and IDLE is transmitted. This command can be used by the CPU to abort a frame currently in transmission. After setting XRES an XPR interrupt is generated in every case.

Note: The maximum time between writing to the CMDR register and the execution of the command is 2.5 clock cycles. Therefore, if the CPU operates with a very high clock in comparison with the HSCX's clock, it's recommended that the CEC bit of the STAR register is checked before writing to the CMDR register to avoid any loss of commands.

Mode Register (READ/WRITE)

Value after RESET: 00_H

	7							0	
MODE	MDS1	MDS0	ADM	TMD	RAC	RTS	TRS	TLP	(22/62)

MDS1, MDS0 . . . Mode Select

The operating mode of the HDLC controller is selected.

00 . . . auto mode

01 . . . non-auto mode

10 . . . transparent mode

11 . . . extended transparent mode

ADM . . . Address Mode

The meaning of this bit varies depending on the selected operating mode:

- Auto mode, non-auto mode

Defines the length of the HDLC address field.

0 . . . 8-bit address field

1 . . . 16-bit address field

In transparent modes, this bit differentiates between two sub-modes:

- Transparent mode

0 . . . transparent mode 0; no address recognition.

1 . . . transparent mode 1; high byte address recognition.

- Extended transparent mode; without HDLC framing.

0 . . . extended transparent mode 0

1 . . . extended transparent mode 1

Note: In extended transparent modes, the RAC bit must be reset to enable fully transparent reception!

TMD . . . Timer Mode

The operation mode of the internal timer is set.

0 . . . external mode

The timer is controlled by the CPU and can be started at any time setting the STI bit in CMDR.

1 . . . internal mode

The timer is used internally by the HSCX for timeout and retry conditions in auto-mode. (refer to the description of the TIMR register)

RAC . . . Receiver Active

Switches the receiver to inoperational state.

0 . . . receiver inactive

1 . . . receiver active

In extended transparent modes this bit must be reset to enable fully transparent reception!

RTS . . . Request To Send

Defines the state and control of RTS pin.

0 . . . The RTS pin is controlled by the HSCX autonomously.

RTS is activated when a frame transmission starts and deactivated after the transmission operation is completed.

1 . . . The RTS pin is controlled by the CPU.

If this bit is set, the RTS pin is activated immediately and remains active till this bit is reset.

TRS . . . Timer Resolution

The resolution of the internal timer (factor k, see description of TIMR register) is selected
0 . . . $k = 32.768$
1 . . . $k = 512$

TLP . . . Test Loop

Input and output of the HDLC channels are intenally connected
(transmitter channel A – receiver channel A/
transmitter channel B – receiver channel B)

Timer Register (READ/WRITE)

	7 … 5	4 … 0	
TIMR	CNT	VALUE	(23/63)

VALUE . . . Sets the time period t_1 as follows:

$t_1 = k$ x (VALUE + 1) x TXP
where

- k is the timer resolution factor which is either 32.768 or 512-clock cycles dependent on the programming of TRS bit in MODE.
- TCP is the clock period of transmit data.

CNT . . . Interpreted differently dependent on the selected timer mode (bit TMD in MODE).

● Internal timer mode (MODE.TMD = 1)

– retry counter (in HDLC known as N2)

CNT indicates the number of S-commands (max. 6) which are transmitted autonomously by the HSCC after expiration of time period t_1, in case an I-frame is not acknowledged by the opposite station.

If CTN is set to 7, the number of S-commands is unlimited.

● External timer mode (MODE, TMD = 0)

CNT plus VALUE indicates the time period t2 after which a timer interrupt will be generated. The time period t_2 is

$t_2 = 32$ x k x CNT x TCP + 11

If CTN is set to 7, a timer interrupt periodically generated after the expiration of t_1.

Transmit Address Byte 1 (WRITE)

	7		0	
XAD1 2-byte address	XAD1 (high byte)	0	(0)	(24/64)
1-byte address	XAD1 (COMMAND)			

XAD1 (and XAD2) can be programmed with one individual address byte which is appended automatically to the frame by HSCX in auto mode. The function depends on the selected address mode (bit ADM in MODE).

– 2-byte address field (MODE. ADM = 1)

XAD1 builds up the high byte of the 2-byte address field. Bit 1 must be set to 0! According to the ISDN LAP D protocol, bit 1 is interpreted as the C/R (COMMAND/RESPONSE) bit. This is manipulated automatically by the HSCX dependet on the setting of the CRI bit in RAH1:

	Bit 1 (C/R)	
Commands transmit	1	0
Responses transmit	0	1
	CRI = 1	CRI = 0

(In the ISDN, the high address byte is known as SAPI).

In accordance with the HDLC protocol, bit 0 should be set to 0, indicating the extension of the address field to two bytes.

– 1-byte address field (MODE.ADM = 0)

According with the X.25 LAP B protocol, XAD1 indicates a COMMAND.

Transmit Address Byte 2 (WRITE)

	7 0	
XAD2 2-byte address	XAD2 (low byte)	(25/65)
1-byte address	XAD2 (RESPONSE)	

Second individually programmable address byte.

– 2-byte address (MODE.ADM = 1)

  XAD2 builds up the low byte of the 2-byte address field
  (In the ISDN, the low address byte is known as TEI)

– 1-byte address (MODE.ADM = 0)

  According to the X.25 LAP B protocol, XAD2 indicates a RESPONSE,

Note: XAD1, XAD2 registers are used only if the HSCX is operated in auto-mode.

Receive Byte Count Low (READ)

	7	0	
RBCL	RBC7	RBC0	(25/65)

Together with RBCH (bits RBC11 – RBC8), the length of the actual received frame (1 . . . 4095 bytes) can be determined. These registers must be read by the CPU following a RME interrupt.

Receive Address Byte High Register 1 (WRITE)

	7		0	
RAH1	RAH1	CRI	0	(26/66)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individual programmable values in RAH1, or RAH2.

RAH1 . . . Value of the first individual high address byte

CRI . . . Command/Response Interpretation
The setting of the CRI bit affects the meaning of the C/R bit in RSTA as follows:

C/R meaning	C/R value	
Commands received	0	1
Responses received	1	0
	CRI = 1	CRI = 0

Important: If the 1 byte address field is selected in auto mode, RAH1 must be set to 00_H.

Receive Address Byte High Register 2 (WRITE)

	7 … 2	1	0	
RAH2	RAH2	MCS	0	(27/67)

RAH2 . . . Value of second individual programmable high address byte.

MCS . . . – Module Count Select –; valid in auto mode only.

The MCS bit adjusts the control field format according to the HDLC (ISDN/LAPD).

0 . . . basic operation (modulo 8)

1 . . . extended operation (modulo 128)

Note: When modulo 128 is selected, in auto mode the "RHCR" register contains compressed information of the extended control field (see RHCR, register description). RAH1, RAH2 registers are used in auto- and non-auto operating modes when a 2-byte address field has been selected (MODE.ADM = 1) and in the transparent mode 0.

Receive Status Register (READ)

	7							0	
RSTA	VFR	RDO	CRC	RAB	HA1	HA0	C/R	LA	(2)/67)

VFR . . . Valid Frame

Determines whether a valid frame has been received.

1 . . . Valid

0 . . . Invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n * 8 bits) in length (e.g. 25 bit), or

– a frame which is too short depending on the selected operation mode via MODE (MDS1, MDS0, ADM) as follows:

- Auto-/non-auto mode (16-bit address): 4 bytes
- Auto-/non-auto mode (8-bit address): 3 bytes
- Transparent mode 1:3 bytes.
- Transparent mode 0:2 bytes.

Note: Shorter frames are not reported.

RDO . . .Receive Data Overflow

A data overflow has occured within the actual frame.

CRC . . . CRC compare/check

0 . . . CRC check failed; received frame contains errors.
1 . . . CRC check o.k.; received frame is error-free.

RAB . . . Receive Message Aborted

The received frame was aborted from the transmitting station.
According to the HDLC protocol, this frame must be discarded by the CPU.

HA1, HA0 . . . High Byte Address Compare; significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the HSCX compares the high byte of a 2-bytes address with the contents of two individual programable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (group address).

Dependent on the result of this comparison, the following bit combinations are possible:
10 . . . RAH1 has been recognized
00 . . . RAH2 has been recognized
01 . . . group address has been recognized

Note: If RAH1, RAH2 contain the identical values, the combination 00 will be omitted.

C/R . . . Command/Response; significant only, if 2-byte address mode has been selected.

Value of the C/R bit (bit of high address byte) in the received frame. The interpretation depends on the setting of the CRI bit in the RAH1 register. Refer also to the description of RAH1 register.

LA . . . Low Byte Address Compare; not significant in transparent and extended transparent operating modes.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two programmable registers (RAL1, RAL2)
0 . . . RAL2 has been recognized
1 . . . RAL1 has been recognized
According to the X.25 LAP B protocol, RAL1 is interpreted as COMMAND and RAL2 interpreted as RESPONSE.

Note: RSTA corresponds to the last received HDLC fram; it is duplicated into RFIFO for every frame (last byte of frame).

Receive Address Byte Low Register 1 (READ/WRITE)

	7 — 0	
RAL1	RAL1	(28/68)

The general function (READ/WRITE) and the meaning or contents of this register depends on the selected operating mode:

– Auto-/non-auto mode (16-bit address) – WRITE:
RAL1 can be programmed with the value of the first individual low address byte.

– Auto-/non-auto mode (8-bit address) – WRITE:
According to X.25 LAP B protocol, the address in RAL1 is recognized as COMMAND address.

– Transparent mode 1 (high byte address recognition) – READ:
RAL1 contains the byte following the high byte of the address in the receive frame (i.e. the second byte after the opening flag).

– Transparent mode 0 (no address recognition) – READ:
RAL1 contains the first byte after the opening flag (first byte of received frame).

– Extended transparent modes 0,1 – READ:
RAL1 contains the actual data byte currently assembled at the RxD pin, by passing the HDLC receiver (fully transparent reception without HDLC framing).

Receive Address Byte Low Register 2 (WRITE)

	7 — 0	
RAL2	RAL2	(29/69)

Value ot the second individual programmable low address byte. If a one byte address field is selected, RAL2 is recognized as RESPONSE according to X.25 LAP B protocol.

Receive HDLC Control Register (READ)

	7	0	
RHCR	RHCR		(29/69)

Value of the HDCL control field of the last received frame.

Note: RHCR is duplicated into RFIFO for every frame.

Transmit Byte Count Low (WRITE)

	7	0	
XBCL	XBC7	XBC0	(2A/6A)

Together with XBCH (bits XBC11 . . . XBC8) this register is used in DMA mode only, to programm the length (1 . . . 4095 bytes) of the next frame to be transmitted.
This allows the HSCX to request the correct amount of DMA cycles after an XTF or XIF command via CMDR.

Baud Rate Generator Register (WRITE)

	7	0	
BGR	BR7	BR0	(2B/6B)

BR7 – BR0 . . . Baude Rate, bit 7-0

Together with bits BR9, BR8 of CCR2, the division factor of the baud rate generator is adjusted.
Dependent on the programmed value N in BR9 – BR8 (N = 0 . . . 1023), the division factor k results as follows:

$$k = (N+1) \times 2$$

Channel Configuration Register 2 (READ/WRITE)
Value after RESET: 00_H

The meaning of the individual bits in CCR2 depends on the selected clock mode via CCR1 as follows:

CCR2 clock mode 0,1	SOC1	SOC0	0	0	0	CIE	RIE	DIV	(2C/6C)
clock mode 2,6	BR9	BR8	BDF	TSS	TIO	CIE	RIE	DIV	
clock mode 3,7	BR9	BR8	BDF	0	TIO	CIE	RIE	DIV	
clock mode 5	SOC1	SOC0	XCS0	RCS0	TIO	CIE	RIE	DIV	
clock mode 4	SOC1	SOC0	0	0	TIO	CIE	RIE	DIV	

SOC1, SOC0 . . . Special Output Control

In a bus configuration (selected via CCR1) the function of pin RTS can be defined
0 0 . . . RTS output is activated during the transmission of a frame.
1 0 . . . RTS output is always high (RTS disabled).
1 1 . . . RTS indicates the reception of a data frame (active low).
In point to point configuration (selected via CCR1) the T x D and R x D pins may be flipped
0 X . . . data is transmitted on T x D, received on R x D pin (normal case)
1 X . . . data is transmitted on R x D, received on T x D pin

BR9, BR8 . . . Baud Rate, Bit 9-8 (higher significant bits, refer to description of BGR register).

BDF . . . Baud Rate Division Factor

0 . . . The division factor of the baud rate generator is set to 1 (constant).
1 . . . The division fachtor is adjusted with BR9 – BR0 bits of CCR2 and BRG register.

TSS . . . Transmit Clock Source Select

0 . . . The transmit clock is input to the T x CLKA/T x CLKB pins
1 . . . The transmit clock is derived from the baud rate generators output divided by 16.

TIO . . . Transmit Clock Input Output Switch

0 . . . T x CLKA, T x CLKB pins are inputs
1 . . . T x CLKA, T x CLKB pins are outputs

CIE . . . Clear To Send Interrupt Enable

Any state transition at the CTS input pin may cause an interrupt which is indicated in the EXIR register (CSC bit). The actual state at the CTS pin can be determined reading the CTS bit of the STAR register.
0 . . . disable
1 . . . enable

RIE . . . Receive Frame Start Interrupt Enable

When, the RFS interrupt (via EXIR) is enabled!

DIV . . . Data Inversion

Only valid if NRZ data encoding is selected. Data is transmitted and received inverted.

XCS0, RCS0 . . . Transmit/Receive Clock Shift, Bit 0

Together with bits XCS2, XCS1 (RCS2, RCS1) in TSAX (TSAR) the clock shift relative to the frame synchronization signal of the transmit (receive) time slot can be adjusted.
A clock shift of 0 . . . 7 bits is programmable (clock mode 5 only!).

Transmit Byte Count High (WRITE)

Value after RESET: 000xxxxx

	7				3	0	
XBCH	DMA	NRM	CAS	XC	XBC11	XBC8	(2D/6D)

DMA . . . DMA Mode

Selects the data transfer mode of HSCX to system memory.
0 . . . Interrupt controlled data transfer (interrupt mode)
1 . . . DMA controlled data transfer (DMA mode)

NRM . . . Normal Response Mode

Valid in auto mode only!
Determines the function of the LAP controller:
0 . . . full-duplex LAP B/LAP D operation
1 . . . half-duplex NRM operation

CAS . . . Carrier Detect Auto Start

When set, a high at the CD (AxCLK) pin enables the respective receiver and data reception is started.

XC . . . Transmit Continuously

Only valid if DMA mode is selected!
If the XC bit is set, the HSCX continuously requests for transmit data ignoring the transmit byte count programmed via XBCX, XBCL.

XBC11 . . .XBC8 . . . Transmit Byte Count (most significant bits)

Valid only if DMA mode is selected!
Together with XBC7 . . . XBC0) the length of the frame to be programmed.

Received Byte Count High (READ)

Value after RESET: 000xxxxx

	7				3	0	
RBCH	DMA	NRM	CAS	OV	RBC11	RBC8	(2D/6D)
	see XBCH						

DMA, NRM, CAS . . . These bits represent the read-back value programmed in XBCH (see XBCH!)

OV . . . Counter Overflow

More than 4095 bytes received!
The received frame exceeded the byte count in RBC11 . . . RBC0.

RBC11 . . . RBC8 . . . Receive Byte Count (most significant bits)

Together with RBCL (bits RBC7 . . . RBC0) the length of the received frame can be determined.

Version Status Register (READ)

	7				3	0	
VSTR	CD	0	0	0	VN3	VN0	(2E/6E)

CD . . . Carrier Detect

This bit represents the inverted state at the CD (AxCLK) pin.
1 . . . CD active (LOW)
0 . . . CD inactive (HIGH)

VN3 . . . VN0 . . . Version Number of Chip

0 . . . Version A1
2 . . . Version A2
4 . . . Version A3

Receive Length Check Register (WRITE)

	7		0	
RLCR	RC	RL6	RL0	(2E/6E)

RC . . . Receive Check (on/off)

0 . . . receive length check feature disabled
1 . . . receive length check feature enabled

RL . . . Receive Length

The maximum receive length after which data reception is suspended can be programmed here. Depending on the value RL programmed via RL6 . . . RL0, the receive length is (RL + 1)x32 bytes! A frame exceeding this length is treated as if it was aborted by the opposite station (RME Interrupt, RAB bit set).

In this case, the Receive Byte Count (RBCH, RBCL) is greater than the programmed receive length.

Channel Configuration Register 1 (READ/WRITE)

Value after RESET: 00_H

	7					0	
CCR1	PU	SC1	SC0	ODS	ITF OIN	CM2 CM1 CM0	(2F/6F)

PU . . . Switches between Power Up and Power Down mode

0 . . . power down (standby)
1 . . . power up (active)

SC1, SC0 . . . Serial Port Configuration

00 . . . NRZ data encoding
10 . . . NRZI data encoding
01 . . . bus configuration, timing mode 1
11 . . . bus configuration, timing mode 2

Note: It bus configuration is selected, only NRZ coding is supported.

ODS . . . Output Driver Select

Defines the function of the transmit data pins (TxDA, TxDB)
0 . . . TxD pins are open drain outputs
1 . . . TxD pins are push-pull outputs

ITF/OIN . . . Interface Time Fill/One Insertion

The function of this bit depends on the selected serial port configuration (bit SC1)

● Point-to-point configurations: ITF
Determines the idle (= no data to send) state of the transmit data pins (TxDA, TxDB)
0 . . . Continuous IDLE sequences are output (TxD pins remain in the "1" state)
1 . . . Continuous FLAG sequences are output ("01111110" bit patterns)

● Bus configurations: OIN
In bus configurations, the ITF is implicitly set to 0, i.e. continuous "1"s are transmitted, and data encoding is NRZ!
When this bit is set, a "ONE" insertion (deletion) mechanism is activated, inserting a "1" after seven consecutive "0"s in the transmit data stream or deleting a "1" in the receive data stream.
Similar to the HDLC's bit-stuffing mechanism (inserting a "0" after five consecutive "1"s), this method proves to be advantageous when the receive clock is recovered from the receive data stream by means of DPLL, because it is guaranted that at least after seven bits a transition occurs in the receive data in case of long "0" sequences!

CM2, CM1, CM0 . . . Clock Mode

Selects one of the 8 different clock modes
000 clock mode 0
. .
. .
. .
111 clock mode 7

Time-Slot Assignment Register Transmit (WRITE)

This registers is only used in clock mode 5!

	7 … 2	1	0	
TSAX	TSNX	XCS2	XCS1	(30/70)

TSNX . . . Time-Slot Number Transmit

Selects one of up 64 possible time slots (00_H-$3F_H$) in which data is transmitted. The number of bits per time slot can pe programmed via XCCR.

XCS2, XCS1 . . . Transmit Clock Shift, Bit 2-1

Together with bet XCS0 in CCR2, the transmit clock shift can be adjusted.

Time-Slot Assignment Register Receive (WRITE)

This register is only used in clock mode 5!

	7 ... 3	2	1 ... 0	
TSAR	TSNR	RCS2	RCS1	(31/71)

TSNR . . . Time-Slot Number Receive

Defines one of up to 64 possible time slots (00_H-$3F_H$) in which data is received. The number of bits per time slot can be programmed via RCCR.

RCS2, RCS1 . . . Receive Clock Shift, Bit 2-1

Together with bit RCS0 in CCR2, the receive clock shift can be adjusted.

Transmit Channel Capacity Register (WRITE)

Value after RESET: 00_H

	7 ... 0	
XCCR	XBC7 ... XBC0	(32/72)

XBC7 . . . XBC0 . . . Transmit Bit Count, Bit 7-0

Defines the number of bits to be transmitted with a time slot:
Number of bits = XBC + 1. (1 . . . 256 bits/time slot)

Receive Channel Capacity Register (WRITE)

	7 ... 0	
RCCR	RBC7 ... RBC0	(33/73)

Value after RESET: 00_H

RBC7 . . . RBC0 . . . Receive Bit Count, Bit 7-0

Defines the number of bits to be received within a time slot:
Number of bits = RBC + 1. (1 . . . 256 bits/time slot)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: SAB SAF	T_A T_A	0 to 70 –40 to 85	°C °C
Storage temperature	T_{stg}	–65 to 125	°C
Voltage on any pin with respect to ground	V_S	–0.4 to V_{DD} +0.4	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5$ V ± 5%, $V_{SS} = 0$ V.

Parameter		Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
L-input voltage		V_{IL}	–0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{CC}+0.4	V	
L-output voltage		V_{OL}		0.45	V	$I_{OL} = 7$ mA (pins TxD, RxD) $I_{OL} = 2$ mA (all other)
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD}-0.5		V V	$I_{OH} = -400$ µA $I_{OH} = -100$ µA
Power supply current	operational	I_{CC}		8	mA	$V_{DD} = 5$ V, $C_P = 4$ MHz Inputs at 0 V/V_{DD}, no output loads
	power down			1.5	mA	
Input leakage current Output leakage current		I_{LI} I_{LO}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

$T_A = 25\,°C$, $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$, $f_C = 1\ MHz$, unmeasured pins returned to GND.

Parameter	Symbol	Limit Values		Unit
		typ.	max.	
Input capacitance $f_C = 1\ MHz$	C_{IN}	5	10	pF
Output capacitance	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	8	15	pF

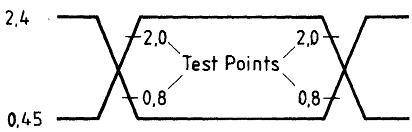
Characteristics

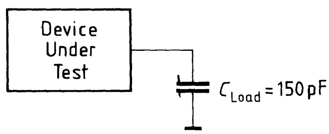
$T_A = 0$ to $70\,°C$, $V_{DD} = 5\ V \pm 5\%$

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

The AC testing inpugt/output waveforms are shown below.

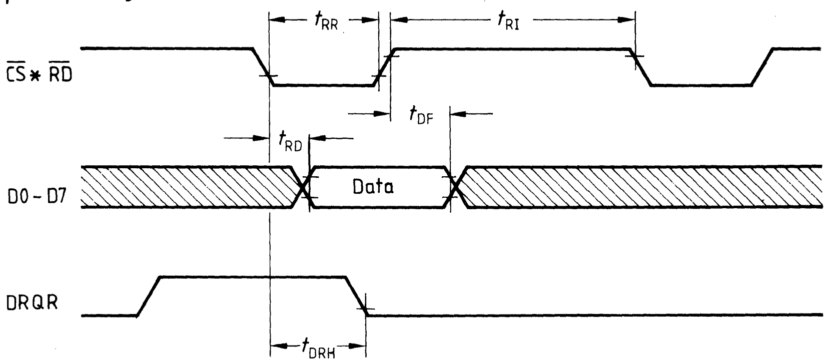
Input/Output Waveform for AC Tests



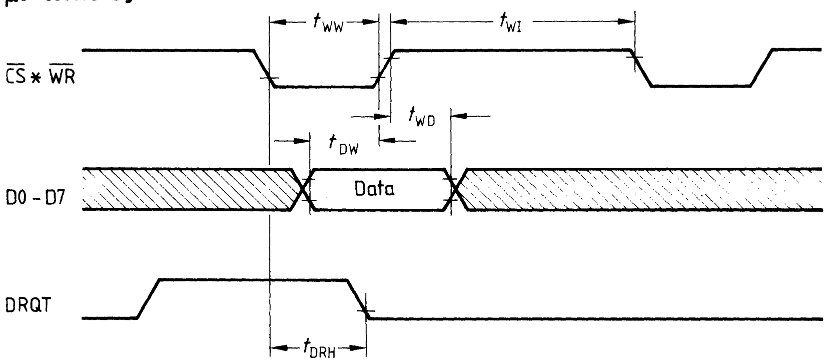


Microcontroller Interface Timing
Intel Bus Mode

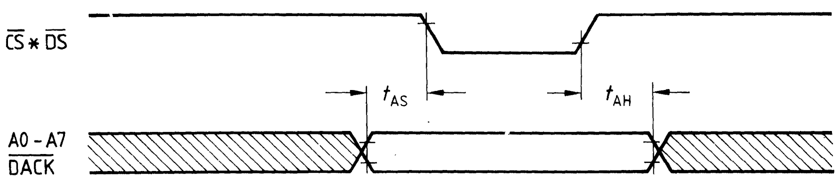
µP Read Cycle



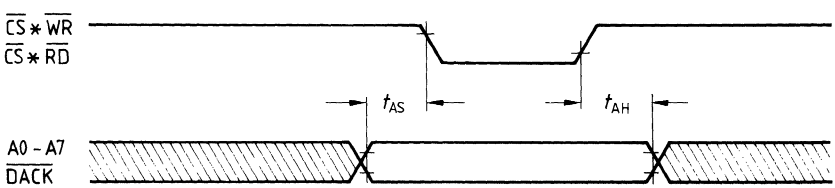
µP Write Cycle



Multiplexed Address Timing

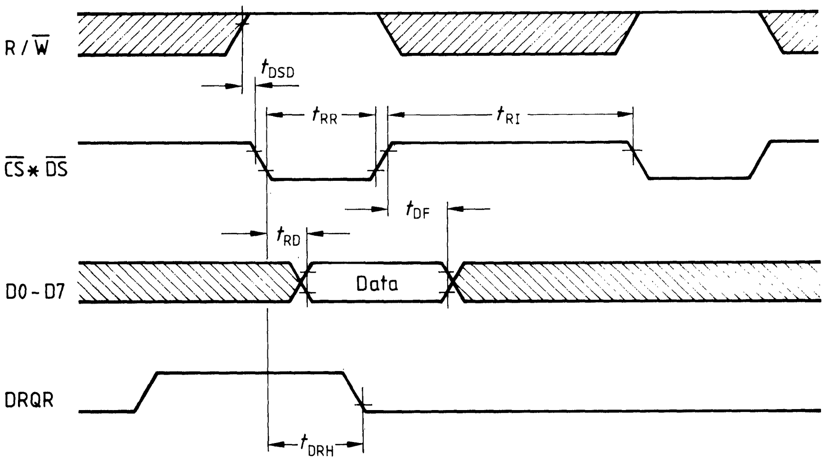


Address Timing

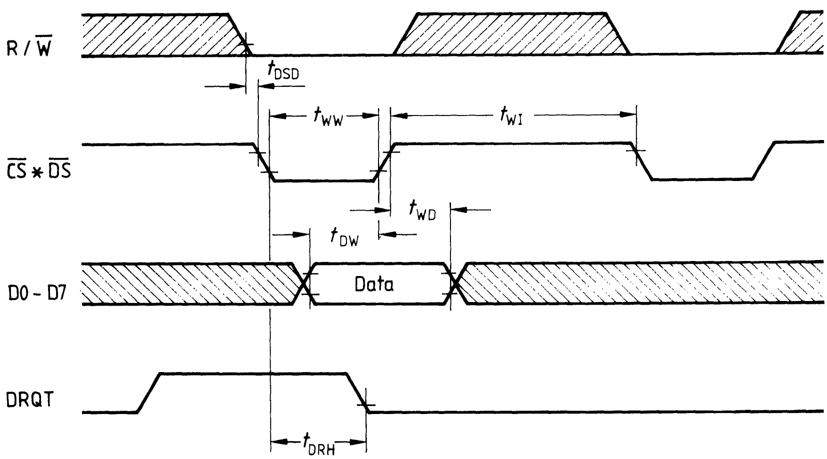


Motorola Bus Mode

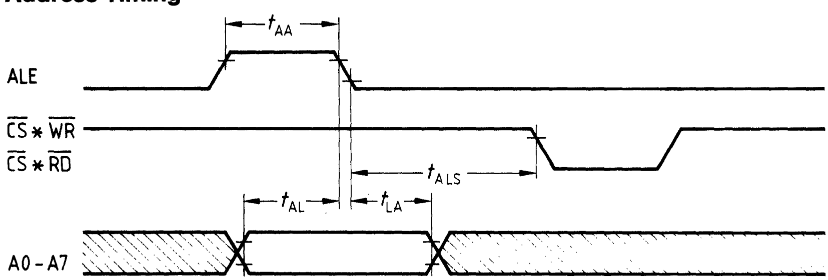
μP Read Cycle



μWrite Cycle



Address Timing

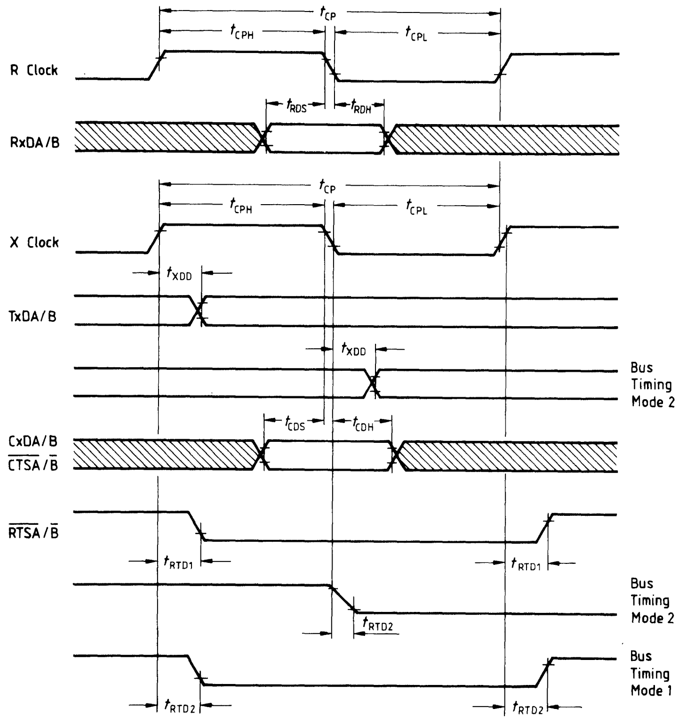


Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	10		ns
Address hold time from ALE	t_{LA}	20		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	20		ns
DMA request delay: SAB SAF	t_{DRH}		85 90	ns ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		120	ns
Data float delay from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	60		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}+\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}+\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	60		ns

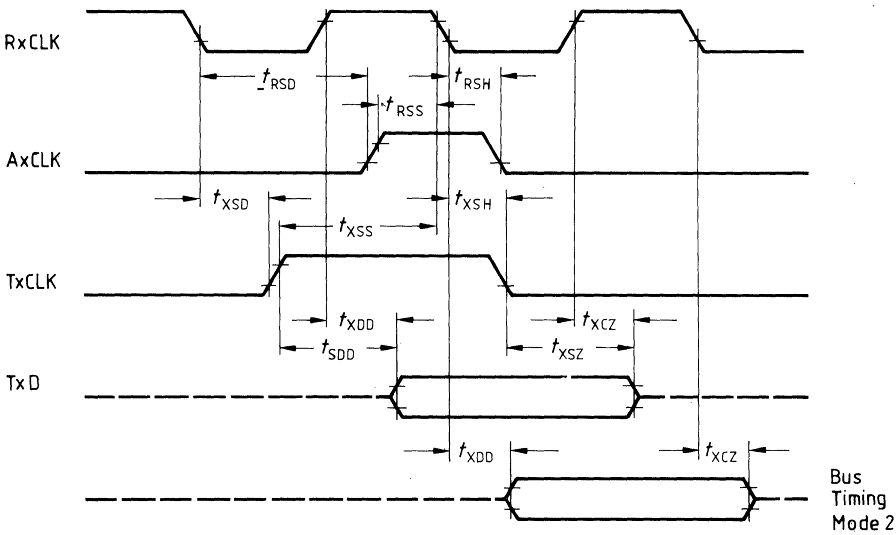
Serial Interface Timing

Clock Mode 1



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive data setup	t_{RDS}	5		ns
Receive data hold	t_{RDH}	30		ns
Collision data setup	t_{CDS}	0		ns
Collision data hold	t_{CDH}	30		ns
Transmit data delay	t_{XDD}	20	70	ns
Request to send delay 1	t_{RTD1}	30	120	ns
Request to send delay 2	t_{RTD2}	20	85	ns
Clock period	t_{CP}	240		ns
Clock period Low	t_{CPL}	90		ns
Clock period High	t_{CPH}	90		ns

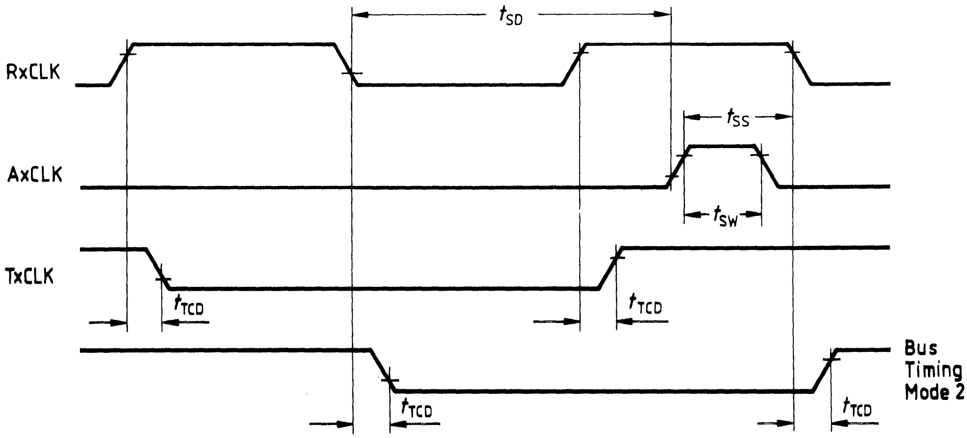
Strobe Timing



Parameter	Symbol	Limit Values min.	max.	Unit
Receive strobe delay	t_{RSD}	30		ns
Receive strobe setup	t_{RSS}	60		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe setup	t_{XSS}	60		ns
Transmit strobe hold	t_{XSH}	30		ns
Transmit data delay	t_{XDD}		70	ns
Strobe data delay	t_{SDD}		90	ns
High impedance from clock	t_{XCZ}		50	ns
High impedance from strobe	t_{XSZ}		50	ns

Clock Mode 5

Figure 17
Synchronization Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Sync pulse delay	t_{SD}	30		ns
Sync pulse setup	t_{SS}	30		ns
Sync pulse width	t_{SW}	40		ns
Time-slot control delay	t_{TCD}	20	75	ns

Clock Mode 2, 3, 6, 7

Internal Clocking

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency Baudrate generator used	f_{CLK}		12.3	MHz
Clock frequency Baudrate generator not used	f_{CLK}		19.3	MHz

Reset Timing

RES Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RES high	t_{RWH}	1800		ns

Appendix A

Upgrades of HSCX Version A3

The HSCX Version A3 is fully upward compatible to Version A2. The differences with respect to HSCX Technical Manual Rev. 2.89 are shown in **table 3**.

Table 3
Differences HSCX A2 – HSCX A3

Differences	Ver. A2	Ver. A3	Data Book Chapter
TRI, TWI value	70 ns	60 ns	Microcontroller Interface Timing
IOL value, pin TxD	2 mA	6 mA	Characteristics
VSTR value	02_H	04_H	VSTR, Register Definition

The following additional are implemented in HSCX A3

- Transmission of back to back frames
  Two or more frames may be transmitted continuously without interframe time fill
- TxD, RxD flip
  In clock modes 0, 1, 4 and 5 pins RxD and Tx may be flipped
- Status Register
  In auto mode, STAR: bit 0 indicates the 'Waiting for Acknowledgement' status