SIEMENS

High-Level Serial Communications Controller (HSCC)

SAB 82520
SAF 82520

Type	Ordering Code	Package
SAB 82520-C	Q67100-H8830	C-CIP-28
SAB 82520-N	Q67100-H8400	PL-CC-28 (SMD)
SAB 82520-P	Q67100-H8014	P-DIP-28
SAF 82520-C	Q67100-H8325	C-DIP-28
SAF 82520-N	Q67100-H8610	PL-CC-28 (SMD)
SAF 82520-P	Q67100-H8512	P-DIP-28

SAB 82520, a High-level Serial Communications Controller (HSCC), has been designed to free the user from tasks occuring in communication via networks and trunk lines.

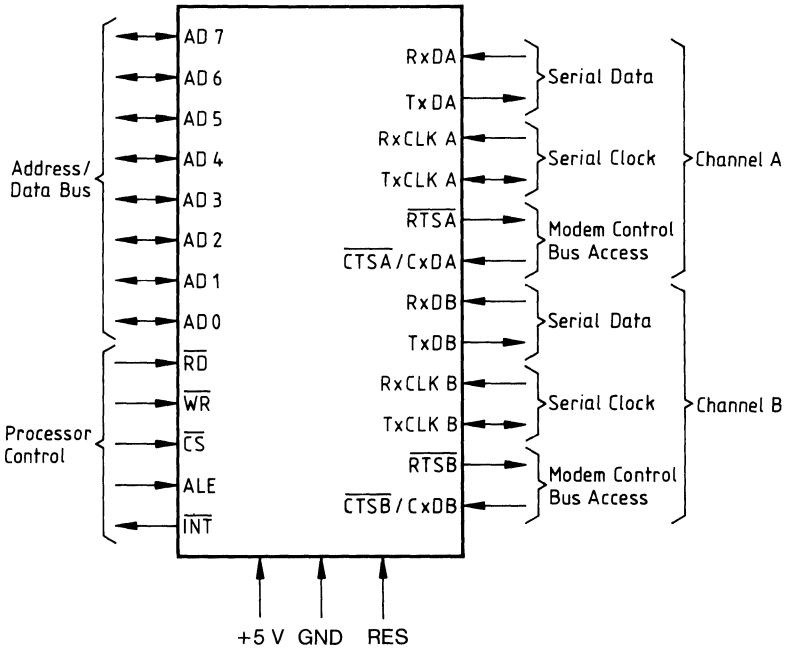
SAB 82520 is an X.25 LAPB/LAPD controller which, to a large degree performs communications procedures independently of CPU support.

A parallel processor bus constitutes the µC system. The communications interface is implemented by two full-duplex HDLC channels, which can be operated independently from one another. The HSCC is connected to the transmission line via additional line drivers or modems. External logic is cost-effective because clock recovery can be performed by an on-chip oscillator, DPLL circuits and a programmable baudrate generator.

Features

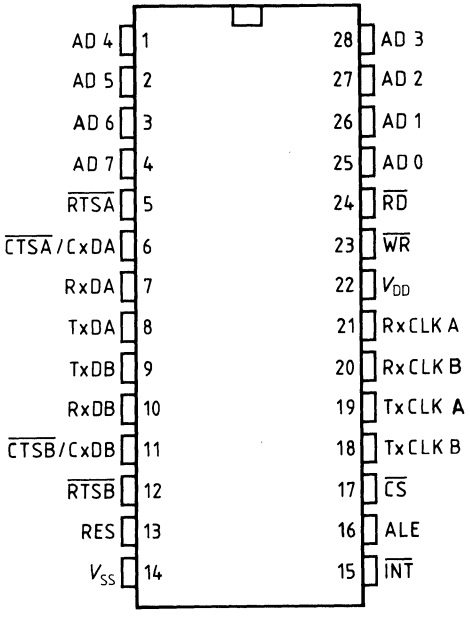
- Two independent HDLC channels
- Implementation of X.25 LAPB/LAPD protocol
- Programmable timeout and retry conditions
- FIFO buffers for efficient transfer of data packets
- Digital phase-locked loop for each channel
- Baudrate generator and oscillator
- Different modes for clock recovery and data encoding
- High-speed data rate (up to 4 MHz)
- Supports bus configuration by collision resolution
- Telecom-specific features programmable
- 8-bit parallel µP interface
- Advanced CMOS technology
- Low power consumption; active: 25 mW at 4 MHz
  standby: 3 mW
- SAB 82520: operating temperature 0 to 70 °C
- SAF 82520: operating temperature −40 to 85 °C

Logic Symbol

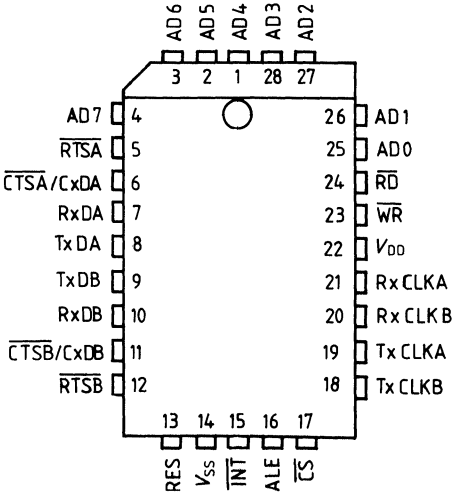


Pin Configurations
(top view)

P-DIP; C-DIP



PL-CC



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Functions
25 26 27 28 1 2 3 4	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address Data Bus** The multiplexed address data bus transfers data and commands between the µP system and the HSCC.
5 12	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O O	**$\overline{\text{Request to Send}}$** When the RTS bit in MODE is set, the $\overline{\text{RTS}}$ signal goes low. When the RTS bit is reset, the signal goes high of the transmitter has finished and there is no further request for a transmission. In a bus configuration, RTS goes low during the actual transmission of a frame shifted by a clock period, excluding collision bits.
6 11	$\overline{\text{CTSA}}$/C x DA $\overline{\text{CTSB}}$/C x DB	I I	**$\overline{\text{Clear to Send}}$/Collision Data** A low on the inputs enables the respective transmitter. If the transmitters are always enabled, $\overline{\text{CTS}}$ should be connected to V_{SS}. In a bus configuration the external serial bus must be connected to the respective C x D pin.
7 10	R x DA R x DB	I I	**Receive Data** These lines receive serial data at standard TTL or CMOS levels.
8 9	T x DA T x DB	O O	**Transmit Data** These lines transmit serial data at standard TTL or CMOS levels. They can be programmed as push-pull or open-drain outputs.
13	RES	I	**RESET** A high on this input forces the HSCC into reset state. The HSCC is in power-up mode during reset and in power-down mode after reset. The minimum pulse length is 1.8 µs.
14	V_{SS}		Ground (0 V)
15	$\overline{\text{INT}}$	O	**$\overline{\text{Interrupt Request}}$** The signal is activated when the HSCC requests an interrupt. It is an open-drain output.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Functions
16	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address data bus, selecting one of the HSCC internal sources or destinations
17	$\overline{CS}$	I	**$\overline{Chip\ Select}$** A low on this signal selects the HSCC for a read/write operation.
18 19	T x CLKB T x CLKA	I/O I/O	**Transmit Clock** These pins can be programmed in several different modes of operation. T x CLK may supply the transmit clock for the respective channel, a receive strobe signal (T x CLKA) and a transmit strobe signal (T x CLKB) or a frame synchronization signal (T x CLKA, clock mode 5). Programmed as outputs, T x CLK supply the transmit clock of the respective channel or a tristate control signal, indicating the programmed transmit time slot (T x CLKB, clock mode 5).
20 21	R x CLKB R x CLKA	I I	**Receive Clock** These pins can be programmed in several different modes of operation. In each channel R x CK may supply the receive clock, the receive and transmit clock, the clock for the baud rate generator or the clock for the DPLL. They also can be programmed for use as a crystal oscillator.
22	V_{DD}		Power +5 V power supply.
23	$\overline{WR}$	I	**$\overline{Write}$** This signal indicates a write operation.
24	$\overline{RD}$	I	**$\overline{Read}$** This signal indicates a read operation.

Applications

Figure 1a
Point-to-Point Configuration

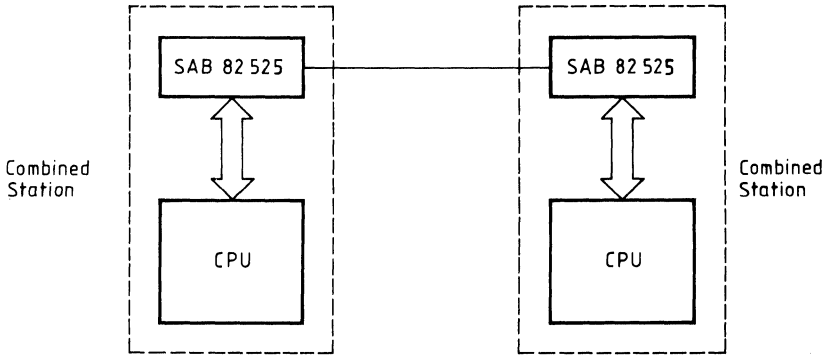


Figure 1b
Point-to-Multipoint Configuration

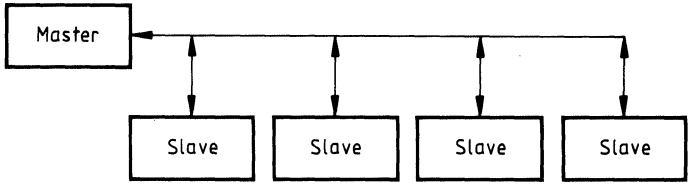
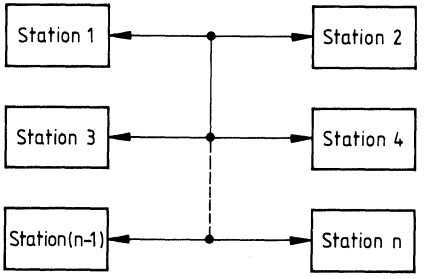


Figure 1c
Multimaster Configuration



Description

In a point-to-multipoint or in a multimaster configuration the HSCC can be used as a central station (master) or a peripheral station. As a peripheral station the HSCC can initiate the transmission of data. An internal function block provides for collision avoidance, which may occur if several stations start the transmitting simultaneously.

Furthermore, in a special operating mode the HSCC can transmit or receive data packets in programmable time slots; this makes SAB 82520 especially suitable for applications in systems designed for packet switching. In this application in particular, the integrated collision-resolution mechanism provides optimal utilization of system-internal PCM paths.

Characteristics

A number of characteristics which distinguish the SAB 82520 from conventional lowlevel HDLC devices are described below.

Support of Layer-2 Functions by HSCC

"Low-level" HDLC devices usually support various of protocols. When applying the HDLC protocol mainly bit-oriented functions such as bit stuffing, CRC check, flag and address recognition are performed. SAB 82520 has been especially designed to support the ISO HDLC protocol. In addition to the bit-oriented functions, the device provides a high degree of procedural support and evaluates the layer-2 control field. The communications procedures are processed between the communications controllers and not between the processors. As a result procedure handshaking is no longer necessary. The processor is informed of the status of the procedure however. The dynamic load of the processor is thus largely reduced. To maintain cost effectiveness and flexibility, not all layer-2 functions have been implemented as hardware. Instead, functions such as connection setup/connection clear-down and error recovery in case of protocol errors are performed by the processor software.

Operating Modes

The distribution of functions between HSCC and CPU applies to the auto mode. As a prerequiste for this operating mode, the window size between transmitted and acknowledged frames has to be limited to 1. Alternatively, transparent modes can be applied, the data field as well as the layer-2 headers are forwarded directly to the CPU. The reception and transmission of messages is fully controlled by the CPU. This operating mode is selected when the component is used as a central station (master) or if the accepted distance between transmitted and received frames (window size) is larger than 1.

Furthermore, there is a possibility to bypass the receiver and to get access to the received data directly.

FIFO Buffers for Efficient Transfer of Data Packets

Another feature of the SAB 82520 can be seen in the buffers that are used for temporary storage of data packets which are transferred between the serial communication interface and the parallel system bus. Due to the overlapping input/output operation (dual-port behavior), the maximum length of the data packets is not limited by the buffer size. The dynamic load of the processor is reduced by transferring the data packets block by block.

One FIFO buffer with a total capacity of 64 bytes per direction and channel is divided into two memory pools of 32 bytes each. When a pool is filled (receive mode) or emptied (transmit mode) via the serial interface, the processor is prompted by interrupt to read or write this pool. Subsequently the second pool is filled or emptied. During this time the CPU can transfer the first block thereby ensuring availability of the pool. With a serial transfer rate of 1 Mbit/s the reaction time between the first prompting and data overflow with loss of data is 256 µs. In addition, the transmit FIFO provides the flexibility for temporarily storing blocks of various lengths, which can be received in rapid succession. The FIFO will also store a data packet when a preceding short data packet stored in the memory has not yet been read by the processor.

The HSCC is especially suitable for cost-critical applications with single chip processors due to its memory organization and on-chip memory control.

Move string commands are available for high-performance applications where fast data rates at the communication interface and a high level of processor performance are required. The FIFO can then be addressed by the automatically incremented address.

Serial Interface

The serial interface provides two independent, high-performance communication interfaces. As already mentioned, the ISO HDLC layer-2 protocol is supported by the HSCC. In addition, layer-1 functions are provided by means of on-chip circuits. Eight different operating modes can be selected to clock the serial data stream.

- During the self-clocked operating mode, the transfer clock is recovered from the received data stream by means of an external crystal only. On-chip oscillator and DPLL circuits sample the received bit stream and adjust the clock edge to the center of the data bit.

- The bit stream is synchronized in the externally clocked operation mode by external clock signals. One the whole, 4 different clock signals separated by direction and channel, can be forwarded.

  In addition to the data clock, an externally supplied strobe signal can be applied to determine the time period during which data is to be received or transmitted. Using another operating mode, a time slot (up to 64 bit) can be programmed for transmitting data and another time slot for receiving data. One time slot consists of eight clock cycles.

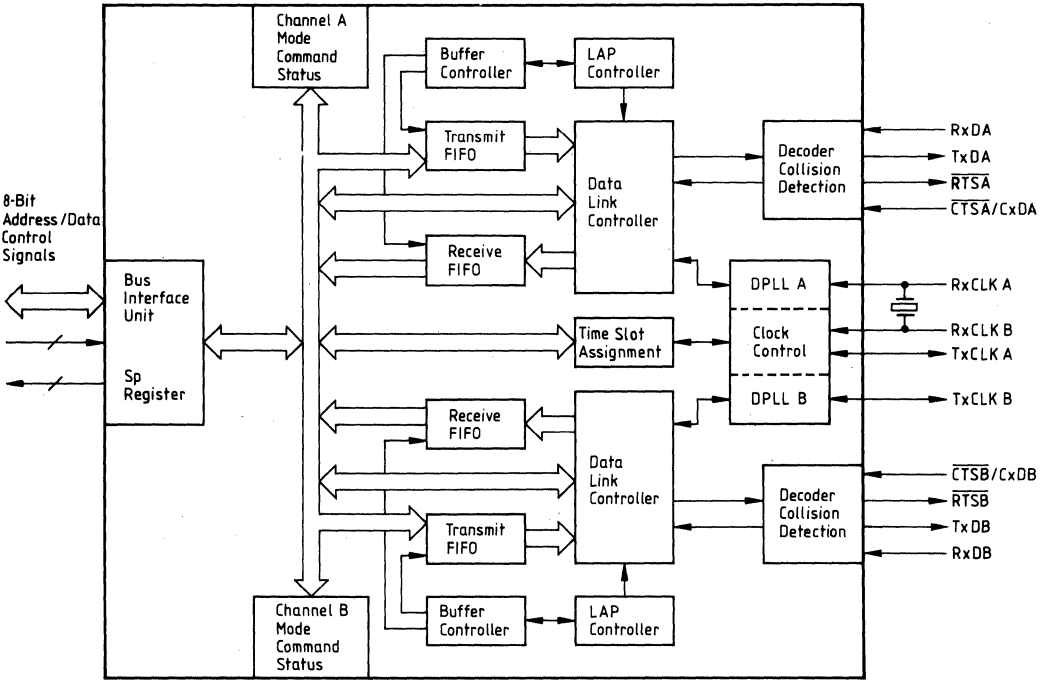
- With the point-to-multipoint configuration, comprising a central station (master) and several peripheral stations (slaves), data transmission can be initiated by a slave. If several stations (slaves) transmit data simultaneously, the bus is assigned to one station by a collision-resolution procedure implemented by the HSCC. The bus assignment functions in accordance with the principle applied with the ISDN S bus. Its collision-resolution procedure helps to ensure a sharing of priority among the slave stations.

- The maximum data rate of the externally clocked operating mode is 4 Mbits per second. In the self-clocked operating mode with an external reference clock or the crystal oscillator, the maximum clock rate is 12 MHz, the maximum data rate will be 750 kbit/s.

Description of Block Diagram

The chip contains a serial interface for two channels, including a DPLL and collision-detection block, a data-link controller and the FIFO buffers. The µP interface, including the status and command registers, is used for both channels. These functions are implemented in 2 µm CMOS technology.

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit
Storage temperature		T_{stg}	−65	125	°C
Operating temperature:	SAB 82520	T_A	0	70	°C
Operating temperature:	SAF 82520	T_A	−40	85	°C
Voltage at any pin vs. ground		V_S	−0.4	V_{CC} +0.4	V

DC Characteristics

SAB 82520: $T_A = 0$ to 70 °C; $V_{CC} = 5\ V \pm 10\%$; GND = 0 V
SAF 82520: $T_A = -40$ to 85 °C; $V_{CC} = 5\ V \pm 5\%$; GND = 0 V

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
L-input voltage H-input voltage	V_{IL} V_{IH}	V_{SS}−0.4		0.8 V_{CC}+0.4	V V	
L-output voltage H-output voltage	V_{OL} V_{OH}	 2.4 V_{CC}−0.5	 V_{CC}	0.45	V V V	I_{OL} = 2 mA I_{OH} = −400 µA I_{OH} = −100 µA
Input leakage current Output leakage current	I_{IL} I_{OL}	−10 −10		10 10	µA µA	$V_{IN} = V_{CC}$ to 0 V $V_{OUT} = V_{CC}$ to 0 V
V_{CC} supply current p. d. p. u.	 I_{CC} I_{CC}		 0.5 5	 1.8 7	 mA mA	 V_{CC} = 5 V, C_P = 4 MHz Inputs at V_{SS}/V_{CC} No output loads

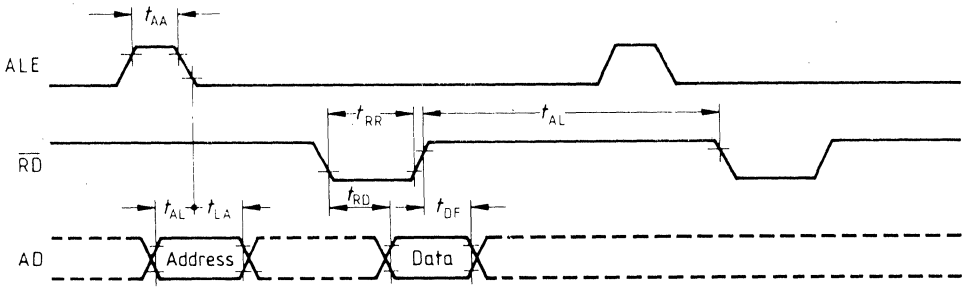
Capacitance

$T_A = 25$ °C; V_{CC} = GND = 0 V

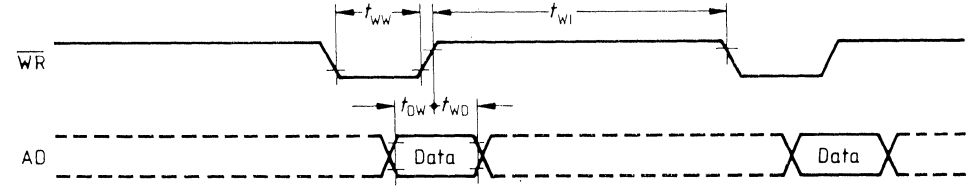
Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Input capacitance f_C = 1 MHz	C_{IN}		5	10	pF
Input/output capacitance	$C_{I/O}$		10	20	pF
Output capacitance unmeasured pins returned to GND	C_{OUT}		8	15	pF

µP Interface Timing

Read Cycle



Write Cycle



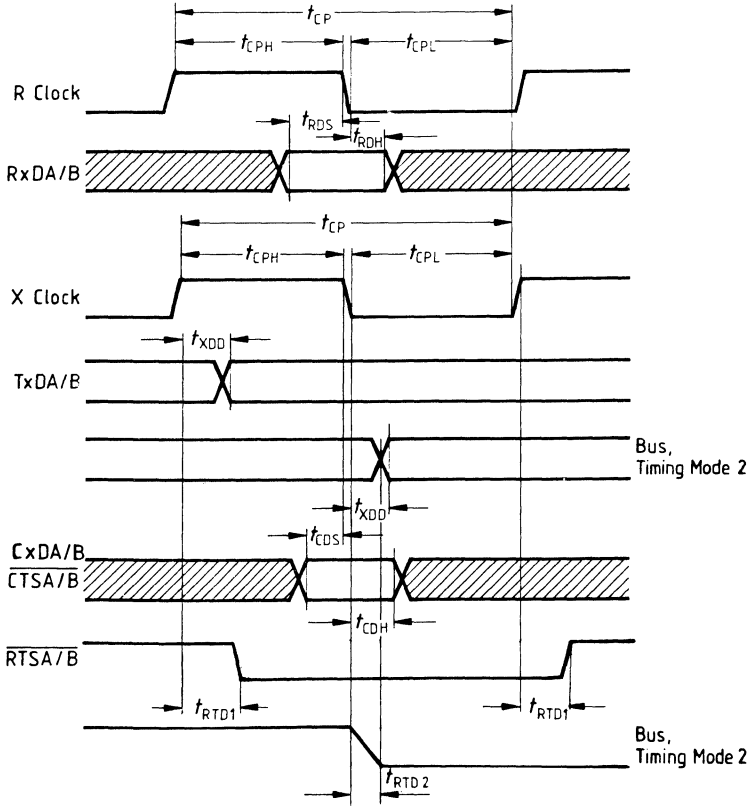
Read Cycle

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Address hold after ALE	t_{LA}	25		ns
Address to ALE setup	t_{AL}	20		ns
Data delay from RD	t_{RD}		110	ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	60		ns
ALE pulse width	t_{AA}	50		ns

Write Cycle

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup to $\overline{WR}$	t_{DW}	30		ns
Data hold after $\overline{WR}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	60		ns

Serial Interface Timing

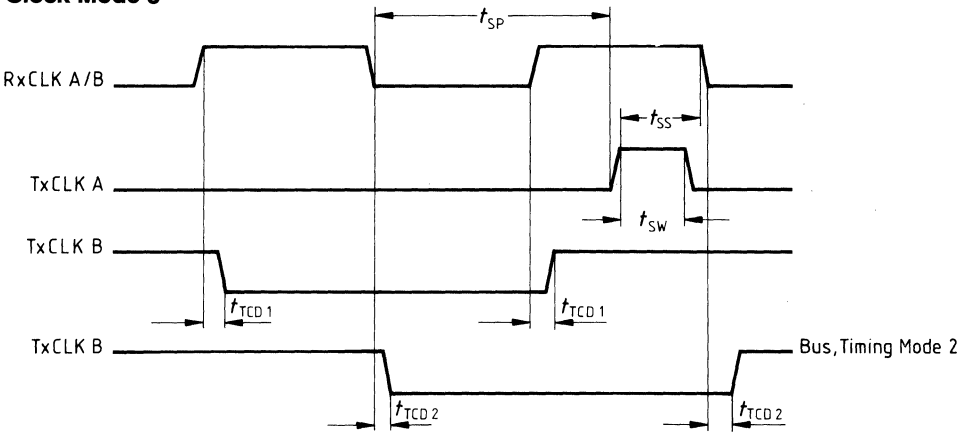


AC Characteristics

SAB 82520: $T_A = 0$ to 70 °C; $V_{CC} = 5\ V \pm 10\%$; GND = 0 V
SAF 82520: $T_A = -40$ to 85 °C; $V_{CC} = 5\ V \pm 5\%$; GND = 0 V

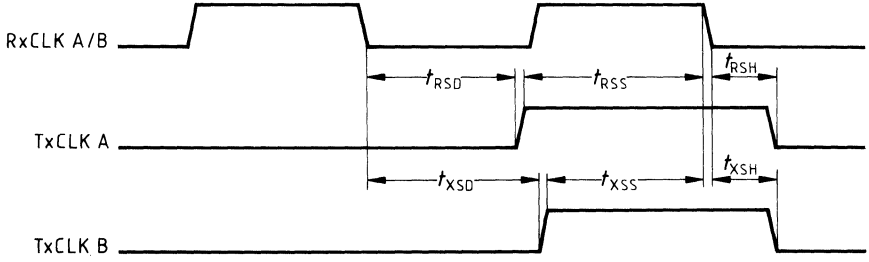
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive data setup	t_{RDS}	0		ns
Receive data hold	t_{RDH}	30		ns
Collision data setup	t_{CDS}	0		ns
Collision data hold	t_{CDH}	30		ns
Transmit data delay	t_{XDD}	20	68	ns
Request to send delay 1	$t_{RTD\,1}$	30	130	ns
Request to send delay 2	$t_{RTD\,2}$	20	85	ns
Clock period	t_{CP}	240		ns
Clock period Low	t_{CPL}	90		ns
Clock period High	t_{CPH}	100		ns

Clock Mode 5



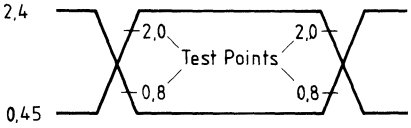
Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Sync pulse delay	t_{SD}	30		ns
Sync pulse setup	t_{SS}	30		ns
Sync pulse width	t_{SW}	40		ns
Time-slot control 2 delay	$t_{TCD\,2}$	20	95	ns
Time-slot control 1 delay	$t_{RCD\,1}$	30	120	ns

Clock Mode 1

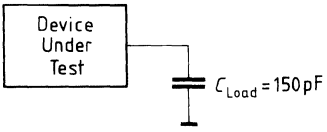


Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Receive strobe delay	t_{RSD}	30		ns
Receive strobe setup	t_{RSS}	70		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe setup	t_{XSS}	90		ns
Transmit strobe hold	t_{XSH}	30		ns

AC Testing Input, Output Waveform



AC Testing Load Circuit



AC Testing

Inputs are driven at 2.4 V for logic "1" and 0.45 V for logic "0".
Timing measurements are made at 2.0 V for logic "1" and at 0.8 V for logic "0".