SIEMENS

Dual Channel Codec Filter (SICOFI-2) PEB 2260

Preliminary Data CMOS IC

Type	Ordering Code	Package
PEB 2260-N	Q67100-H6067	PL-CC-28 (SMD)

The Dual Channel Codec Filter PEB 2260 (SICOFI®-2) is a fully integrated PCM codec and filter fabricated in low power CMOS technology for applications in digital communication systems. Based on an advanced digital filter concept, the PEB 2260 provides excellent transmission performance and high flexibility. The digital signal processing approach includes attractive programmable features such as transhybrid balancing, impedance matching, gain and frequency response correction.

The SICOFI-2 can be programmed to communicate either with SLD or with IOM®2 compatible PCM interface controllers (e.g. PEB 2050/51/52/55).

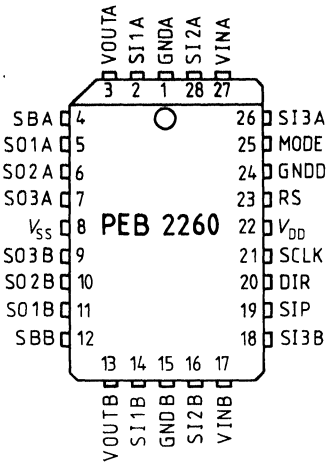
The device bridges the gap between analog and digital voice signal transmission in modern telecommunication systems.

High performance oversampling Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) provide the conversion accuracy required. Analog antialiasing Prefilters (PREFI) and smoothing Postfilters (POFI) are included. The dedicated on chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The SLD/IOM-2 interface handles digital voice transmission, SICOFI-2 feature control and access to the SICOFI-2 signal pins. Specific filter programming is done by downloading coefficients to the coefficient RAM (CRAM).

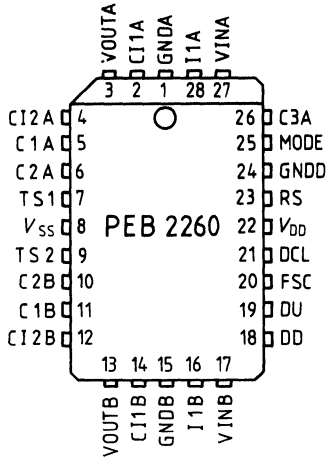
Features

- Dual channel single chip codec and filter
- Band limitation according to CCITT and AT&T recommendations
- Digital signal processing techniques
- PCM encoded digital voice transmission (A-law or μ-law)
- Programmable digital filters for
  - Impedance matching
  - transhybrid balancing
  - gain
  - frequency response correction
- SLD- and IOM2-interface
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities, per channel
  - three digital loop back modes
  - two analog loop back modes
  - two programmable tone generators
- No trimming or adjustments
- No external components
- Advanced low power CMOS technology
- Power supply +/−5 V

Pin Configuration for SLD Mode
(top view)



Pin Configuration for IOM-2 Mode
(top view)



Pin Definitions and Functions for SLD Mode

Pin No.	Symbol	Input (I) Output (O)	Function
22	V_{DD}	I	Power supply +5 V
8	V_{SS}	I	Power supply −5 V
24	GNDD	I	Ground digital. Not internally connected to GNDA or GNDB. All digital signals are referred to this pin.
1	GNDA	I	Ground analog channel A. Not internally connected to GNDD or GNDB. All channel A analog signals are referred to this pin.
15	GNDB	I	Ground analog channel B. Not internally connected to GNDD or GNDA. All channel B analog signals are referred to this pin.
27	VINA	I	Channel A analog voice input
3	VOUTA	O	Channel A analog voice output
17	VINB	I	Channel B analog voice input
13	VOUTB	O	Channel B analog voice output
25	MODE	I	Operating mode selection, connected to ground.

Pin Definitions and Functions for SLD Mode (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
21	SCLK	I	Slave clock
20	DIR	I	Direction signal, 8-kHz-frame synchronization.
19	SIP	I/O	Serial interface port, bidirectional serial data port.
23	RS	I	Reset input, RS forces the SICOFI-2 to basic settings.
2 28 26 14 16 18	SI1A SI2A SI3A SI1B SI2B SI3B	I I I I I I	Signaling input: Data present at SI1A...SI3B are sampled and transmitted via the serial interface
5 6 7 11 10 9	SO1A SO2A SO3A SO1B SO2B SO3B	O O O O O O	Signaling output: Data received via the serial interface are latched and fed to SO1A...SO3B.
4 12	SBA SBB	I/O I/O	Bidirectional signaling pin: SBA, SBB pins may be programmed as input or output individually with adequate SICOFI-2 status settings.

Pin Definitions and Functions for IOM-2 Mode (cont'd)

Pin No.	Symbol	Input I Output (O)	Function
22	V_{DD}	I	Power supply +5 V
8	V_{SS}	I	Power supply −5 V
24	GNDD	I	Ground digital. Not internally connected to GNDA and GNDB. All digital signals are referred to this pin.
1	GNDA	I	Ground digital channel A. Not internally connected to GNDD and GNDB. All channel A analog signals are referred to this pin.
15	GNDB	I	Ground analog channel B. Not internally connected to GNDD and GNDA. All channel B analog signals are referred to this pin.

Pin Definitions and Functions for IOM-2 Mode (cont'd)

Pin No.	Symbol	Input I Output (O)	Function
25	MODE	I	Operating mode selection, connected to V_{DD}.
27	VINA	I	Channel A analog voice input to transmit path
3	VOUTA	O	Channel A analog voice output of the received digital voice
17	VINB	I	Channel B analog voice input to transmit path
13	VOUTB	O	Channel B analog voice output of the received digital voice
21	DCLK	I	Data clock
20	FSC	I	Frame synchronisation clock
19	DU	O	Data upstream, serial data port output
18	DD	I	Data downstream, serial data port input
23	RS	I	Reset input, active high RS forces the SICOFI-2 to power down mode and resets the configuration registers
28 16	I1A I1B	I I	Indication input: Data present at I1A...I1B are sampled and transmitted via the serial interface.
5 6 26 11 10	C1A C2A C3A C1B C2B	O O O O O	Command output: Data received via the serial interface are latched and fed to C1A...C3A and C1B...C2B.
2 4 14 12	CI1A CI2A CI1B CI2B	I/O I/O I/O I/O	Bidirectional command/indication pin: C/1A...CI2B pins may be programmed as input or output individually with adequate SICOFI-2 status settings.
7 9	TS1 TS2	I I	Time-slot selection pin 1..2.

IOM-2 – Operating Modes

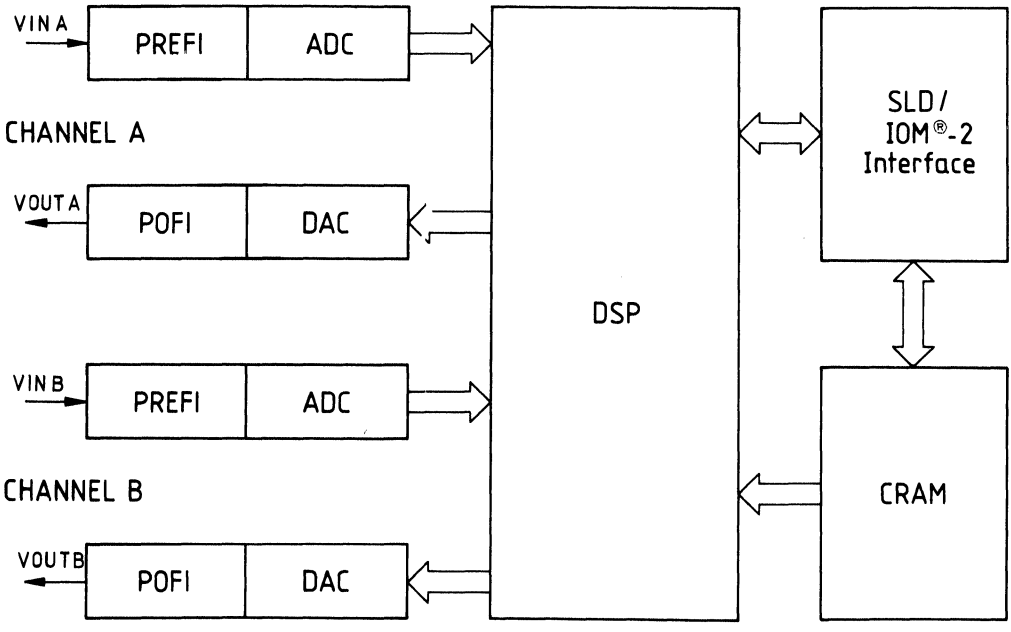
The SICOFI-2 is able to operate IOM-2-interfaces with two different Data Clock (DCL) frequencies (512 kHz or 4096 kHz). Time-Slot Assignment of 8 time slots is available with 4096-kHz DCLK frequency.

The IOM-2-operating mode and time-slot selection is set up by pin-strapping of two pins TS1 and TS2, which work with ternary logic (–5 V, 0 V and +5 V).

TS1	TS2	
N	N	'Slow' IOM-mode (DCLK = 512 kHz)
O	O	'Fast' IOM-mode, time slot 0 selected
O	N	'Fast' IOM-mode, time slot 1 selected
P	O	'Fast' IOM-mode, time slot 2 selected
P	N	'Fast' IOM-mode, time slot 3 selected
O	P	'Fast' IOM-mode, time slot 4 selected
N	O	'Fast' IOM-mode, time slot 5 selected
P	P	'Fast' IOM-mode, time slot 6 selected
N	P	'Fast' IOM-mode, time slot 7 selected

N... –5 Volt (V_{SS}) applied to pin TS1/TS2
0... 0 Volt (GNDD) applied to pin TS1/TS2
P... +5 Volt (V_{DD}) applied to pin TS1/TS2

Block Diagram



Transmission Characteristics

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing B; line termination Z; frequency-response correction: X, R) needs a complete knowledge of the SICOFI-2's analog environment. Unless otherwise stated, the programmable filters have the following transfer functions:

$H(Z) = H(B) = 0$; $H(X) = H(R) = H(GR) = H(GX) = H(AGR) = H(AGX) = 1$

A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms. A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V. (A-law,[μ-law]).

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain (either value) $R_L > 1$ kΩ Gain absolute 1 kHz at 0 dBm0 300 Ω $< R_L <$ 1 kΩ	G	−0.15 −0.25	0 0	0.15 0.15	dB
Gain variation with supply voltage and temperature 1 kHz at 0 dBm0	G_V	−0.15	0	0.15	dB
Total harmonic distortion[1]	THD			−44	dB
Intermodulation $2f_1 - f_2$ [2] $2f_1 - f_2$ [3]	 IMD IMD			 −44 −50	 dB dB
Crosstalk between individual channels 0 dBm0 f = 300 Hz to 3400 Hz	CT			−70	dB
Idle channel noise psophometric weighted transmit receive[4]	 N_{RP} N_{RP}			 −67 −78	 dBm0p dBm0p

[1] Single-frequency components between 300 Hz and 3400 Hz produced by a 0 dBm0 sine wave in the range between 300 Hz and 3400 Hz.
[2] Equal input levels in the range between −4 dBm0 and −21 dBm0; different frequencies in the range between 300 Hz and 3400 Hz.
[3] Input level −9 dBm0, frequency range 300 Hz to 3400 Hz and −23 dBm0, 50 Hz.
[4] Test conditions to be defined.

Attenuation Distortion

Attenuation deviations stay within the limits in the figures below.

Figure 1

Receive: Reference frequency 1 kHz, input signal level 0 dBm0

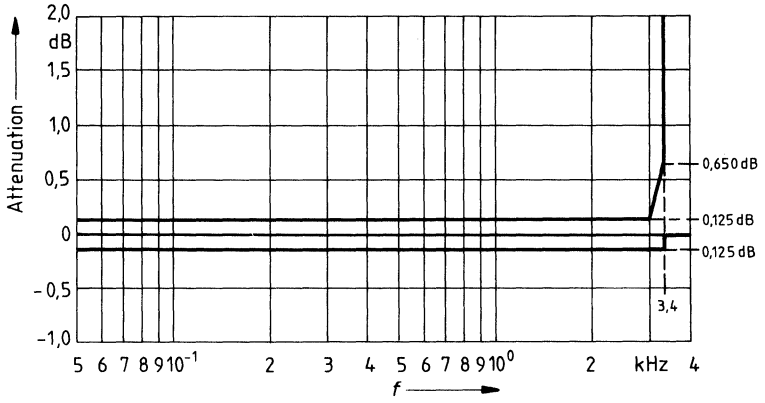
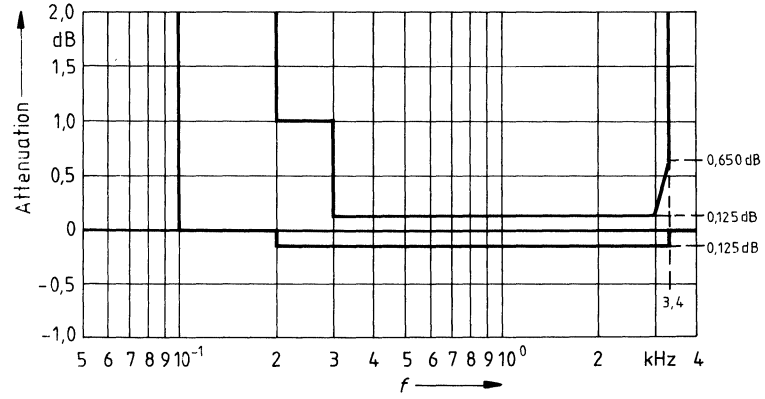


Figure 2

Transmit: Reference frequency 1 kHz, input signal level 0 dBm0



Gain Adjustment

Transmit gain values GX are programmable from 0 to 8 dB in steps ≤ 0.25 dB. Receive gain values GR are programmable from 0 to −8 dB in steps ≤ 0.25 dB. Together with the analog gain adjustments AGX, AGR (0, 6, 12, 14 dB) the SICOFI-2 offers a programming range of 22 dB.

Group Delay

Maximum delays for operating the SICOFI-2 with H(B) = H(Z) = 0 and H(R) = H(X) = 1, including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

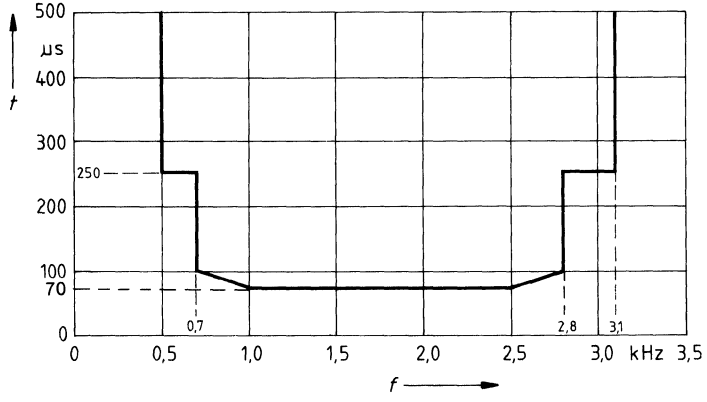
Group delay deviations stay with the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Transmit Delay $f = 1.4$ kHz	D_{XA}			340	µs
Receive Delay $f = 300$ Hz	D_{RA}			280	µs

Figure 3

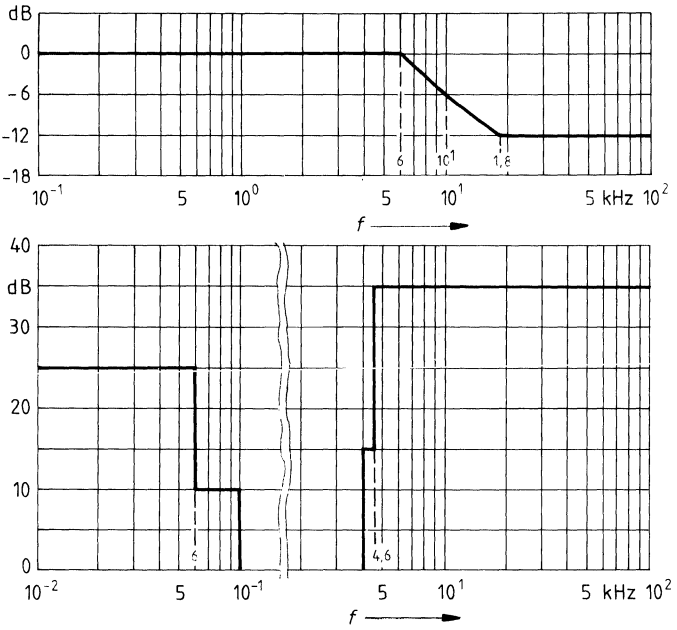
Group Delay Distortion: Input signal level 0 dBm0



Out-of-Band Signals at Analog Input

With an out-of-band sine wave signal with frequency *f* and level A applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below level A.

Figure 4



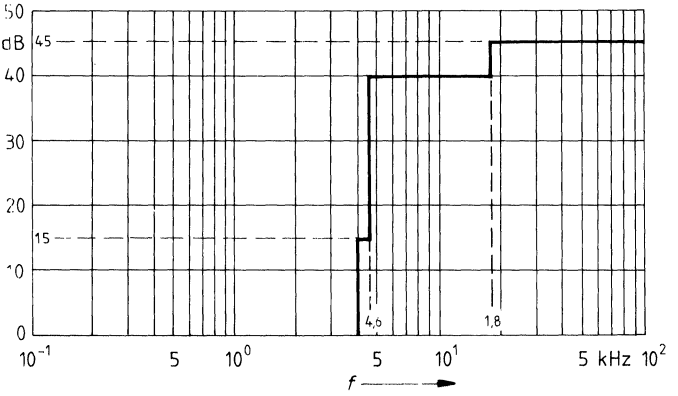
Maximum input level A at analog input

Transmit out-of-band discrimination X

Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave of frequency *f* applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

Figure 5



Receive out-of-band discrimination X

Gain Tracking (Receive and Transmit)

The gain deviations stay within the limits in the figures below

Figure 6

Gain Tracking: Measured with noise signal according to CCITT recommendations
Reference level is −10 dBm0

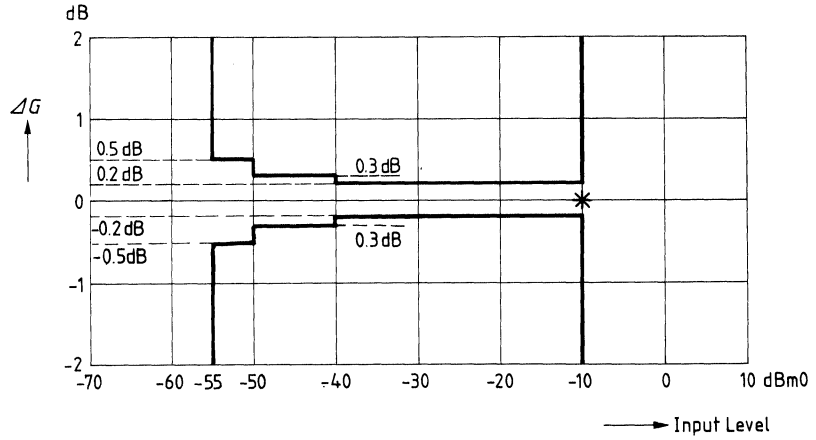
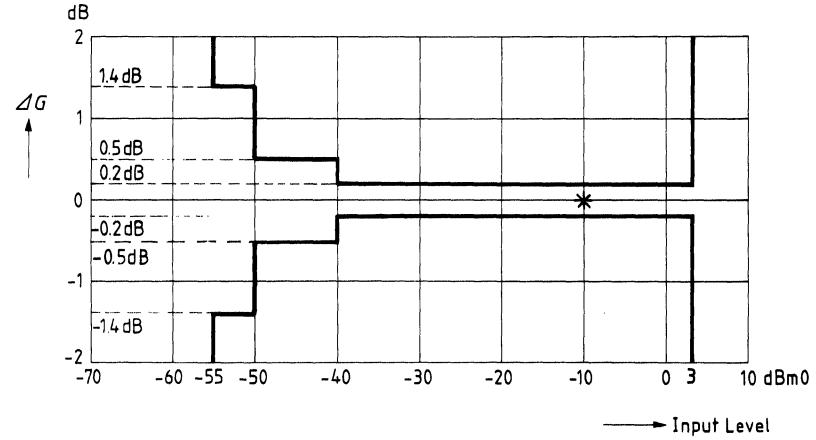


Figure 7

Gain Tracking: Measured with sine wave in the range 700 to 1100 Hz
Reference level is −10 dBm0



Total Distortion (Receive and Transmit)

The signal-to-distortion ratio exceeds the limits in the following figures.

Figure 8

Total Distortion: Measured with noise signal according to CCITT recommendations

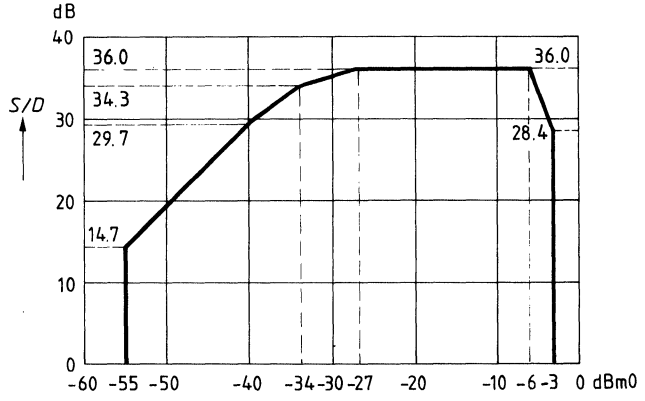
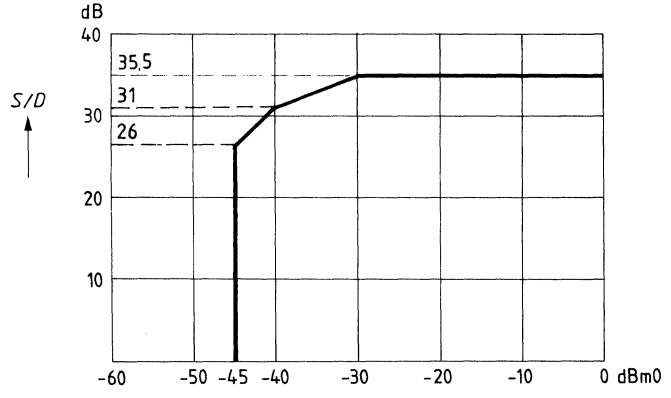


Figure 9

Total Distortion: Measured with sine wave in range 700 to 100 Hz



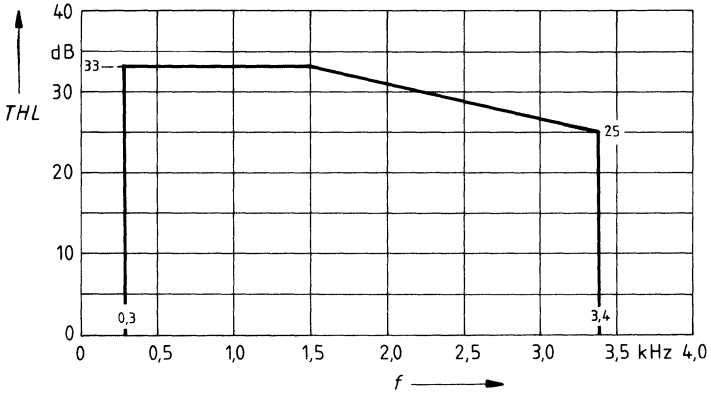
Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay.

The SICOFI-2 transhybrid-loss is measured the following way: A sine wave signal with level A and a frequency in the range of 300-3400 Hz is applied to the digital input. The resulting analog output signal at pin V_{OUT} is directly connected to V_{IN} e.g. with the SICOFI-2 testmode "Digital Loop Back via Analog Port" **(see CR3)**. The programmable filters R, Gr, X, Gx and Z are disabled, H(AGR) = H(AGX) = 1 and the balancing filter B is enabled with coefficients optimized for this configuration $V_{IN} = V_{OUT}$).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the following figure.

Figure 10



Note:

B-filter coefficients recommended for transhybrid loss measurement with $V_{OUT} = V_{IN}$:

B-filter part 1 (03) = see PEB 2060 pp. 185
B-filter part 2 (08) = see PEB 2060 pp. 185
B-filter Delay (18) = see PEB 2060 pp. 185

Absolute Maximum Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{DD} referred to GNDD		−0.3	5.5	V
V_{SS} referred to GNDD		−5.5	0.3	V
GNDA, GNDB to GNDD		−0.3	0.3	V
Analog input and output voltage				
referred to $V_{DD} = 5$ V; $V_{SS} = -5$ V	V_{IN}	−10.3	0.3	V
referred to $V_{SS} = -5$ V; $V_{DD} = 5$ V	V_{IN}	−0.3	10.3	V
All digital input voltages				
referred to GNDD = 0 V; $V_{DD} = 5$ V	V_{IN}	−0.3	5.3	V
referred to $V_{DD} = 5$ V; GNDD = 0 V	V_{IN}	−5.3	0.3	V
Power dissipation	P_D		1	W
Storage temperature	T_{stg}	−60	125	°C
Ambient temperature under bias	T_A	−10	80	°C

Operating Range

$T_A = 0$ to 70 °C; $V_{DD} = 5$ V ± 5%; $V_{SS} = -5$ V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
V_{DD} supply current	I_{DD}					
standby			0.5	0.8	mA	± 5% supply
operating			14	20	mA	± 5% supply
V_{SS} supply current	I_{SS}					
standby			0.1	0.2	mA	± 5% supply
operating			10	15	mA	± 5% supply
Power supply rejection (of either supply/direction)	*PSRR*	35			dB	1 kHz 80 mV_{rms} ripple
Power dissipation standby	P_{Ds}		3	5	mW	± 5% supply
Power dissipation operating	P_{Do}		120	175	mW	± 5% supply

Digital Interface

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = -5\ V \pm 5\%$; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
L-input voltage	V_{IL}	−0.3	0.8	V
H-input voltage	V_{IH}	2.0	$V_{DD}+0.3$	V
L-output voltage $I_O = -2$ mA	V_{OL}		0.45	V
H-output voltage $I_O = 400\ \mu A$	V_{OH}	2.4		V
Input leakage current $-0.3 \le V_{IN} \le V_{DD}$	I_{IL}		±1	µA

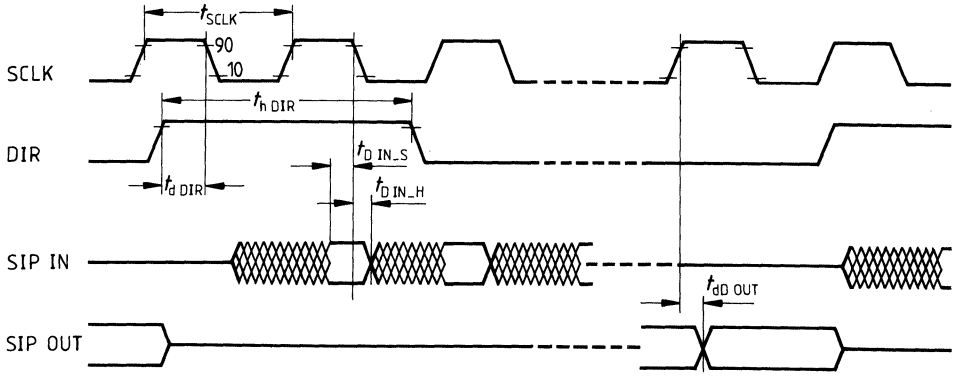
Analog Interface

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = -5\ V \pm 5\%$; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Analog input resistance	R_I	10		MΩ
Analog output resistance	R_O		10	Ω
Input offset voltage	V_{IO}		±50	mV
Output offset voltage	V_{OO}		±50	mV
Input voltage range	V_{IR}		±3.2	V
Output voltage range $R_L \ge 300\ \Omega$; $C_L \le 50$ pF	V_{OR}	±3.1		V

SLD-Bus Interface Timing

Figure 11

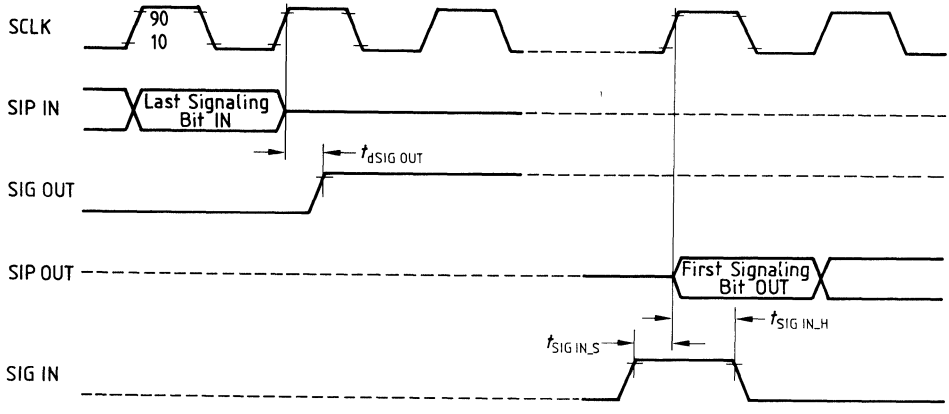


Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period SCLK	t_{SCLK}		1/512 kHz		
Duty Cycle		10		90	%
Period DIR	t_{DIR}		125		µs
DIR delay timw	t_{dDIR}	+20			ns
DIR high time	t_{hDIR}	500			ns
SIP data in setup time	$t_{DIN\,S}$	50			ns
SIP data in hold time	$t_{DIN\,H}$	0			ns
Thermal resistance junction to ambient	t_{dDOUT}			200	ns
SIP data out tristate delay vs. SCLK				50	ns
RS high time		250			ns

Signaling Interface Timing

Figure 12



Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Delay signaling out vs. SCLK[1])	$t_{dSIGout}$			200	ns
SIG in setup time[2])	$t_{SIGin\ S}$	50			ns
SIG in hold time[2])	$t_{SIGin\ H}$	100			ns

[1]) Pins SO1A...SO3B; Pins SBA, SBB as output
[2]) Pins SI1A...SI3B; Pins SBA, SBB as input