SIEMENS

ISDN Primary Access Transceiver (IPAT) PEB 2235

Preliminary Data **CMOS IC**

Type	Ordering code	Package
PEB 2235-C	Q67100-H8604	C-DIP-28
PEB 2235-N	Q67100-H8685	PL-CC-28 (SMD)
PEB 2235-P	Q67100-H8603	P-DIP-28

The ISDN Primary Access Transceiver IPAT™ (PEB 2235) is a monolithic CMOS device which implements the analog receive and transmit line interface functions to primary rate PCM carriers. It may be programmed or hard wires to operate in 24 channel (T1) or 32 channel (CEPT) carrier systems.

The IPAT recovers clock and data using an adaptively controlled receiver threshold. It is transparent to ternary codes and shapes the output pulse following the AT&T Technical Advisory # 34 or CCITT G.703. The jitter tolerance of the device meets the latest CCITT (I.431 DRAFT), latest US recommendations (TR-TSY-000312), NTT specification and many other specifications by AT&T/BELLCORE. Diagnostic facilities are included.

Specially designed line interface circuits simplify the tedious task of protecting the device against overvoltage damage while still meeting the return loss requirements.

The IPAT is suitable for use in a wide range of voice and data applications such as for connections of digital switches and PABX's to host computers, for implementations of primary ISDN subscriber loops as well as for terminal applications. The maximum range is determined by the maximum allowable attenuation.

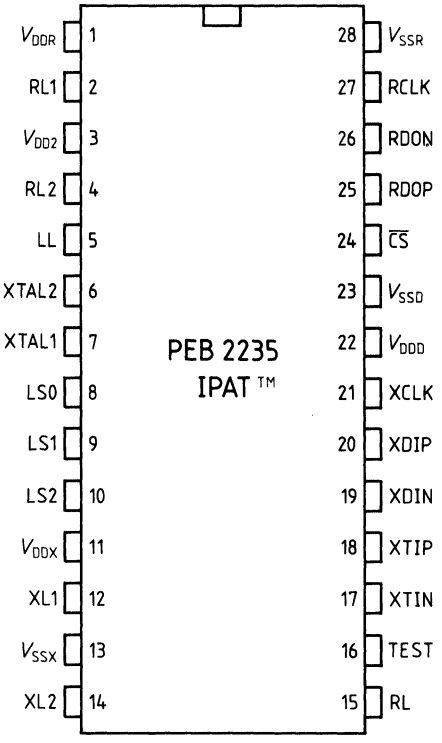
The IPAT's power consumption is mainly determined by the line length and type of the cable.

Features

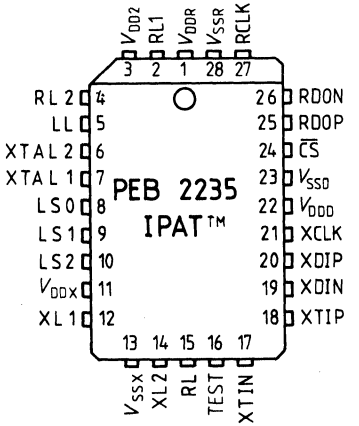
- ISDN line interface for 1544 and 2048 kbit/s (T1 and CEPT)
- Data and clock recovery
- Transparent to ternary codes
- Low transmitter output impedance for a high return loss with reasonable protection resistors (CCITT G.703 requirements for the line input return loss fulfilled).
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 applications
- Jitter specifications of CCITT I.431 DRAFT, TR-TSY-000312 and many AT&T / BELLCORE publications met.
- Jitter tolerance of receiver: 0.43 UI s
- Implements local – and remote loops for diagnostic purposes
- Monolithic line driver for a minimum of external components
- Low power, reliable 2 µ CMOS technology

Pin Configurations
(top view)

P-DIP-28



PL-CC-28



Pin Definition and Functions

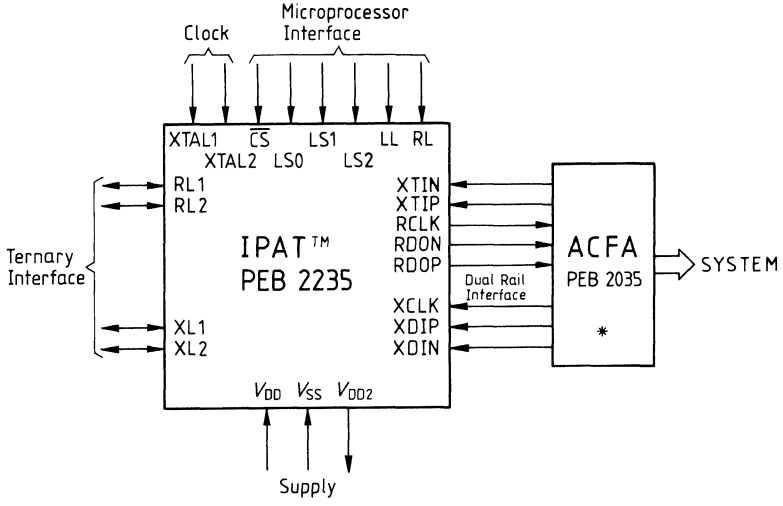
Pin No.	Symbol	Input (I) Output (O)	Function
1	$V_{DD\,R}$	I	Positive power supply for the receive subcircuits
2	RL1	I	Line receiver pin 1
3	$V_{DD\,2}$	O	Reference voltage output for tapping the input transformer
4	RL2	I	Line receiver pin 2

Pin Definition and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
5	LL	I	Local loopback: A high level selects the device for the local loopback mode
6 7	XTAL2 XTAL1	I I	Reference clock input: A 24704 or 32768 kHz crystal reference should be connected to these pins for T1 or CEPT applications, respectively. It is also possible to connect an external precision clock to XTAL1 leaving XTAL2 unconnected. The external reference must be provided at full CMOS levels.
8 9 10	LS0 LS1 LS2	I I I	Line length select: determine to what extent the line output signals are preshaped prior to transmission
11	$V_{DD\,X}$	I	Positive power supply for transmit subcircuits
12	XL1	O	Line transmitter pin 1
13	$V_{SS\,X}$	I	Ground for transmit subcircuits
14	XL2	O	Line transmitter pin 2
15	RL	I	Remote loopback: A high level puts the device to the remote loopback mode
16	TEST	I	Test input not connected or connected to V_{DD}
17 18	XTIP XTIN	I I	Positive and negative transmit test data inputs, active low, half or fully bauded
19 20	XDIP XDIN	I I	Positive and negative transmit data inputs, active low, half or fully bauded
21	XCLK	I	Transmit clock
22	$V_{DD\,D}$	I	Positive power supply for the digital subcircuits
23	$V_{SS\,D}$	I	Power ground supply for the digital subcircuits
24	$\overline{CS}$	I	$\overline{\text{Chip Select}}$: A low level selects the PEB 2235 for a register write operation
25 26	RDOP RDON	O O	Receive data output positive and negative, fully bauded, active low
27	RCLK	O	Receive clock
28	$V_{SS\,R}$	I	Power ground supply for receive subcircuits

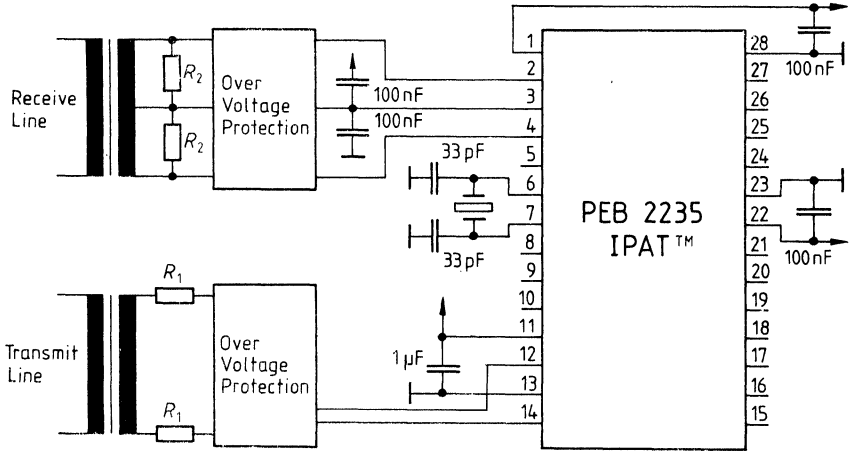
Logic Symbol and Wiring

Figure 1
Logic Diagram of the IPAT



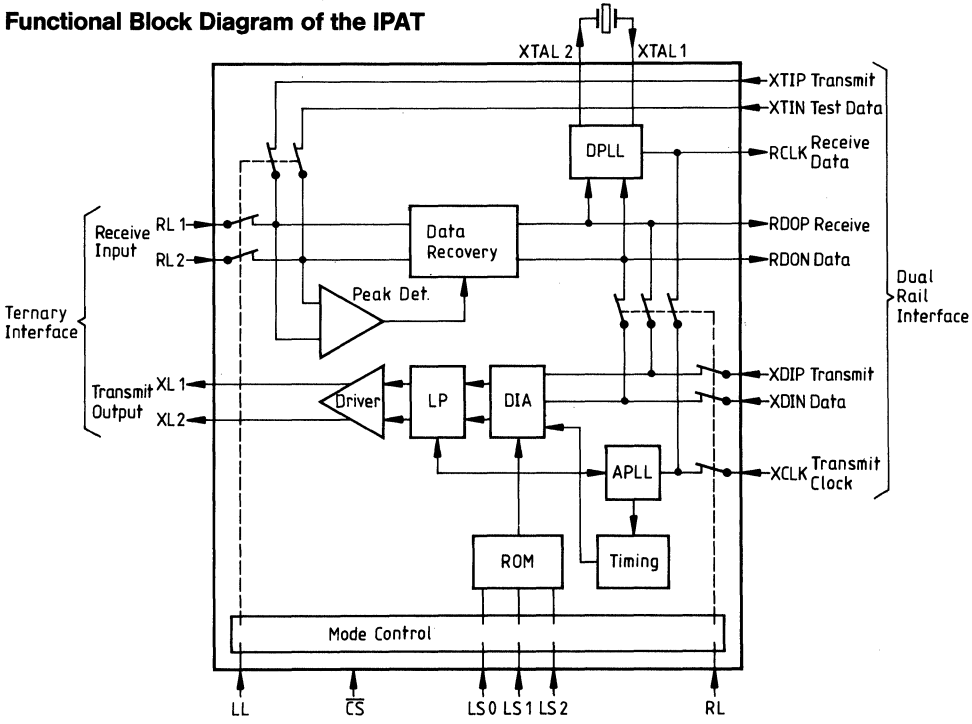
* Advanced CMOS Frame Aligner ACFA (PEB 2035) for frame alignment, coding/decoding, error checking, elastic buffering and facility signaling

Figure 2
External Wiring of the IPAT



Functional Description

Figure 3
Functional Block Diagram of the IPAT



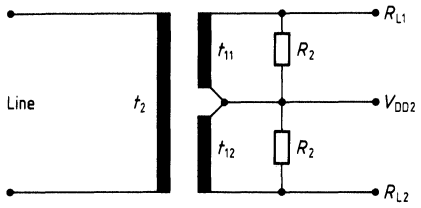
Receiver

Basic Functionally

The receiver recovers data from the ternary coded signal at the ternary interface and outputs it as two unipolar signals at the dual rail interface. One of the lines carries the positive pulses, the other the negative pulses of the ternary signal.

The signal at the ternary interface is received at both ends of a center-tapped transformer as shown in **figure 4.**

Figure 4
Receiver Configuration



The transformer is center-tapped at the IPAT-B side. The recommended transmission factors for the different line characteristic impedances are listed in **table 1.**

Table 1

Recommended Receiver Configuration Values

Application	T1	CEPT	
Characteristic Impedances [Ω]	100	120	75
$R_2 \pm (2.5\%)$ [Ω]	28.7	60	60
$t_2 : t_1 = t_2 : (t_{11} + t_{12})$	69 : 52 69 : (26 + 26)	52 : 52 52 (26 + 26)	41 : 52 41 : (26 + 26)

Wired in this way the receiver has a return loss

$a_r > 12$ dB for $0.025\, f_b \leq f \leq 0.05\, f_b$,

$a_r > 18$ dB for $0.05\ f_b \leq f \leq 1.0\, f_b$ and

$a_r > 14$ dB for $1.0\ \ f_b \leq f \leq 1.5\, f_b$,

with f_b being 2048 kHz. Thus is complies with CCITT G.703.

The receiver is transparent to the logical 1's polarity and outputs positive logical 1's on RDOP and negative logical 1's on RDON. RDON and RDOP are active low and fully bauded. The comparator threshold to detect logical 1's and logical 0's is automatically adjusted to be 56% of the peak signal level.

Provided the noise is below 10 $\mu V/\sqrt{Hz}$ the bit error rate will be less than 10^{-7}. The data is stable, and hence may be sampled at the falling edge of the recovered clock RCLK.

PLL

A digital PLL extracts the receive clock RCLK from the data stream received at the RL1 and RL2 lines. The PLL uses as a reference either a crystal at XTAL1 and XTAL2 or an external oscillator at XTAL1. The IPAT-B does not remove any jitter. Since the crystal frequency is 16 times the input data frequency the digital PLL adds an jitter of max. 0.0625 UI (unit intervals). In the absence of an input signal the jitter of clock, and recovered data lies within the tolerance range of the used reference.

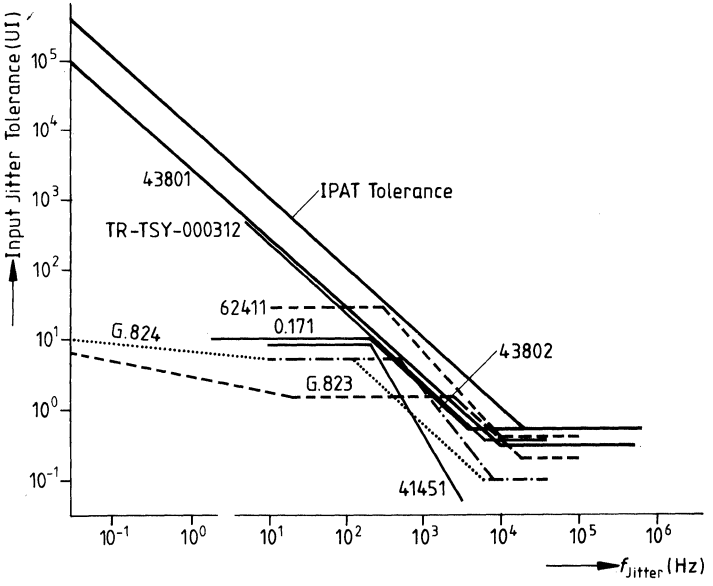
Input Jitter Tolerance

The IPAT-B receiver's tolerance to input jitter complies to CCITT and AT&T requirements for CEPT and T1 application.

Figure 5 shows the curves of the different input jitter specifications stated above as well as the IPAT-B performance at the S1/S2 interfaces.

As can be seen in **figure 5**, the curve for the IPAT-B at low frequencies describes a 20 dB/decade fall off, and at high frequencies are horizontal (at least 0.43 UI).

Figure 5
Comparison of Input Jitter Specification and IPAT Performance



Transmitter

Basic Functionality

The transmitter transforms unipolar data to ternary (alternate bipolar) return to zero signals of the appropriate shape. The unipolar data is provided at XDIP (positive pulses) and XDIN (negative pulses), synchronously with the transmit clock XCLK. XDIP and XDIN are active low and can be half or fully bauded.

The transmitter includes a programmable pulse shaper to satisfy the requirements of the AT&T Technical Advisory # 34 at the cross connect point for T1 applications. The pulse shaper is programmed via the line length selection pins LS0, LS1 and LS2. The pulse shape is formed using an analog PLL, which multiplies by four the transmit clock XCLK. This signal is used internally to generate the four segment/bit transmit pulse (CEPT: two segment/bit).

For T1 application the line length selection supports both low capacitance cable with a characteristic line capacitance of C' ≤ 40 nF/km = 65 nF/mile (e.g. MAT, ICOT) and higher capacitance cable with a characteristic line capacitance of 40 nF/km ≤ C' ≤ 54 nF/km (65 nF/mile ≤ C' ≤ 87 nF/mile) e.g. ABAM, PIC and PULP cables. This ensures that for various cable types the signal at the DSX-1 cross connect point complies with the pulse shape of the AT&T Technical Advisory #34.

The line length is selected programming the LS0, LS1 and LS2 pins as shown in **table 2.**

Table 2
Line Length Selection

LS2 LS1 LS0		PIC/PULP-Cable range/m	ICOT-Cable range/m*
0 0 0	CEPT	–	–
0 0 1	T1/NTT	0 – 35	0 – 80
0 1 0	T1	25 – 65	65 – 145
0 1 1	T1	55 – 95	130 – 210
1 0 0	T1	85 – 125	195 – 275
1 0 1	T1	115 – 155	260 – 340
1 1 0	T1	145 – 185	325 – 405
1 1 1	T1	175 – 210	390 – 470

Note: For ICOT-cable the characteristic impedance is 140 Ω

By selecting an all-zero code for LS0, LS1 and LS2 the IPAT-B can be adopted for CEPT applications.

The pulse shape for NTT applications is achieved by using the same line length selection code as for the lowest T1 cable range. To switch the device into a low power dissipation mode, XDIP and XDIN should be held high.

The transmitter requires an external step up transformer to drive the line. The transmission factor and the source serial resistor values can be seen in **figure 6** and **table 3** for the various applications.

Figure 6
Transmitter Configuration

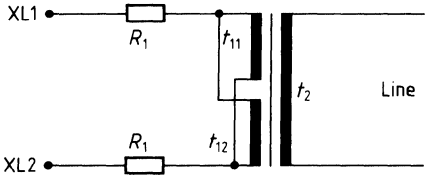


Table 3
Transmitter Configuration Values

Application	T1	CEPT	
Characteristic line impedance [Ω]	100	120	75
$t_{11}:t_2 = t_{12}:t_2$	26:69	26:52	26:41
R_1 (± 2.5%) [Ω]	4.3	15	15

Wired in this way the transmitter has a return loss

$a_r > 8$ dB for $0.025\, f_b \leq f \leq 0.05\, f_b$,

$a_r > 14$ dB for $0.05\, f_b \leq f \leq f_b$ and

$a_r > 10$ dB for $1.0\, f_b \leq f \leq 1.5\, f_b$.

with f_b being 2048 kHz (CEPT applications). A termination resistor of 120 Ω is assumed.

In T1 applications the return loss is heigher than 10 dB.

Please note, that the transformer ratio at the receiver is half of that at the transmitter. The same type of transformer can thus be used at the receiver and at the transmitter. At the transmitter the two windings are connected in parallel, at the receiver in series. Thus, unbalances are avoided.

Output Jitter

In the absence of any input jitter the IPAT-B generates an output jitter at most 0.014 UI in CEPT and 0.01 UI in T1 applications.

Local Loopback

The local loopback mode disconnects the receive lines RL1 and RL2 from the receiver. Instead of the signals coming from the line the data provided at XTIP and XTIN is routed through the receiver. The XDIN and XDIP signals continue to be transmitted on the line. The local loopback occurs in response to LL going high.

Remote Loopback

In the remote loopback mode the clock and data recovered from the line inputs RL1 and RL2 are routed back to the line outputs XL1 and XL2 via the transmitter. As in normal mode they are also output at RDOP, RDON and RCLK. XDIP and XDIN are disconnected from the transmitter. In this mode a device jitter of 0.0765 UI for CEPT and 0.0725 UI for T1 is added.

The remote loopback mode is selected by a high RL signal.

Please keep in mind that the IPAT-B is not capable of removing jitter. Therefore in remote loopback mode jitter is not reduced. In normal applications, however, the data stream being output from the IPAT-B runs through an elastic buffer (e.g. the ACFA PEB 2035) which itself reduces jitter.

Microprocessor Interface

The IPAT-B is fully controlled by five parallel data lines (LS0, LS1, LS2, LL and RL) and one control line ($\overline{CS}$). To adapt the device to a standard microprocessor interface the low state of $\overline{CS}$ is decoded from the microprocessor address, $\overline{CS}$, $\overline{WR}$ and $\overline{ALE}$ lines.

To hardwire the chip, $\overline{CS}$ must be fixed to ground.

Loss of Signal Indication

In the case that the signal at the line receiver input (pins RL1, RL2) becomes smaller than $V_{IN} \leq 0.4\ V_{OP}$ loss of signal is indicated. This voltage value correspondings to a line attenuation of about 12 dB in the CEPT case. This is performed by turning both signals RDOP, RDON after at least 16 bits simultaneously to 5 V, i.e. a logical 0 or both lines. The following ACFA processes this indication for the system.

Operational Description

- **Reset**

  In order to work properly, the IPAT™-B needs to be started with a software reset. This is done by simultaneously setting the pins RL and LL to logical 1 (i.e. 5 V) far at least one bit period and releasing both lines thereafter simultaneously.

  It is possible to connect the pins RL and LL to V_{DD} and to consequently turn on the power supply. In this way a power-up reset is achieved.

- **Selection of CEPT of T1 Application**

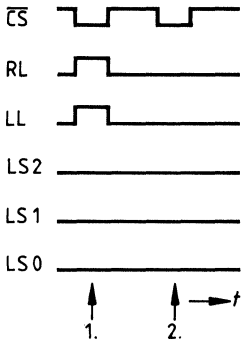
  Besides the crystal frequency the selections of CEPT or T1 application is achieved by setting the pins LS2, LS1, LS0 simultaneously with the reset to 000 for CEPT application or to a T1 line length code (001...111 **see table 2**).

- **Line Length Selection**

  In the second step the line selection code has to be given. This will be normally the same one as in the first step.

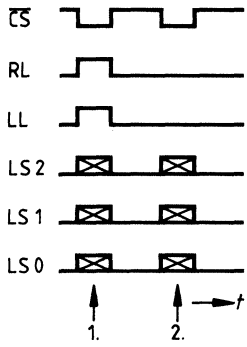
The following figures explain the procedure in some examples.

Figure 7
Timing of Software Programming for CEPT Applications



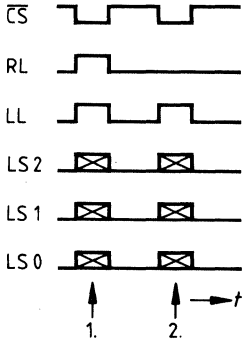
1. Reset and selection of CEPT application
2. Regular operation in CEPT application

Figure 8
Timing of Software Programming for T1 Application



1. Reset and selection of T1 application
2. Regular operation in T1 application with selected line code

Figure 9
Timing of Software Programming for LL Operation at CEPT or T1 Application



1. Reset
2. Local loop and line code selection

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	Pins
L-input voltage	V_{IL}	−0.4	0.8	V		All pins except RLx, XLx, XTALx, $V_{DD\,2}$
H-input voltage	V_{IH}	2.0	V_{DD}+0.4	V		
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA	
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD}−0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$	
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	$0\ V < V_{IN} < V_{DD}$ to 0 V $0\ V < V_{OUT} < V_{DD}$ to 0 V	
Peak voltage of a mark (CEPT) Peak voltage of a mark (T1)	$V_{X\,CEPT}$ $V_{X\,T1}$	2.7 1.8 1.8	3.3 3.4 3.4	V V V	wired according **figure 6** and **table 3** T1 application: depending on line length	XL1, XL2
Transmitter output impedance	R_X		0.3	Ω		
Transmitter output current	I_X		50 150	mA mA	CEPT application T1 application: depending on line length	
Receiver input peak voltage of a mark	V_R*	0.4	2.5	V	BER 10^{-7}, wired according **figure 4** **table 1**	RL1, RL2
Receiver input threshold	$V_{R\,TH}$		56	%	of mark peak	
Voltage at V_{DD2}	$V_{DD\,2}$	2.4	2.6	V		
L-input voltage	$V_{XTAL\,IL}$	−0.4	1.0	V		XTAL1, XTAL2
H-input voltage	$V_{XTAL\,IH}$	4.0	V_{DD}+0.4	V		
Input leakage current	I_{XTALI}		10	µA	$0\ V \le V_{IN} \le V_{DD}$ to 0 V	
Operation power supply current	I_{CC}	40 55	100 220	mA mA	CEPT application T1 application, min value for all zeros, max value for all ones and max lines length for T1 appl.	

* measured against V_{DD2}

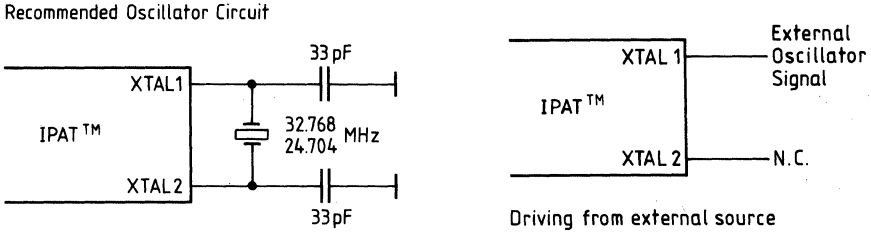
Capacitances

$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limit Values		Unit	Pins
		min.	max.		
Input capacitance	C_{IN}		10	pF	all except RLx, XLx, XTALx
Output capacitance	C_{OUT}		15	pF	all except RLx, XLx, XTALx
Input capacitance	C_{IN}		7	pF	RLx
Output capacitance	C_{OUT}		20	pF	XLx
Load capacitance	C_{LD}		10	pF	XTALx

Recommended Oscillator Circuits

Figure 10
Oscillator Circuits



If no crystal is used XTAL1 has to be connected to an external precision clock source and XTAL2 left unconnected.

In CEPT applications, the oscillator circuit should provide a 32768 kHz clock, in T1 applications 24704 kHz.

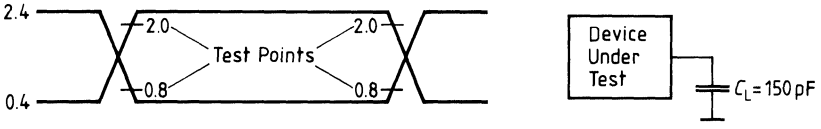
If no signal is received, a ± 50 ppm frequency range of the oscillator circuit transforms into a ± 50 ppm range of the RCLK signal.

AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

Figure 11

Oscillator Circuits



Except from the ternary and clock interface, inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown in **figure 13.**

In the receive direction the IPAT-B adds at most 0.0625 UI intrinsic jitter. This is true for both jitter free as well as jitterized inputs. In transmit direction the IPAT-B adds at most 0.014 UI of jitter in CEPT and 0.01 UI in T1 applications measured in the frequency range 20 Hz...185 kHz.

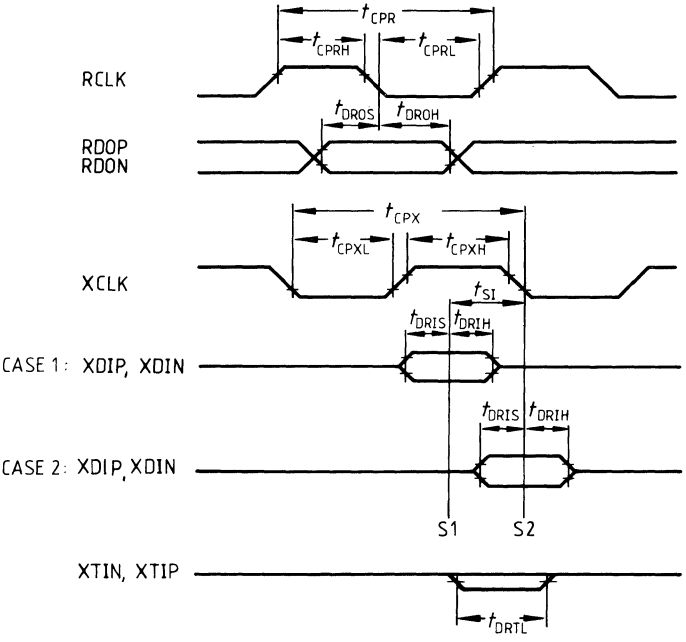
In both directions the device does not remove or attenuate the accumulated jitter.

Dual Rail Interface

RDOP, RDON, XDIP, XDIN, XTIP, XTIN are active low.

Figure 12

Timing of the Dual Rail Interface

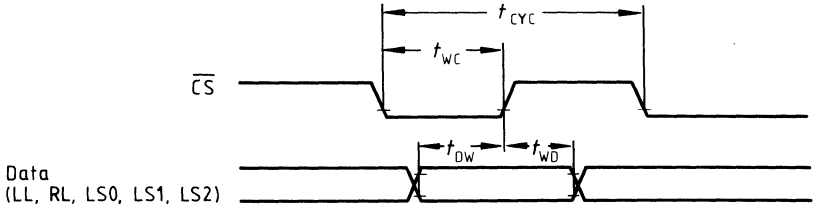


Dual Rail Interface Timing Parameter Values

Parameter	Symbol	Limit Values				Unit
		PCM 30		PCM 24		
		min.	max.	min.	max.	
RCLK clock period	t_{CPR}	typ. 488		typ. 648		ns
RCLK clock period low	$t_{CPR\,L}$	235		310		ns
RCLK clock period high	$t_{CPR\,H}$	235		310		ns
Dual rail output setup	$t_{DRO\,S}$	230		300		ns
Dual rail output hold	$t_{DRO\,H}$	230		300		ns
XCLK clock period	t_{CPX}	typ. 488		typ. 648		ns
XCLK clock period low	$t_{CPX\,L}$	80	300	100	430	ns
XCLK clock period high	$t_{CPX\,H}$	125	350	170	500	ns
Sampling intervall	t_{SI}	55	67	75	87	ns
Dual rail input setup	$t_{DRI\,S}$	25		25		ns
Dual rail input hold	$t_{DRI\,H}$	25		25		ns
Dual rail test low	$t_{DRT\,L}$	170		220		ns

Microprocessor Interface

Figure 13
Timing of the Microprocessor Interface

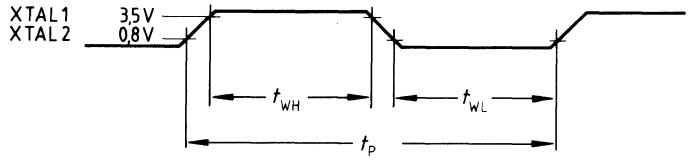


Parameter	Symbol	Limit Values		Unit
		min.	max.	
$\overline{CS}$ pulse width	t_{WC}	60		ns
Data set up time to $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{CS}$	t_{WD}	10		ns
Cycle Time	t_{CYC}	120		ns

XTAL Timing

Figure 14

Timing of XTAL1/XTAL2



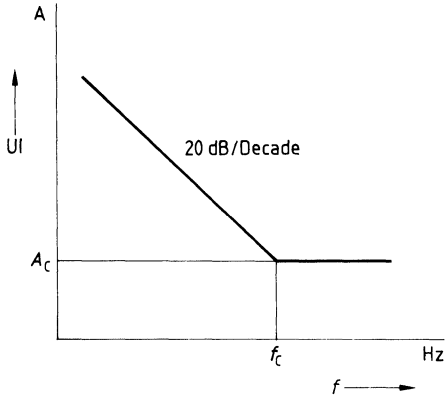
Clock Rail Interface Timing Parameter Values

Parameter		Symbol	Limit Values min.	typ.	max.	Unit
Clock period of crystal/clock	CEPT	t_P		30.5		ns
	T1	t_P		40.5		ns
High phase of crystal/clock	CEPT	t_{WH}	10			ns
	T1	t_{WH}	14			ns
Low phase of crystal/clock	CEPT	t_{WL}	10			ns
	T1	t_{WL}	14			ns

Ternary Interface – Receiver

Figure 15

IPAT Receive Jitter Tolerance



IPAT Receive Jitter Tolerance

Parameter		Symbol	Limit Values min.	max.	Unit
Corner frequency	CEPT	f_C	40		kHz
	T1	f_C	30		kHz
Corner amplitude	CEPT	A_C	0.43		UI
	T1	A_C	0.43		UI

Ternary Interface – Transmitter

The IPAT-B meets both CCITT and T1 pulse template requirements.

Figure 16

Pulse Template at the Transmitter Output for CEPT Applications

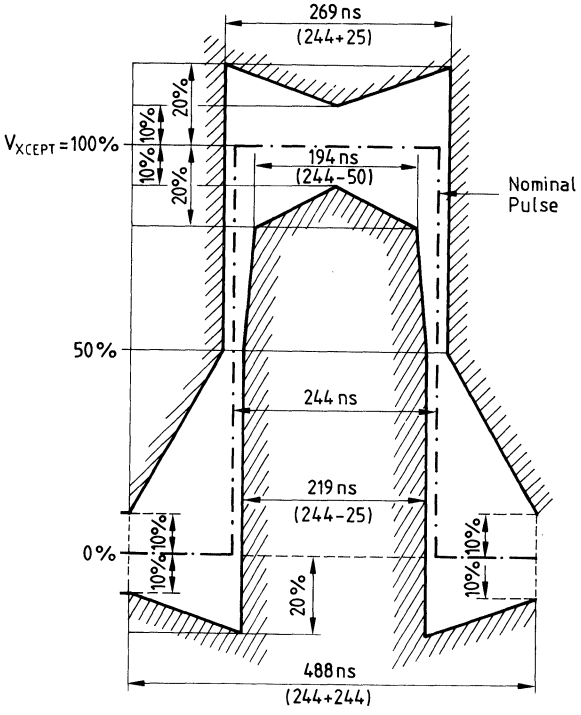


Figure 17

T1 Pulse Shape at the Cross Connect Point

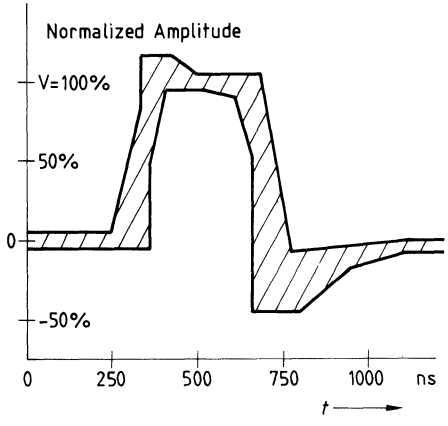


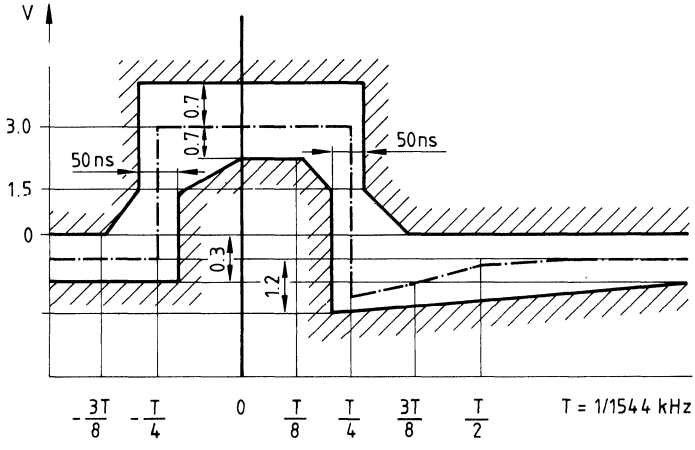
Table 4

T1 Pulse Template Corner Points at the Cross Connect Point

Maximum Curve	Minimum Curve
(0, 0.05)	(0, -0.05)
(250, 0.05)	(350, -0.05)
(325, 0.80)	(350, 0.50)
(325, 1.15)	(400, 0.95)
(435, 1.15)	(500, 0.95)
(500, 1.05)	(600, 0.90)
(675, 1.05)	(650, 0.50)
(725, -0.07)	(650, -0.45)
(1100, 0.05)	(800, -0.45)
(1250, 0.05)	(925, -0.20)
	(1100, -0.05)
	(1250, -0.05)

Figure 18

Pulse Shape at NTT Interface



Overvoltage Tolerance

To prevent the IPAT from being damaged by overvoltage (i.e. from lightning), external devices like diodes or resistors have to be connected to one or both sides of the line interface transformers. Thus, overvoltage peaks are cut off. However, some residual overvoltage may remain.

The IPAT simplifies the task of designing external protection circuit. Its transmitter exhibits a low line impedance so that reasonable external resistors can be connected to the line outputs. **Figure 6** with the element values of **table 3** gives an example of how an overvoltage protection against residual overvoltages at the ternary interface can be accomplished. The solution shown also meets the stated return loss requirements.

A similar consideration applies to the receiver. The resistors R2 of **figure 4** provide protection against residual overvoltages by attenuating voltages of both polarities across RL1 and RL2.

The maximum input current allowed to reach the IAPT pins under overvoltage conditions is given as a function of the width of a rectangular input current pulse according to **figure 18. Figure 19** shows the curve of the maximum allowed input current across the pins RL1 and RL2, **figure 20** across the pins XL1 and XL2.

Figure 18

Measurement of Overvoltage Stress

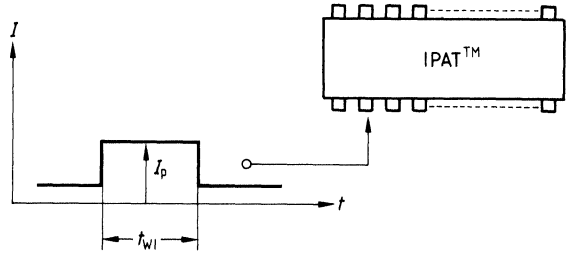


Figure 19

Tolerated Input Current at the RL1,2 Pins

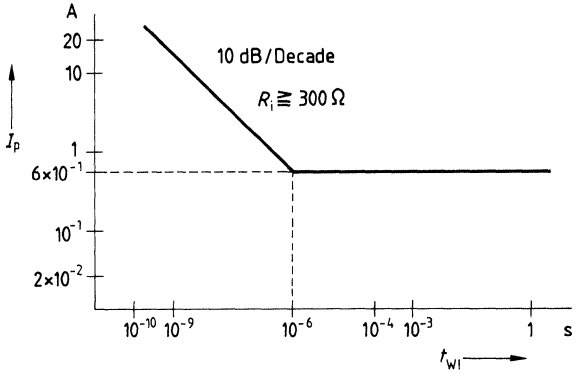
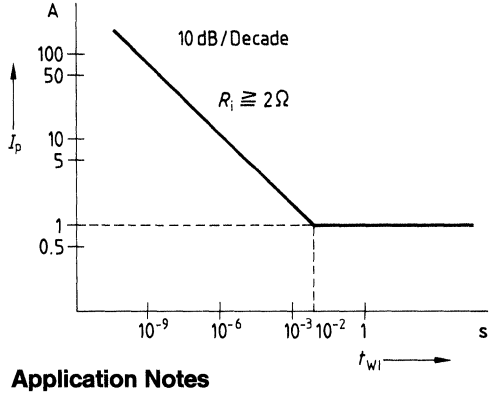


Figure 20

Tolerated Input Current at the XL1,2 Pins



Application Notes

The high transmitter output currents of up to 160 mA require a careful consideration of the on board power supply and ternary interface output line routing.