General Description

In addition to four-wire S-interface terminals, the IOM architecture also supports two-wire terminals for PBX applications. A survey of PBX-loop conditions demonstrates that typically 95% of the subscriber loops show line lengths below 2 km. Therefore, a more economical solution which is optimized to these shorter loop lengths is required.

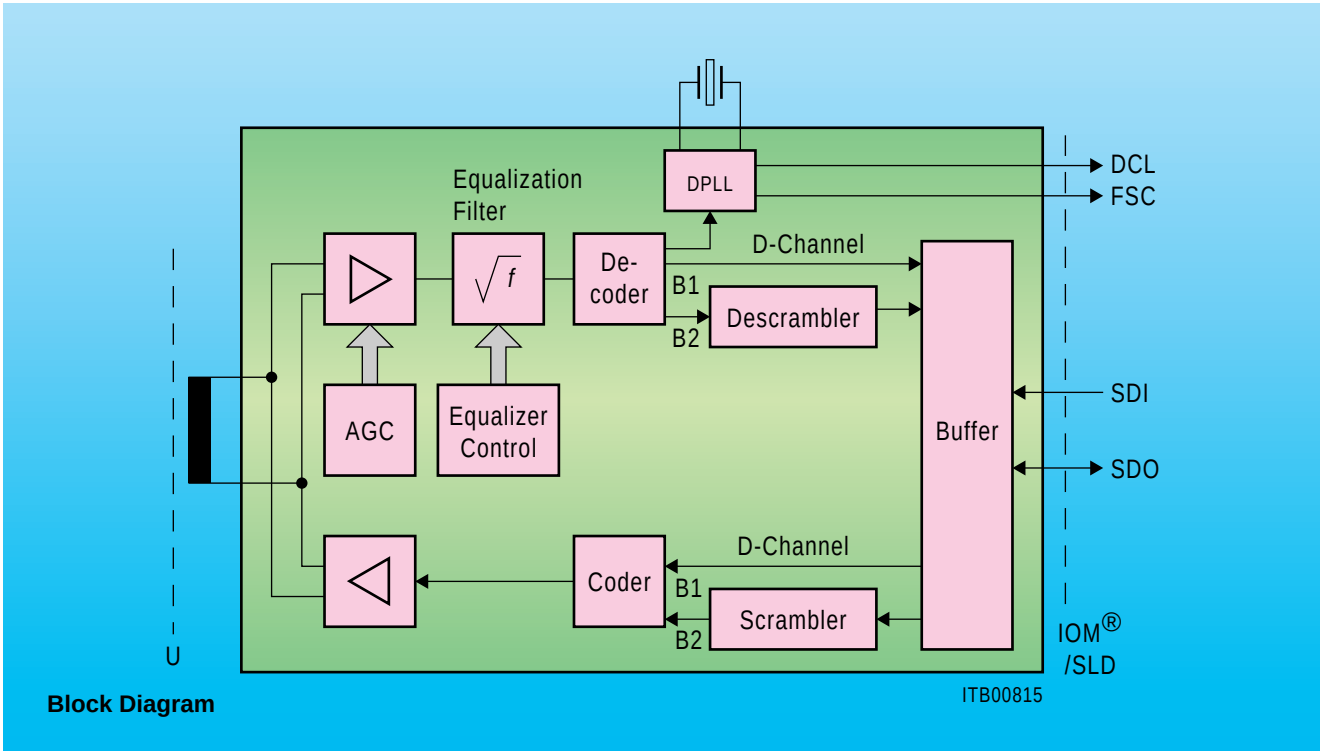
A time-compression multiplex concept has been chosen which – for separation of direction – divides the framing into a transmit and receive section. Taking synchronization bits and line conditions into account, a clock rate of 384 kbit/s, twice as high as for the S-bus, has been found to be optimal with respect to time compression, interference line attenuation and delay. The transceiver uses AMI coding, scrambling, automatic gain control and $\sqrt{f}$-equalizing to obtain excellent transmission quality.

From a system point of view, the IOM-compatible IBC is compatible with the IEC or SBC/SBCX as well as with the EPIC/ELIC and the IDEC on digital line card applications. Similar to the other components, the device is designed in 2-µm CMOS technology resulting in low power consumption of less than 80 mW in the active state.

Type	Package
PEB 2095-N	P-LCC-28-2 (SMD)
PEB 2095-P	P-DIP-24-1 (not for new designs)

Features

- Half-duplex burst-mode two-wire transceiver
- 144-bit/s user bit rate (B+B+D)
- 384-kHz line clock rate including maintenance and synchronization
- U_{P0} interface, industry standard for 2-wire PBXs (AMI-line code)
- IOM-interface compatible (IOM-1 or IOM-2)
- Adaptive line equalization (SC filter)
- Recovery of clock and frame signals from data stream
- Activation/deactivation procedure according to CCITT recommendation
- Awake in power-down mode
- Switching of test loops
- Transmission range up to 3.5 km with 0.6-mm wire
- 2-µm CMOS technology
- Low power consumption
  Active: 80 mW (typ.)
  Power-down: 6 mW (typ.)



Block Diagram