

VIP

Single-Chip VLSI ISDN Subscriber Processor

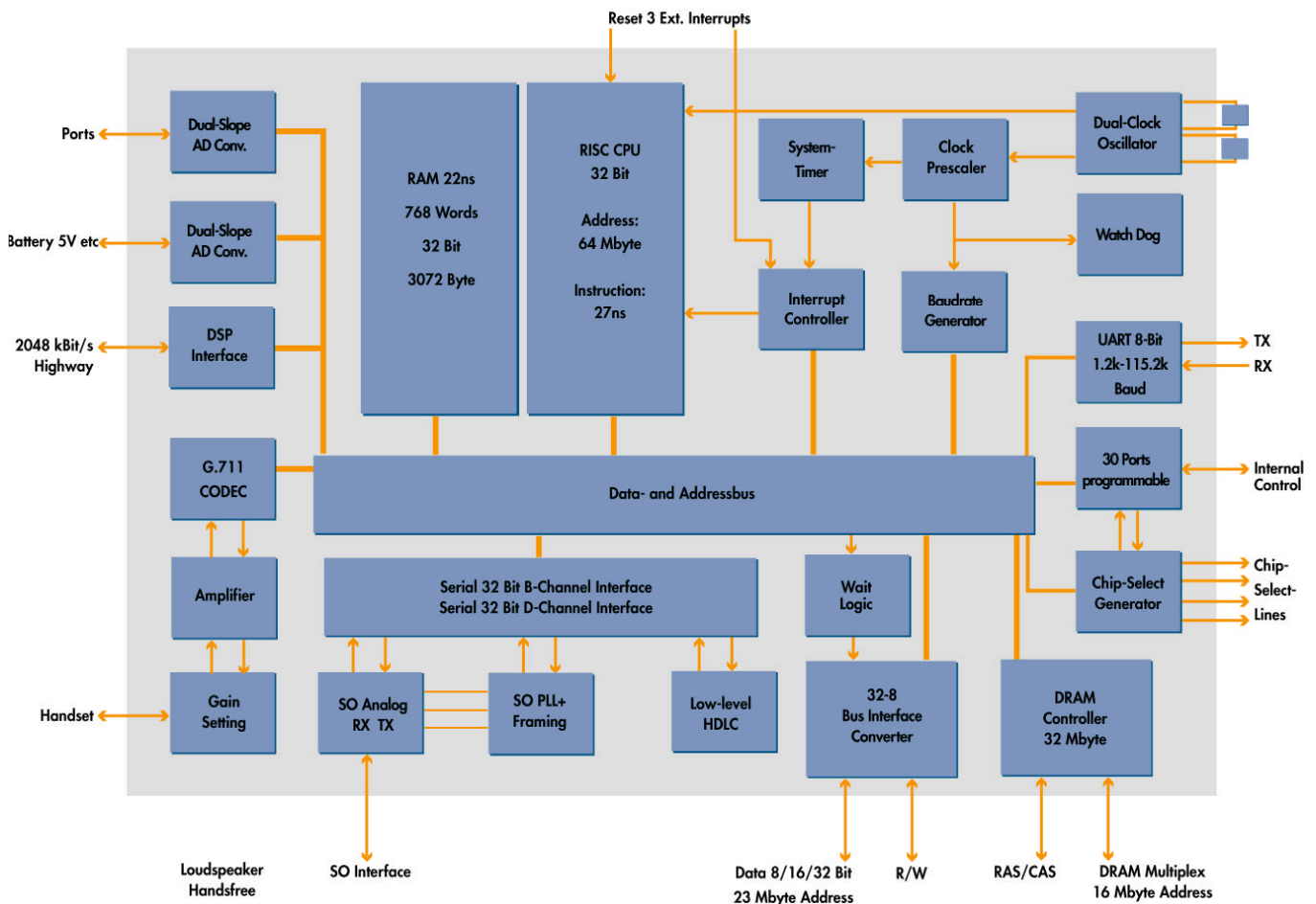
OVERVIEW

The VLSI ISDN Subscriber Processor (VIP) offers in a single device a powerful programmable engine for ISDN subscriber communications. It includes most of the circuitry required to implement a full featured ISDN terminal, making it the most highly integrated and cost competitive solution.

FEATURES

- Full static operation
- 32-bit RISC ARM processor running at 36.8 MHz
- 3 Kbytes of on-chip high speed cache SRAM
- Programmable clock speed
- Programmable power-down with event wake-up
- Support of 8/16/32-bit wide external SRAM/ ROM/ DRAM (54ns to 1.2µs access time)
- Fast Interrupt controller, fully maskable for all peripherals
- On-chip SO-Interface transceiver containing AFE, data/clock recovery and framing circuitry (conforming to the ITU spec. I.430)
- Low level D-channel data link controller providing Layer 1 and basic Layer 2 functions in hardware
- G.711 PCM CODEC, complete with Programmable AFE, tone ringer out-

Block Diagram





put, additional input and output together with sophisticated powerdown modes

- Internal 14-bit linear PCM format

APPLICATIONS

- ISDN terminal equipment
- Domestic and digital PABX telephones
- H.320 videophones
- Integrated PC communications ISDN-to-DECT
- domestic and business applications
- ISDN-to-PCMCIA communication cards

ISDN Interface Configurations

The VIP is designed to facilitate the integration of basic-rate ISDN terminal equipment. The device supports two 64 Kbit/s and one 16 Kbit/s channels (ie. 2B+D), and interfaces to the ISDN network via an on-chip SO-Interface. Fig(2) shows the application area for VIP in relation to the standard ISDN network termination reference points. In this figure, the SO-Interface defines the interface for connection of individual ISDN terminals. It separates the user terminal equipment from the network related communications functions. The U-Interface defines the full duplex signal on the digital subscriber line.

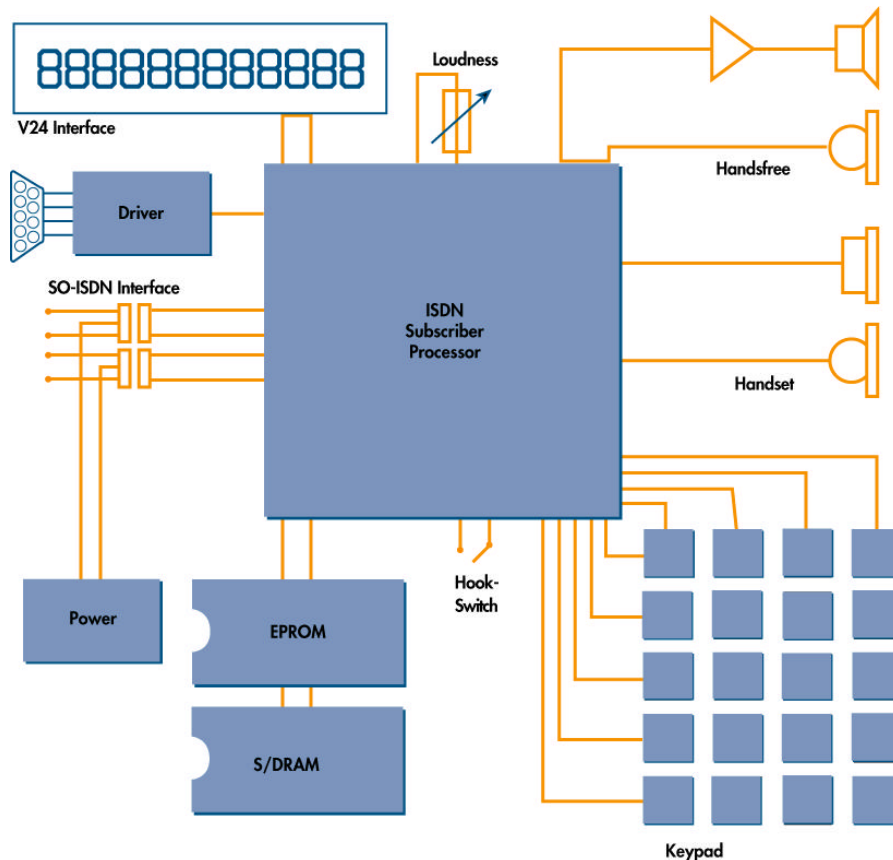
FUNCTIONAL DESCRIPTION

The VIP is a highly integrated solution facilitating the implementation of ISDN terminal equipment such as feature-phones and terminal adapters. The device has been designed using VLSI's FSB™ methodology. Each of these FSB™ elements will now be discussed in turn.

ARM RISC Core

At the heart of VIP is the ARM RISC processor. This high performance, low power CPU allows many of the functions previously implemented in hardware to be performed in software, thereby reducing silicon area and cost.

System Configuration



On-Chip Memory

The VIP contains 3 Kbytes of on-chip cache memory. This allows-speed critical routines to run at maximum speed.

Memory Interface

The Memory Interface allows the connection of external 8-, 16- or 32-Bit static RAM/ROM. An internal DRAM timing controller supports non sequential and fast page mode DRAM access.

SO-Interface

The SO-interface transceiver allows direct connection to the SO-Interface Bus. It contains all the Layer 1 functions defined in the ITU I.430 specification. The D-channel data link controller provides the Layer 1 and the basic Layer 2 frame formatting. The remaining Layer 2 functions are performed by software running on the ARM. All bits in the So-Frame are accessible to the ARM.

10M2 Interface

For communication with other serial devices such as CODEC's DSP's or peripherals, the VIP incorporates a full duplex serial port with a 64-bit serial - parallel converter to drive standard 8-bit telecom or 14-bit linear CODEC's.

Audio CODEC

The G.711 PCM CODEC contains an analog front end (AFE) that allows direct connection to both a telephone handset as well as a handsfree microphone and speaker. A tone ringer output is also provided for call alert etc.

UART

The ACTIS includes an on-chip UART, allowing serial communications with a personal computer etc. This simple full duplex serial interface has a complexity equivalent to an 8251 UART. Baud rates are programmable from 1.2 kBaud up to a maximum of 115.2

kBaud Keypad Interface The keypad interface consists of 6 inputs with internal pull-down resistors and an Or-Gate. The row lines are derived using a number of I/O ports. The occurrence of a key action – push and release – can generate a maskable interrupt, which under the control of the ARM can be used to determine the key depressed.

Power Management

A flexible power management controller enables the system clock speed to programmed down to stop.

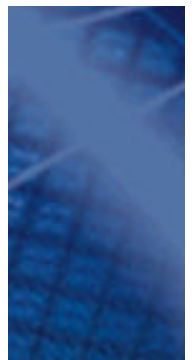
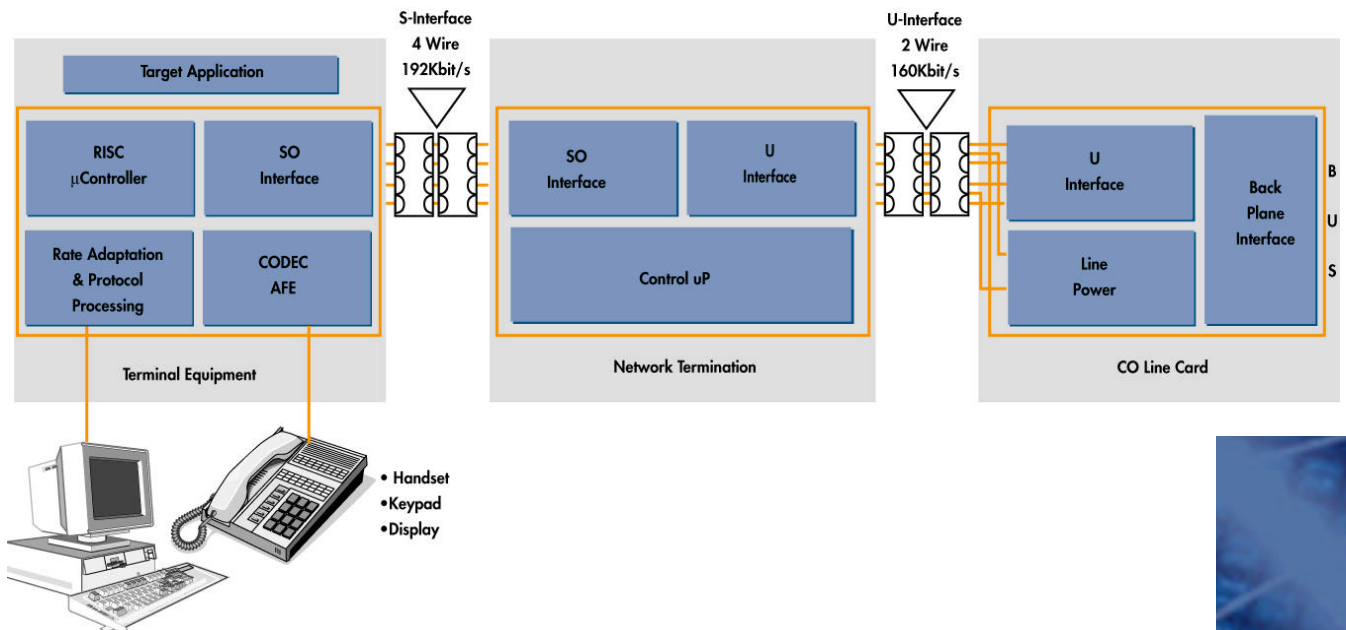
I/O Ports

All Ports are bi-directional and can be programmed to have special functions in the various configurations supported by the VIP.

Technology

The VIP has been designed using VLSI's 0.6µ CMOS, triple-layer metal, mixed-signal technology, and is available in a 144 pin MQFP package.

ISDN Interface Configuration



DEVELOPMENT ENVIRONMENT

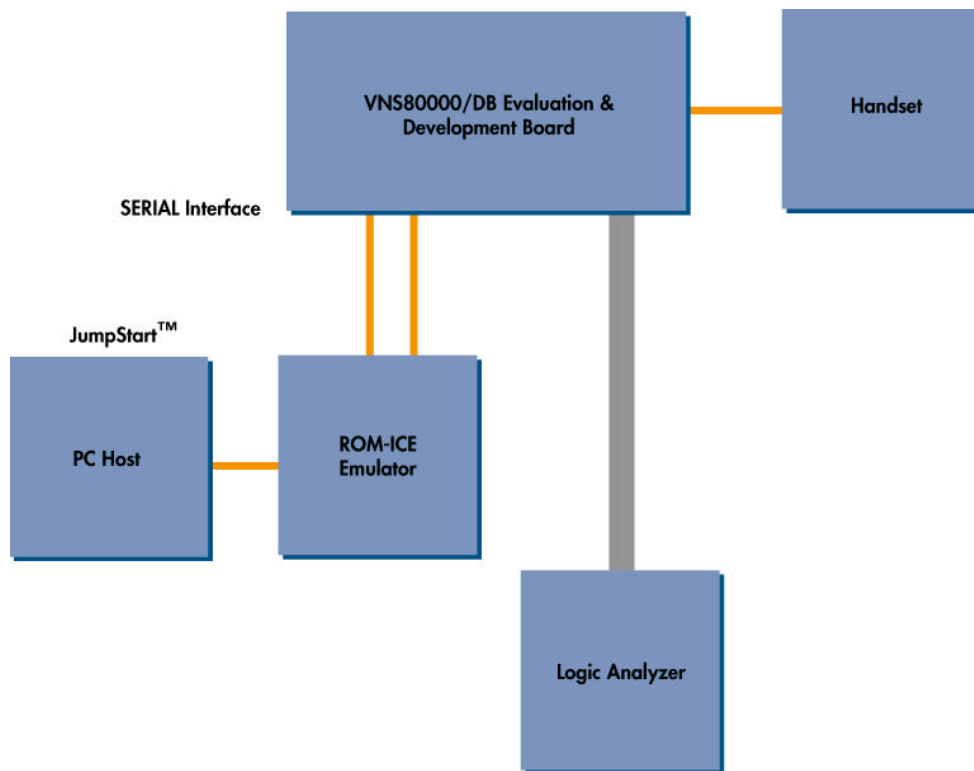
To support the integration of applications based on the VIP, VLSI offers a complete set of hardware development tools as well as demonstration and evaluation systems. Fig(3) shows a typical development environment.

Since both VIP and ACTIS (Single-

chip VLSI ISDN data processor) use a compatible design methodology, the same development tool environment can be used to develop either ISDN data communications equipment or ISDN Terminals, thereby maintaining our objective of a common platform for different applications. This is mandatory to reduce time-to-market.

ACTIS/VIP Development Board
The Development Board, (VNS80000/DB) serves the dual function of product evaluation and development. From a hardware point of view it functions as and ISDN telephone and can be used as a hardware & software development platform connecting to the ISDN S0-bus as defined by the ITU I.430 and ETSI, ETS 300 012 specifications.

Serial Interface



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