FINAL

Am79C30A/32A

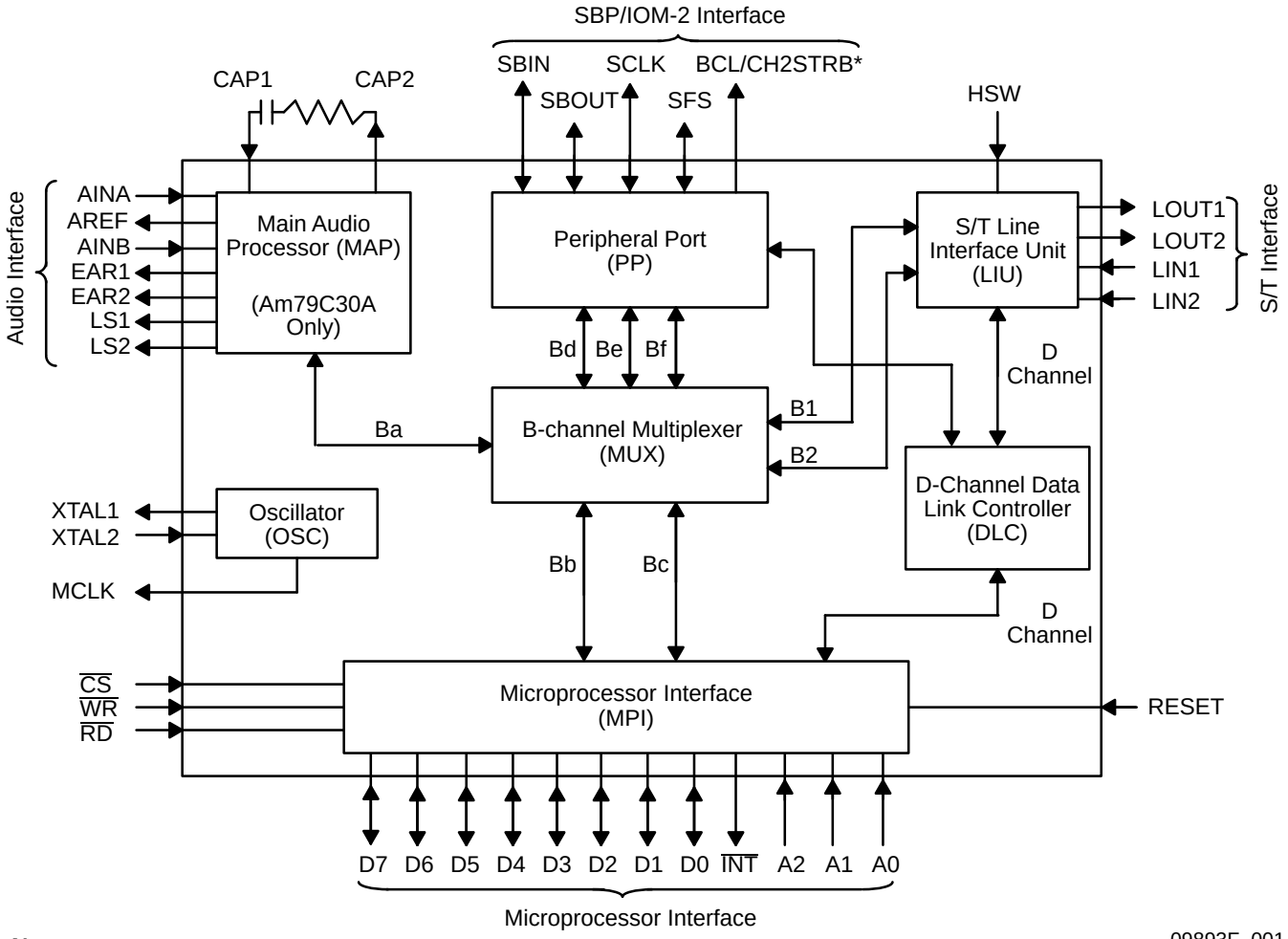
Digital Subscriber Controller™ (DSC™) Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Combines CCITT I.430 S/T-Interface Transceiver, D-Channel LAPD Processor, Audio Processor (DSC device only), and IOM-2 Interface in a single chip**
- **Special operating modes allow realization of CCITT I.430 power-compliant terminal equipment**
- **S- or T-Interface Transceiver**
  - —Level 1 Physical Layer Controller
  - —Supports point-to-point, short and extended passive bus configurations
  - —Provides multiframe support
- **Certified protocol software support available**
- **CMOS technology, TTL compatible**
- **D-channel processing capability**
  - —Flag generation/detection
  - —CRC generation/checking
  - —Zero insertion/deletion
  - —Four 2-byte address detectors
  - —32-byte receive and 16-byte transmit FIFOs

BLOCK DIAGRAM



09893F–001

Note:

**BCL/CH2STRB signal present for PLCC and TQFP packages only.*

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DISTINCTIVE CHARACTERISTICS (continued)

- **Audio processing capability (DSC circuit only)**
  - —Registers for implementation of software-based speaker phone algorithms
  - —Dual audio inputs
  - —Earpiece and loudspeaker drivers
  - —Codec/filter with A/μ selection
  - —Programmable gain and equalization filters
  - —Programmable sidetone level
  - —Programmable DTMF, single tone, progress tone, and ringer tone generation
  - —Programmable on-chip microphone amplifier
- **Pin and software compatible with the Am79C32A ISDN Data Controller (IDC™) Circuit. The Am79C32A is used in data-only applications.**

GENERAL DESCRIPTION

The Am79C30A Digital Subscriber Controller (DSC) Circuit and Am79C32A ISDN Data Controller (IDC) Circuit, shown in the Block Diagram, allow the realization of highly-integrated Terminal Equipment for the ISDN. The Am79C30A/32A is fully compatible with the CCITT-I-series recommendations for the S and T reference points, ensuring that the user of the device may design TEs which conform to the international standards.

The Am79C30A/32A provides a 192-Kbit/s full duplex digital path over four wires between the TE located on the subscriber's premises and the NT or PABX linecard. All physical layer functions and procedures are implemented in accordance with CCITT Recommendation I.430, including framing, synchronization, maintenance, and multiple terminal contention. Both point-to-point and point-to-multipoint configurations are supported.

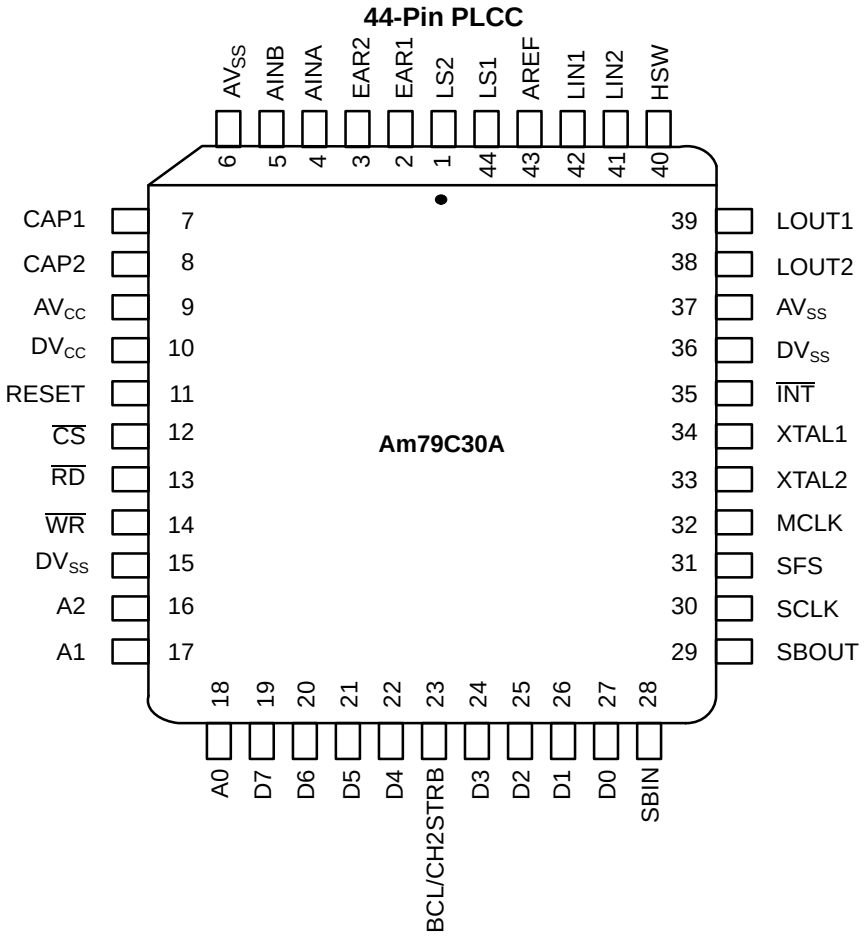
The Am79C30A/32A processes the ISDN basic rate bit stream, which consists of B1 (64 Kbit/s), B2 (64 Kbit/s), and D (16 Kbit/s) channels. The B channels are routed to and from different sections of the Am79C30A/32A under software control. The D channel is partially processed by the DSC/IDC circuit and is passed to the microprocessor for further processing.

The Main Audio Processor (MAP) uses Digital Signal Processing (DSP) to implement a high performance codec/filter function. The MAP interface supports a loudspeaker, an earpiece, and two separate audio inputs. Programmable on-chip gain is provided to simplify use of low output level microphones. The user may alter frequency response and gain of the MAP receive and transmit paths. Tone generators are included to implement ringing, call progress, and DTMF signals.

A Peripheral Port (PP) is provided to allow the B channels to be routed off-chip for processing by other peripherals. This port is configurable as either an industry-standard IOM-2 port, or as a serial bus port (SBP).

The TE design process is simplified by the availability of certified protocol software packages, which provide complete system solutions through OSI Layer 3.

CONNECTION DIAGRAMS
Top View



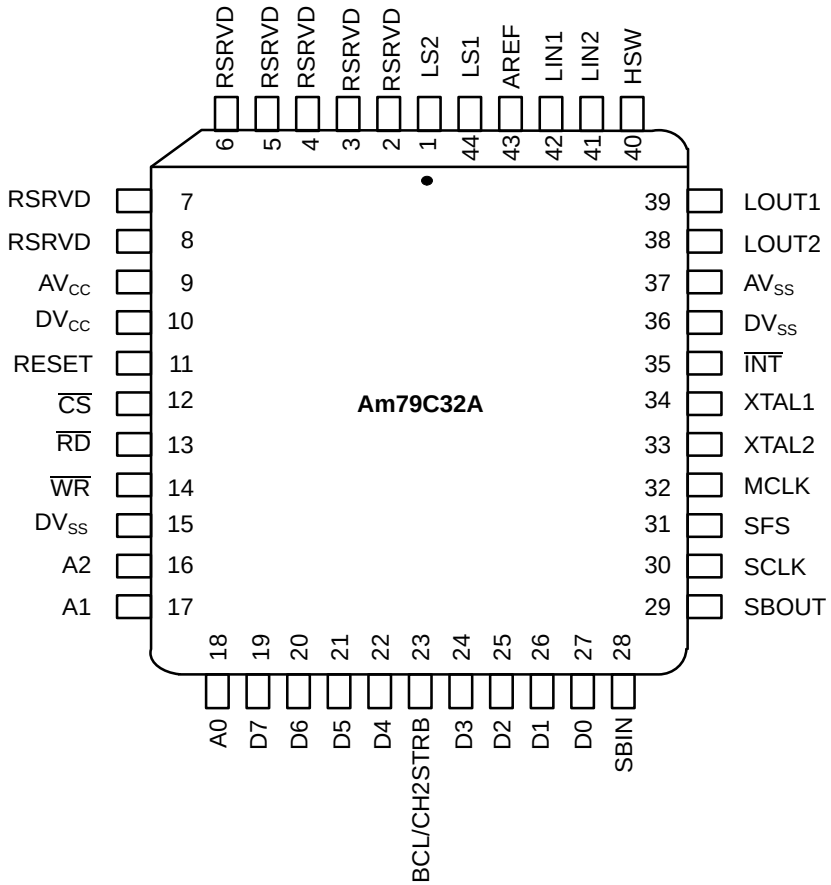
Note:

Pin 1 is marked for orientation purposes.

CONNECTION DIAGRAMS (continued)

Top View

44-Pin PLCC



Note:

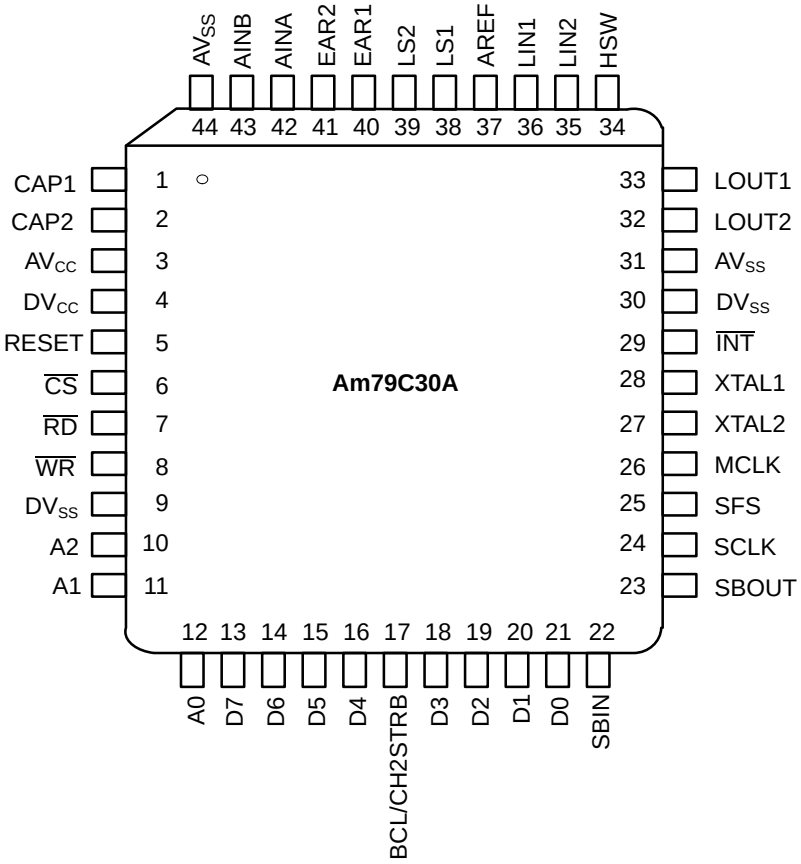
1. Pin 1 is marked for orientation purposes.

2. RSRVD = Reserved pin, should not be connected externally to any signal or supply.

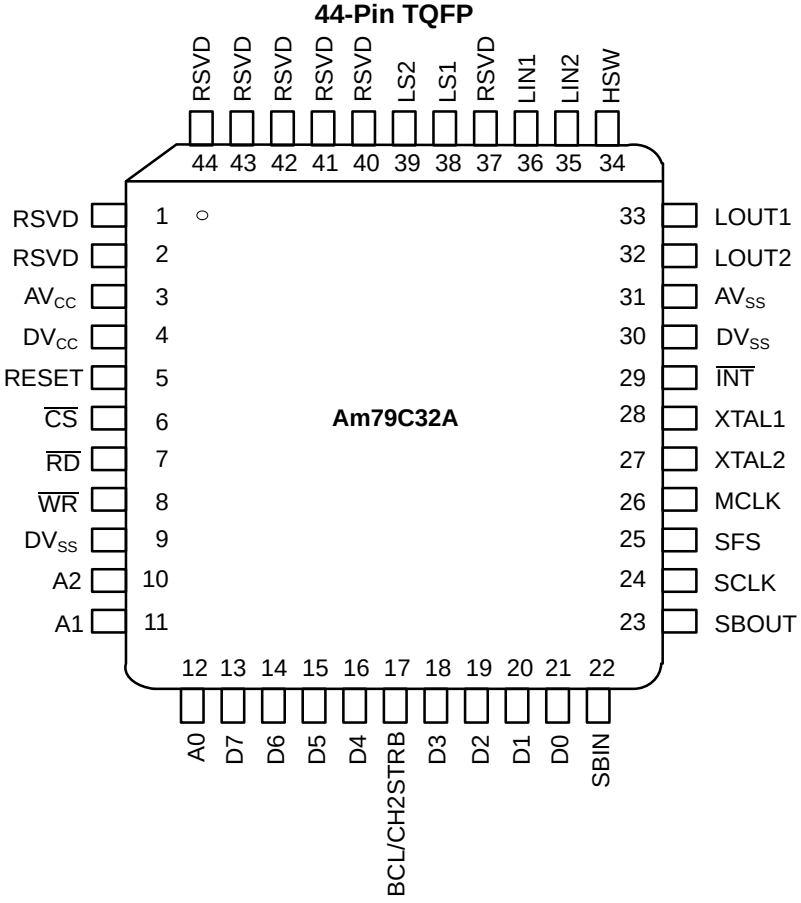
CONNECTION DIAGRAMS (continued)

Top View

44-Pin TQFP



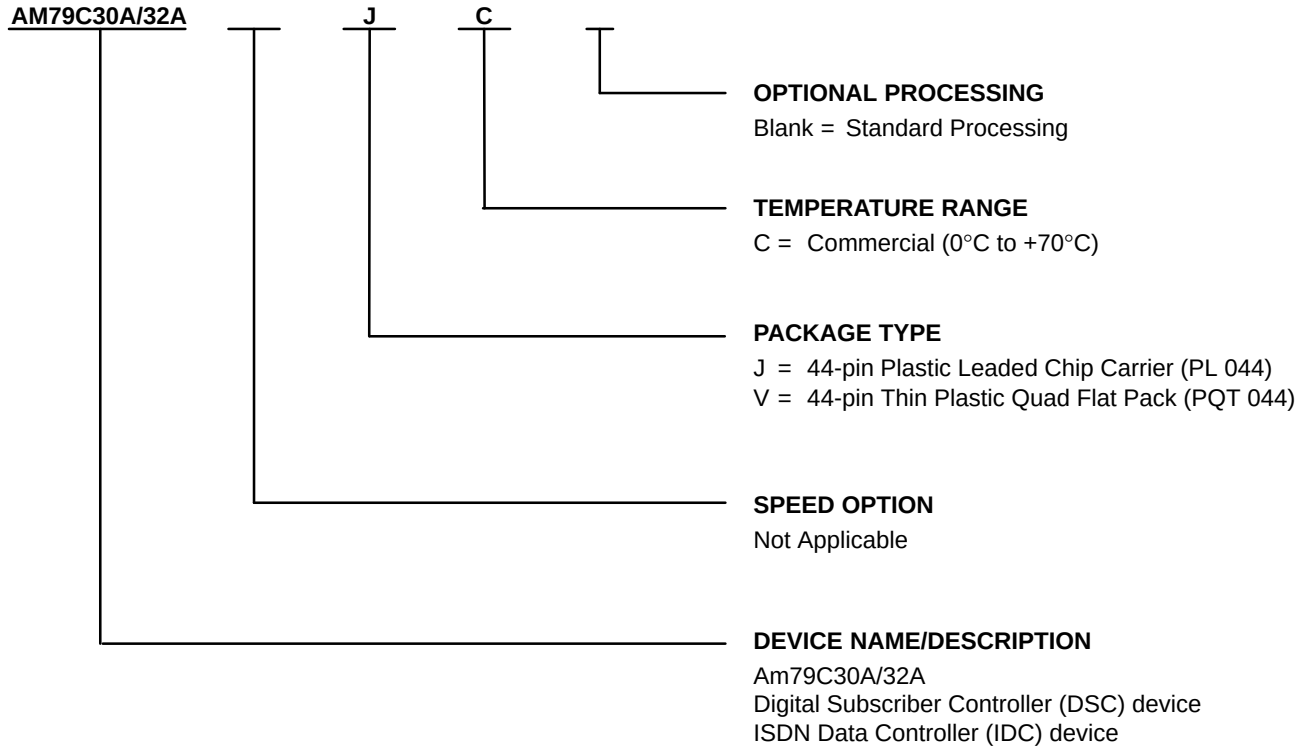
44-Pin TQFP



ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C30A	JC, VC
AM79C32A	JC, VC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

PIN DESCRIPTION*

Line Interface Unit (LIU)

HSW
Hook-Switch (Input)

The HSW signal indicates if the hook-switch is on or off hook. This signal may be generated with a mechanical switch wired to ground with a pull-up resistor to $V_{CC.}$ Any change in the HSW state causes an interrupt.

LIN1, LIN2
Subscriber Line Input (Differential Inputs)

The LIN1 and LIN2 inputs interface to the subscriber (S reference point) via an isolation transformer. LIN2 is the positive input; LIN1 is the negative input. These pins are not TTL compatible.

LOUT1, LOUT2
Subscriber Line Output (Differential Outputs)

The LOUT1 and LOUT2 line driver output signals interface to the subscriber line at the S reference point via an isolation transformer and resistors. LOUT2 is the positive S-interface driver (sources current during a High mark), and LOUT1 is the negative S-interface driver (sources current during Low mark). For multipoint applications, all TEs must maintain the same polarity on the S Interface. These pins are not TTL compatible**.**

Main Audio Processor (MAP)

All MAP pins are analog, and therefore are not TTL compatible.

AINA, AINB
Analog (Inputs)

These analog inputs allow for two separate analog (audio) inputs to the transmit path of the codec/filter. Input signals on either of these pins must be referenced to AREF.

AREF
Analog Reference (Output)

This is a nominal 2.25-V reference voltage output for biasing the analog inputs. When the MAP is disabled, this pin is high impedance.

CAP1, CAP2
Capacitor/Resistor (CAP1, Input; CAP2, Output)

An external resistor and capacitor are connected in series between these pins. These components are needed for the integrator in the Analog-to-Digital Converter (ADC).

EAR1, EAR2
Earpiece Interface (Differential Outputs)

EAR1 and EAR2 are the outputs from the receive path of the codec/filter. These differential outputs can directly drive a minimum load of 540 ohms.

LS1, LS2
Loudspeaker Interface (Differential Outputs)

LS1 and LS2 are push-pull outputs which can directly drive a minimum load of 40 ohms.

Microprocessor Interface (MPI)

A2–A0
Address Line (Inputs)

A2, A1, and A0 signals select source and destination registers for read and write operations on the data bus.

$\overline{CS}$
Chip Select (Input)

$\overline{CS}$ must be Low to read or write to the Am79C30A/32A. Data transfer occurs over the bidirectional data lines (D7–D0).

D7–D0
Data Bus (Bidirectional with High-Impedance State)

The eight bidirectional data bus lines are used to exchange information with the microprocessor. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). A High on the data bus line corresponds to a logic 1, and Low corresponds to a logic 0. These lines act as inputs when both $\overline{WR}$ and $\overline{CS}$ are active and as outputs when both $\overline{RD}$ and $\overline{CS}$ are active. When $\overline{CS}$ is inactive or both $\overline{RD}$ and $\overline{WR}$ are inactive, the D7–D0 pins are in a high-impedance state.

$\overline{INT}$
Interrupt (Output)

An active Low output on the $\overline{INT}$ pin informs the external microprocessor that the Am79C30A/32A needs interrupt service. $\overline{INT}$ is updated once every 125 µs. The $\overline{INT}$ pin remains active until the Interrupt Register (IR) is read or the Am79C30A/32A is reset.

RESET
Reset (Input)

Reset is an active High signal which causes the Am79C30A/32A to immediately terminate its present activity and initialize to the reset condition. When reset returns Low, the Am79C30A/32A enters the Idle mode. The MCLK output remains active while RESET is held High.

Note

** All signal levels are TTL compatible unless otherwise stated.*

$\overline{RD}$
Read (Input)

The active Low read signal is conditioned by $\overline{CS}$ and indicates that internal information is to be transferred onto the data bus. A number of internal registers are user accessible. The contents of the accessed register are transferred onto the data bus after the High to Low transition of the $\overline{RD}$ input.

$\overline{WR}$
Write (Input)

The active Low write signal is conditioned by $\overline{CS}$ and indicates that external information on the data bus is to be transferred to an internal register. The contents of the data bus are loaded on the Low to High transition of the $\overline{WR}$ input.

Oscillator (OSC)

MCLK
Master Clock (Output)

The MCLK output is available for use as the system clock for the microprocessor. MCLK is derived from the 12.288-MHz crystal via a programmable divider in the Am79C30A/32A which provides the following MCLK output frequencies: 12.288, 6.144, 4.096, 3.072, 1.536, 0.768, and 0.384 MHz.

XTAL1, XTAL2
External Crystal (Output, Input)

XTAL1 and XTAL2 are connected to an external parallel resonant crystal for the on-chip oscillator. XTAL2 can also be connected to an external source instead of a crystal, in which case XTAL1 should be left disconnected. The frequency must be 12.288 MHz, ± 80 ppm.

Peripheral Port (PP)

SBIN
Serial Data (Input/Output)

When the Peripheral Port is programmed to SBP mode, SBIN operates as an input for serial data. When the Peripheral Port is programmed to IOM-2 mode, SBIN functions as the data input except in the special case of IOM-2 Slave mode, when it becomes an open-drain output during part or all of the IOM-2 frame, or when deactivated.

SBOUT
Serial Data (Input/Output)

When the Peripheral Port is programmed to SBP mode, SBOUT operates as an output for serial data. When the Peripheral Port is programmed to IOM-2 mode, SBOUT functions as the data output except in the special case of IOM-2 Slave mode when it becomes an input during part or all of the IOM-2 frame.

SCLK
Serial Data Clock (Input/Output)

When the PP is programmed to SBP mode, SCLK outputs a 192-kHz data clock, which may be inverted under software control. When the PP is programmed to IOM-2 Master mode, SCLK outputs a 1.536-MHz 2X data clock. In IOM-2 Slave mode, SCLK functions as the clock input. The SCLK pin defaults to a high-impedance state upon reset, but becomes active after any MUX connection is made or if the PP is programmed to IOM-2 Master mode.

SFS
Serial Frame Sync (Input/Output)

In SBP mode, SFS outputs an 8-kHz frame synchronization signal. SFS is an output in IOM-2 Master mode, and an input in IOM-2 Slave mode. As an output, SFS is active for 8-bit periods. The SFS pin defaults to a high-impedance state upon reset, but becomes active after any MUX connection is made or if the PP is programmed to IOM-2 Master mode. For SBP mode, the active signal state is Low during Idle and 8 kHz in Active Data Only and Active Voice and Data modes.

BCL/CH2STRB
Bit Clock/SBP Channel 2 Strobe
(Output, Three-state) (present only in PLCC package)

In SBP mode, this pin provides a strobe during the 8-bit times of the second 64-kbit/s data channel. In IOM-2 Master mode, this pin provides a 768-kHz bit clock to aid in the connection of non-IOM-2 devices to the port. In IOM-2 Slave mode, this pin is high-impedance.

Power Supply Pins

PLCC Packages

AV_{CC}	+5-V analog power supply, ±5% (PLCC only)
AV_{SS}	Analog ground (PLCC only)
DV_{SS}	Digital ground (PLCC only)
DV_{CC}	+5-V digital power supply, ±5% (PLCC only)

DIP Packages

V_{CC}	+5-V power supply, ±5% (DIP only)
V_{SS}	Ground (DIP only)

Note:

For best performance, decoupling capacitors should be installed between V_{CC} and V_{SS} as close to the chip as possible. Do not use separate supplies for analog and digital power and ground connections.

FUNCTIONAL DESCRIPTION

Microprocessor Interface (MPI)

The Am79C30A/32A can be connected to any general purpose 8-bit microprocessor via the MPI. The MCLK from the Am79C30A/32A can be used as the clock for the microprocessor. The MPI is an interrupt-driven interface containing all the circuitry necessary for access to the internal programmable registers, status registers, coefficient RAM, and transmit/receive buffers.

Line Interface Unit (LIU)

The LIU connects to the four-wire S Interface through a pair of isolation transformers, one for the transmit and one for the receive direction, as shown in Figure 1.

The receiver section of the LIU consists of a differential receiver, circuitry for bit timing recovery, circuitry for detecting High and Low marks, and a frame recovery circuit for frame synchronization. The receiver converts the received pseudo-ternary coded signals to binary before delivering them to the other blocks of the Am79C30A/32A. It also performs collision detection (E- and D-bit comparison) per the CCITT recommendations so several TEs can be connected to the same S Interface.

The transmitter consists of a binary to pseudo-ternary encoder and a differential line driver which meets the CCITT recommendations for the S Interface.

The Am79C30A/32A can establish multiframe synchronization, receive S bits, and transmit Q bits synchronized to the received frame.

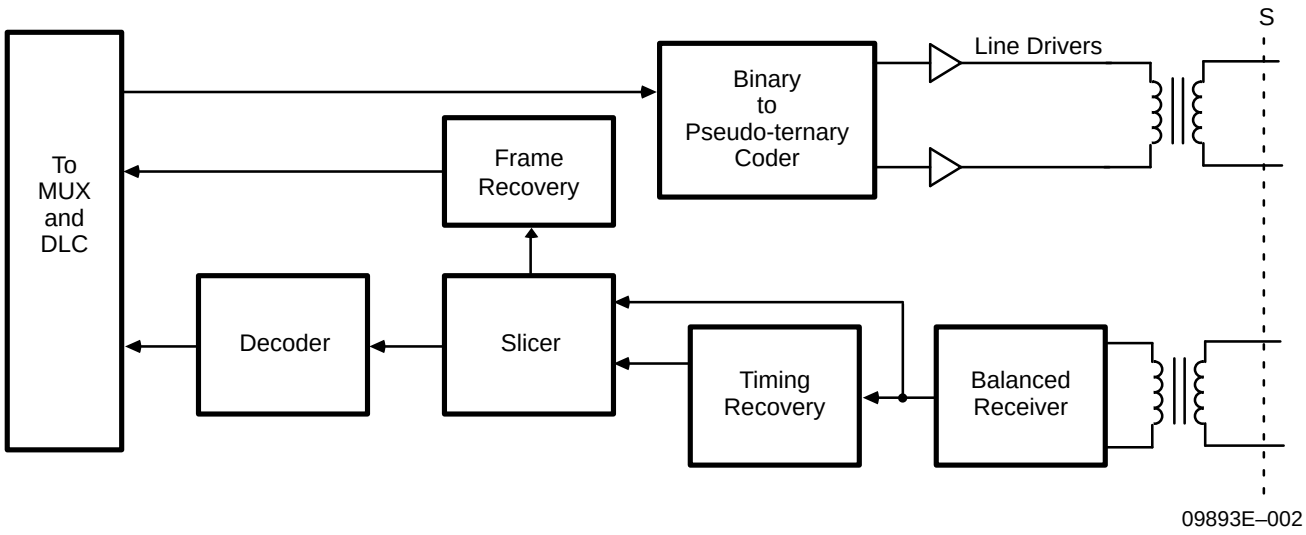


Figure 1. LIU Block Diagram

Main Audio Processor (MAP)

(Am79C30A only)

Overview

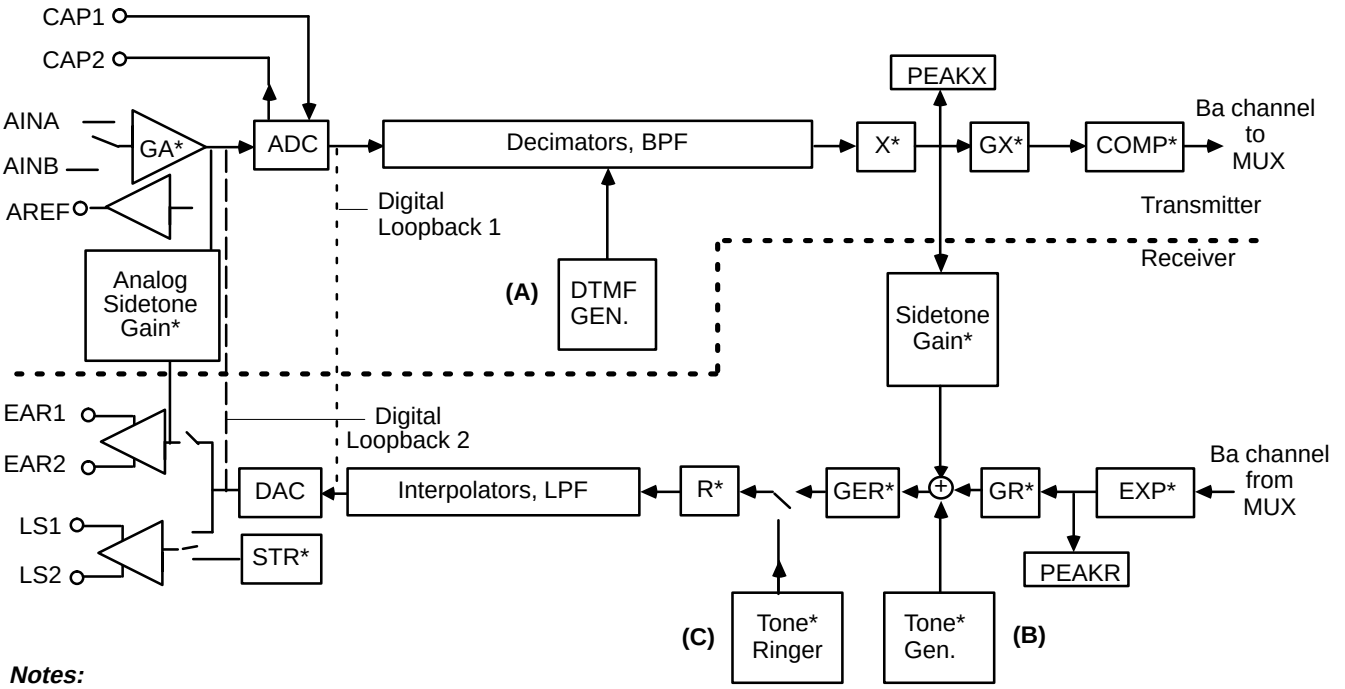
The MAP, as illustrated in Figure 2, implements audio-band analog-to-digital (ADC) and digital-to-analog (DAC) conversions together with a wide variety of audio support functions. Analog interfaces are provided for a handset earpiece, a handset mouthpiece, a microphone, and a loudspeaker. A programmable analog preamplifier is included in front of the A/D converter. The codec and filter functions are implemented using digital signal processing (DSP) techniques to provide operational stability and programmable features. There is one programmable digital gain stage in the transmit path and two in the receive path to allow precise signal level control. Sidetone attenuation is programmable, and programmable equalization filters are present in both the receive and transmit paths in order to modify the frequency response of either or both paths. Tone generation capability is included to allow generation of ringing signals, DTMF tones, and call progress signals. MAP operation is described in detail in the following sections.

Audio Inputs

The audio input port consists of two inputs (AINA and AINB) which are selectable, one at a time, by register programming. Signals applied to these inputs must be AC-coupled.

Earpiece and Loudspeaker Drivers

The earpiece and loudspeaker drivers each consist of amplifiers with differential, low-impedance outputs. The MAP receive path signal may be routed to either of these outputs, or to both outputs simultaneously. Alternatively, the MAP receive path may be routed to the EAR outputs while the Secondary Tone Ringer (STR) is routed to the LS outputs. The EAR drivers can drive loads $\geq$130 ohms between the EAR1 and EAR2 pins, while the LS drivers can drive loads $\geq$40 ohms between the LS1 and LS2 pins. The maximum capacitive-loading between EAR1 and EAR2 or between LS1 and LS2 is 100 pF. The EAR outputs are high-impedance when the MAP is disabled. The LS outputs are high impedance when both the MAP and the Secondary Tone Ringer are disabled.



Notes:

	Minimum	*Default*	*Maximum*	*Step*
GX	*0 dB***	*0 dB*	*12 dB*	*0.5 dB*
GER	*–10 dB***	*0 dB*	*18 dB*	*0.5 dB*
GR	*–12 dB***	*0 dB*	*0 dB*	*0.5 dB*
STG	*–18 dB***	*–18 dB*	*0 dB*	*0.5 dB*
GA	*0 dB*	*0 dB*	*24 dB*	*6.0 dB*
ASTG	*–27 dB***	*∞*	*–6 dB*	*1.5 dB*

** Programmable*

***These registers can also be programmed for infinite attenuation to break the signal path if desired.*

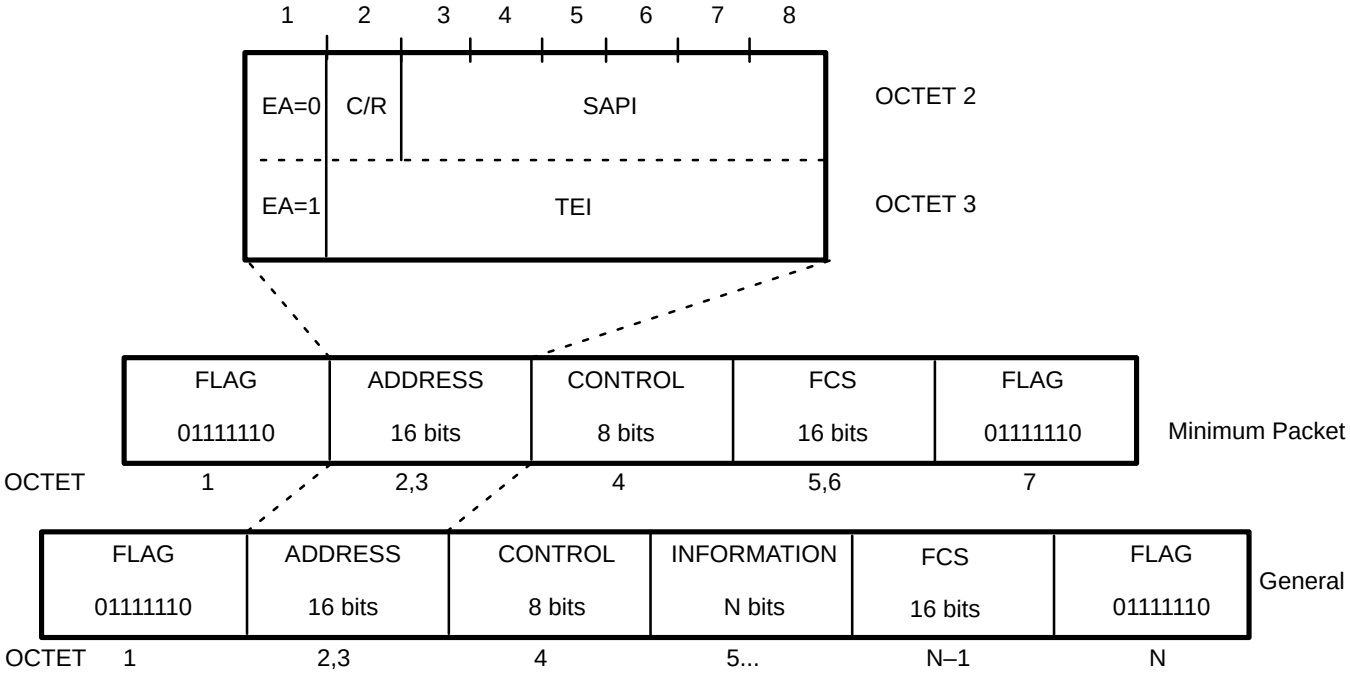
Figure 2. Main Audio Processor Block Diagram

Data Link Controller (DLC)

Overview

A 16-Kbit/s D-channel is time-multiplexed within the frame structure of the S Interface. The data carried by the D channel is encoded using the Link Access Protocol D-channel (LAPD) format shown in Figure 3. The D channel can be used to carry either end-to-end signaling or low-speed packet data. Further information concerning LAPD protocol can be found in the CCITT recommendations. The LIU controls the multiplexing and demultiplexing of the D-channel data between the S Interface and the DLC.

The DLC performs processing of Level-1 and partial Level-2 LAPD protocol, including flag detection and generation, zero deletion and insertion, Frame Check Sequence (FCS) processing for error detection, and some addressing capability. High level protocol processing is done by the external microprocessor. The microprocessor may process the address field in the LAPD frame depending on the programmed state of the DLC. The status of the DLC is held in the status registers and relevant interrupts are generated under user program control. In addition to transmit and receive data FIFOs, the DLC contains a 16-bit pseudo-random number generator (RNG) used in the CCITT D-channel address allocation procedure.



Notes:

EA = Address Field Extension bit
C/R= Command/Response Field bit
SAPI= Service Access Point Identifier
TEI= Terminal Endpoint Identifier
FCS= Frame Check Sequence

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Figure 3. Level-2 Frame Structure Formats

Peripheral Port (PP)

Overview

The purpose of the Peripheral Port is to allow external peripherals to be connected to the DSC/IDC circuit. There are two basic modes of operation, Serial Bus Port mode, and IOM-2 Terminal mode. Within IOM-2 Terminal mode, the DSC/IDC circuit may be configured as any combination of IOM-2 timing/control master or slave. The definition of the Peripheral Port pins depends on the operating mode of the port, as described in Table 1.

Table 1. Pin Operation versus Peripheral Port Modes

Pin	SBP On	Port Disabled	IOM-2 M Activated	IOM-2 M Deactivated	IOM-2 S* Bus Reverse Activated	IOM-2 S* Bus Reverse Deactivated	IOM-2 S No Bus Reverse Activated	IOM-2 S No Bus Reverse Deactivated
SBIN	IN	Z	IN	IN	IN/OD	OD	OD	OD
SBOUT	OUT	Z	OD	Z	OD/IN	Z	IN	Z
SCLK	OUT	Z	OUT	Low	IN	IN	IN	IN
SFS	OUT	Z	OUT	Low	IN	IN	IN	IN
BCL/ CH2STRB	OUT	Z	OUT	Low	Z	Z	Z	Z

IN = Input OUT = Output Z = High Impedance OD = Open Drain Output

Note:

**The Am79C30A is a non-Layer-1 component when operated in the Slave mode; however, it has a microprocessor interface. As a result, it is required to change the direction of its I/O pins at certain times in order to communicate with both the upstream Layer-1 device and any downstream peripheral devices. In the IOM-2 Slave mode, the direction of data flow is reversed with respect to the DSC circuit during Sub-frame 0 and during the deactivated state. The rule is that the upstream Layer-1 device only uses Sub-frame 0 and does not reverse its pins. Any non-Layer-1 component that does not contain a microprocessor interface (i.e., program by the DSC circuit over the Monitor channel in Sub-frame 1) uses Sub-frame 0 to talk to the Layer-1 device and Sub-frame 1 to talk to the DSC circuit. It does not reverse its pins.*

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage temperature . . . . . –65°C to +150°C
Ambient temperature
with power applied . . . . . –55°C to +125°C
Supply voltage to ground,
potential continuous . . . . . 0 V to +7.0 V
Lead temperature (soldering, 10 sec) . . . . . 300°C
Maximum power dissipation . . . . . 1.5 W
Voltage from any
pin to V_{SS} . . . . . V_{SS} – 0.5 V to V_{CC} + 0.5 V
DC input/output current
(except LS1, LS2) . . . . . 10 mA
DC output current, LS1, LS2 only . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) devices
Operating V_{CC} range with respect
to V_{SS} . . . . . 4.75 V to 5.25 V
Ambient temperature (T_A) . . . . . 0°C to +70°C

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics over Commercial Operating Ranges (unless otherwise specified)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary		Unit
			Min	Max	
V_{IH}	Input High Level, except XTAL2		2.0	V_{CC} + 25	V
V_{IH2}	Input High Level XTAL2		0.80 V_{CC}	V_{CC} + 25	V
V_{IL}	Input Low Level		V_{SS} – 0.25	0.80	V
V_{OL}	Output Low Level, except SBOUT	I_{OL} = 2 mA		0.40	V
	Output Low Level, SBOUT only	I_{OL} = 7 mA		0.40	
V_{OH}	Output High Level	I_{OH} = –400 µA	2.4		V
		= –10 µA	0.90 V_{CC}		
I_{OL}	Output Leakage Current	0 < V_{OUT} < V_{CC}		± 10	µA
		Output in High-Z State			
I_{IL}	Input Leakage Current	0 < V_{IN} < V_{CC}			
	Digital Inputs			± 10	µA
	LIN1/LIN2			± 200	µA
	XTAL2			5.5 (TYP)	µA
C_I	Input Capacitance	Temp = 25°C		10 (TYP)	pF
	Digital Input	Freq = 1 MHz			
C_O	Output Capacitance	Temp = 25°C		10 (TYP)	pF
	Digital Input/Output	Freq = 1 MHz			

Table 2. Revision E Power Specifications for CCITT-Restricted Mode Phone Operation

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary		Unit
			Typ	Max	
$I_{CC}0$	V_{CC} Supply Current (Power-Down mode)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; mode = Power-Down; Clocks & Oscillator Stopped; LIU Receiver Enabled; S Interface Silent (INFO 0)	4	5	mW
$I_{CC}1$	V_{CC} Supply Current (Idle mode)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; mode = Idle; f_{MCLK} = 384 kHz; LIU Receiver Enabled; S Interface Silent (INFO 0)	20	25	mW
$I_{CC}2$	V_{CC} Supply Current (Active; Call Set-Up)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; mode = Active, Data Only; f_{MCLK} = 3.072 MHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D-channel Only; S-interface Load = 50 ohms	80	105	mW
$I_{CC}3$	V_{CC} Supply Current (Active; Voice mode)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; mode = Active Voice & Data; f_{MCLK} = 384 MHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D-channel and one B-channel; S-interface Load = 50 ohms; AINA = –15 dBm0, 1-kHz Sine Wave; EAR1/EAR2 = –15 dBm0, 1-kHz Tone Driving 600 ohms	155	190	mW
$I_{CC}4$	V_{CC} Supply Current (Active; Ringing, No Load*)	V_{CC} = 5.25 V; $V_{IH} = V_{CC}$; $V_{IL} = V_{SS}$; mode = Active, Data Only; f_{MCLK} = 384 kHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D-channel Only; S-interface Load = 50 ohms; Secondary Tone Ringer Enabled at 0 dB, 400 Hz, No Load	125	150	mW

Note:
All power measurements assume PP disabled or in IOM-2 Deactivated mode.

*Power consumption with the output loaded will be $I_{CC}4 + \frac{(V_{OUT}, \text{peak})}{R_{LOAD}}(V_{CC})$

For R_{LOAD} = 50 ohms and V_{OUT} = –12 dB (625 mV, peak), the maximum power consumption will be 215 mW.

AC Characteristics

V_{CC} = 5 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C; MCLK = 3.072 MHz

Table 3. MAP Analog Characteristics (Am79C30A only)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary			Unit
			Min	Typ	Max	
Z_{IN}	Analog Input Impedance AINA or AINB to AREF	–1.25 V < V_{IN} < +1.25 V f_{IN} < 4 kHz	200			Kohm
V_{IOS}	Allowable Offset Voltage at AINA or AINB	with respect to AREF pin	–5		+5	mV
L_{LS}	Allowable Load LS1 to LS2			R_{LOAD} > 40 ohms and C_{LOAD} < 100 pF		
L_{EAR}	Allowable Load EAR1 to EAR2			R_{LOAD} > 540 ohms and C_{LOAD} < 100 pF		
L_{AREF}	Allowable Load AREF to V_{SS} or V_{CC}			R_{LOAD} > 1 Kohm and C_{LOAD} < 100 pF		
V_{AREF}	Analog Reference Voltage		2.1	2.25	2.4	V