

CY7C1399

Features

- Single 3.3V power supply
- Ideal for low-voltage cache memory applications
- High speed — 12/15 ns
- Low active power — 255 mW (max.)
- Low CMOS standby power (L) — 180 μW (max.), f=f_{MAX}
- 2.0V data retention (L)
 - —**40** μW
- Low-power alpha immune 6T cell
- Plastic SOJ and TSOP packaging

Functional Description

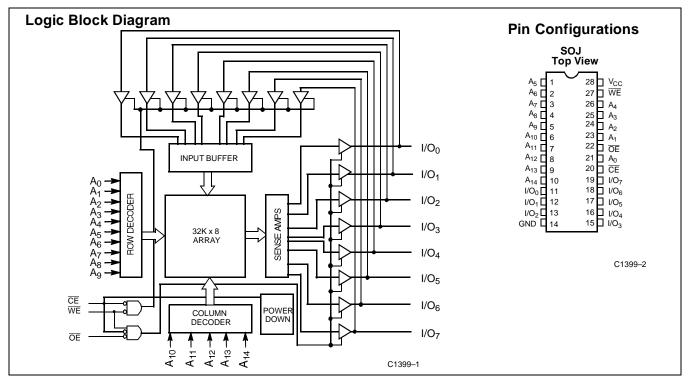
The CY7C1399 is a high-performance 3.3V CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion

32K x 8 3.3V Static RAM

is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 95% when deselected.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH. The CY7C1399 is available in standard 300-mil-wide SOJ and 28-pin TSOP type I packages.



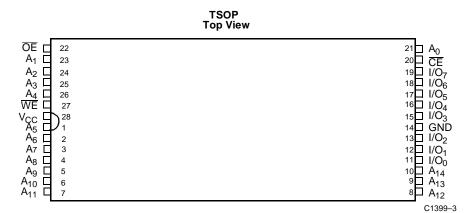
Selection Guide

	7C1399–12	7C1399–15	7C1399–20	7C1399–25	7C1399–35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	60	55	50	45	40
Maximum CMOS Standby Current (μA)	500	500	500	500	500
Maximum CMOS Standby Current (μA) L	50	50	50	50	50

Shaded area contains advanced information.



Pin Configurations (continued)



Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)
Storage Temperature65°C to +150°C
Ambient Temperature with Power Applied55°C to +125°C
Supply Voltage on V_{CC} to Relative $GND^{[1]}$ –0.5V to +4.6V
DC Voltage Applied to Outputs in High Z State ^[1] 0.5V to V_{CC} + 0.5V DC Input Voltage ^[1] 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	>2001V
(per MIL-STD-883, Method 3015)	
Latch-Up Current	>200 mA

Operating Range

Ranç	ge	Ambient Temperature	v _{cc}
Commerc	cial	0°C to +70°C	3.3V ±300 mV

Electrical Characteristics Over the Operating Range^[1]

			7C1399-12		7C13	899–15	7C13	899–20	
Parame- ter	Description	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.3V	2.2	V _{CC} +0.3V	2.2	V _{CC} +0.3V	V
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current		-1	+1	-1	+1	-1	+1	μΑ
I _{OZ}	Output Leakage Current	$GND \le V_I \le V_{CC},$ Output Disabled	-5	+5	-5	+5	-5	+5	μΑ
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	$V_{CC} = Max., I_{OUT} = 0 mA,$ f = f _{MAX} = 1/t _{RC}		60		55		50	mA
I _{SB1}	Automatic CE Power-Down	Max. $V_{CC}, \overline{CE} \ge V_{ H},$		5		5		5	mA
	Current — TTL Inputs	$V_{IN} \ge V_{IH}$, or $V_{IN} \le V_{IL}$, $f = f_{MAX}$	L	3		3		3	
I _{SB2}	Automatic CE Power-Down	Max. $V_{CC}, \overline{CE} \ge V_{CC} - 0.3V, V_{IN} \ge 100$		500		500		500	μΑ
	Current — CMOS Inputs ^[4]	$\label{eq:V_CC} \begin{split} V_{CC} &= 0.3V, \mbox{ or } V_{IN} \leq 0.3V, \\ WE \geq V_{CC} - 0.3V \mbox{ or } WE \leq 0.3V, \\ f = f_{MAX} \end{split}$	L	50		50		50	

Shaded area contains advanced information.

1. Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.

Note:



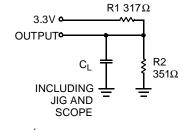
					399–25	7C1399–35			
Parameter	Description	Test Conditions	Min.	Max.	Min.	Max.	Unit		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 4.0 mA			0.4		0.4	V	
V _{IH}	Input HIGH Voltage			2.2	V _{CC} +0.3V	2.2	V _{CC} +0.3V	V	
V _{IL}	Input LOW Voltage ^[2]			-0.3	0.8	-0.3	0.8	V	
I _{IX}	Input Load Current		-1	+1	-1	+1	μA		
I _{OZ}	Output Leakage Current	$GND \le V_I \le V_{CC},$ Output Disabled	-5	+5	-5	+5	μΑ		
I _{OS}	Output Short Circuit Cur- rent ^[3]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA		
ICC	V _{CC} Operating Supply Current	$V_{CC} = Max., I_{OUT} = 0 mA,$ f = f _{MAX} = 1/t _{RC}			45		40	mA	
I _{SB1}	Automatic CE Power-Down	Max. $V_{CC}, \overline{CE} \ge V_{H},$			5		5	mA	
	Current — TTL Inputs				3		3	mA	
I _{SB2}	Automatic CE Power-Down	Max. $V_{CC}, \overline{CE} \ge V_{CC} - 0.3V, V_{IN} \ge$			500		500	μΑ	
	Current — CMOS Inputs ^[4]	$V_{CC} = 0.3V$, or $V_{IN} \le 0.3V$, WE $\ge V_{CC} = 0.3V$ or WE $\le 0.3V$, f=f _{MAX}			50		50	μA	

Electrical Characteristics Over the Operating Range^[2] (continued)

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Addresses	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{V}$	5	pF
C _{IN} : Controls			6	pF
C _{OUT}	Output Capacitance		6	pF

AC Test Loads and Waveforms

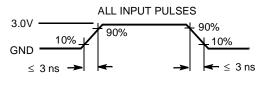


167Ω

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Equivalent to: THÉVENIN EQUIVALENT

OUTPUT



C1399-4

Notes:

See the last page of this specification for Group A subgroup testing information. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds. Device draws low standby current regardless of switching on the addresses. Tested initially and after any design or process changes that may affect these parameters. 2. 3. 4. 5.

-o 1.73V



Switching	Characteristics	Over the Operating Range ^[2,6]
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	7C1399–12		7C13	7C1399–15		99–20	7C13	99–25	25 7C1399–35		
Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
LE				1		•	1	1		11	
Read Cycle Time	12		15		20		25		35		ns
Address to Data Valid		12		15		20		25		35	ns
Data Hold from Address Change	3		3		3		3		3		ns
CE LOW to Data Valid		12		15		20		25		35	ns
OE LOW to Data Valid		5		6		7		8		10	ns
OE LOW to Low Z ^[8]	0		0		0		0		0		ns
OE HIGH to High Z ^[7,8]		5		6		6		7		7	ns
CE LOW to Low Z ^[8]	3		3		3		3		3		ns
CE HIGH to High Z ^[7,8]		6		7		7		8		8	ns
CE LOW to Power-Up	0		0		0		0		0		ns
CE HIGH to Power-Down		12		15		20		25		35	ns
LE ^[8, 9]											
Write Cycle Time	12		15		20		25		35		ns
CE LOW to Write End	8		10		12		15		20		ns
Address Set-Up to Write End	8		10		12		15		20		ns
Address Hold from Write End	0		0		0		0		0		ns
Address Set-Up to Write Start	0		0		0		0		0		ns
WE Pulse Width	8		10		12		15		20		ns
Data Set-Up to Write End	6		9		10		11		12		ns
Data Hold from Write End	0		0		0		0		0		ns
WE LOW to High Z ^[7]		7		7		7		7		7	ns
WE HIGH to Low Z ^[8]	3		3		3		3		3		ns
	ERead Cycle TimeAddress to Data ValidData Hold from Address Change \overline{CE} LOW to Data Valid \overline{OE} LOW to Data Valid \overline{OE} LOW to Data Valid \overline{OE} LOW to Low $Z^{[8]}$ \overline{OE} HIGH to High $Z^{[7,8]}$ \overline{CE} LOW to Low $Z^{[8]}$ \overline{CE} LOW to Power-Up \overline{CE} LOW to Power-Up \overline{CE} HIGH to Power-Down $LE^{[8, 9]}$ Write Cycle Time \overline{CE} LOW to Write EndAddress Set-Up to Write EndData Set-Up to Write EndData Hold from Write EndWE LOW to High $Z^{[7]}$	DescriptionMin.LERead Cycle Time12Address to Data Valid12Address to Data Valid3CE LOW to Data Valid1OE LOW to Data Valid0OE LOW to Low Z ^[8] 0OE HIGH to High Z ^[7,8] 3CE LOW to Low Z ^[8] 3CE LOW to Power-Up0CE HIGH to Power-Down12CE LOW to Power-Up12CE LOW to Vite End8Address Set-Up to Write End8Address Set-Up to Write End0Address Set-Up to Write Start0WE Pulse Width8Data Hold from Write End6Data Hold from Write End0WE LOW to High Z ^[7] 1	Description Min. Max. Image: Image	DescriptionMin.Max.Min.IERead Cycle Time1215Address to Data Valid1212Data Hold from Address Change33CE LOW to Data Valid1212OE LOW to Data Valid50OE LOW to Data Valid50OE LOW to Low Z ^[8] 00OE HIGH to High Z ^[7,8] 33CE LOW to Low Z ^[8] 33CE LOW to Power-Up00CE LOW to Power-Up00CE HIGH to Power-Down1215CE LOW to Write End810Address Set-Up to Write End810Address Set-Up to Write End00WE Pulse Width810Data Hold from Write End69Data Hold from Write End00WE LOW to High Z ^[7] 7	DescriptionMin.Max.Min.Max.Read Cycle Time121515Address to Data Valid121215Data Hold from Address Change3315OE LOW to Data Valid121215OE LOW to Data Valid1256OE LOW to Data Valid566OE LOW to Low Z ^[8] 0106OE HIGH to High Z ^[7,8] 337CE LOW to Low Z ^[8] 367CE HIGH to Power-Up007CE HIGH to Power-Down1215CE HIGH to Power-Down1215CE LOW to Write End810Address Set-Up to Write End810Address Set-Up to Write End810Address Set-Up to Write End810Mite Pulse Width810Data Hold from Write End69Data Hold from Write End69Mite LOW to High Z ^[7] 77	DescriptionMin.Max.Min.Max.Min.Read Cycle Time121520Address to Data Valid121520Data Hold from Address Change3333CE LOW to Data Valid12121515OE LOW to Data Valid56100OE LOW to Data Valid5600OE LOW to Low Z ^[8] 0000OE HIGH to High Z ^[7,8] 3333CE LOW to Low Z ^[8] 36710CE LOW to Power-Up012150CE LOW to Power-Up0121512CE LOW to Power-Up0121520CE LOW to Write End8101212Address Set-Up to Write End81000Address Set-Up to Write End8101212Address Set-Up to Write End691012Data Abid from Write End691012Data Set-Up to Write End6910Data Hold from Write End6910WE LOW to High Z ^[7] 777	DescriptionMin.Max.Min.Max.Min.Max.Read Cycle Time12151520Address to Data Valid12121520Data Hold from Address Change33320DE LOW to Data Valid12151520OE LOW to Data Valid12151020OE LOW to Data Valid56720OE LOW to Data Valid5676OE LOW to Low Z ^[8] 0566CE LOW to Low Z ^[8] 3333CE HIGH to High Z ^[7,8] 6777CE LOW to Power-Up0121520CE HIGH to Power-Up0121520CE HIGH to Power-Down12152020CE LOW to Power-Up0121520CE LOW to Write End8101220CE LOW to Write End8101212Address Set-Up to Write End8101212Address Set-Up to Write End8101212Data Set-Up to Write End691012Data Hold from Write End691012Data Hold from Write End6900WE LOW to High Z ^[7] 7777	DescriptionMin.Max.Min.Max.Min.Max.Min.Read Cycle Time1215152025Address to Data Valid1212152020Data Hold from Address Change31233203CE LOW to Data Valid1215152020OE LOW to Data Valid121566710OE LOW to Data Valid000000OE LOW to Data Valid566767OE LOW to Low Z ^[8] 0566767CE LOW to Low Z ^[8] 3667777CE LOW to Power-Up0000000CE HIGH to Pigh Z ^[7,8] 121215201515CE LOW to Power-Up01215202515CE LOW to Power-Down121215201515Address Set-Up to Write End81012151515Address Set-Up to Write End6910101115Data Hold from Write End69100101115Data Set-Up to Write End691001011Data Hold from Write End691001011Data Hold from Write End67777	Min.Max.Min.Max.Min.Max.Min.Max.Read Cycle Time1215152025Address to Data Valid1215152025Data Hold from Address Change33332025Data Hold from Address Change3121532025DE LOW to Data Valid121515202025DE LOW to Data Valid12156678DE LOW to Data Valid101000010DE LOW to Low Z ^[8] 0106610678DE LOW to Low Z ^[8] 31033103DE HIGH to High Z ^[7,8] 667108CE LOW to Low Z ^[8] 3121510020DE HIGH to Pighz Z ^[7,8] 6715201025CE LOW to Power-Up01215201525CE LOW to Write End81012151515Address Set-Up to Write End81012121515Address Set-Up to Write End6910101115Data Hold from Write End6910101115Data Hold from Write End69100011Data Hold from Write End69101011<	DescriptionMin.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min.Max.Min. <td>DescriptionMin.Max.Min.Max.Min.Max.Min.Max.Min.Max.Read Cycle Time12M15M20M25M35Address to Data ValidM12M15M20M25M35Data Hold from Address Change3MMMMMMMMMMCE LOW to Data ValidM12M15M20M25M35OE LOW to Data ValidM12MMMMMMMMMMOE LOW to Low Z^[8]MMMMMMMMMMMMMMOE HIGH to High Z^[7,8]MMMMMMMMMMMMMMMMMCE LOW to Low Z^[8]MMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMM</td>	DescriptionMin.Max.Min.Max.Min.Max.Min.Max.Min.Max.Read Cycle Time12M15M20M25M35Address to Data ValidM12M15M20M25M35Data Hold from Address Change3MMMMMMMMMMCE LOW to Data ValidM12M15M20M25M35OE LOW to Data ValidM12MMMMMMMMMMOE LOW to Low Z ^[8] MMMMMMMMMMMMMMOE HIGH to High Z ^[7,8] MMMMMMMMMMMMMMMMMCE LOW to Low Z ^[8] MMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMM

Data Retention Characteristics (Over the Operating Range)

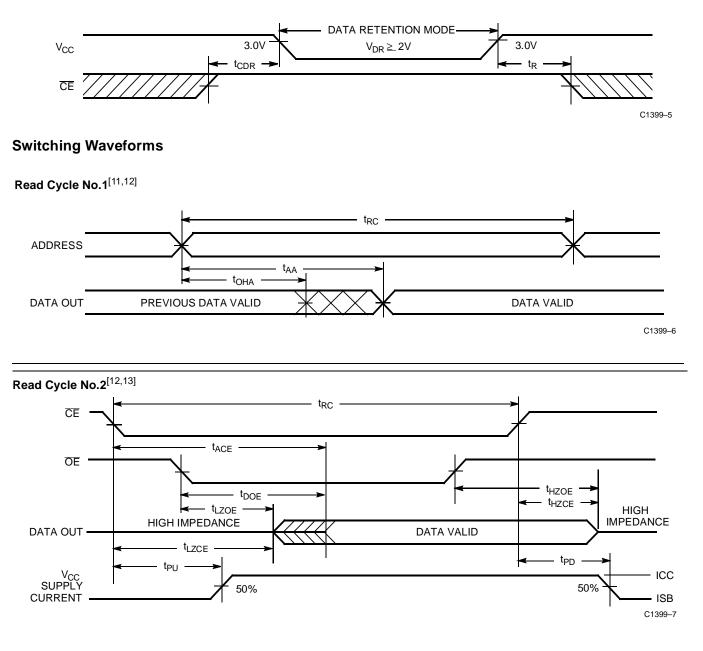
Parameter	Description		Conditions	Min.	Max.	Unit
V _{DR}	V _{CC} for Data Retention			2.0		V
I _{CCDR}	Data Retention Current		$V_{CC} = V_{DR} = 2.0V$		200	μΑ
		L	$CE \ge V_{CC} - 0.3V$, $V_{W} \ge V_{CC} - 0.3V$ or		20	μΑ
t _{CDR} ^[5]	Chip Deselect to Data Retention Time	·	$\label{eq:V_CC} \begin{array}{l} \underbrace{V_{CC} = V_{DR} = 2.0V,} \\ \overline{CE} \geq V_{CC} - 0.3V, \\ V_{IN} \geq V_{CC} - 0.3V \text{ or} \\ V_{IN} \leq 0.3V \end{array}$	0		ns
t _R ^[5]	Operation Recovery Time			t _{RC}		ns

Notes:

Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified l_{QL}/l_{QH} and capacitance C_L = 30 pF.
 t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
 At any given temperature and voltage condition, t_{HZCE} is less than t_{LZOE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} for any given device.
 The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
 The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.



Data Retention Waveform



Notes:

 I1.
 Device is continuously selected.
 \overline{OE} , $\overline{CE} = V_{IL}$.

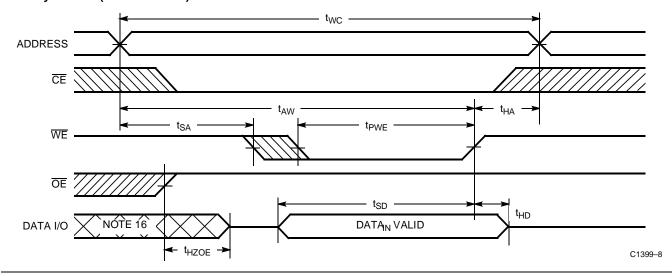
 12.
 WE is HIGH for read cycle.

 13.
 Address valid prior to or coincident with \overline{CE} transition LOW.

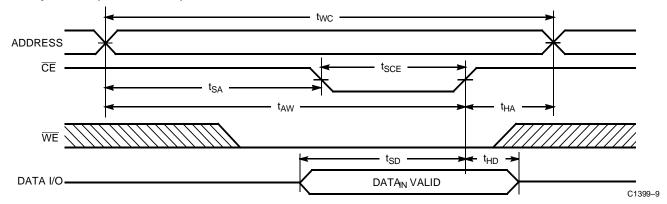


Switching Waveforms (continued)

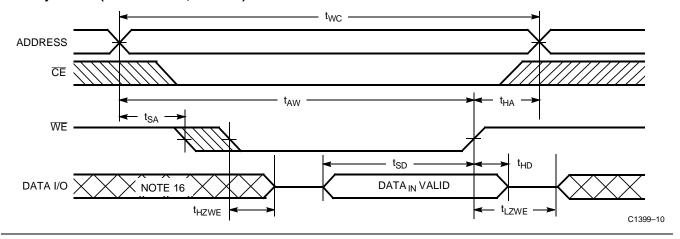
Write Cycle No.1 (WE Controlled)^[9,14,15]



Write Cycle No.2 (CE Controlled)^[9,14,15]



Write Cycle No.3 (WE Controlled, OE LOW)^[10,15]



Notes:

- 14. Data I/O is high impedance if OE = V_{IH}.
 15. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
 16. During this period, the I/Os are in the output state and input signals shold not be applied.



Truth Table

CE	WE	OE	Input/Output	Mode	Power
Н	Х	Х	High Z	Deselect/Power-Down	Standby (I _{SB})
L	Н	L	Data Out	Read	Active (I _{CC})
L	L	Х	Data In	Write	Active (I _{CC})
L	Н	Η	High Z	Deselect, Output Disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Pack- age Name	Package Type	Operating Range
12	CY7C1399-12VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L-12VC	V21	28-Lead Molded SOJ	
	CY7C1399-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L-12ZC	Z28	28-Lead Thin Small Outline Package	
15	CY7C1399-15VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L-15VC	V21	28-Lead Molded SOJ	_
	CY7C1399-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L-15ZC	Z28	28-Lead Thin Small Outline Package	
20	CY7C1399-20VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L-20VC	V21	28-Lead Molded SOJ	_
	CY7C1399-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L-20ZC	Z28	28-Lead Thin Small Outline Package	_
25	CY7C1399-25VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L-25VC	V21	28-Lead Molded SOJ	
	CY7C1399-25ZC	Z28	28-Lead Thin Small Outline Package	_
	CY7C1399L-25ZC	Z28	28-Lead Thin Small Outline Package	_
35	CY7C1399-35VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L-35VC	V21	28-Lead Molded SOJ	1
	CY7C1399-35ZC	Z28	28-Lead Thin Small Outline Package	1
	CY7C1399L-35ZC	Z28	28-Lead Thin Small Outline Package	1

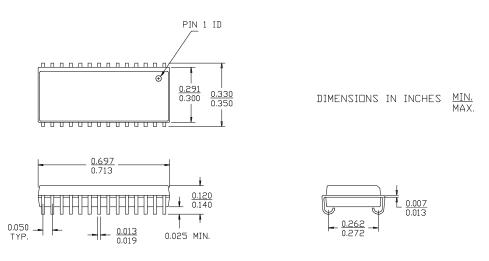
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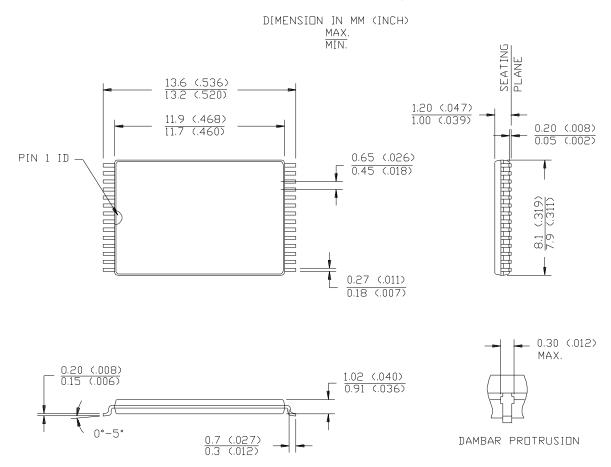


Package Diagrams

28-Lead Molded SOJ V21



28-Lead Thin Small Outline Package Z28



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