

Audio Ringing Codec Filter (ARCOFI)

PSB 2160

Preliminary Data

CMOS IC

Type	Ordering Code	Package
PSB 2160-N	Q67100-H6031	PL-CC-28 (SMD)
PSB 2160-P	Q67100-H8503	P-DIP-24

The PSB 2160 ARCOFI® provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. The ARCOFI fulfils all necessary requirements for the completion of a low cost digital telephone. Full featured applications including hands-free telephony are carried out by the addition of a voice switched speakerphone circuit. The ARCOFI performs all coding, decoding and filtering functions according to CCITT and AT&T norms.

The ARCOFI integrates a DTMF generator in the transmit direction and a tone generator plus a ringing generator in the receive path. The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on chip as well as a secondary input for a handsfree microphone. The microphone analog gains is user programmable under microprocessor control.

Features

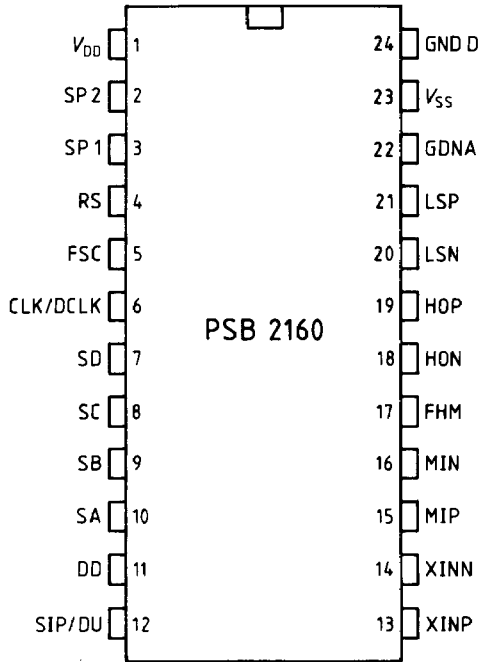
- Audio, ringing, codec, filter for digital telephone
- Programmable codec filter
- Programmable DTMF, tone and ringing generators
- Programmable A- and μ -law
- Test and maintenance loopbacks in the analog front end and the digital processor
- SLD or IOM®-2 serial interface bus
- Flexible Peripheral Control Interface (PCI)
- Separate output for piezo ringer
- Dual analog inputs for handset and "hands-free" microphones plus an auxiliary differential analog input
- Two sets of differential outputs for a handset earpiece and a loudspeaker
- Low power CMOS technology
- Power dissipation: active 150 mW, standby 10 mW
- Temperature range: -25 to 70 °C

Applications

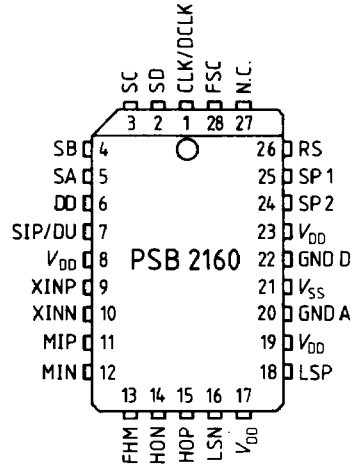
Digital terminal equipment including a voice path.

Pin Configurations
(top view)

P-DIP-24



PL-CC-28



Pin Definitions and Functions

Pin No. P-DIP	Pin No. PL-CC	Symbol	Function
1	8, 17, 19, 23	V _{DD}	+5 V; Positive power supply
2 3	24 25	SP2 SP1	Supplementary Function: Appropriate pin strapping access supplementary functions including test modes.
4	26	RS	Reset Input: When pin RESET is forced high the ARCOFI is placed in a power down mode. All configuration registers are reset to default values. I/O pins SA-SD and SIP/DU are programmed as inputs until the ARCOFI is reconfigured.
5	28	FSC	Frame Sync: 8-kHz signal, phase locks to CLK. When high, SIP behaves as an input and the ARCOFI can receive data through pin SIP. When low, SIP behaves as an output and data can be transferred from the ARCOFI to the system via pin SIP. When in IOM-2 mode FSC supplies to the ARCOFI a synchronization signal according to the IOM-2 specification.
6	1	CLK/DCLK	CLK System Clock: 512 kHz supplied by the application system clock when SLD mode is selected. DCLK System Clock: 1.536 MHz supplied by the application system clock when IOM-2 mode is selected.
7 8 9 10	2 3 4 5	SD SC SB SA	Programmable I/O PCI Pins: With the appropriate bit setting in configuration register CR2, each SA-SD pin can be declared independently as input or as output. The data are received from or forwarded to the signaling channel according to the programming of the PCI pins. When selected, the tone generator signals can be directed to pins SA & SB. (SA & SB then in opposite phase).
11	6	DD	DD; Data Downstream: Receive data from a layer-1 controlling device when IOM-2 mode is selected.
12	7	SIP/DU	SIP; Serial Interface Port: This serial bidirectional port is clocked by CLK when SLD mode is selected. DU; Data Upstream: Transmit data to the layer-1 controlling device when IOM-2 mode is selected.
13 14	9 10	XINP XINN	X Input: These auxiliary inputs provide a normalized differential audio input for an additional analog device.
15 16	11 12	MIP MIN	Hand-set Microphone Inputs: MIP & MIN provides highly symmetrical differential inputs for commonly used telephone microphones.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Function
17	13	FHM	Hands-Free Microphone: This single ended input can be used to interface an electret microphone for speakerphone applications.
18 19	14 15	HON HOP	Hand-set Earpiece Outputs: HOP & HON are differential output pins which can drive handset earpiece transducers directly.
20 21	16 18	LSN LSP	Loudspeaker Outputs: LSN and LSP are differential output pins which can drive a 50 Ω loudspeaker directly. A piezo transducer connected via SA and SB can also be used for ringing signals instead of a loudspeaker.
22	20	GNDA	Analog Ground: Not internally connected to GNDD. All analog signals are referred to this pin.
23	21	V_{SS}	-5 V; Negative power supply
24	22	GNDD	Digital Ground: (0 V) not internally connected to GNDA. All digital signals are referred to this pin.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{DD} referred to GNDA	V_S	-0.3	5.5	V
V_{SS} referred to GNDA	V_S	-5.5	0.3	V
GNDA to GNDD	V_S	-0.3	0.3	V
Analog input and output voltages referred to V_{DD}	V_S	-10.3	0.3	V
referred to V_{SS}	V_S	-0.3	10.3	V
All digital input and output voltages referred to GNDD	V_S	-0.3	5.3	V
referred to V_{DD}		-5.3	0.3	V
Power dissipation	P_D		1	W
Storage temperature	T_{stg}	-60	125	$^{\circ}\text{C}$
Ambient temperature under bias	T_A	-30	80	$^{\circ}\text{C}$

DC Characteristics
 $V_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = -5\text{ V} \pm 5\%$, $GNDD = 0\text{ V}$, $T_A = -25\text{ to }70\text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
DIGITAL Input leakage current	I_{IL}			± 1	μA	$-0.3 \leq V_{IH} \leq V_{DD}$
H-input level	V_{IH}	2.4		$V_{DD}+0.3$	V	
L-input level	V_{IL}	-0.3		0.8	V	
H-output level	V_{OH}	2.4			V	$I_O = 400\ \mu\text{A}$
L-output level	V_{OL}			0.45	V	$I_O = -2\ \text{mA}$
V_{DD} supply current standby	I_{DD}			2	mA	$V_{SS} = 0\text{ V}$ $V_{DD} = 5.25\text{ V}$
standby operating*)			11	TBD 15	mA mA	$\pm 5\%$ supply $\pm 5\%$ supply
V_{SS} supply current standby	I_{SS}			TBD	mA	$\pm 5\%$ supply
operating*)			-8	-13	mA	$\pm 5\%$ supply
Standby power dissipation	P_{DO}			TBD	mW	$\pm 5\%$ supply
Standby power dissipation	P_{DO}			10	mW	$V_{SS}=0\text{V}$, $V_{DD}=5.25\text{V}$ Clock = 512 kHz
Standby power dissipation	P_{DO}			5	mW	$V_{SS}=0\text{V}$; $V_{DD}=5.25\text{V}$ No clock
Operating power dissipation*)	P_{D1}		100	150	mW	$\pm 5\%$ supply
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	

TBD: To Be Determined

*) Operating power dissipation is measured with all analog outputs open.

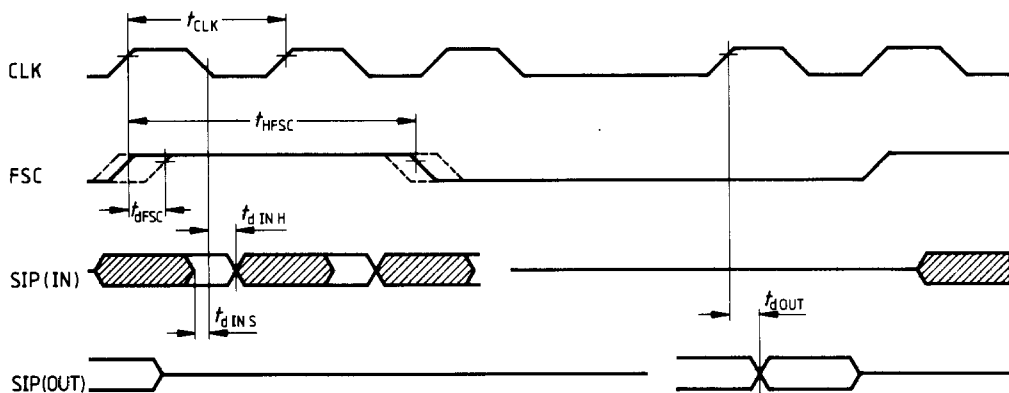
DC Characteristics (cont'd)

SLD Bus Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
CLK period	t_{CLK}	1.76	1.953	2.15	μs
CLK duty cycle	$t_d CLK$	30	50	70	%
FSC Period	t_{FSC}		125		μs
FSC delay time	$t_d FSC$	-20		80	ns
FSC high time	$t_H FSC$	0.5	62.5		μs
SIP data in setup time	$t_d IN S$	50			ns
SIP data in hold time	$t_d IN H$	80			ns
SIP data out delay	$t_d OUT$			200	ns
SIP data out tristate delay				50	ns

Note: SIP is an I/O pin; SIP IN denotes timings for incoming data and SIP OUT denotes timings relation with outgoing data.

SLD Bus Timing Diagram



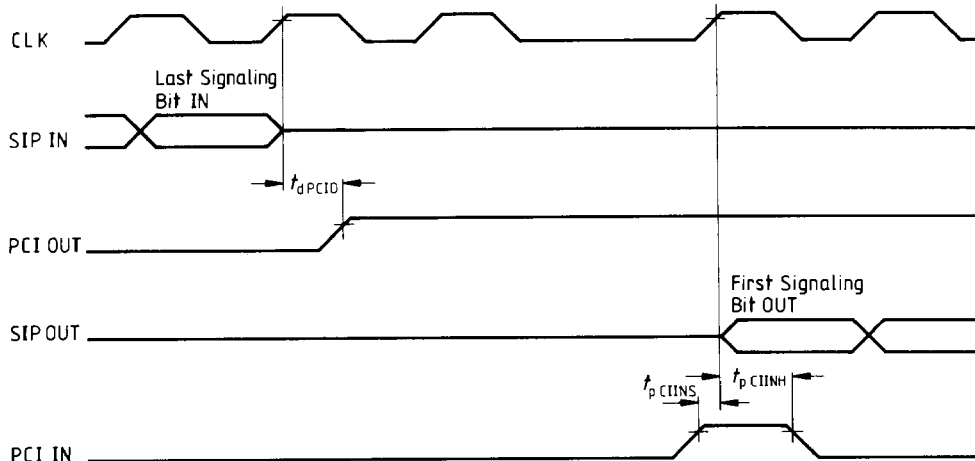
PCI Switching Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SIP IN to PCI OUT	$t_{d\text{ PCIO}}$		300	ns
PCI IN setup time	$t_{p\text{ CIINS}}$	50		ns
PCI IN hold time	$t_{p\text{ CIINH}}$	100		ns

Reset Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{DD} rise time	t_{rVDD}	0	20	ms
Reset pulse width	t_{RS}	1		μs
Power stable to reset low	t_{SRS}	1		μs
Reset transition time	t_{tr}		1	ms

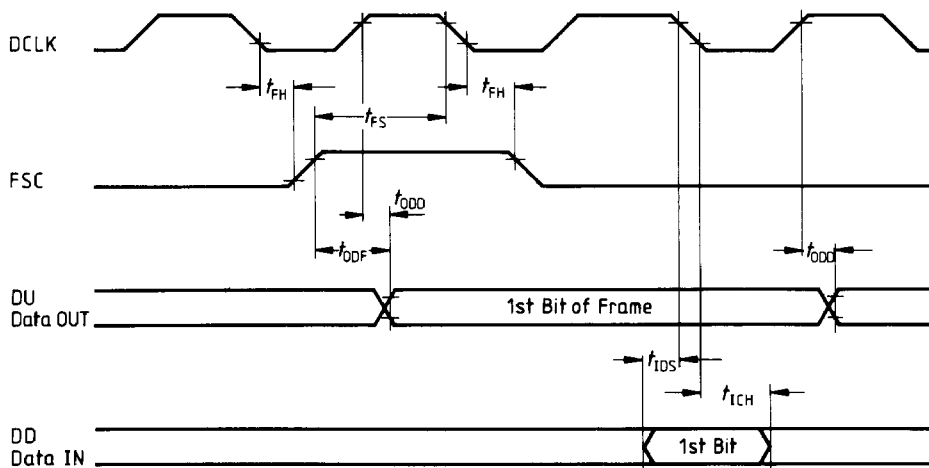
PCI Timing Diagram



IOM Bus Switching Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC setup time	t_{FS}	60		ns
FSC hold time	t_{FH}	30		ns
Output data delay from DCLK	t_{ODD}		60	ns
Input data set-up time	t_{IDS}	25		ns
Input data hold	t_{IDH}	20		ns
Output data delay from FSC	t_{ODF}	30		ns

IOM-2 Bus Timing Diagram



Analog Front End Electrical Interface Inputs

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Hand-set microphone input impedance	Z_{HM}	150		k Ω	300-3400 Hz
Hand-set microphone max. input voltage swing*	V_{HM}		7.58	mVpk	
Hand-set microphone amplifier gain AHM + HR	G_{AHM+AR}	16	52.0	dB	pin MIP, MIN 386 mV 1 kHz
Hands-free microphone input impedance	Z_{FHM}	150		k Ω	300-3400 Hz
Hands-free microphone max. input voltage swing*	V_{FHM}		127	mVpk	
Hands-free microphone amplifier gain	G_{AFHM}		28.0	dB	pin FHM 19.5 mV 1 kHz
Auxiliary pin input impedance	Z_{XIN}	150		k Ω	300-3400 Hz
Auxiliary XIN max. input voltage swing*	V_{XIN}		563	mVpk	
Auxiliary XIN amplifier gain AX + AR	G_{AXIN}		15.1	dB	pin XINN & XINP 270 mV 1 kHz

* A maximum swing signal corresponds to a 3.14 dBm0 signal at the A/D converter. This corresponds also to a PCM code overload ± 127 . ($3.14 \text{ dBm0} = 2.26 V_{\text{rms}} = 3.2 V_p = 6.4 V_{\text{pp}}$).

Analog Front End Electrical Interface Outputs

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Hand-set earpiece output impedance	Z_{HO}		1	Ω	300-3400 Hz
Hand-set earpiece max. output voltage swing*	V_{HO}		457	mVpk	load measured from HOP to HON
Hand-set earpiece output high voltage*	V_{HOH}		455	mVpk	input load -1 mA HOP/HOP
Hand-set earpiece output low voltage*	V_{HOL}		455	mVpk	input load +1 mA HOP/HOP
Loudspeaker output impedance	Z_{LS}		2	Ω	300-3400 Hz
Loudspeaker max. output voltage swing*	V_{LS}		2.75	Vpk	load measured from LSN to LSP
Loudspeaker output high voltage*	V_{LSOH}		2.55	V	input load -100 mA LSN/LSP
Loudspeaker output low voltage*	V_{LSOL}		2.55	V	input load +100 mA LSN/LSP

* The max. output voltage swing corresponds to a max. incoming PCM code (± 127).

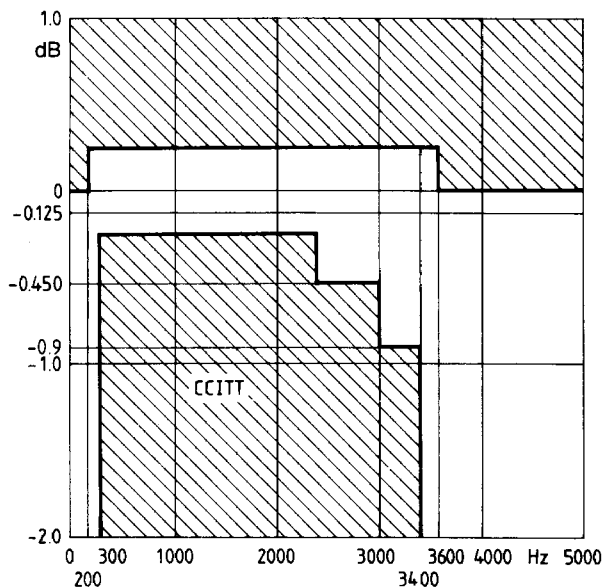
Analog Front End Attenuation Plan

Transmit	min.	typ.	0 dBmO	max.	peak	Unit	Ref.
MIP/MIN Microphone Input level at Max gain AHM+AR = 52 dB ¹⁾	2.15E-04 1.52E-04 -80.3 -74.13 52	1.21E-03 8.56E-04 -65.3 -59.13 52	5.60E-03 3.96E-03 -52 -45.83 52	6.81E-03 4.82E-03 -50.3 -44.13 52	8.04E-03 5.68E-03 -48.86 -42.69 52	Vpk Vrms dBmO dBm dB	V V 1.576V 0.775V gain
Xin Input level AX-AR gain ¹⁾	1.51E-02 1.07E-02 -43.4 -37.23 15.1	8.48E-02 5.99E-02 -28.4 -22.23 15.1	3.92E-01 2.77E-01 -15.1 -8.93 15.1	4.77E-01 3.37E-01 -13.4 -7.23 15.1	5.63E-01 3.98E-01 -11.96 -5.79 15.1	Vpk Vrms dBmO dBm dB	V V 1.576V 0.775V gain
FHM Input level AFHM gain ¹⁾	3.41E-03 2.41E-03 -56.3 -50.13 28	1.92E-02 1.36E-02 -41.3 -35.13 28	8.87E-02 6.28E-02 -28 -21.83 28	1.08E-01 7.63E-02 -26.3 -20.13 28	1.27E-01 9.01E-02 -24.86 -18.69 28	Vpk Vrms dBmO dBm dB	V V 1.576V 0.775V gain
A/D Input level ARCOFI (Bypass mode) PCM value	8.57E-02 6.06E-02 -28.3 -22.13 ± 43	4.82E-01 3.41E-01 -13.3 -7.13 ± 83	2.23E+00 1.58E+00 0 6.17 ± 118	2.71E+00 1.92E+00 1.7 7.87 ± 123	3.20E+00 2.26E+00 3.14 9.31 ± 127	Vpk Vrms dBmO dBm	V V 1.576V 0.775V PCM word

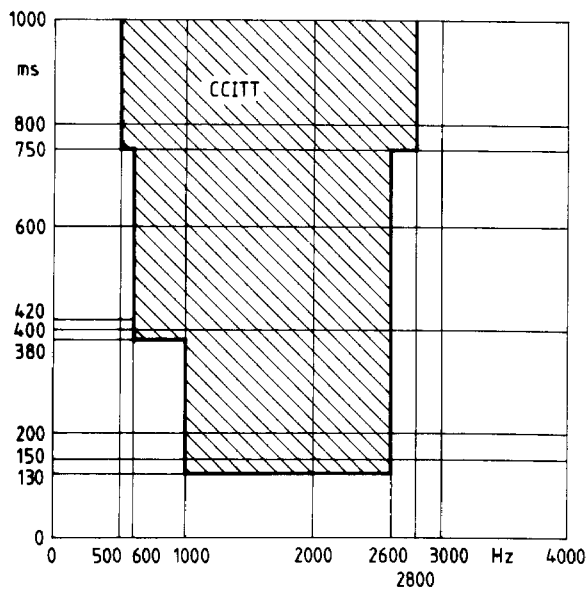
Receive	min.	typ.	0 dBmO	max.	Peak	Unit	Ref.
LSN/LSP Output level Symmetric in a 50 Ω load ALS gain	8.57E-02 6.06E-02 -28.3 -22.13 0	4.82E-01 3.41E-01 -13.3 -7.13 0	2.23E+00 1.58E+00 0 6.17 0	2.71E+00 1.92E+00 1.7 7.87 0	3.20E+00 2.26E+00 3.14 9.31 0	Vpk Vrms dBmO dBm dB	V V 1.576V 0.775V attenuat.
HOP/HON ¹⁾ Output level Symmetric in a 200 Ω load AHO attenuation	6.81E-02 4.82E-02 -30.3 -24.13 2	3.83E-01 2.71E-01 -15.3 -9.13 2	1.77E+00 1.25E+00 -2 4.17 2	2.15E+00 1.52E+00 -0.3 5.87 2	2.54E+00 1.80E+00 1.14 7.31 2	Vpk Vrms dBmO dBm dB	V V 1.576V 0.775V attenuat.
D/A Output level ARCOFI (Bypass mode)	8.57E-02 6.06E-02 -28.3 -22.13	4.82E-01 3.41E-01 -13.3 -7.13	2.23E+00 1.58E+00 0 6.17	2.71E+00 1.92E+00 1.7 7.87	3.20E+00 2.26E+00 3.14 9.31	Vpk Vrms dBmO dBm	V V 1.576V 0.775V

¹⁾ The HOP/HON attenuation values can be changed in future versions of ARCOFI

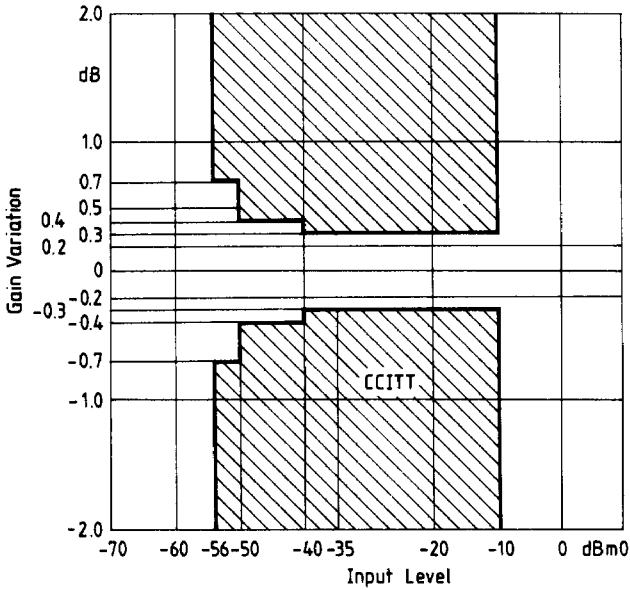
Attenuation Distortion in Transmit & Receive Direction



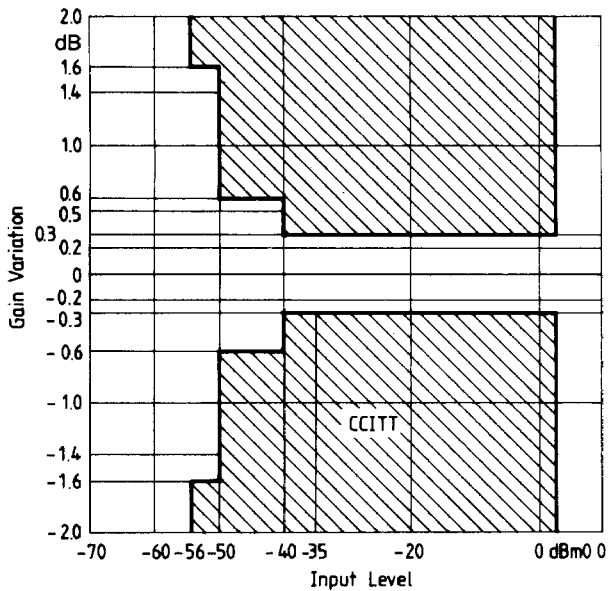
Group Delay Distortion in Transmit & Receive Direction (ref. 1500 Hz)



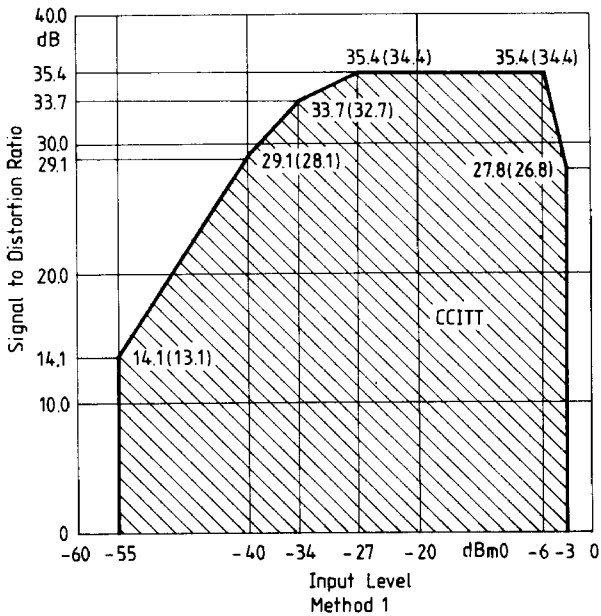
Gain Tracking in Transmit & Receive Direction (Method 1; Noise)



Gain Tracking in Transmit & Receive Direction (Method 2; Sinus)

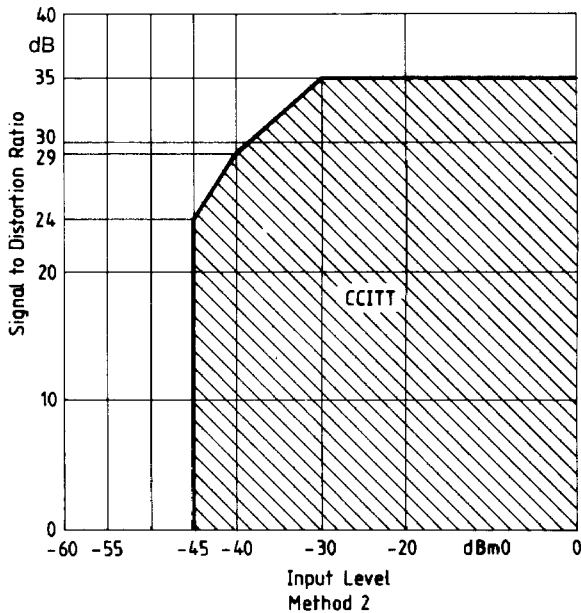


Total Harmonic Distortion in Receive and Transmit *) Direction (Method 1; Noise)



*) Remark: Between brackets, values for transmit direction

Total Harmonic Distortion in Receive and Transmit Direction (Method 2; Sinus)



Out-of-Band Signals at Analog Inputs

When applying an out-of-band sine-wave signal with frequency f and level A to the analog inputs, the level of any frequency component below 4 kHz at the digital output is attenuated according to the following table.

The reference level used for this measurement is a 800 Hz, 0dBmO signal applied to the FHM analog input in by-pass mode. The digital gain GX in configuration register CR1 has to be set to a flat 0dB.

Out-of-Band Input Frequency f	Out-of-Band Input Level A	Attenuation at Digital Output
0 Hz $\leq f \leq$ 60 Hz	-45 dBmO $\leq A \leq$ 0 dBmO	25 dB
60 Hz $\leq f \leq$ 100 Hz	-45 dBmO $\leq A \leq$ 0 dBmO	10 dB
3400 Hz $\leq f \leq$ 4000 Hz	-45 dBmO $\leq A \leq$ 0 dBmO	0 dB
4000 Hz $\leq f \leq$ 4600 Hz	-45 dBmO $\leq A \leq$ 0 dBmO	14 dB
4600 Hz $\leq f \leq$ 12 kHz	-45 dBmO $\leq A \leq$ -15.8 dBmO	35 dB
12 kHz $\leq f \leq$ 20 kHz	-45 dBmO $\leq A \leq$ -23.2 dBmO	35 dB
20 kHz $\leq f$	-45 dBmO $\leq A \leq$ -25 dBmO	35 dB

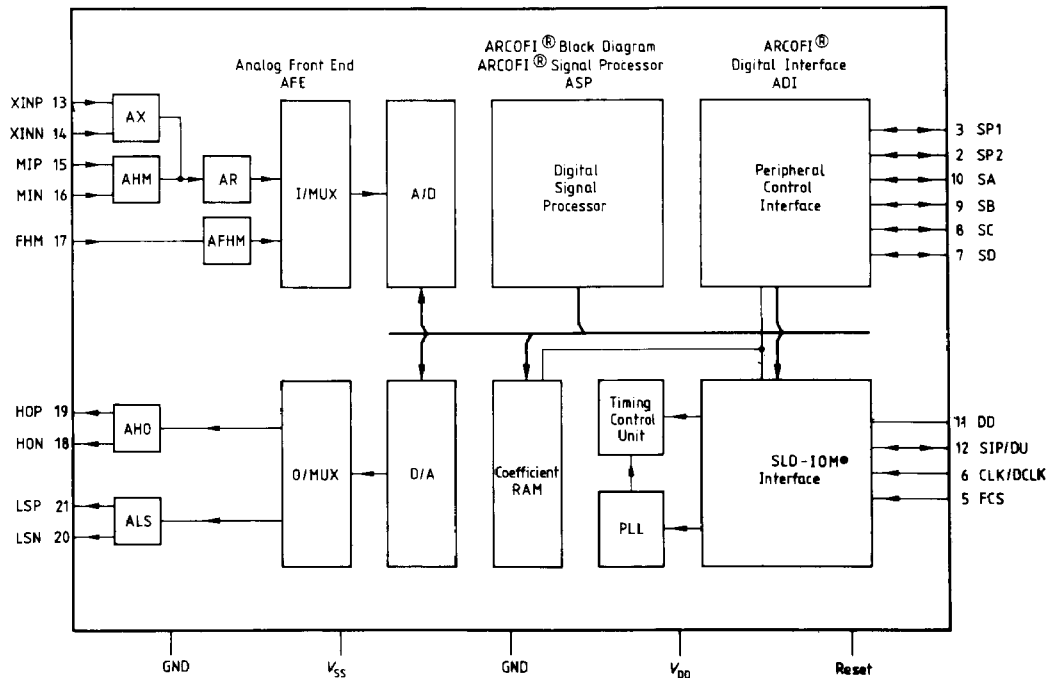
Functional Description

The ARCOFI bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM digital world by providing a full PCM CODEC (coder + decoder) with all the necessary transmit and receive filters. A block diagram of the ARCOFI is shown in figure 1.

The ARCOFI can be subdivided in three main blocks;

- The ARCOFI Analog Front End (AFE)
- The ARCOFI Signal Processor (ASP)
- The ARCOFI Digital Interface (ADI)

Figure 1
Block Diagram



Analog Front End

The **Analog Front End** section of the ARCOFI interfaces the analog transducers with the subsequent signal processor. In the transmit direction the AFE function is to amplify the transducer input signals (microphones) and convert them into digital signals. In the AFE receive section, the incoming digital signals are converted to analog signals output to an earpiece and a loudspeaker. The attenuation plan and electrical characteristics of the AFE are adapted to meet commonly used voice transducers.

Analog Inputs

A high sensitive differential input MIP and MIN connects a handset microphone to a gain programmable amplifier AHM. When selected, the differential X inputs can be activated (amplifier AX) while deselecting the MIP/MIN inputs;

Coming from AHM or AX the signal is forwarded via a fixed amplification stage AR to the input of the analog multiplexer driving the oversampling A/D converter. A third analog input source is provided through pin FHM. This "hands-free" microphone input connects the multiplexer via amplifier AFHM. The programmable amplifier AHM provides a first gain adjustment allowing a perfect adaptation to various types of microphone transducers. This gain adjustment is then tuned in the digital domain via the programmable gain adjustment filter GX (see ARCOFI signal processing section).

Analog Outputs

Fully differential outputs HOP and HON connect the amplifier AHO to the hand-set earpiece. Differential outputs LSN & LSP are provided for use with a 50 Ω loudspeaker. Up to 100 mW of power can be delivered to the loudspeaker via amplifier ALS. The power amplifier ALS is short-circuit protected. All outputs are sourced by a digital-to-analog converter via an output analog multiplexer. The selection of the output source is performed through the configuration register CR3 via the SLD interface.

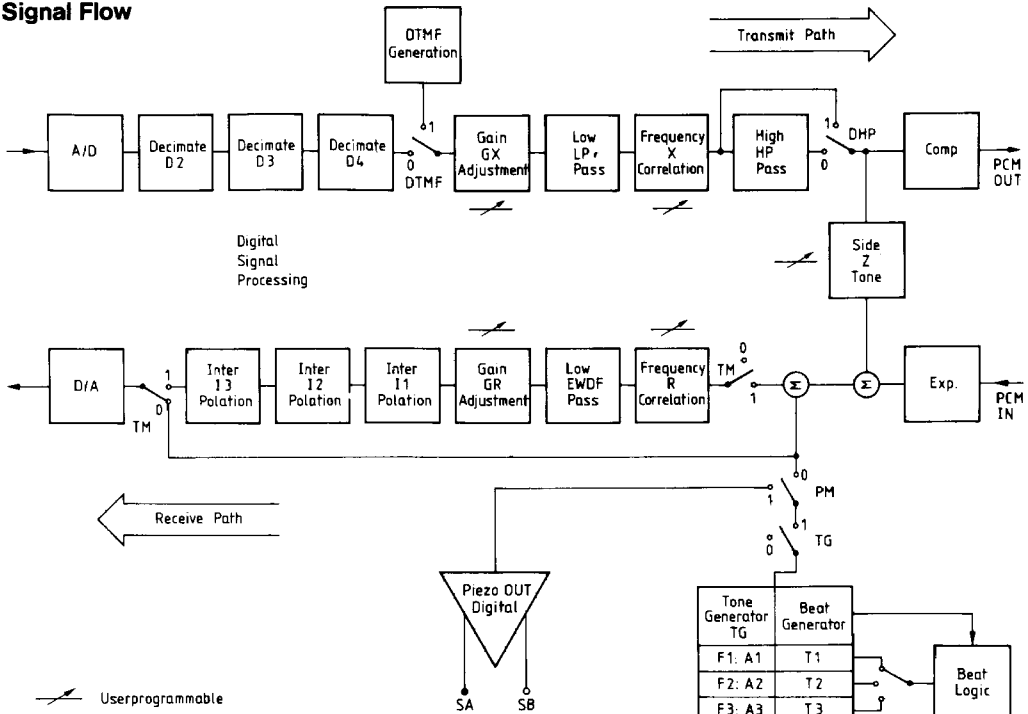
ARCOFI Signal Processor (ASP)

The **ARCOFI Signal Processor (ASP)** has been conceived to perform all CCITT recommended filtering in both the transmit and receive path and is therefore fully compatible to the G.714 CCITT specification. The code processed by the ASP is provided in the transmit direction by an oversampling A/D converter situated in the analog front end (AFE). Once processed the speech signal is converted into an 8 bit A-law or μ -law PCM format or remains a 16-bit linear word according to the bit setting in the configuration register 3.

In the receive direction the incoming PCM-signal is expanded in a linear format and subsequently processed until passed to the D/A converter.

The entire ARCOFI signal flow plan is shown in **figure 2**.

Figure 2
Signal Flow



Transmit Path Signal Processing

In the transmit direction a series of decimation filters reduces the sampling rate down to the 8-kHz PCM rate. These filters attenuate out-of-band noise by limiting the received signal to the voiceband.

The decimation stages end with a low-pass filter which band limits the voice signal according to the CCITT recommendation G.714. A high-pass filter is also provided to remove power line frequencies. The ARCOFI meets or exceeds all CCITT, and North American recommendation on attenuation distortion and group delay distortion.

The GX gain adjustment stage is digitally programmable allowing the gain to be programmed from -45 to +12 dB within a ± 0.25 dB tolerance range. However the CCITT templates are not guaranteed in the whole area.

The voice signal after being linearly processed can be output as an 8-bit PCM word according to the CCITT G.711 A-Law or the North American μ -Law format. If desired the compression stage can be by-passed, a 16-bit linear word is then outputted to the ARCOFI digital interface.

The transmit path contains a frequency correction filter FX allowing an optimum adaptation to different type of microphones (dynamic, piezoelectric or electret).

Receive Path Signal Processing

In the receive path the incoming PCM signal is expanded into a linear code according to the selected A or μ -Law. If the linear mode is chosen, the PCM expander circuit is by-passed and a 16-bit linear word has to be provided to the processor.

A programmable sidetone gain stage Z adds a sidetone signal to the incoming voice signal. The sidetone gain can be programmed from -50 to -2.5 dB within a ± 1 dB tolerance range (0 dB is also possible).

The FR frequency correction filter is similar to the FX filter allowing an optimum adaptation to different type of loudspeakers and earpieces.

A low-pass EWDF filter limits the signal bandwidth in the receive direction according to CCITT recommendations. The GR gain adjustment stage is digitally programmable from -45 dB to $+12$ dB within a 0.25 dB tolerance range. However the CCITT templates are not guaranteed in the whole area.

A series of low-pass interpolation filters increase the sampling frequency up to 128 kHz. The last interpolator feeds the D/A converter.

Tone Ring and Tone Generator

The ASP receive path contains two signal generators; a tone ring and a beat tone generator (TG & BT). Those generators can be used for tone alerting; call progress tones or other audible feedback tones. All generated tones can be provided at either the handset earpiece, the loudspeaker output or the piezo ringer output (SA & SB).

Distinctive alerting signals allowing for example the use of different multitone ringing patterns, are all programmable using the beat tone generator in conjunction with the tone ringer. In the case of a two or three tone ringing signal, the tone ring generator controls the output frequency pitch whilst the beat tone generator controls the repetition rate.

ARCOFI Digital Interface (ADI)

The ADI features are:

- A selectable SLD or IOM-2 serial bus interface through which the ARCOFI transfers voice channels and communicates with the system microcontroller.
- A programmable multipurpose interface PCI (Peripheral Control Interface) which provides 4 programmable I/O pins to control peripheral devices.

SLD Bus

The SLD serial interface consists of a bidirectional data line SIP, a synchronization clock input CLK and a data direction input FSC. Data bits are loaded or read out of the serial interface pin SIP under control of a direction signal FSC. Bits are clocked in or clocked out on the rising edge of the slave clock pin CLK (512 kHz). FSC and CLK inputs must be phase locked.

An SLD frame lasts 125 μs and consists of 32 bits transferred to the ARCOFI (FSC high) followed by 32 bits transferred from the ARCOFI to the SLD bus (FSC low).

The SLD interface thus provides a full duplex 256 kbit/s communication capacity. This capacity is subdivided in two 64 kbit/s voice/data channels reserved for the ISDN B1 and B2 channels. The remaining bandwidth is used by a feature control channel (64 kbit/s) and a signaling channel (64 kbit/s). Bytes in all channels are serialized MSB first.

A command received over the SLD-bus can cause a response over the SLD-bus within the same frame. This leaves the ARCOFI 31.25 μs to interpret the command and generate the appropriate answer in the following SLD half-frame.

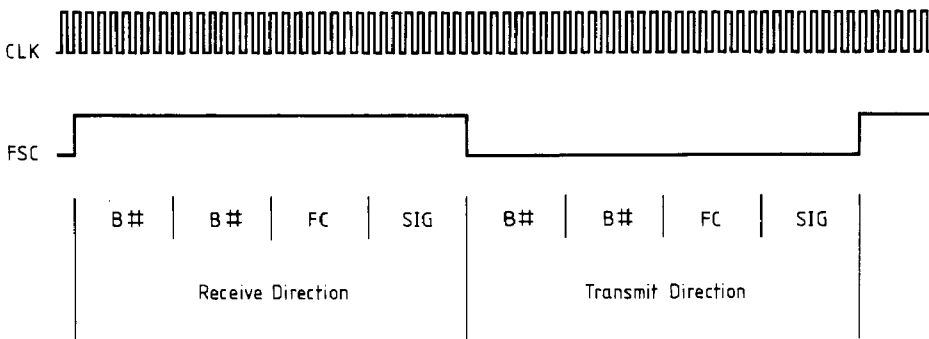
All ARCOFI internal registers are accessible via the SLD-bus in the time slot allocated to the command channel. The first byte transferred in the command channel specifies the type of operation and the number of bytes allocated to the transfer set-up.

When in power down (PU=0 ;CMDR), the command channel remains active in both transmit and receive direction providing that the address bit (AD ;CMDR) matches the address strapped on SP1, SP2.

In power down however both data channels are disabled; SIP being tristated during data channel transmit time slots.

Receive direction (RX)
SLD → ARCOFI

Transmit direction (TX)
ARCOFI → SLD



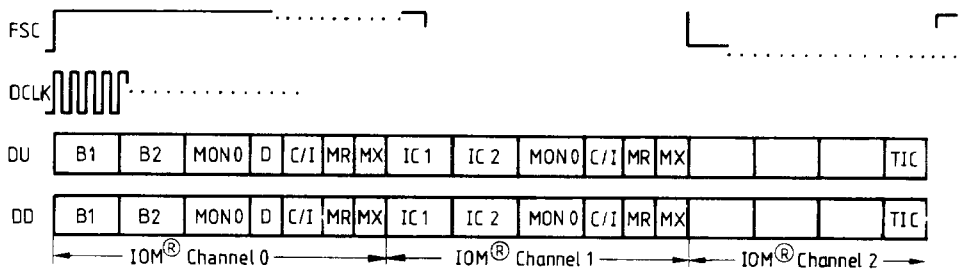
B# 1,2: Data Channel
FC : Feature Control Channel
SIG : Signaling Channel

IOM-2 Interface

The IOM-2 interface consists of two data lines and two clock lines. DU: Data Upstream carries data from the ARCOFI to the layer-1 device and DD: Data Down stream carries data from the layer-1 device to the ARCOFI. A FSC Frame Synchronization Clock is supplied to the ARCOFI as well as a DCLK 1.536-MHz data clock for bit clocking.

In terminal mode the IOM-2 frame consists of three IOM channels numbered respectively 0,1 and 2. The ARCOFI can receive and transmit voice data in the IOM B1 & B2 channels as well as in the IC1 and IC2 intercommunication channels located in IOM channel 0 and 1 respectively.

The IC1 and IC2 intercommunication channels can be used in the terminal for local bearer data communication. This makes post-processing of voice/data information possible.



IOM-2 Monitor Channel

All programming data required by the ARCOFI including coefficients are transmitted exclusively in the monitor 1 time slot in the IOM channel 1. The MON1 monitor channel allows a point to multi-point access where the layer-1 component acts as master to programmable devices like the ARCOFI. Each programmable device is accessed by sending a specific address byte at the start of each command stream followed by an identification byte. The programmable device compares the received address byte with its own internally wired IOM address before executing a command.

All programmed coefficients can be read back when issuing an appropriate CMDR read. The ARCOFI responds by sending two IOM-2 specific bytes unambiguously identifying the chip type and version followed by the issued SOP or COP read sequence.

Monitor Transfer Protocol

The transfer of a low of commands in the MON1 channel is regulated by a handshake protocol mechanism implemented by two bits MX and MR in the fourth slot of the IOM channel 1. The maximum effective transfer rate in the MON1 channel is 32 kbit/s. Thanks to the implemented handshake mechanism a command sequence can be delayed at the convenience of the transmitting IOM bus master device and resumed subsequently. An abort mechanism allows the interruption of a command sequence. In that case the command may be partially executed by the ARCOFI (i.e. coefficients partially modified in the ARCOFI CRAM). If use of the abort mechanism is made, a new command has to be issued to program the ARCOFI.

C/I Channel

The first four bits of the IOM Channel 1 C/I channel are transparently routed to the four ARCOFI PCI pins SA-SD. SA & SB from the presently addressed ARCOFI are shown in the 3rd and 4th C/I bit position. The SP1 and SP2 strapping as well as the AD-bit in the CMDR register determine which ARCOFI is addressed.

Pins SA-SD can be configured individually as input or output and will appear respectively in the DD or DU CH1-C/I channel.

The mapping of the peripheral control interface (PCI) pins SA,SB,SC,SD into the six C/I channel bits depends on the hardwired SP1 address as follows:

SP1 = 1

DD and DU	-	-	SB	SA	SD	SC	-	-
-----------	---	---	----	----	----	----	---	---

SP1 = 0 (AM = 0; two chip mode)

DD and DU	SD	SC	-	-	-	-	-	-
-----------	----	----	---	---	---	---	---	---

SP1 = 0 (AM = 1; one chip mode)

DD and DU	SD	SC	SB	SA	-	-	-	-
-----------	----	----	----	----	---	---	---	---

The ARCOFI with the address pin SP1 strapped to 0 transmits/receives the SD and SC values on DU/DD

In case a reset has been asserted, the SA to SD pins are programmed as input, however the SA to SD values are not switched to the C/I channel unless a CR1 to CR4 SOP_0 write command is issued.

Programmable Registers

The SLD or the IOM-2 bus mode is used to control and program the operations performed by the ARCOFI. The following lists the ARCOFI internal registers.

ARCOFI Digital Interface (ADI)

- CMDR: 8-bit command register
- CR1-4: four 8-bits configuration registers

ARCOFI Signal Processor (ASP)

- Two transmit gain registers (GX)
- Two receive gain registers (GR)
- 10 FX filter coefficient registers
- 10 FR filter coefficient registers
- One Z sidetone gain register
- Two DTMF frequency tone registers
- 6 Tone ring/tone generator frequency register
- 3 Tone ring/tone generator amplitude register
- 6 Beat tone generator timing register

To familiarize the user with ARCOFI, a program, named ARCOS, is available. (see description of ARCOS page 602).

This software tool allows the user to program the different ARCOFI registers and to evaluate the chip in a real environment.

Filter Programming Ranges

Parameter	Symbol	Limit Values		Unit	Tolerance
		min.	max.		
GX-filter ¹⁾		0	6	dB	0.25 dB
GR-filter		-6	0	dB	0.25 dB
Z-filter		$-\infty$	0	dB	± 1 dB
Tone generator gain	G_{Tone}	$-\infty$	0	dB	
Tone generator frequency	f_{Tone}	0	4000	Hz	
Tone generator time	t_{Tone}	1	16384	ms	
DTMF generator		380	1630	Hz	$\pm 1\%$

1) Remark: The programming of GX-filter depends on the programming of the half-channel (AFE).

A DTMF generator is also built into the ARCOFI transmit path.

A preemphasis of 2 dB is guaranteed between the high and the low DTMF frequency groups. The total power level of all unwanted frequency components is at least 20 dB below the level of the low frequency group component of the signal.

The level of any unwanted frequency component does not exceed the following limits:

- In the frequency band 0-300 Hz: > -33 dB
- In the frequency band 300-3400 Hz: > 20 dB
- In the frequency band 3400-4000 Hz: > -33 dB

All generated DTMF frequencies are guaranteed within a $\pm 1\%$ deviation.

DTMF Frequency Programming

CCITT Q.23	ARCOFI Nominal	Relative Deviation from CCITT*	Hex Coefficient H nibble/L nibble
Low Group			
697	697.754	+1081 ppm	F8
770	773.438	+4464 ppm	A8
852	852.783	- 513 ppm	F9
941	939.453	-1646 ppm	BA
High Group			
1209	1203.125	-4883 ppm	21
1336	1339.844	+2877 ppm	40
1477	1476.563	- 295 ppm	10
1633	1632.813	- 114 ppm	00

*: The deviations due to the inaccuracy of the incoming clock CLK, when added to the nominal deviations tabulated above give the total absolute deviation from the CCITT recommended frequencies.

Command Register (CMDR)

	Logical 1	Logical 2
BIT 7	AD=1; if bit AD matches the address convention strapped on SP1; pin SIP is active as output during SLD transmit time slots.	AD=0; if address bit is not consistent with the logical level strapped on SP1; SIP is tristated during SLD transmit time slots.
BIT 6	R/W=1; reading from CR1, CR2, CR3, CR4 or CRAM.	R/W=0; writing to CR1, CR2, CR3, CR4 or CRAM.
BIT 5	PU=1; The ARCOFI is in a normal operating mode (powered up).	PU=0; The ARCOFI is placed in stand by (powered down). All register contents are saved.
BIT	RCS=1; receive and transmit in CH-B2.	RCS=0; receive and transmit in CH-B1.

Note: RCS versus AM bit

- a) In case of one chip mode (AM=1) RCS operates as described above.
- b) In case of two chip mode (AM=0) and pin SP1 is strapped to 0 same as above. If SP1 is strapped to 1, RCS operates in reverse order:

RCS=1 RX and TX in channel B1

RCS=0 RX and TX in channel B2

This provides a contention-free switching of the B1 & B2 channels while in two-chip mode.

A full sequence consists of a command byte followed by <..>n byte coefficients.

BIT	3	2	1	0	CMD Name	Status Mode	CMD Sequence Length	CMD Sequence Description	; Comments
0	0	0	0	0	SOP_0	R/W	5	<CR4><CR3><CR2><CR1>	; Reset F flag
0	0	0	0	1	COP_1	R/W	5	<t1><t1><f1><f1>	; Beat tone time span ; T1 & tone generation ; frequency F1
0	0	1	0	0	COP_2	R/W	3	<gx1><gx2>	; GX gain
0	0	1	1	1	COP_3	R/W	5	<t2><t2><f2><f2>	; Beat tone time span ; T2 & tone generation ; frequency F2
0	1	0	0	0	SOP_4	R/W	2	<CR1>	; Configuration reg. 1
0	1	0	1	1	SOP_5	R/W	2	<CR2>	; Configuration reg. 2
0	1	1	0	0	SOP_6	R/W	2	<CR3>	; Configuration reg. 3
0	1	1	1	1	SOP_7	R/W	2	<CR4>	; Configuration reg. 4
1	0	0	0	0	COP_8	R/W	3	<dtmf_high><dtmf_low>	; DTMF frequencies
1	0	0	1	1	COP_9	R/W	5	<gz><a3><a2><a1>	; GZ gain & tone ; generator amplitudes ; A1, A2, A3
1	0	1	0	0	COP_A	R/W	9	<fx1><fx2><fx3><fx4> <fx5><fx6><fx7><fx8>	; FX frequency correc- ; tion coefficient set 1
1	0	1	1	1	COP_B	R/W	3	>gr1><gr2>	; GR gain
1	1	0	0	0	COP_C	R/W	9	<fr1><fr2><fr3><fr4> <fr5><fr6><fr7><fr8>	; FR frequency correc- ; tion coefficient set 1
1	1	0	1	1	COP_D	R/W	5	<fr9><fr10><fx9><fx10>	; FX & FR coefficient ; set 2
1	1	1	0	0	COP_E	R/W	5	<t3><t3><f3><f3>	; Beat tone time span ; T3 & tone generation ; frequency F3
1	1	1	1	1	NOP	R		<hFF>	; No operation; CMDR ; bits 7,6,5,4 ; are masked
						W			; No operation, CMDR ; bits 7,6,5,4 can be ; written

W: ; write
R: ; read
<..> ; mandatory byte coefficient sequence

BITS	7	6	5	4	3	2	1	0
	AD	R/W	PU	RCS	CMB3	CMB2	CMB1	CMB0

Initial value on RESET: 0F_H (NOP)

Configuration Register 2 (CR2)

	Logical 1	Logical 0
BIT 7	SD=1; SD pin programmed as input.	SD=0; SD pin programmed as output.
BIT 6	SC=1; SC pin programmed as input.	SC=0; SC pin programmed as output.
BIT 5	SB=1; SB pin programmed as input.	SB=0; SB pin programmed as output.
BIT 4	SA=1; SA pin programmed as input.	SA=0; SA pin programmed as output.
BIT 3	ELS=1; PCI pins SA-SD, which are not programmed as TX-SIG transmit inputs, tristate SIP in TX direction.	ELS=0; pins SA-SD, which are not TX-SIG inputs, are sending zeros.
BIT 2	AM=1; only one device is connected to the SLD bus, send NOP's during TX-FC.	AM=0; two devices are to the SLD bus, tristate SIP during TX-FC.
BIT 1	TR=1; Three party conferencing enabled CH-B1 is added to CH-B2 in the RX direction.	TR=0; Three party conferencing disabled.
BIT 0	SLD Mode EFC=1; Enable feature control. TX-FC channel is enabled.	EFC=0; TX-FC channel disabled (high Z).
	IOM-2 Mode SEL=1; Bearer channels transmit & receive in IOM channel 0.	SEL=0; B channels transmit & receive in IOM channel 1.

BITS	7	6	5	4	3	2	1	0
	SD	SC	SB	SA	ELS	AM	TR	EFC/SEL

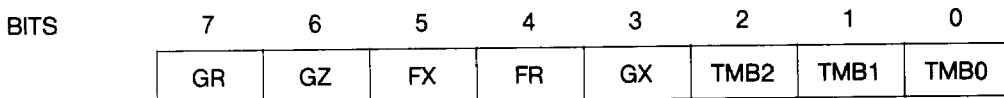
Initial value on RESET: F9_h

Configuration Register 1 (CR1)

	Logical 1	Logical 0
BIT 7	GR=1; GR gain loaded from CRAM	GR=0; GR gain set to 0 dB
BIT 6	GZ=1; Z gain loaded from CRAM	GZ=0; Z gain set to -18 dB
BIT 5	FX=1; X filter loaded from CRAM	FX=0; X filter set to 0 dB flat
BIT 4	FR=1; R filter loaded from CRAM	FR=0; R filter set to 0 dB flat
BIT 3	GX=1; GX gain loaded from CRAM	GX=0; GX gain set to 0 dB



BIT	2	1	0	Test Mode	Configuration Description
	0	0	0	NOT	No test mode
	0	0	1	ALS	Analog loop back via converter registers.
	0	1	0	ALM	The MIC/XIN input is looped back to HON & HOP. (AHO amplifier) the FHM input is looped back to analog MUX. FHM input is looped back to LSN & LSP. (ALS amplifier)
	0	1	1	BYP	By-pass: the analog front end is by-passed. FHM serves as a direct single ended input to the A/D-converter while HOP outputs the single ended signal generated by the D/A converter.
	1	0	0	IDR	Data RAM initialisation, reset all data RAM locations to hex 00.
	1	0	1	DLS	Digital loop back via converter registers.
	1	1	0	DLM	The D/A output is looped back to the A/D input via the analog I/O MUX.
	1	1	1	DLP	Digital loop back via PCM registers.



Initial value on RESET: 00_H

Configuration Register 3 (CR3)

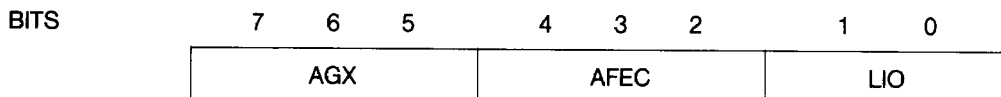
BIT	7	6	5	Analog gain adjustment in transmit direction for the MIC input. Gain factor tolerance range ± 0.5 dB			
	0	0	0	52.0 dB default on RESET	0	1	1
	0	0	1	46.0 dB	1	0	0
	0	1	0	40.0 dB	1	0	1
	1	1	1	X input enabled with a 15.1 dB amplification factor MIC input disabled	1	1	0
							34.0 dB
							28.0 dB
							22.0 dB
							17.0 dB

BIT 4 3 2 Operating mode Configuration description
Analog Front End Control (AFEC)

Code	State	MIC/IN	FHM	H OUT	L OUT	Comments
0 0 0	POR	OFF	OFF	OFF	OFF	Power on reset
0 0 1	RDY	ON	OFF	ON	OFF	Ready
0 1 0	LH1	OFF	OFF	OFF	ON	Loud hearing 1
0 1 1	LH2	ON	OFF	OFF	ON	Loud hearing 2
1 0 0	LH3	ON	OFF	ON	ON	Loud hearing 3
1 0 1	HFS	OFF	ON	OFF	ON	Hands-free
1 1 0	MUT	OFF	OFF	ON	OFF	Mute
1 1 1	RES	X	X	X	X	Reserved

BIT 1 0 Operating Mode Linear Input/Output (LIO)

0 0	LIO 0 Normal I/O Mode	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>B#1</td><td>B#2</td><td>FC</td><td>SIG</td></tr></table>	B#1	B#2	FC	SIG	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>B#1</td><td>B#2</td><td>FC</td><td>SIG</td></tr></table>	B#1	B#2	FC	SIG
B#1	B#2	FC	SIG								
B#1	B#2	FC	SIG								
0 1	LIO 1; ELS = 0 Mixed I/O Mode	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>B#1</td><td>B#2</td><td>FC</td><td>SIG</td></tr></table>	B#1	B#2	FC	SIG	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>B#1</td><td>B#2</td><td>MSB</td><td>LSB</td></tr></table>	B#1	B#2	MSB	LSB
B#1	B#2	FC	SIG								
B#1	B#2	MSB	LSB								
1 0	LIO 2 Linear I/O Mode	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>MSB</td><td>LSB</td><td>FC</td><td>SIG</td></tr></table>	MSB	LSB	FC	SIG	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>MSB</td><td>LSB</td><td>FC</td><td>SIG</td></tr></table>	MSB	LSB	FC	SIG
MSB	LSB	FC	SIG								
MSB	LSB	FC	SIG								
1 1	LIO 3 Reserved										



Initial value on RESET: 00_h

Configuration Register 4 (CR4)

	Logical 1	Logical 0
BIT 7	DHF=1; digital high-pass in TX direction enabled	DHF=0; digital high-pass in TX disabled
BIT 6	DTMF=1; DTMF generator enabled	DTMF=0; DTMF generator disabled
BIT 5	TG=1; tone ring enabled	TG=0; tone ring disabled
BIT 4	BT=1; beat tone generator enabled	BT=0; beat tone generator disabled
BIT 3	TM=1; tone mode bit set, incoming voice is activated	TM=0; incoming voice is blocked
BIT 2	BM=1; beat mode. 3 tone ring activated when BT generator enabled.	BM=0; 2 tone ring activated when BT generator enabled.
BIT 1	PM=1; piezo mode bit set, tone generator is outputted to the piezo ring pins SA & SB	PM=0; the tone generator is directed to the loudspeaker (D/A out)
BIT 0	A/ μ =1; μ law enabled	A/ μ =0; A law enabled

BITS	7	6	5	4	3	2	1	0
	DHF	DTMF	TG	BT	TM	BM	PM	A/ μ

X: don't care

Initial value of RESET: 00_H

ARCOFI Software Tool: ARCOS

The ARCOS program kit provides the means to exercise the PSB 2160 ARCOFI in a real environment. The ARCOFI capabilities are made easily understandable thanks to a "DIALOG MODE" allowing direct programming of the component. Various operating conditions can be programmed into the ARCOFI registers so as to evaluate its performances. The support software has also been designed to generate all the necessary coefficients to program the Siemens PSB 2160 ARCOFI signal processor.

ARCOS supports:

- Generation of coefficients for the three ARCOFI tone generator registers
- Generation of coefficients for the ARCOFI DTMF tone generator registers
- Generation of coefficients for the two ARCOFI programmable gain registers GX and GR.
- Generation of coefficients for the Z side tone gain register
- Generation of coefficients for the FX and FR correction filter registers. Adaptive software calculates coefficients to fit a target amplitude frequency response. All these features are provided under the "Search Coefficient" mode.
- A user friendly dialogue mode allowing full programming of the ARCOFI configuration registers and coefficient RAM.
- Statistical information menus allowing users to explore the programming possibilities of the ARCOFI
- ARCOFI transmission measurements using the Wandel & Goltermann PCM-4.

Figure 3**ARCOS Main Menu**

ARCOFI® COEFFICIENT SOFTWARE			
ARCOS			Version 3.0
Copyright 1988	Siemens AG	Munich,	West-Germany
Search Coefficient			(S)
Statistical Information			(I)
Dialog-Mode			(D)
Quit			(Q)
ARCOS>			

Search Coefficient Mode

With this mode the user can ask whether a specific value of a filter is available or not. The answer is the closest values available, their corresponding coefficient as well as the deviation from the desired value.

Figure 4

Search Coefficient Mode

Syntax		Unit	Search Coefficient		Range
D[TMF]	{Frequency}	[Hz]	D	660 1200	380 .. 1650 Hz
F[req]S	{Frequency}	[Hz]	FS	500 600.5	0 .. 8000 Hz
F[req]	{Frequency}	[Hz]	FT	500 600.5	0 .. 4000 Hz
T[ime]	{Time}	[ms]	T	1000 20 333	1 .. 16400 ms
					- ∞ .. 0 dB
GZ or G[ain]	{Gain}	[dB]	GZ	8	- ∞ .. 14 dB
GX or GR	{Gain}	[dB]	GX	12 2 -4	0 .. 1
GZ> or G>	{Value}	[--]	GZ>	0.34	0 ..
GX> or GR>	{Value}	[--]	GX>	2.34 0.54	
FX or FR A gain Fb freq Fc freq [A gain Fb freq Fc freq]					
FX or FR Filename [Fast Middle Best]					
FX or FR ? [Filename =]					
S[ound]		--	Sounds last specified		
O[utput]		--	Square-Frequencies and Times		
Q[uit]		--	Output to PRN, Harddisk, Screen		
<CR>		--	Quit		
		--	This Picture		
ARCOS>					



Statistical Information Mode

The "Statistical Information" mode permits the generation of tables showing the coefficients of different filters or generators and makes analysis of accuracy possible.

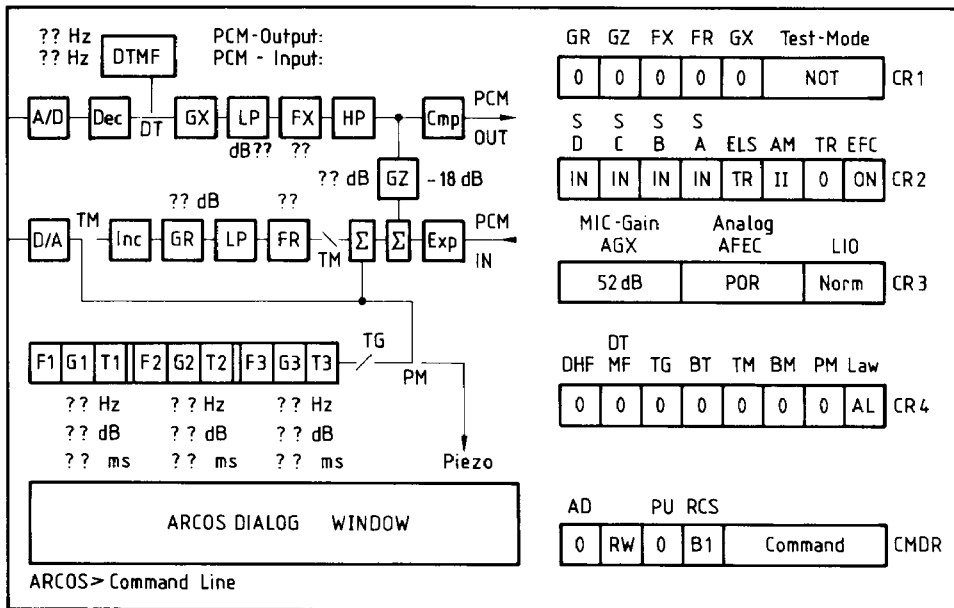
Figure 5**Statistical Information Menu**

Statistical Information	
Frequency DTMF-Tone Generator	(D)
Frequency Tone Generator (Trapezoid)	(F)
Frequency Tone Generator (Square)	(S)
Time Tone Generator	(T)
Gain Tone Generator and GZ-Filter	(G, Z)
Gain GX- and GR-Filter	(X, R)
Output to PRN, Harddisk, Screen	(O)
Quit	(Q)
ARCOS > T	

Dialog Mode

With the dialog mode the user becomes familiar with the ARCOFI chip in a real environment. The configuration registers as well as coefficients in CRAM can be read and written. Any change of register content is instantaneously carried out and the new status of ARCOFI is displayed on the screen.

Figure 6
Dialog Mode



The program ARCOFI runs on IBM- and IBM-compatible PC when the last is equipped with a Siemens ISDN User Board SIPB 5000.

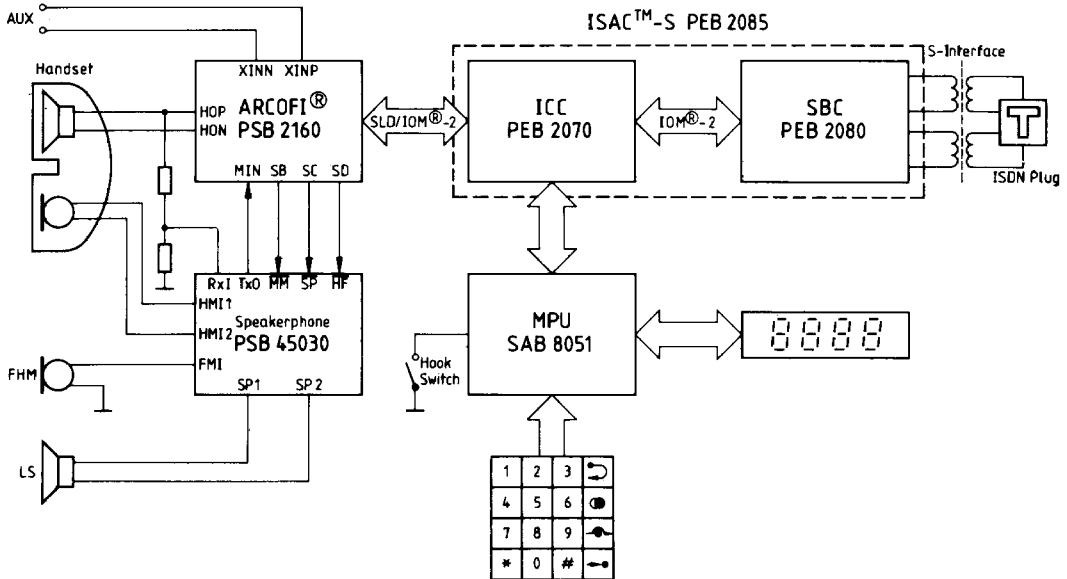
Nevertheless a shrunken version of ARCOFI, named ARCOFI-D (ARCOFI-DEMO), works without user board and provides the user with the modes "Search Coefficient" and "Statistical Information".

Application Suggestions

The ARCOFI forms, together with a PEB 2070 ICC and a PEB 2080 SBC (resp. a PEB 2085 ISAC-S) a solution for a complete digital telephone as specified in the CCITT I-series recommendation at the "S" reference point.

The digital telephone can be expanded for hands-free applications by adding the voice switched speakerphone circuit PSB 45030.

Application Circuit



The terminal mode IOM-2 frames consist of three IOM channels numbered respectively 0,1 and 2. The ARCOFI can receive and transmit voice data in the IOM B1 & B2 channels as well as in the IC1 and IC2 intercommunication channels located in IOM channels 0 and 1 respectively.

The IC1 and IC2 intercommunication channels can be used in the terminal for local data communication. This makes postprocessing of voice/data information possible (see figure 7).

Figure 7
Post Processing the ARCOFI Voice Channels

