SAMSUNG Semiconductor

KM658128

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

May 1991

FEATURES

- Fast Access Time:
  — $\overline{CE}$ Access Time ..... 80, 100, 120ns (Max)
  — Cycle Time Random Read/Write Cycle Time
  .....130, 160, 190ns (Max)
- Low Power Dissipation .....200mW typ (Active)
  0.5mW typ (Standby)
- Single 5V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- Non Multiplexed Address
- Three-State Output
- 512 Refresh Cycles/8ms
- Self Refresh Current:
  1mA (Max, Standard)
  200μA (Max, Low Power Version)
  100μA (Max, Low, Low Power Version)
- Data Retention Supply Voltage: 3.0V or 5.5V
- Battery Back-Up Capability with
  KM658128LDXX-XXL
- CS Mode Standby Cycle
- 32-pin JEDEC Standard Plastic Package
  — DIP (600 mil), SOP (450 mil), SOP (525 mil)

DESCRIPTION

The KM658128 is a 1,048,576-bit high-speed Pseudo Static Random Access Memory organized as 131,072 words by 8 bits fabricated using advanced CMOS technology.

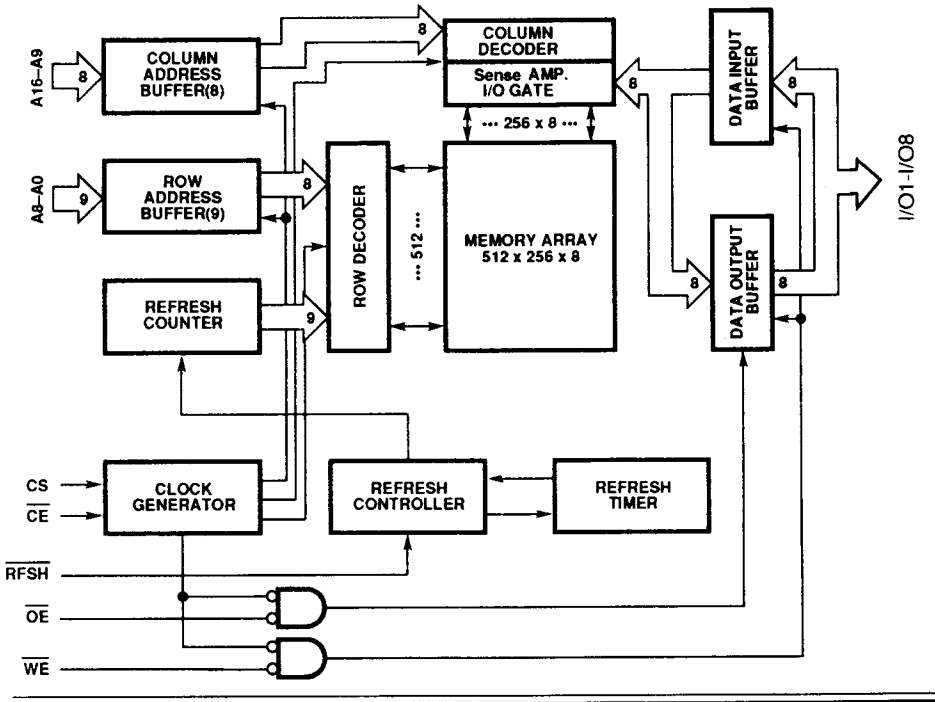
The device, utilizing a one transistor DRAM cell with on-chip refresh timer, provides the advantages of DRAM (low cost, high density) and Static RAM (low standby power and ease of use).

The pin-out of KM658128 follows the JEDEC standard for Static RAM with the addition of a $\overline{RFSH}$ input. The $\overline{RFSH}$ input allows two types of refresh operation: Auto Refresh and Self Refresh.

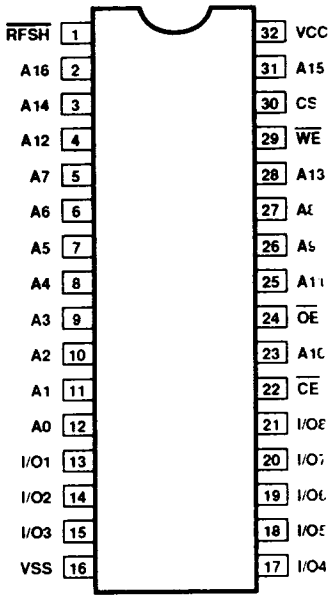
The $\overline{CE}$ only Refresh is also supported.

The KM658128 supports a write function similar to static RAM in that the input data is written into the memory a the rising edge of $\overline{WE}$, thus simplifying the interface to standard microprocessors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Names	Pin Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
CS	Chip Select
I/O1~I/O8	Data Inputs/Outputs
VCC	Power Supply
VSS	Ground

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	Tstg	−65 to +150	°C
Storage Temperature Under Bias	Tstg	−10 to +85	°C
Operating Temperature	Ta	0 to +70	°C
Soldering Temperature · Time	Tsolder	260 · 10	°C · sec

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1.0	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = 3.0V for pulse width ≤ 10 ns

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ	Max	Units
Input Leakage Current	I_{LI}	All Inputs, V_{IN} = 0 to V_{CC}		−10	—	+10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}		−10	—	+10	μA
Operating Power Supply Current	I_{CC1}	I/O = 0mA, t_{CYC} = t_{RC} min. $\overline{CE}$, CS, Address Cycling	130ns 160ns 190ns	— — —	— — —	70 60 50	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}		—	1	2	mA
	I_{SB2}	$\overline{CE}$ ≥ V_{CC} − 0.2V $\overline{RFSH}$ ≥ V_{CC} − 0.2V	KM658128XX-XX KM658128LXX-XX KM658128LXX-XXL	— — —	— — —	1 200 100	mA μA μA
Self Refresh Current	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}		—	1	2	mA
	I_{CC3}	$\overline{CE}$ ≥ V_{CC} − 0.2V $\overline{RFSH}$ ≤ 0.2V	KM658128XX-XX KM658128LXX-XX KM658128LXX-XXL	— — —	— — —	1 200 100	mA μA μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	10	pF

Note: Capacitance is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	OUT	READ
L	H	X	X	L	IN	WRITE
L	H	X	H	H	High-Z	$\overline{CE}$ Refresh
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh
H	X	H	X	X	High-Z	Standby

Note: X = Don't care

AC CHARACTERISTICS

Test Conditions (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Input Pulse Level 0.6V
Input Rise and Fall Time 5ns
Input Timing Reference Level ..... V_{IH}=2.4V, V_{IL}=0.8
Output Timing Reference Level ..... V_{OH}=2.2V, V_{OL}=0.8V
Output Load ..... C_L = 100pF + 1 TTL

Item	Symbol	KM658128-8		KM658128-10		KM658128-12		Units
		Min	Max	Min	Max	Min	Max	
Random Read or Write Cycle Time	t_{RC}	130	—	160	—	190	—	ns
Random Read Modify Write Cycle Time	t_{RWC}	190	—	220	—	260	—	ns
Chip Enable Access Time	t_{CEA}	—	80	—	100	—	120	ns
Output Enable Access Time	t_{OEA}	—	30	—	30	—	40	ns
Chip Disable to Output in High-Z	t_{CHZ}	0	30	0	30	0	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}	20	—	20	—	20	—	ns
Output Disable to Output in High-Z	t_{OHZ}	—	25	—	25	—	30	ns
Output Disable Hold Time	t_{ODH}	10	—	10	—	10	—	ns
Output Disable Set-up Time	t_{ODS}	0	—	0	—	0	—	ns
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip Enable Pulse Width	t_{CE}	80n	10µ	100n	10µ	120n	10µ	s
Chip Enable Precharge Time	t_P	40	—	50	—	60	—	ns
Address Set-up Time	t_{AS}	0	—	0	—	0	—	ns
Address Hold Time	t_{AH}	30	—	30	—	35	—	ns
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns

AC CHARACTERISTICS (Continued)

Item	Symbol	KM658128-8		KM658128-10		KM658128-12		Units
		Min	Max	Min	Max	Min	Max	
$\overline{RFSH}$ Hold Time	t_{RHC}	15	—	15	—	15	—	ns
Refresh Command Delay Time (Standby Mode)	t_{RCD}	—	5	—	5	—	5	ns
Chip Select Set-Up Time	t_{CSS}	0	—	0	—	0	—	ns
Chip Select Hold Time [8]	t_{CSH}	30	—	30	—	35	—	ns
Write Command Pulse Width	t_{WP}	30	—	30	—	35	—	ns
Chip Enable to End of Write	t_{CW}	80	—	100	—	120	—	ns
Data In to End of Write	t_{DW}	25	—	25	—	30	—	ns
Data In Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	ns
Write to Output in High-Z	t_{WHZ}	—	20	—	25	—	30	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	40	—	50	—	60	—	ns
Refresh Precharge Time	t_{FP}	40	—	40	—	40	—	ns
Refresh Reset Time (Automatic Refresh)	t_{RFA}	0	—	0	—	0	—	ns
Refresh Command Pulse Width (Automatic Refresh)	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s
Automatic Refresh Cycle Time	t_{FC}	130	—	160	—	190	—	ns
Refresh Command Pulse Width (Self Refresh)	t_{FAS}	8	—	8	—	8	—	μs
Refresh Reset Time (Self Refresh)	t_{RFS}	130	—	160	—	190	—	ns
Refresh Periods (512 cycles)	t_{REF}	—	8	—	8	—	8	ms

Notes:

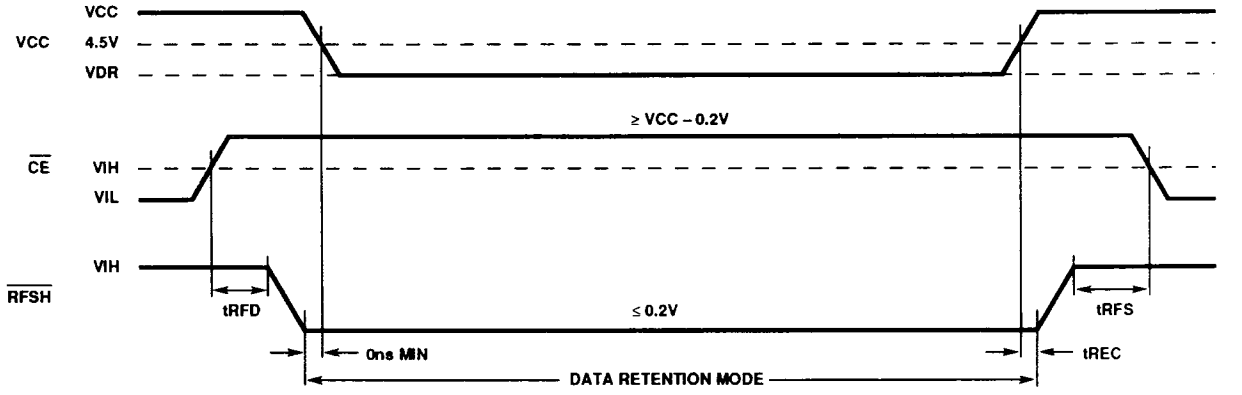
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under condition of t_T = 5ns and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
5. Transition time t_T is measured between V_{IH} (min) and V_{IL} (max).
6. After power-up, pause more than 100μs and execute at least 8 initialization cycles.
7. 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15μs after self refresh, in order to meet the refresh specification of 8ms and 512 cycles.
8. Under $\overline{OE}$ low fixed condition, t_{WP} must be longer to account for the write-to-output high Z (t_{WHZ}) and data set-up (t_{DW}).
   $t_{WP} = t_{WHZ} + t_{DW}$.

DATA RETENTION MODE CHARACTERISTICS (T_A = 0 to 70°C) (V_{DR}=3V, KM658128LDXX-XXL Only)

Item		Symbol	Min	Typ	Max	Units
Data Retention Supply Voltage		V_{DR}	3.0	—	5.5	V
Self Refresh Current	V_{DR} = 3V	I_{CC3}*	—	—	60	μA
	V_{DR} = 5.5V		—	—	100	
Recovery Time		t_{REC}	5	—	—	ms

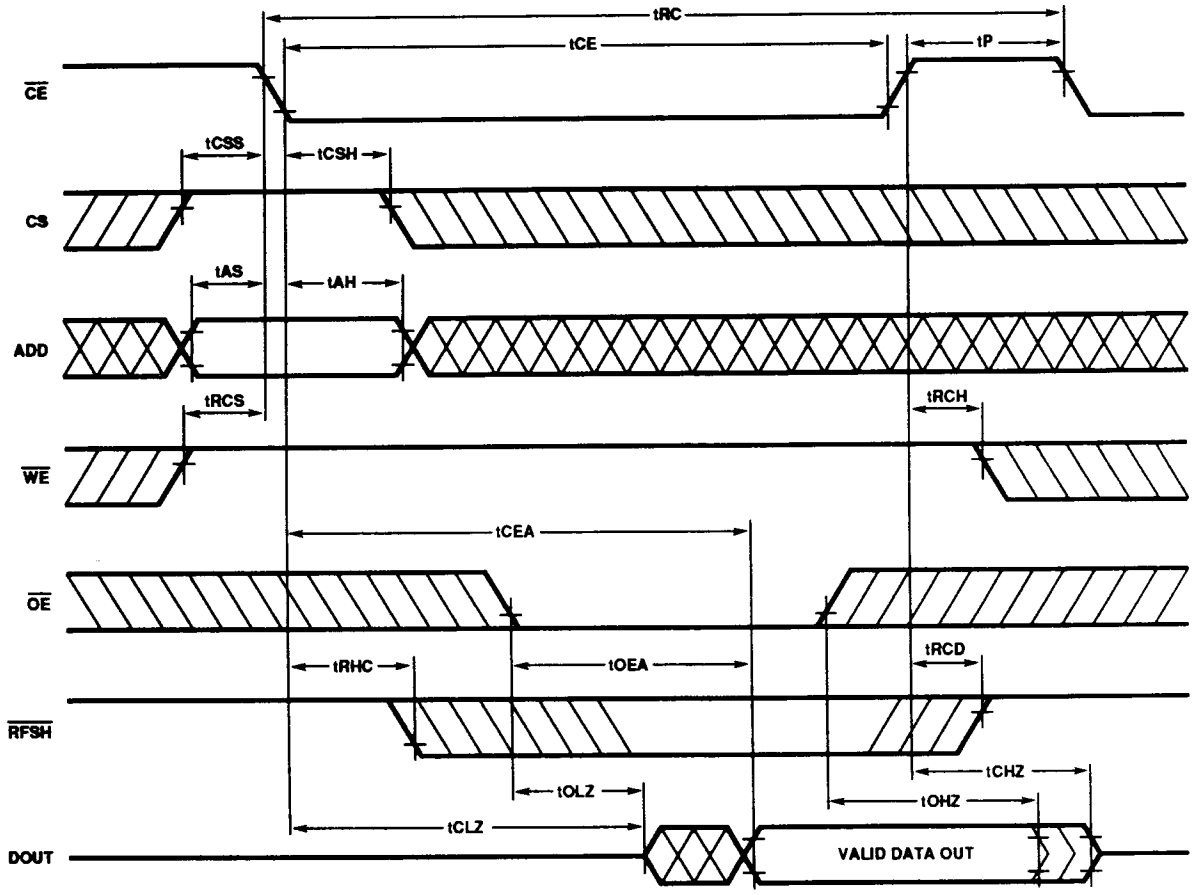
Notes: * $\overline{CE} \geq V_{CC} - 0.2V$ and $\overline{RFSH} \leq 0.2V$

1. The ramping rate of V_{CC} must be greater than |20ms/V| in order to maintain the proper operation of the device, i.e., the transition time from V_{CC} to V_{DR}, and V_{DR} to V_{CC} must be greater than 50ms during battery backup data retention mode.
2. Other than data retention mode, self refresh, automatic refresh or $\overline{CE}$ only refresh requires 512 refresh cycles/8ms.
3. During data retention mode, CS, $\overline{OE}$, $\overline{WE}$, A0 ~ A16 = Don't Care.



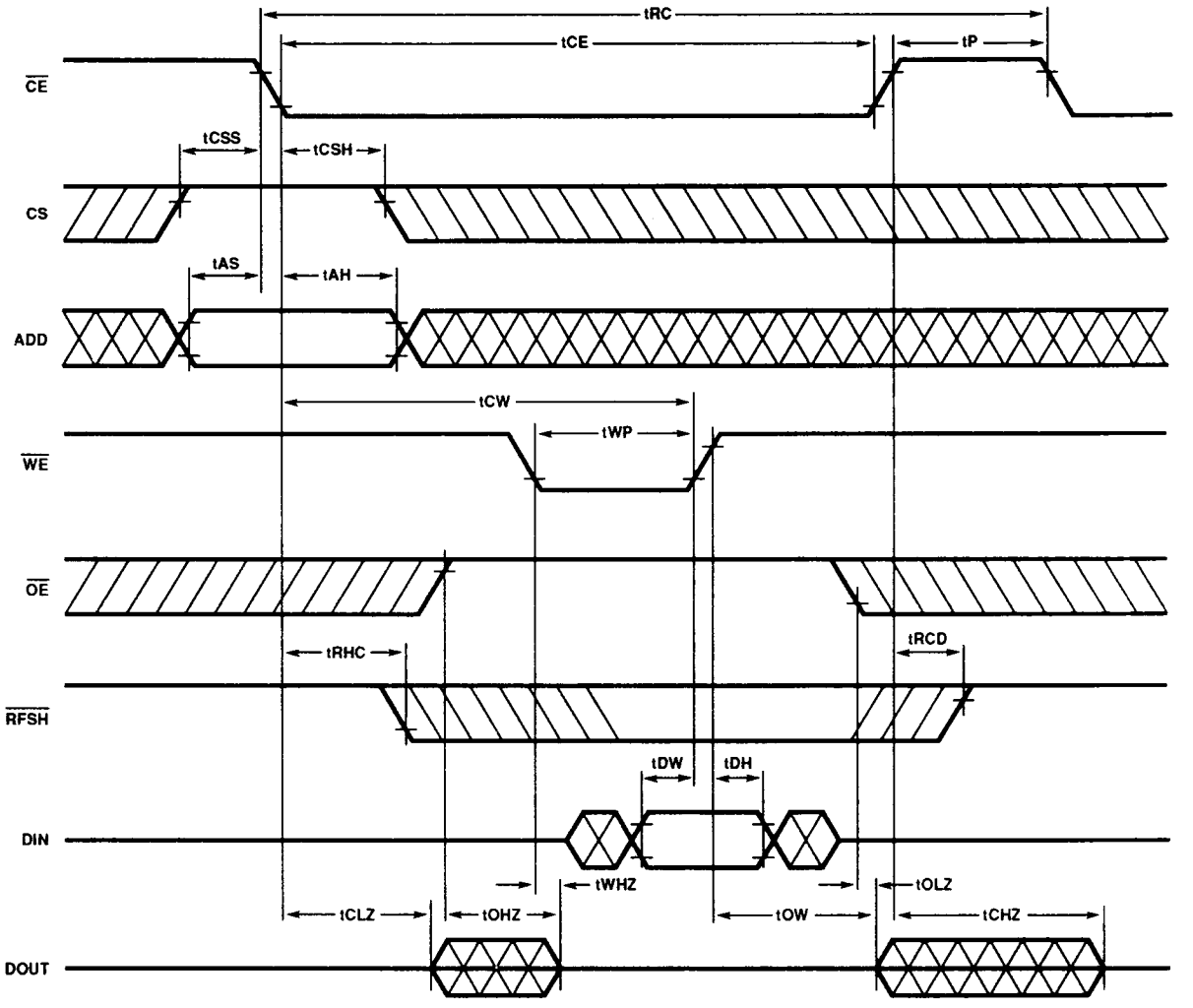
TIMING DIAGRAMS

Read Cycle



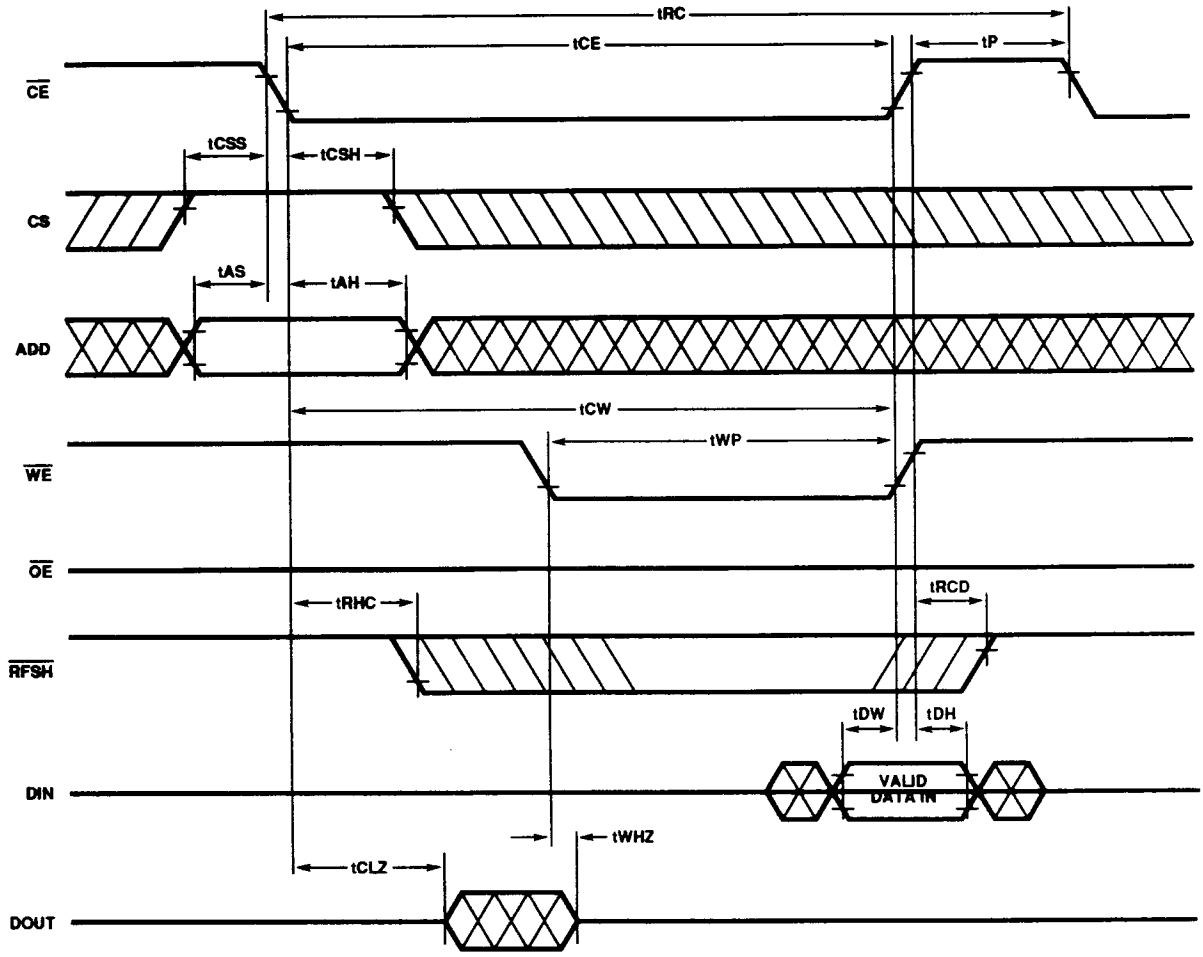
TIMING DIAGRAMS (Continued)

Write Cycle No. 1 ($\overline{OE}$ Controlled)



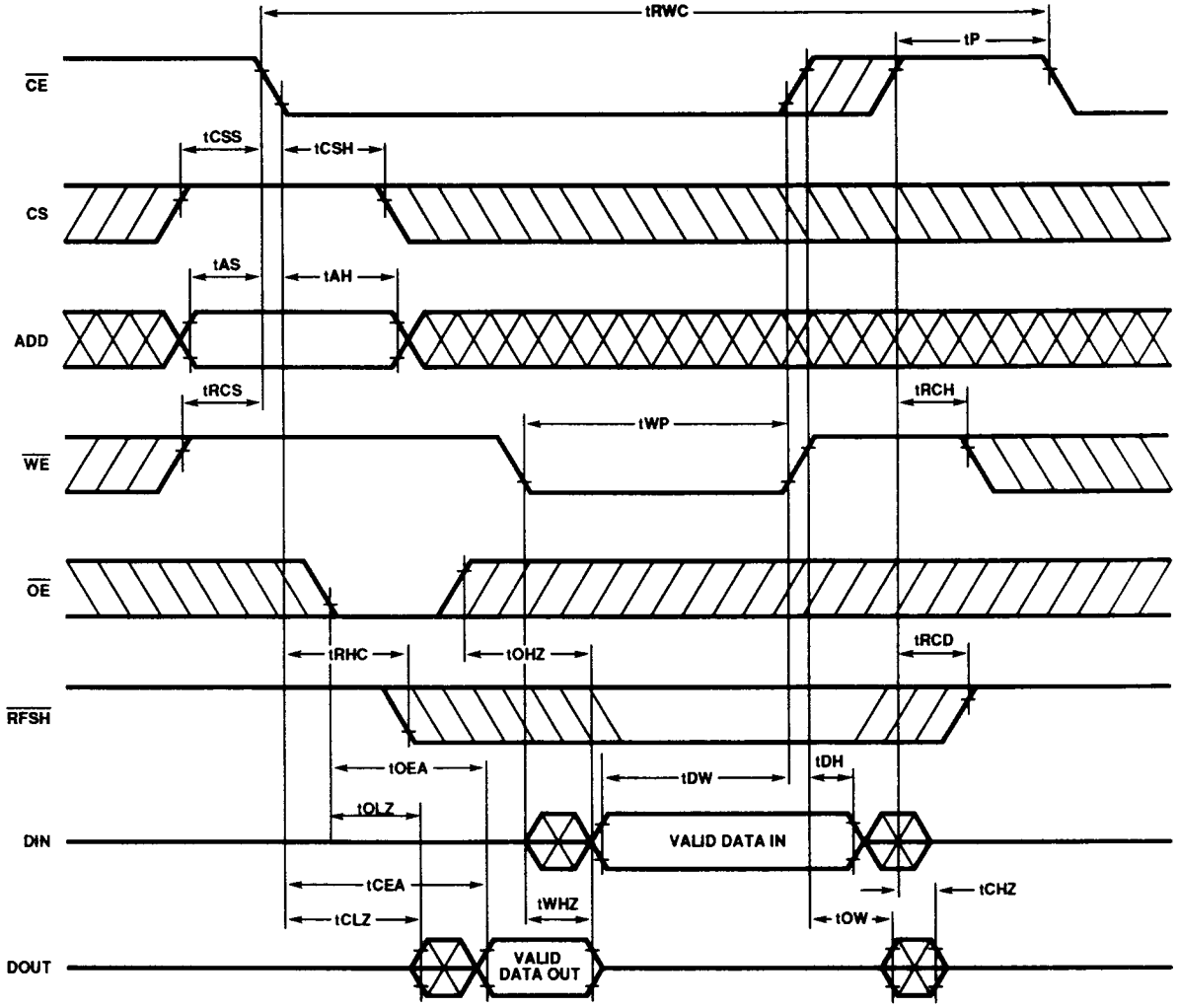
TIMING DIAGRAMS (Continued)

Wite Cycle No. 2 ($\overline{OE}$ Low Fixed)



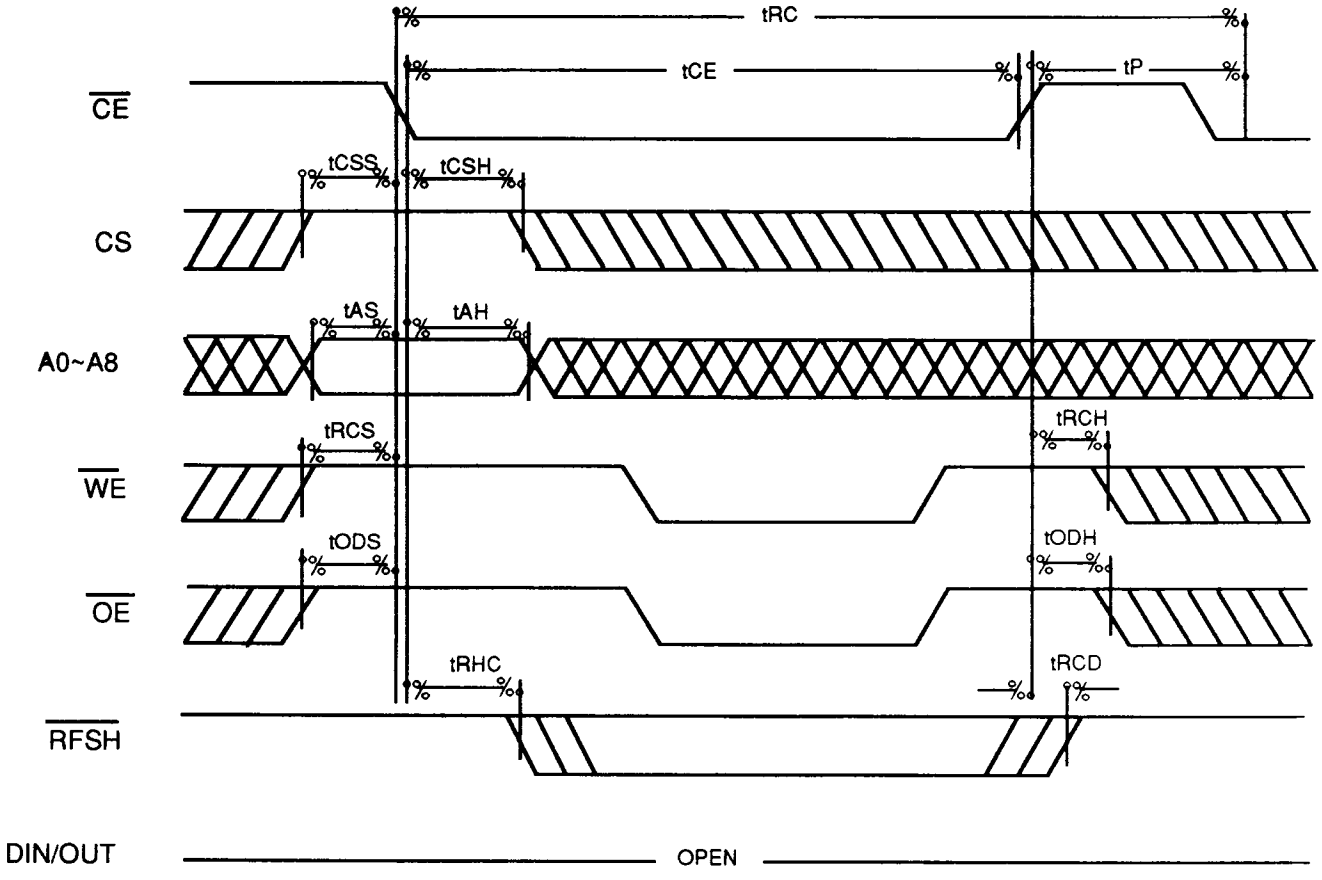
TIMING DIAGRAMS (Continued)

Read Modify Write Cycle



TIMING DIAGRAMS (Continued)

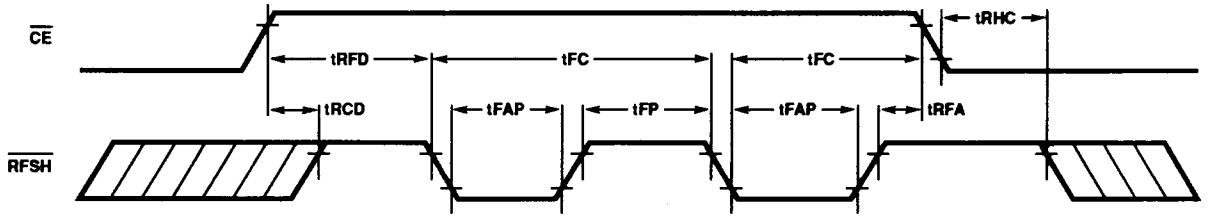
$\overline{CE}$ only Refresh



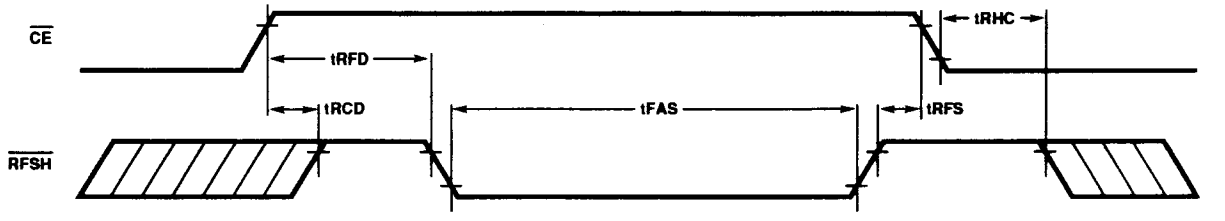
Note: Add 9~16 Don't Care

TIMING DIAGRAMS (Continued)

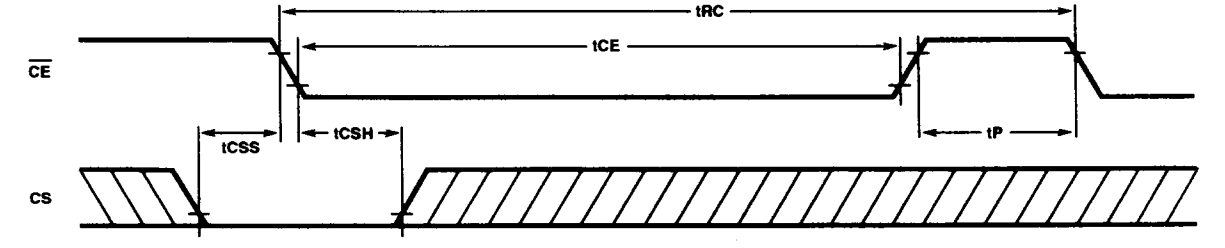
Automatic Refresh Cycle



Self Refresh Cycle



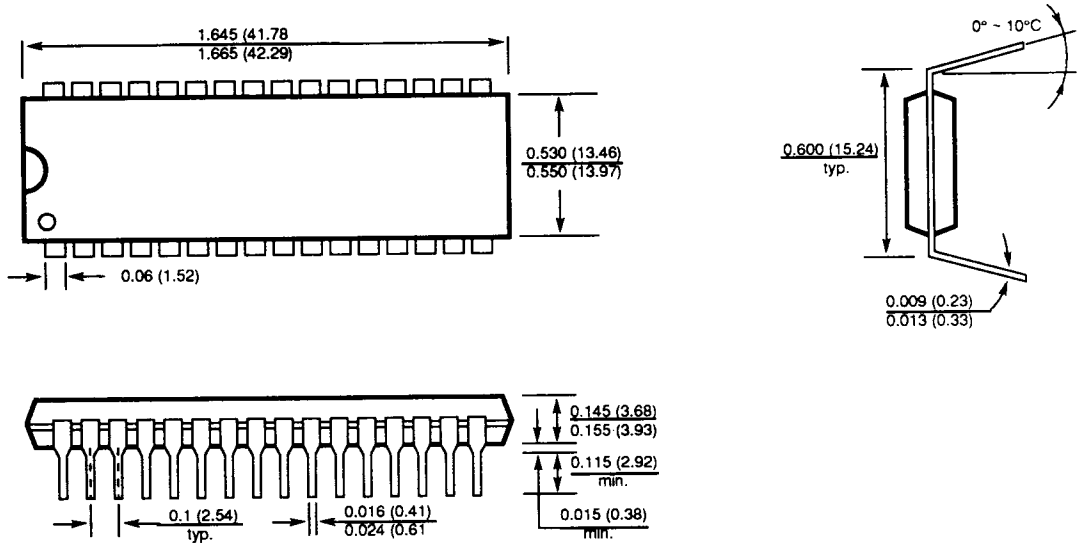
CS Standby Mode



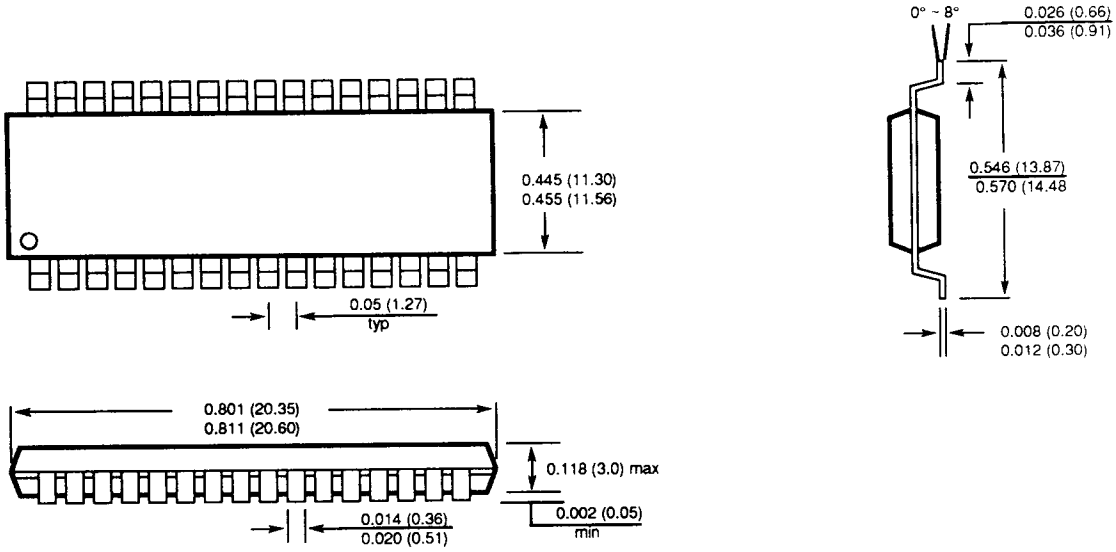
PACKAGE DIMENSIONS

32 Pin Plastic Dual In Line Package (600 mil)

Unit: Inches (Millimeters)



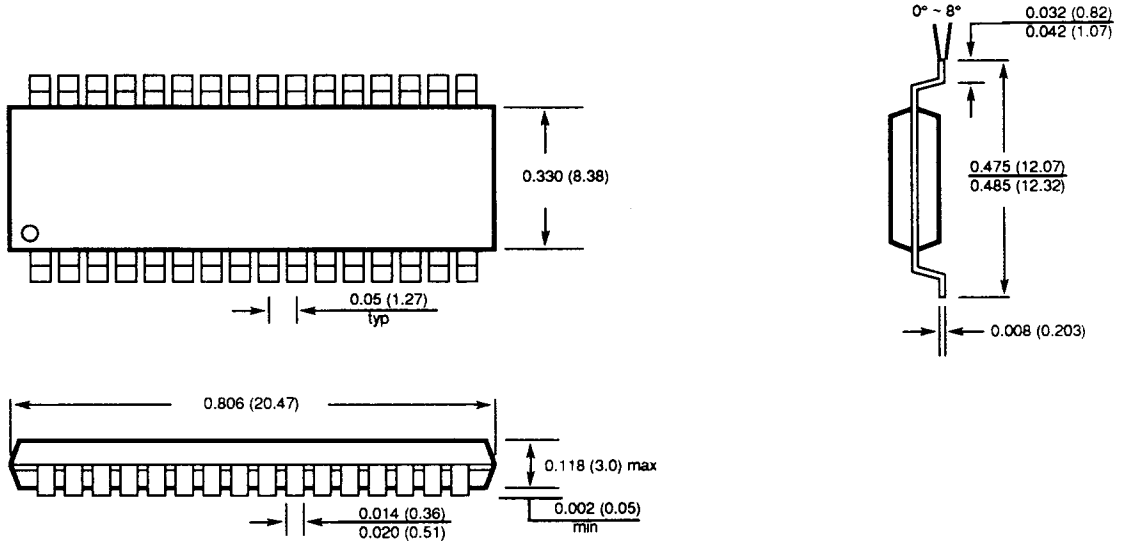
32 Pin Plastic Small Outline Package (525 mil)



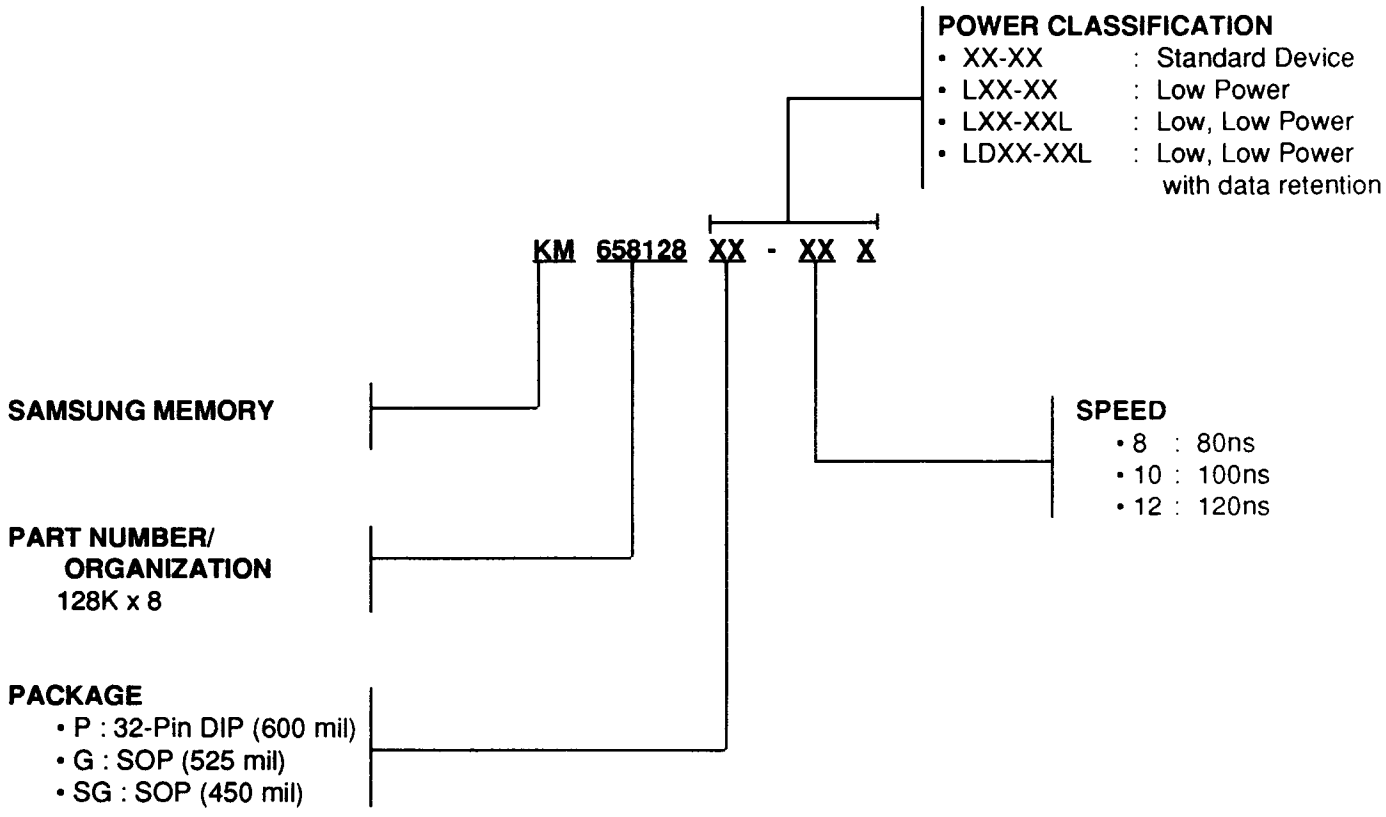
PACKAGE DIMENSIONS (Continued)

32 Pin Plastic Small Out Line Package (450 mil)

Unit: Inches (Millimeters)



ORDERING INFORMATION



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FAX:(617)273-9363

SAMSUNG
Semiconductor

3725 North First Street
San Jose, CA 95134-1708
Telephone: (408) 954-7000
(800) 423-7364
FAX: (408) 954-7873
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