Order this document by
MC68360UM/AD

Microprocessor and Memory Technologies Group

MC68360

Errata and Added Information to

MC68360 Quad Integrated Communication Controller User's Manual Rev 1

January 8, 1998

This document describes the latest information and changes to the first revision of the MC68360 user's manual.

Section 2 – Signal Descriptions

1. QUICC Functional Signal Groups.

On page 2-2, Figure 2-1, the signal names in the left column had a typo. The corrections for the typo are in the right column.

As seen on page 2-2	Correction
A31-A27/$\overline{WE3}$-$\overline{WE0}$	A31-A27/$\overline{WE0}$-$\overline{WE3}$
$\overline{SDACK2}$/L1TSYNCB/$\overline{CTS3}$/PC8	$\overline{SDACK2}$/L1TSYNCB/$\overline{CTS3}$/PC8
L1RSYNB/$\overline{CD3}$/PC9	L1RSYNB/$\overline{CD3}$/PC9
$\overline{SDACK1}$/L1TSYNCA/$\overline{CTS4}$/PC10	$\overline{SDACK1}$/L1TSYNCA/$\overline{CTS4}$/PC10
L1RSYNCA/$\overline{CD4}$/PC11	L1RSYNCA/$\overline{CD4}$/PC11

2. Error on TRIS

On page 2-4, Table 2-1, the function description of TRIS stated that it is sampled during system reset. This is not true. The TRIS signal is always sampled except during reset.

3. Missing Note.

On page 2-8, section 2.1.7.2 the following note should be added:

NOTE

User should note that the pin $\overline{AVEC}$/$\overline{IACK5}$ is always an open drain output.

4. MC68040 Companion Mode Bus Cycle Note.

On page 2-14, section 2.2, add the following note after the second paragraph:

NOTE

In MC68040 companion mode, the QUICC understands MC68040-type bus cycles but cannot generate them. If the QUICC becomes busmaster, e. g. for SDMA transfers, it will drive normal MC68030-type bus cycles with TT1 becoming $\overline{DS}$ again. This should normally be no problem since the MC68040 does not interpret these input signals, but external circuitry handling these signals must be aware of this fact.

Section 3 – Memory Map

1. Dual port RAM MAP

On page 3-3, Table 3-1 indicates that the address range DPRBASE+700 to DPRBASE+BFF can be used for User data / BDs. This is not true. The address range 700-7FFF can be used for User data / BDs but address range 800-BFFF is reserved.

2. Missing Underline in Table.

On pages 3-5 through 3-10, Tables 3-3 and 3-4, the following entries should have been underlined.

RSR, CSR1, SDSR, CSR2, CIPR, CISR, TER1, TER2, TER3, TER4, SCCE1, SCCE2, SCCE3, SCCE4, SMCE1, SMCE2, SPIE

3. Missing Bold face in Table.

On pages 3-5 through 3-10, Tables 3-3 and 3-4, the following entries should have been in bold face.

All entries in Table 3-3, ICCR, SDCR, PAPAR, PCPAR, TGCR, RCCR, PBPAR.

Section 4 – Bus Operation

1. Byte Write Enable.

On page 4-5, section 4.1.8 the following sentences:

“The equations of the byte write enables for 32-bit port (16BM = 1) are as follows”

“The equations of the byte write enables for 16-bit port (B16M = 0) are as follows:”

are not correct, the correct text is below.

“The equations of the byte write enables for 32-bit port (DPS/SPS set to 32 bit) are as follows:”

“The equations of the byte write enables for 16-bit port (DPS/SPS set to 16 bit) are as follows:”

Also in the same section the first sentence of the note:

“Note that the $\overline{WE}$ signals are not affected by dynamic bus sizing.” is not correct and should be removed.

2. Error in slave mode bus arbitration diagram.

On page 4-56, figure 4-38 an arrow head and text was missing.

The line top line between “QUICC waiting for bus, BR asserted” and “IDLE” state should have an arrow head facing the IDLE state.

Also on the same figure, the Idle state should have a test of “BG Negated” under the text of “BR Negated”.

3. Power on reset operation

On page 4-65, the note “User should make sure the ramp up time of Vcc never be faster than 4mSec to ensure proper power on reset sequence. “This restriction has been removed and the note should be deleted.

NOTE for Rev C.0

Due to a problem with Revision C.0 of the QUICC (masks 0E63C and 0F15W), a 4ms minimum Vcc ramp-up specification was added. Characterization of Revision C.1 QUICCs (masks 1E68C and 0E68C) has demonstrated that this specification is no longer necessary.

Users of Revision C.0 QUICCs should remain aware of this potential problem source. Revision C.0 QUICCs used in systems with very fast ramp-up times may experience problems at power-on reset. When the problem occurs, the QUICC never comes out of reset and no bus activity occurs (similar to latch-up, but without the high current drain). If the problem occurs, the only solution is powering the device down and reapplying power (i.e. another power-on reset).

Hardware reset (RESETH) will not solve the problem.

Section 5– CPU32+

1. Error in figure

On page 5-3, the data bus on figure 5-1 shows the data bus to be 16 bit. This is not correct, the data bus on the QUICC™ is 32 bit wide.

Section 6 – System Integration Module

1. Added Information On Crystal Operation.

On page 6-13 the following sections should be added:

6.5.1.1 Using Oscillator as Input Clock

The preferred mode of operation of the 68360 is by driving the EXTAL pin with the output of an oscillator. Oscillators are more costly than crystal circuits but are not subject to the same sensitivity as crystal circuits. You have the choice of using a full speed oscillator (i.e. 25 MHz oscillator) or using a lower speed oscillator such as 4 MHz or 32 kHz and having the system frequency generated by the on-board PLL. Use of a lower speed oscillator will allow your system to draw less power in a power-down mode.

NOTE

There are some limits to the speed of the oscillator that you can use in certain situations. Please see Additional Information: Phase Lock Loop for a description of these special situations.

6.5.1.2 Using Crystal as Input Clock

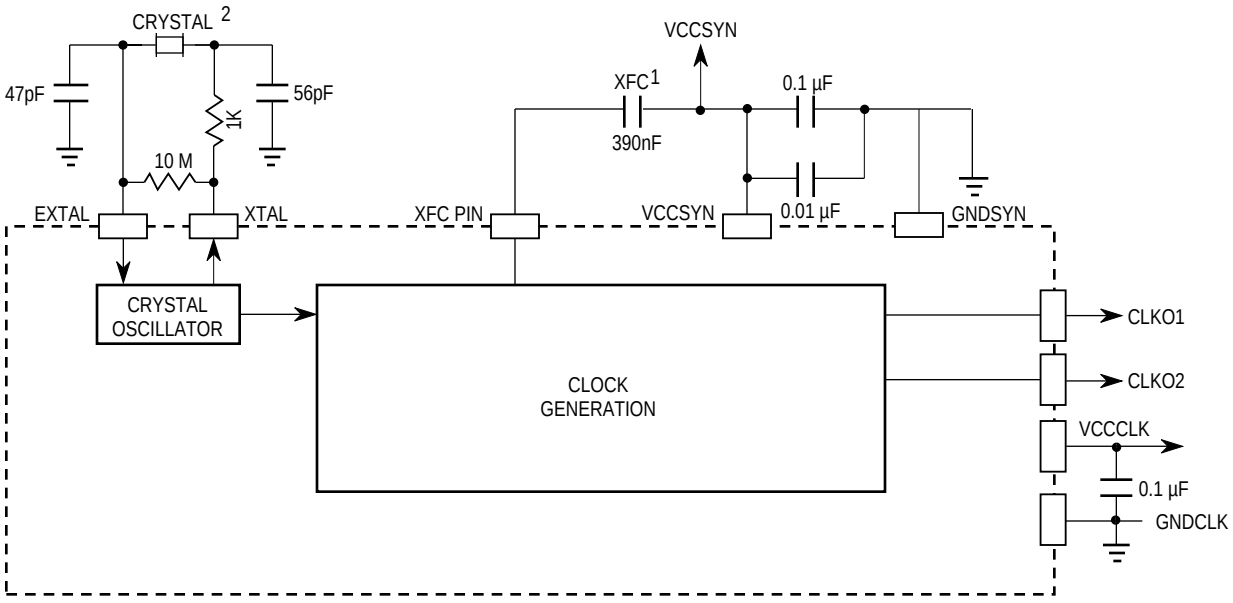
The 68360 has the ability to use a low speed crystal as its clock source. The on-chip PLL can multiply the output of the crystal circuit up to the final system frequency. A crystal circuit consists of a parallel resonant crystal, two capacitors, and two resistors. Example values for both a 32kHz crystal and a 4MHz crystal are shown in Figures 6-6 and 6-6A. Note that these are example values. Your circuit may require slightly different values to operate properly. Crystals are typically much cheaper than similar speed oscillators. However, they may not be as stable since they are affected by parameters such as: trace length, component quality, board layout, 68360 package type, 68360 shrink level, etc. While crystal circuits are typically stable, it is impossible to guarantee that they will remain stable due to 68360 process changes or external component shifts.

NOTE

The internal frequency of the 68360 and the output of the CLKO pins is dependent upon both the quality of the crystal circuit and the multiplication factor (MF) used in the PLLCR register. Please

see Additional Information: Phase Lock Loop for a description of the PLL performance.

Also on page 6-14 the following figure should be added.



NOTE:
1. Must be low-leakage capacitor. See Section 10 Electrical Characteristics for recommended values.
2. Values are for 4.194MHz crystal and may vary due to capacitance on PCB.

Figure 6-6A External Components for 4.192MHz

1. Missing Text.

On page 6-16, section 6.5.5.1, the following sentence should be added to the end of the paragraph:

In the case where MODCK0-1 is 10, then SPCLK = EXTAL/128.

2. Error on Configuration Pins.

On page 6-19, Section 6.5.8, the last sentence states that the MODCK1-0 pins have an internal pullup during reset. This is not correct and the sentence should be removed.

3. Missing Text.

On page 6-30, section 6.9.3.1, the note “SUPERVISOR ONLY” should appear below the MCR register.

4. Typo on Reset Status Register.

On page 6-34, section 6.9.3.3, the 2nd bit of the register should be a reserved bit, not LOC. Also the description of LOC in the following page should be removed.

5. Typo on SYPCR.

On page 6-35, section 6.9.3.5, the reset value for bits SWT1 and SWT0 were wrong. The correct value for both bits is MODCK1.

6. Typo on PITR.

On page 6-36, section 6.9.3.7. The reset value for bits SWP and PTP were wrong. The correct value for both bits is $\overline{\text{MODCK1}}$.

7. Error in Text.

On page 6-36, section 6.9.3.5, the word EXTALDIV should be replaced with SPCLK.

8. Typo on Register Default.

On page 6-37, section 6.9.3.5, the description for DBFE and BME was not correct. The correct descriptions are as follows:

DBFE—Double Bus Fault Monitor Enable

0 = Disable the double bus fault monitor function. (Default)
1 = Enable the double bus fault monitor function.
For more information, see 6.3.1.2.3 Double Bus Fault Monitor and Section 5 CPU32+.

BME—Bus Monitor External Enable

0 = Disable bus monitor function for the external bus cycles. (Default)
1 = Enable bus monitor function for the external bus cycles.
For more information see 6.3.1.2.1 Bus Monitor.

9. Typo on BKCR.

On page 6-47, section 6.9.3.13, the following statement, “NEG is ignored if the MA bits are 00" where NEG bit is described is not correct and should be removed.

10. Addition of note on External master support.

On page 6-57, section 6.11.7, the following note should be added after the first paragraph.

NOTE

The MC68EC040 and MC68040 type master is not supported when the QUICC is configured to a master mode.

11. Corrections for RCNT—Refresh Counter Period Description.

On page 6-64, section 6.13.1, make the following corrections:

a) ‘RFCNT’ in the equation should be ‘RCNT’.
b) ‘24 (decimal)’ in the example should be ‘23 (decimal)’.
c) ‘24 / (25 MHz / 16)’ in the example should be ‘(23 + 1) / (25 MHz / 16)’.

12. Typo on Global Memory Register.

On page 6-65, section 6.13.1, the following should replace the definition of PGS2-PGS0:

PGS2–PGS0—Page Size

This attribute determines the page size and AMUX for the DRAM controller (see Table 6-9). For multiplexing information see Table 6-8 on page 6-59. The page size is the smallest DRAM size the user needs to support page mode capability.

Table 6-9. DRAM Page Size

DRAM Size	PGS2-PGS0	Address Lines Compared for Page Hit or Miss	# Address/Page in Page Compare
128k	000	A10-25(32), A9-25(16)	256 Addresses
256k	001	A11-25(32), A10-25(16)	512 Addresses
512k	010	A11-25(32), A10-25(16)	512 Addresses
1M	011	A12-25(32), A11-25(16)	1024 Addresses
2M	100	A12-25(32), A11-25(16)	1024 Addresses
4M	101	A13-25(32), A12-25(16)	2048 Addresses
8M	110	A13-25(32), A12-25(16)	2048 Addresses
16M	111	A14-25(32), A13-25(16)	4096 Addresses

Delay Write QUICC Bit Definition.

On page 6-66, section 6.13.1, the description of the DWQ bit was not clear. The bit definition should be replaced as follows:

DWQ—Delay Write for QUICC (DRAM Bank Only)

This attribute is used to add a clock to the assertion and negation of the $\overline{\text{CAS}}$ signal on DRAM page hit write cycles. The write cycle lasts one additional clock in this case. This attribute is applicable to an internal QUICC master and to an external MC68030/QUICC.

0 = Reads and writes are the same length.
1 = Add one clock to write cycles for DRAM banks.

NOTE

This bit must be set by the user if page mode is enabled for this DRAM bank (PGME = 1), and when a zero wait state DRAM is implemented by setting TCYC to be zero. If this is not done the DRAM may latch invalid data during writes.

13. External MC040 type cycle (SRAM)

The following table should be placed after the table 6-11 on page 6-67.

TCYC =	External MC68040 Type bus cycle Length	
	TSS40=0	TSS40=1
0	2	3
1	3	4
2	4	5
3	5	6
4	6	7
5	7	8
6	8	9
…		
15	17	18

14. Missing Note on Parity.

On page 6-71, section 6.13.3, the note below should be added after the note under the definition of parity checking enable:

Parity is not supported with external assertion of $\overline{\text{DSACK}}$ or $\overline{\text{TA}}$.

15. Error in note on CSNT40.

On page 6-72, the note on the top of the page states that SYNC bit must be set for CSNT40 function to take effect. This is not true. Regardless of the setting of SYNC bit CSNT40 will take an effect.

16. Missing Statement on BACK40.

On page 6-72, the description of the BACK40, for the zero case, the following statement should be added:

“The QUICC will assert TBI on an access to this memory area”.

17. Error in Note at TRLXQ.

On page 6-72, the 3rd note under TRLXQ-Timing Relax:

“User should avoid setting both TRLXQ and CSNTQ = 1, when TCYC = 0. This combination will result in a bus cycle without $\overline{\text{CS}}$ assertion.” is not correct and should be removed.

18. Missing NOTE.

On page 6-74, bits 3 and 2 of the option register should have an asterisks. Also on the bottom of the page the following note should be added.

NOTE

The default setting of bits 3 and 2 for option register 1 is determined by the settings of configuration pin.

19. Error in Table 6-14.

On page 6-77, The last column heading on Table 6-14 has an error. The heading should be:

“Number of clocks (DRAM)” not “Number of Wait States (DRAM)”

Section 7 – Communication Processor Module

1. Global advisory concerning Buffer Descriptor status bits.

The user is responsible for clearing (writing a zero) any buffer descriptor (RxBD or TxBD) status bits set by the communication processor.

2. Deletion of STP bit.

On page 7-26, section 7.6.2.1. The STP bit in the ICCR was designed to conserve power when IDMA was not in use. This function has been removed due to erratic behavior. The user must keep this bit clear. Bit 15 of ICCR is now reserved.

3. Error in note.

On page 7-33, the note under section 7.6.3 Interface Signals should be as follows.

NOTE

DREQ must be level sensitive if IDMA uses buffer chaining or auto buffer mode.

4. Wrong section number.

On page 7-34, the last sentence on the page "7.5.2.5 Timer Capture Register..." The section was not correct. The correct section number is 7.6.2.5.

5. Wrong table reference.

On page 7-35, first sentence in section 7.6.4.2.1 reference, table 7-2. This should be table 7-3.

6. Error in sentence.

On page 7-40, Section 7.6.4.4.3 The last sentence in the first paragraph. " If $\overline{\text{DREQX}}$ is negated long enough for the IDMA to win the bus, cycles will continue as long as $\overline{\text{DREQx}}$ is asserted and no higher priority bus master or interrupt occurs." This sentence should be replaced with. " If $\overline{\text{DREQX}}$ is asserted long enough for the IDMA to win the bus, cycles will continue as long as $\overline{\text{DREQx}}$ is asserted and no higher priority bus master requests the bus or interrupt occurs."

7. Missing paragraph in IDMA.

On page 7-41, section 7.6.4.4.3. The following paragraph should be added after point 6.

7. If the IDMA is being used in auto-buffer or buffer-chaining mode, the $\overline{\text{DREQ}}$ signal will not be sampled at the S3 sampling time. It will be sampled after the RISC CP has reconfigured the IDMA with the information contained in the next buffer descriptor. Thus, you should continually assert $\overline{\text{DREQ}}$ until you receive a $\overline{\text{DACK}}$ when using buffer chaining mode or auto-buffer mode.

Also on page 7-43 the following paragraph should be added after point 3.

4. You may not use cycle steal mode if you are using buffer-chaining or auto-buffer mode.

8. Error in example

On page 7-55, the third step in the buffer chaining example was printed incorrectly. The correct step is as follows.

3. FCR1 = $89. Destination function code is 1000; Source function code is 1001.

9. Error in SDMA Bus Arbitration and Bus Transfers

On page 7-57, the first sentence of the last paragraph should read '…but the SDMA always reads words (16 bits).'

10. Error in Programming the SI RAM Entries.

On page 7-72, section 7.8.4.5, the bit order of SSEL1-SSEL4 is not represented correctly. The correct representation is as follows:

Bit 13 -> SSEL4
Bit 12 -> SSEL3
Bit 11 -> SSEL2
Bit 10 -> SSEL1

11. Error in Signal Name.

On Page 7-73, section 7.8.4.5, the four strobe signal names L1STA1, L1STA2, L2STB1, and L1STB2 in the SSEL1-SSEL4 should be replaced with L1ST1, L1ST2, L1ST3, and L1ST4.

12. Typo in SI Mode Register.

On page 7-81, section7.8.5.2, the bit definition of Grant Mode for TDM A or B has a typo and should be replaced with the following text:

> "1 = IDL mode. A GRANT mechanism is supported if the corresponding GR1-GR4 bits in the SICR register are set. The grant is a sample of the L1GRx pin while L1TSYNCx is asserted. This GRANT mechanism implies the IDL access controls for transmission on the D channel. Refer to 7.8.6.2 IDL Interface Programming."

13. Typo on Time Slot Assigner Examples.

On pages 7-83 to 7-85, the acronym for frame sync delay was printed incorrectly. The correct acronym is FSD, not SFD.

14. Typo in SI Status Register.

On page 7-87, section 7.8.5.5, first paragraph, second sentence, "The value of this register is valid only when the corresponding bit in the SIGMR is clear." The acronym SIGMR should have been SICMR.

15. Errata and missing note in GSMR

On page 7-113, the note under the description of CDP was not clear and should be replaced with the following.

NOTE

This bit must be set if this SCC is used in transparent mode and must be cleared when used and non-transparent mode.

The same note should be added below the description of CTSP.

16. Clarification of TDCR—Transmit Divide Clock Rate Description.

One page 7-117, section 7.10.2, replace the second sentence of the TDCR description beginning "If the DPLL is not used …" with the following:

"To bypass the DPLL, choose the 1x value, except in asynchronous UART mode where 8x,16x, or 32x still must be used."

17. Missing Note on Transmission on Demand.

One page 7-121, section 7.10.5, the following note should be added at the bottom of the page:

The first bit of the frame will typically be clocked out 5-6 bit times after TOD has been set to one.

18. Missing Last Step for SCC Initialization.

One page 7-129, section 7.10.9, add the following last step when initializing an SCC:

15. Setup buffer descriptors including control bits as required by the respective protocol ; clear status bits by writing with zero.

19. Missing Note on Disable Receiver while Transmitting.

On page 7-158, the following note should be added after the description of DRT bit:

User should set the preamble bit in the transmit buffer descriptor if the QUICC™ is being used in multi-drop UART mode.

Also on page 7-158, the following note should be added after the description of SYN (Synchronous Mode) bit.

NOTE.

RINV bit in the GSMR must be cleared if synchronous UART mode is selected.

20. Missing bits in HDLC mode register.

On page 7-178, the following bit definition was missing from the manual.

Bit 2 – BPM (HDLC BUS Priority Mode)

This bit determines the number of idle bits needed to be counted prior to a frame transmission after a successful transmission.

0 = 10 bits
1 = 9 bits

Bit 1 – BCM (HDLC BUS Collision Sense Mode)

This bit determines the sample point of collision detection.

0 = collision is sensed after 1/2 bit delay
(or at 3/4 bit delay if the clock duty cycle is 25%).
1 = collision is sensed after one bit delay

21. Corrections for HDLC Mode Register PSMR[DRT] Bit Description.

On page 7-179, replace the DRT—Disable Receiver While Transmitting description with the following:

DRT—Disable Receiver While Transmitting
0 = Normal operation
1 = Reserved—not allowed in HDLC bus mode. Use address filtering to implement the same functionality.

22. Missing boldface for HDLC RxBD control bits.

On the top of page 7-181, the **E**, **W**, **I**, and **CM** control bits of the HDLC RxBD should be boldfaced to denote user-initialized.

23. Corrections for Transparent Event Register (SCCE).

On page 7-232, section 7.10.21.11, make the following corrections:

a) 'RCH' in the table should be '—'.
b) Reserved bits (indicated below table) should include bit 3.
c) RCH—Receive Character text description should be removed.

24. Missing Note on Ethernet Collision.

On Page 7-241, section 7.10.23.5, the following note should be added at the end of the third paragraph:

NOTE

If an Ethernet frame is made up of multiple buffers, the user should not reuse the first buffer descriptor until the last buffer descriptor of the frame has had its ready bit cleared by the CPM.

25. Typo on MAXD1 and MAXD2 Value.

On pages 7-247 and 7-249, the manual states that the user should set this parameter to 1518 decimal. The user should instead set the parameter to 1520 decimal.

26. Wrong font on DMA_cnt.

On page 7-247, Table 7-11. The parameter DMA_cnt was printed with a bold face indicating that the parameter should be initialized by user. This is not correct DMA_cnt does not need to be initialized by the user and should have been in plain font.

27. Typo on Table 7-11.

On page 7-248, the last three entries of Table 7-11 were mistyped.The correct entries are:

SCC Base + 9E	TADDR_H	Word	Temp Address (LSB)
SCC Base + A0	TADDR_M	Word	Temp Address
SCC Base + A2	TADDR_L	Word	Temp Address (MSB)[2]

28. Missing Bit in Ethernet Receive Buffer Descriptor.

On page 7-260, the figure of the receive buffer descriptor is not correct. The correct figure is:

OFFSET + 0	**E**	—	**W**	**I**	L	F	—	M	—	—	LG	NO	SH	CR	OV	CL
OFFSET + 2	DATA LENGTH															
OFFSET + 4	**RX DATA BUFFER POINTER**															
OFFSET + 6																

29. Replace the DEF Explanation.

On Page 7-263, section 7.10.23.19, the DEF—Defer Indication explanation should be replaced with the following paragraph:

This frame was deferred before being successfully sent. Deferral means that the the transmitter had to wait for carrier sense before sending because the line was busy. This is not an indication of a collision; collisions are indicated in the Retry Count (RC).

30. Additional Information on Using TSA for Synchronization.

On Page 7-296, section 7.11.10.7, the second paragraph from the bottom is not sufficient and should be replaced with the following paragraph:

Once the TEN bit is set in SMCMR, the SMC waits for the transmit FIFO to be loaded before attempting to achieve synchronization. Once the transmit FIFO is loaded, synchronization and transmission begin according to the following conditions.

If a buffer is made ready when the SMC is enabled, then the first byte will be placed in time slot 1 if CLSN is set to 8 and slot 2 if CLSN is set to 16.

If a buffer has its SMC is enabled, then the first byte in the next buffer can appear in any time slot associated with this channel.

If a buffer is ended with the L-bit set, then the next buffer can appear in any time slot associated with this channel.

31. Over bar missing in table.

On page 7-363, table 20. RTS1-2 should have an over bar but was omitted in the table. On page 7-365, table 7-21. The following signal should have an over bar but was omitted in the table. RTS1-2, CST1-4 and CD1-4 should all have over bar.

32. Typo on Port C Special Options.

On page 7-369, the bit definition for external request to the RISC is not supported and should be removed from the users manual.

Section 8 – Scan Chain Test Access Port

1. Error on TRIS.

On page 8-1 the paragraph in the middle of the page below NOTE states that the TRIS pin is sampled during system reset. This is not true and should be change to TRIS pin is always sampled with exception to system reset.

The same errata is duplicated on page 8-11 section 8.4.5.

2. Missing Word.

On Page 8-3, section 8.3, first paragraph, third sentence:

“The XTAL and XFC pins are associated with analog signals and are not included in the boundary scan register.” was missing the word EXTAL. The sentence should be, “The EXTAL, XTAL, and XFC pins are associated with analog signals and are not included in the boundary scan register.”

3. Error in Pin Name.

On Page 8-6, Table 8-2, the pin name for pins 105 and 106 was mislabeled. The pin name CLKO0 for pin 105 should have been CLKO1 and the pin name CLKO1 for pin 106 should have been CLKO2.

4. Error in Boundary Scan Chain in Bit Definition Table.

The scan chain is reversed in Table 8-2. PERR is cell 0 and RESETH is cell 195.

Section 9 – Applications

1. Typo in Figure 9-1.

On page 9-2, Figure 9-1, the MODCK0-1 pins are shown to be connected to Vcc. The correct figure has MODCK0 connected to ground and MODCK1 connected to Vcc.

2. Inconsistent text in Clocking strategy.

On page 9-3, section 9.1.1.2. The paragraph describes the clocking strategy using a 32.768KHz crystal where the Figure 9-1 shows a 25MHz crystal oscillator set up. To be consistent the following text should replace the text of section 9.1.1.2.

9.1.1.2 Clocking Strategy.

In this application, the system clock is generated from a 25MHz crystal oscillator output into the QUICC. The QUICC's internal phase-locked loop (PLL) locks to the input, multiplies the frequency by one, and uses the 25 MHz as the result system frequency. The PLL also multiply the clock by two and outputs a 50 MHz signal on CLKO2. Neither CLKO pin is required for the application. It is recommended that the CLKO outputs be disabled in software to save power.

The use of a 25MHz crystal oscillator is not a requirement in the application. A 4-MHz crystal or a 32.768-kHz crystal could have been used, if desired. (See section 6.5 for notes on crystal use.)

The QUICC clocking section allows for the clock oscillator to be kept running through the VDDSYN pin in a power-down situation. This section does not address low-power issues, however.

3. Typo on Configuring the Memory Controller.

On page 9-11, section 9.1.3.2, the first statement on page 9-12:

“NCS should normally be cleared”

This should be:

“NCS should normally be set”

4. Error in text.

On page 9-13, the first sentence “To configure the QUICC for 16 bit data bus...” Should be replaced with “User should drive the 16BM pin when the QUICC™ is in reset. User should NOT simply tie 16BM to RESETH/RESETS since PRTY3 and PRTY2 pins will be driven the QUICC even though there are not applicable to the current bus size.

5. MC68040 Companion Mode Bus Cycle Note.

On page 9-31, section 9.4, add the following note:

NOTE

In MC68040 companion mode, the QUICC understands MC68040-type bus cycles but cannot generate them. If the QUICC becomes busmaster, e. g. for SDMA transfers, it will drive normal MC68030-type bus cycles with TT1 becoming $\overline{DS}$ again. This should normally be no problem since the MC68040 does not interpret these input signals, but external circuitry handling these signals must be aware of this fact.

6. Error in Figure 9-8.

On page 9-33, Figure 9-8, the buffer between RESETH, RSTI, the pushbutton and CONFIG2 should not have an inverting output; it should be a non-inverting buffer.

7. Error in Reset Strategy.

On Page 9-34, section 9.4.1.3, the first sentence “If a QUICC is configured to provide the global chip select, it will also provide an internal power-on reset generation.” is not correct. QUICC will provide internal power-on reset generation regardless of chip select configuration.

8. Error in Caching Sample Code.

On Page 9-53, section 9.5.4, correct the following in the code sample:

a) ‘MOVE.L #$003FC020,D0’ should be changed to ‘MOVE.L #$003FC040,D0’.
b) ‘MOVE.L #$403FC010,D0’ should be changed to ‘MOVE.L #$403FC020,D0’.

9. Error in Figure 9-33. 1-Mbyte DRAM Bank—32 Bits Wide.

On Page 9-87, Figure 9-33, correct the following:

a) On the first MC74F157, B0-B3 should be connected to A11-A14, not A12-A15.
b) On the second MC74F157, B0-B3 should be connected to A15-A18, not A16-A19.
c) On the third MC74F157, A1 and B1 should be unused (unconnected).
d) On the third MC74F157, B0 should be connected to A19, not A20.
e) On the third MC74F157, Y1-Y3 should be unused (unconnected).

Section 10 – Electrical Characteristics

1. Missing Note on Maximum Ratings

On Page 10-1, the following note should be added to the maximum ratings figure:

3. The supply voltage V_{CC} must start and restart from 0.0 V; otherwise, the 360 will not come out of reset properly.

2. DC ELECTRICAL SPECIFICATIONS

On Page 10-5, Figure 10-5, some specifications were incorrectly printed. The correct specifications are as follows:

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Input Only Pins except TMS, TDI, and TRST) Vin = 0/5 V	Iin	-2.5	2.5	µA
Input Leakage Current (All Input Only Pins except TMS, TDI, and TRST) Vin = 0.5/2.4 V	Iin	-2.5	2.5	µA
Hi-Z (Off-state) Leakage Current (All Non-crystal Outputs and I/O Pins except TMS, TDI, and TRST). Vin = 0/5 V	IOZ	-2.5	2.5	µA
Hi-Z (Off-state) Leakage Current (All Non-crystal Outputs and I/O Pins) except TMS, TDI, and TRST. Vin = 0.5/2.4 V	IOZ	-2.5	2.5	µA
Output Low Voltage (For 3.3 volt part) I_{OL} = 2.0 mA A31–A0, FC3–0, SIZ0–1, D31–D0, CLKO1–2,FREEZE, IPIPE0–1, IFETCH, BKPTO I_{OL} = 3.2 mA PA0, 2, 4, 6, 8–15, PB0–5, PB8–17, PC0–11, TDO, PERR, PRTY0–3, IOUT0–2, AVECO, AS, CAS3–0, BLCRO, RAS0–7 I_{OL} = 5.3 mA, DSACK0–1, R/W, DS, OE, RMC, BG, BGACK, BERR I_{OL} = 7 mA TXD1–4 I_{OL} =8.9 mA PB6, PB7, HALT, RESET, BR (Output)	V_{OL}	—	 0.5 0.5 0.5 0.5 0.5	V

3. Removal of specification on Vcc ramp.

On page 10-5,the specification tRamp has been removed. For more information see Error in slave mode bus arbitration diagram. on page 3 of this document.

4. Typo on CLKO2 Rise and Fall Time.

On page 10-7, the specification 4A, 5A for 33MHz was printed incorrectly. The correct specification is 1.6ns max, not 2ns.

5. Error and Missing Specification.

The following table corrects errors in Table 10.9 on page 10-9.

Num.	Characteristic	Symbol	3.3 V/5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
			Min	Max	Min	Max	
8	CLKO1 High to Address, FC, SIZ, RMC invalid	t_{CHAZn}	-2	—	-2	—	ns
11A[11]	Address, FC, SIZ, RMC Valid to CSx/RASx Asserted	t_{AVCA}	30	—	22.5	—	ns
13A[13]	CSx Negated to Address, FC, SIZ Invalid (Address Hold)	t_{CNAI}	30	—	22.5	—	ns
14[10,12]	AS, CSx, OE, WE (and DS Read) Width Asserted	t_{SWA}	75	—	56.25	—	ns
14C[11,13]	CSx Width Asserted	t_{CWA}	35	—	26.25	—	ns
14A	DS Width Asserted (Write)	t_{SWAW}	35	—	26.25	—	ns
14B	AS, CSx, OE, WE, IACKx (and DS Read) Width Asserted (Fast Termination Cycle)	t_{SWDW}	35	—	26.25	—	ns
15[3,10,12]	AS, DS, CSx, OE, WE Width Negated	t_{SN}	35	—	26.25	—	ns
17A[13]	CSx Negated to R/W High	t_{CNRN}	30	—	22.5	—	ns
18	CLKO1 High to R/W High	t_{CHRH}	3	20	3	15	ns

20	CLKO1 High to R/$\overline{W}$ Low	t_{CHRL}	3	20	3	15	ns
20A	$\overline{CASx}$ Low to R/$\overline{W}$ Low (Only in page mode and when the load capacitance is the same on $\overline{CAS}$ and R/$\overline{W}$ Pin)	t_{CARL}	0	—	0	—	ns
23	CLKO1 High to Data-Out Valid	t_{CHDO}	—	23	—	18	ns
23A	CLKO1 High to parity Valid	t_{CHPV}	—	25	—	20	ns

Also in the same table on page 10-11, specification 49 duplicates specification 58 and should be removed.
Also on the same table spec 12 should not have a superscript of 12.

6. Missing Specification.

On page 10-11, Table 10.9, the following specification should be added:

Num.	Characteristic	Symbol	3.3 V/5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
			Min	Max	Min	Max	
58B	CLKO1 high to $\overline{BERR}$, $\overline{RESETS}$, $\overline{RESETH}$ tri-stated		—	20	—	15	ns

7. Error on note.

On page 10-12, Note 10 and 11 indicated that $\overline{RASx}$ and $\overline{RASxDD}$ may be tied together. This is not true. Signals $\overline{RASx}$ and $\overline{RASxDD}$ should not be tied together since it will cause contention on the signal pins upon boot.

10. These $\overline{CSx}$ specs are for TRLX=0.

11. These $\overline{CSx}$ specs are for TRLX=1.

8. Clarification on specification.

On page 10-28, Table 10-10 specification 103 was not clear. The following clarification takes into account page and no-page mode as well as WBTQ modes.

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
		Min	Max	Min	Max	
103A	$\overline{RASx}$ Width Negated (Back to Back Cycles) Non page mode @WBTQ=0	75		56.25		ns
103B	$\overline{RASx}$ Width Negated (Back to Back Cycles) Page mode @WBTQ=0	55		41.25		ns
103C	$\overline{RASx}$ Width Negated (Back to Back Cycles) Non page mode @WBTQ=1	115		86.25		ns
103D	$\overline{RASx}$ Width Negated (Back to Back Cycles) Non page mode @WBTQ=1	95		69.23		ns

9. Typo on R/$\overline{W}$ Low to $\overline{CASx}$ Asserted.

On page 10-28, Table 10.10 specification 115 was printed incorrectly. The correct spec is as follows:

Num.	Characteristic	3.3 V or 5.0 V		5.0V		Unit
		25.0 MHz		33.34MHz		
		Min	Max	Min	Max	
115	R/$\overline{W}$ Low to $\overline{CASx}$ Asserted (Write)	52.5		40		ns

10. Typo on DRAM Page-Mode Page-Hit.

On page 10-31, Figure 10-23, address valid timing for the initial access is specification 6 not 6A.

Also on same figure the Specification 8 should be removed.

Also on the same figure Specification 106 was drawn to be referenced off of the rising edge between S0 and S1. This is not correct. The correct reference clock edge is a rising edge between S5 and S0.

11. Error in superscript.

On page 10-33, table 10-11, The superscript on specs 130, 132, 134, 135, 142 and 144 were not correct. Specs. 130 and 132 should have no superscripts at all. Specs 134 and 135 should have a superscript of 2 only. Specs 142, 143 and 144 should have a superscript of' 2' instead of '3'.

12. Typo on $\overline{BGACK}$/$\overline{BB}$ Negation Specification.

On page 10-33 and 10-49 there are two specifications for the negation of $\overline{BGACK}$/$\overline{BB}$. Specification 139 and specification 238 are not ~~correct~~ *needed* and should be deleted. The Figures affected are 10-25, 10-26 for 030/360 external masters and Figure *10-39 on page* 10-50 for 040 external masters.

13. Error in Figure.

On pages 10-34, and 10-35, the negation timing for $\overline{BCLRO}$ is not correct. In both figures the negation of the signal $\overline{BCLRO}$ is shown to be at the rising edge of CLKO1 where $\overline{BGACK}$ is asserted. The signal is instead negated at the rising edge of CLKO1 where $\overline{BGACK}$ is negated.

Also on same figures the negation delay between $\overline{BR}$ and $\overline{BG}$, specification 136, should be removed from the figures.

14. Missing Note on Bus Request Negation.

On pages 10-34 and 10-35, the following note should be added:

User should note that the negation timing of bus request from a slave QUICC pin may not meet the required input specification for the QUICC in master mode. Because of this the

master QUICC may assert a spurious bus grant. If more than one QUICC slave is used with a QUICC in master mode the user should not wire-or the bus grant signal to avoid bus contention due to this spurious bus grant assertion.

15. Missing Minimum Specification.

On page 10-36, Table 10.12, the minimum specification for specification 152 was not correct. The correct specifications are 20ns for 25MHz and 15ns for 33MHz. On the same page the maximum specification for specification 161A was missing. The max spec is 23ns for 33MHz. On the same page the minimum specification for 166 was missing. The minimum specification should have been 3ns for both 25MHz and 33MHz.

Also on page10-36, at the bottom of the table, note 2 should state:

"2. For internal/external bus master to external memory or peripheral. The max for J17A and newer masks is 12ns; J17A was released 2Q97."

16. Typo on Figure 10-31.

On page 10-42, Figure 10-31, specification 187 was referenced to the wrong place. The correct reference should be from assertion of $\overline{\text{MBARE}}$ to assertion of $\overline{\text{DS}}$.

17. Typo on specification number.

On page 10-45 and page 10-47 the specification number for R/$\overline{\text{W}}$ to $\overline{\text{AS}}$ assertion should be 214 not 164

18. Typo on External MC68030/MC68360 DRAM Asynchronous Cycle Timing Diagram.

On page 10-47, Figure 10-35, the specification for AMUX signal negation should be 119. Specification 209 should be replaced with specification 119.

19. The clock reference is EXTAL, not CLKO1.

On pages 10-51 and 10-56, the following note should be added:

3. The clock reference is EXTAL, not CLKO1.

On the same pages, superscript of 3 should be added for specifications 252, 258 and 296. Also on the same page spec 252 the max value for 33MHz should be 5nSec not 6nSec.

20. Correction on Figure 10-40.

On page 10-52, Figure 10-40, the note under D31–D0 should be "(040 READ)" and "(OUTPUT)".

21. Typo and Missing Note on Table 10.17.

On page 10-56, Table 10.17, the specification 295 characteristic should be “Clock low to $\overline{\text{CASx}}$ low (040 Burst Read only)” not “Clock high to $\overline{\text{CASx}}$ high (040 Burst Read only)”.

Also on the same table the specification 288 was improved. The following is the new specification.

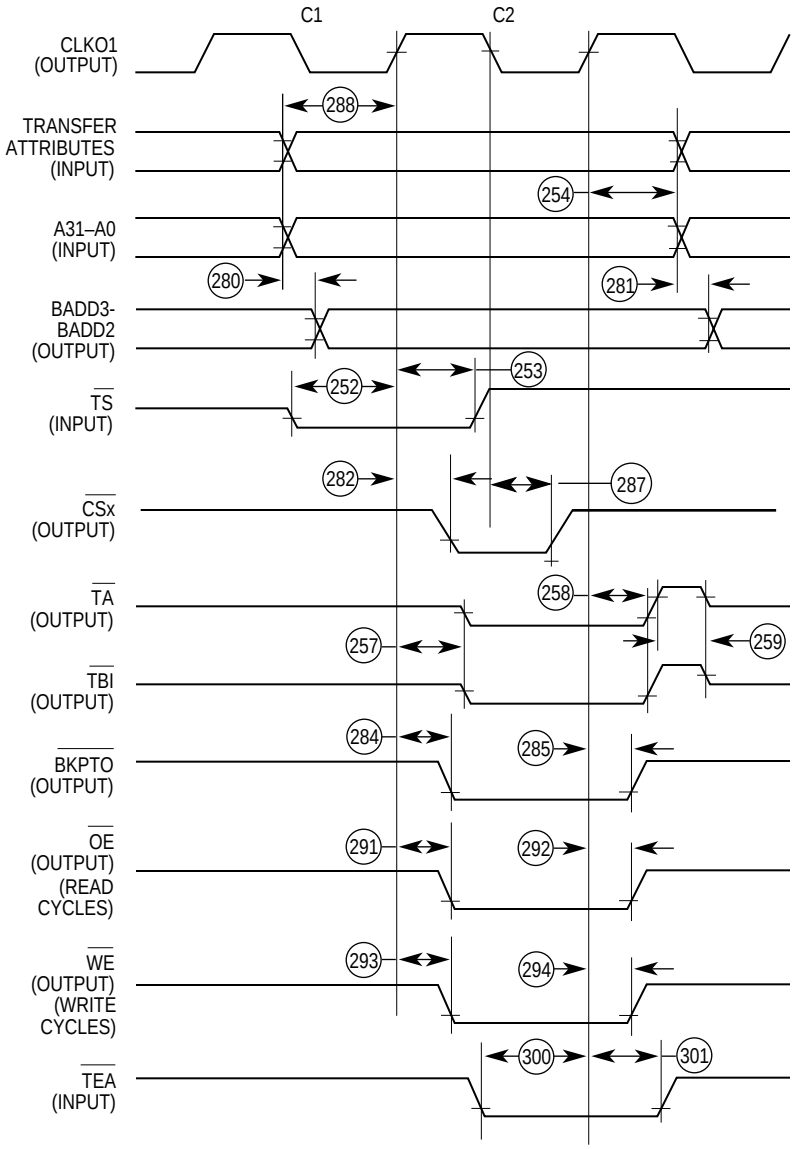
Num.	Characteristic	3.3 V or 5.0 V		5.0V		Unit
		25.0 MHz		33.34MHz		
		Min	Max	Min	Max	
288[1]	Address Transfer Attributes Valid to EXTAL High (TSS40=0)	10	—	10	—	ns

22. Missing information and figures on MC68040 SRAM R/W.

On page 10-57 the figure title should be replaced with the following

Figure 10-44(a). MC68040/EC040 SRAM Read Cycles (TSS40=0, CSNT40=1)

The following figure should be added after figure 10-44(a)



NOTE: MC68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK

Figure 10-44(b) MC68040/EC040 SRAM Write cycle (TSS40=0, CSNT40=1)

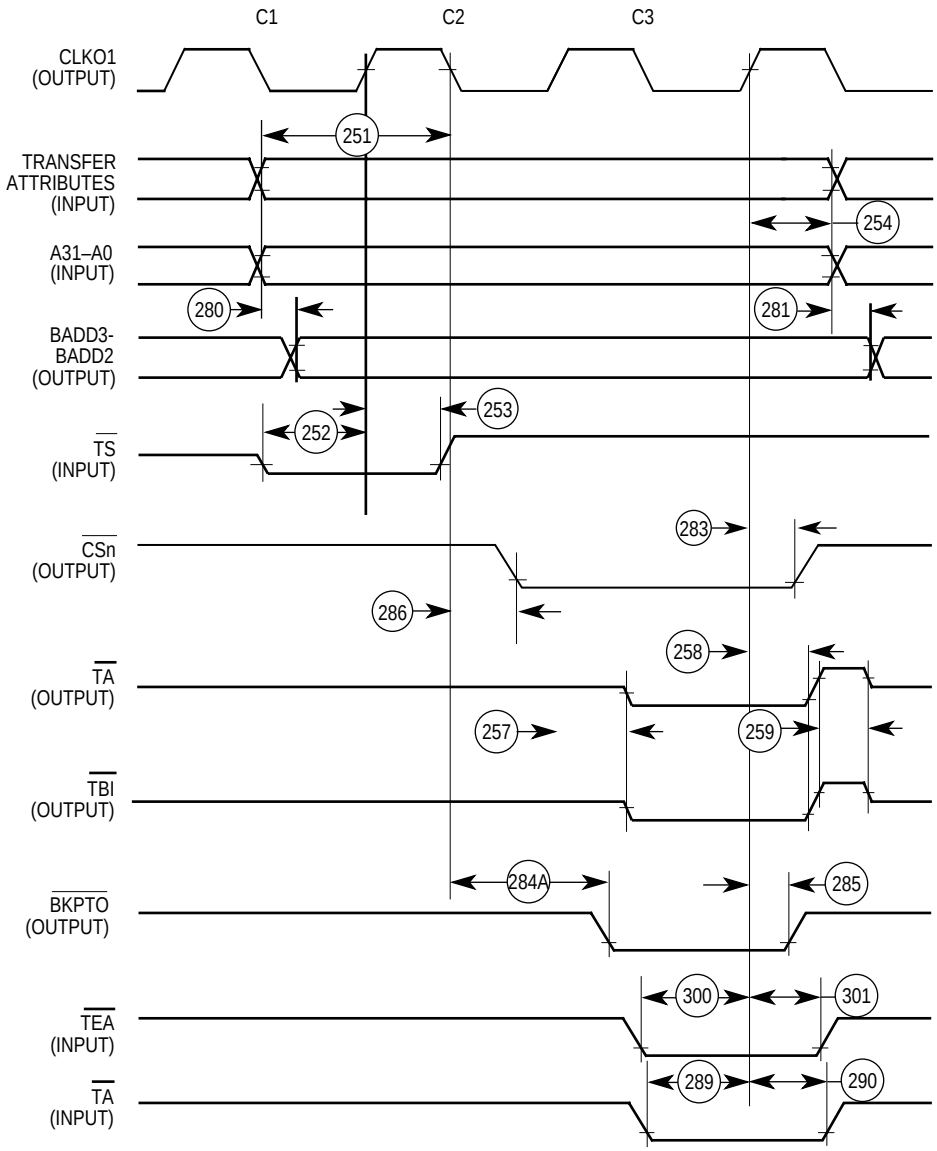
On page 10-58 the figure title for FIGURE 10-45 should be replaced with the following.

Figure 10-45(a) MC68040/MC68EC040 SRAM Write cycle (TSS40=1, CSNT40=1)

NOTE

OE and WE signals are not supported when TSS40 is set to 1.

The following figure should be added below figure 10-45(a)



NOTE: MC68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/W, LOCK
OE and WE are not supporrted when TSS40 is set to 1

Figure 10-45(b) MC68040/EC040 SRAM Read Cycle (TSS40=1, CSNT40=1)

23. New IDMA AC Electrical Specifications.

On page 10-62, replace the entries for specification numbers 1 and 2 with the following:

Num.	Characteristic	3.3 V or 5.0 V 25.0 MHz		5.0V 33.34MHz		Unit
		Min	Max	Min	Max	
1	CLKO1 Low to DACK, DONE Asserted	3	24	3	18	ns
2	CLKO1 Low to DACK, DONE Negated	3	24	3	18	ns

24. Typo on Figures 10-60 and 10-61.

On pages 10-70 and 10-71, in the middle of both Figures a reference bubble states RFCD = 1. This should have been RFSD = 1.

Also on Figure 10-61, the heading for the top clock should be L1RCLK (FE=0, CE=1) and the second clock should be L1RCLK (FE = 1, CE = 0).

Also on figures 10-60 and 10-62 had a spec. missing. Specification 88 should be shown between the first rising edge of L1RCLK (FE=0, CE=0) and the rising edge of the L1RSYNC pulse.

25. Typo on Figure 10-63.

On page 10-73, Figure 10-63, the first two headings for the clocks should have been L1TCLK and not L1RCLK.

26. Typo on SCC in NMSI Mode Specification for 33MHz.

On page 10-75, Table 10.25, the specification for 33MHz was printed incorrectly. The following is the correct specification:

Num.	Characteristic	3.3 V or 5.0 V		5.0 V		Unit
		25.0 MHz		33.34 MHz		
		Min	Max	Min	Max	
105	$\overline{\text{CTS1}}$ Setup Time to TCLK1 Rising Edge	40	—	40	—	ns
106	RXD1 Setup Time to RCLK1 Rising Edge	40	—	40	—	ns
107[2]	RXD1 Hold Time from RCLK1 Rising Edge	0	—	0	—	ns
108	$\overline{\text{CD1}}$ Setup Time to RCLK1 Rising Edge	40	—	40	—	ns

Section 11 – ORDERING INFORMATION AND MECHANICAL DATA

1. Missing pin name for BGA.

On page 11-5, the pin name for pin R16 is missing. This pin should be labeled NC

2. Typo on CQFP dimension.

On page 11-6, The specification for G should have been 0.197 BSC not 0.019 BSC

Additional Information

1. Initialize the Dual port ram.

After Reset the dual port ram of the QUICC™ will come up at random setting. User should always initialize the Dual port ram to ZERO after reset. This will prevent any unwanted bit to be set in the dual port ram that may cause undesired result.

2. IMPORTANT DEBUGGING TIP

PLL loss-of-lock resets are no longer supported, and MUST be disabled.

Background:

The original release of the 68360 supported a feature whereby if loss of PLL lock was detected, a hardware reset could be generated. This feature was enabled by setting a bit in the CLKOCR (bit5; RSTEN). However, the circuits which detect loss-of-lock are hyper sensitive, and sometimes cause hardware resets when PLL lock is not lost. As this feature was problematic and provided little extra functionality, it was decided to no longer support this feature. This change is included in Revision 1 of the 68360 User's Manual.

Problem symptoms:

Sporadic resets. After reset, bit 2 will be set in the RSR.

Recommended action:

For the purpose of robustness, we request that bit 5 in the CLKOCR (formerly known as RSTEN) be set to zero, regardless of whether a problem is currently exhibited. This will help safeguard against problems in the future. Clearing bit 5 in the CLKOCR will disable loss-of-lock resets.

3. Phase Lock Loop.

The following section describes the performance guidelines for the on-chip phase locked loop on the QUICC. The following explanations should be considered as general observations on expected PLL behavior and should not be considered as specifications. The parts are not tested to verify these exact numbers. These observations were measured on a LIMITED number of parts and were not verified over the entire temperature and voltage ranges.

4. Phase Skew Performance.

The phase skew of the PLL is defined as the time difference between the rising edges of EXTAL and CLKO1/2 for a given capacitive load on CLKO1/2, over the entire process, temperature and voltage ranges. This is defined in specifications 5B, 5C, and 5D (on page 10-7, Table 10.7). For input frequencies greater than 10MHZ and MF<=4, the skew is between 0.0ns and less than 2.0ns (for rise time of 4ns), otherwise, this skew is not guaranteed. However, for MF<10 and input frequencies greater than 10MHz, this skew is between -3.0ns and +4.0ns.

5. Phase Jitter Performance.

The phase jitter of the PLL is defined as the variations in the skew between the rising edges of EXTAL and CLKO1/2 for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKO1/2. These variations are result of the PLL locking mechanism. For input frequencies greater than 10MHZ and MF<=4, this jitter is less than +/-1.0ns. Otherwise, this jitter is not guaranteed. However, for MF<10 and input frequencies greater than 10MHz this jitter is less than +/-2.6ns.

6. Frequency Jitter Performance.

The frequency jitter of the PLL is defined as the variation of the frequency of CLKO1/2. For small MF (MF<10) this jitter is smaller than 0.5%. For mid-range MF (10 < MF < 500) this jitter is between 0.5% and ~2%. For large MF (MF > 500), the frequency jitter is 2-3%.

7. Input (EXTAL) Jitter Requirements.

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency at EXTAL is slow (i.e. it does not jump between the min and max values in one cycle) or the frequency of the jitter is fast (i.e. it does not stay at an extreme value for a long time) then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

8. K-Factor for A.C. Specification.

The following numbers should be used to estimate derating of load capacitance.

a. K-factor for decreasing load (less then 100pf) = 0.2 [ns/10Pf]

b. K-factor for increasing load (more then 100pf) = 0.6 [ns/10pf]

9. Low Frequency Oscillator Use.

The output of the Voltage Controlled Oscillator (VCO) shown in Figure 6-5 is twice the resultant clock of the PLL. Thus, a 25 MHz clock yields a VCO output of 50 MHz. If a user wishes to use a low speed clock, the output of VCO must be at least 10 MHz. If the MODCK values of 11 or 10 are used, the default multiplication factor is 401. Therefore, the lowest speed input clock that can be used is 12 kHz. However, the system can operate with even slower system frequency (slower than 12 kHz). This can be achieved by dividing down the clock using the CDVCR. If the user chooses this method, the following conditions apply:

(a). EXTAL and QUICC internal clock phases will not be synchronized.

(b). CLKO1 will not be a 50% duty cycle.

(c). CLKO2 output (if enabled) will be the frequency of PLL's output before division.

(d). PLL will be working around 13MHz, consuming current accordingly.

10. Master/Slave Clocking.

If the system has multiple QUICCs on board, user must use a full speed oscillator which is then fanned out to each QUICC (possibly via buffers or a PLL). The use of CLKO1 output of one QUICC to be the input clock of other QUICC(s) is not recommended. When using a crystal, the CLKO1 output does not meet the jitter requirements of the EXTAL input.