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Product Brief

PC312 Single-Chip Eight-User HSPA Femtocell SoC

PC312 Features

- Implements a complete 3GPP Release 6 WCDMA Femto Access Point (FAP) SoC supporting 8 user
  - 8 users
  - Up to 14Mbps HSDPA
  - Up to 5.7Mbps HSUPA
- Programmable architecture allows reconfiguration to network monitoring functions to support zero-touch femtocell provisioning or OEM specific code
- High performance ARM11 subsystem suitable for running femtocell stacks that can support secure 3GPP Iuh or SIP/IMS
  - ARM1176JZ-S 400MHz processing core
  - Advanced security features including TrustZone Security
  - Hardware accelerator support for authentication and encryption suitable for IPsec, SRTP and Kasumi
- picoArray Programmable PHY
  - Network Monitor
  - Software upgrades
  - Customer programmed features
- 10/100 Ethernet MAC and MII
  - NTP/PTP Timestamp or IEEE1588 based synchronization
- Dual high speed DDR2 SDRAM Interfaces
  - 400MHz Clock/800MHz Data
  - 256Mbit to 2Gbit
- Glueless RF Radio Interfaces
  - with Radio Sequencing Engine enabling accurate radio timing control
- Energy saving modes to enable very low power FAP implementations.

Description

The Picochip PC312 is a complete single chip 3GPP 3G Home NodeB (HNB) modem SoC (TR25.820).

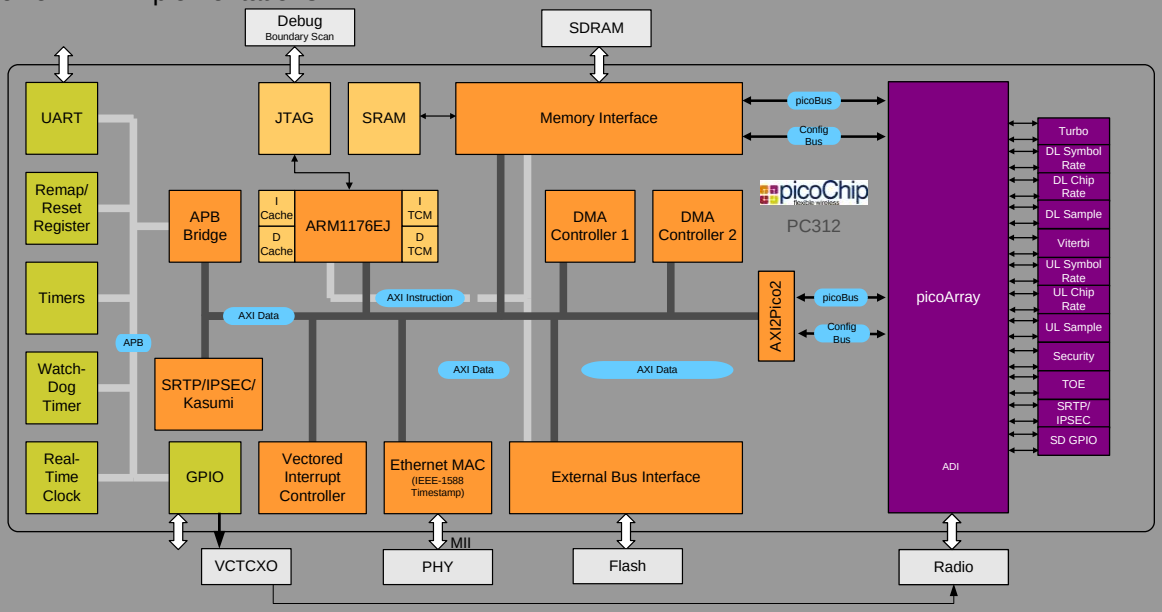
The PC312 consists of a 3GPP NodeB PHY, ARM11 processor, cryptographic engine, high-speed accelerators, and peripherals to support HSPA WCDMA FAP requirements. All baseband processing requirements from digital samples to and from RF through to network interfacing is integrated enabling an extremely low BOM cost.

Software support is provided for 3GPP Release 6 WCDMA FDD, greatly reducing development effort and time. Release 8 Home BS specifications apply. The PHY is based Picochip's field trial robust and proven femtocell technology.

RNC stacks are available which have been optimized for the PC312 and support network interfaces such as the HNB Iuh or SIP/IMS architectures.

Software to aid zero-touch provisioning is available such as 2G and 3G network monitoring functions for cell planning and handoff to enable Self Organizing Networks SON (TR32.821) functions and Dynamic Spectrum Management.

Enhanced security features are supported for authentication, location detection, encryption and the code protection



PC312 Baseband Processing

The PC8219-312 PHY which runs on the PC312 is dimensioned to support up to 8 users. The PC8219-312 provides all baseband processing from RF sample rate interface to a backward compatible API to the RNC stack running on the integrated ARM11 sub-system. The API interface provides Iub FP framed data, NBAP-like control and OA&M interfaces to the upper layers.

RF Interface and Sample-Rate Processing

PC312 includes a parallel RF interface which provides a dual IQ (up to) 15-bit, 4X chip-rate (15.36Msample) transmit bus and a dual IQ (up to) 15-bit, 8X chip-rate (30.72Msample) receive bus. A MaxPHY LVDS interface is also provided together with decimation and interpolation functions suitable for the Maxim radio chipset.

The transmit path in the RF interface includes Root-Raised Cosine (RRC) filtering which achieves the spectral shaping required by TS25.104. Transmit power is controlled by a low-latency Power Control loop.

The receive paths also include filtering to provide RRC spectral shaping and contribute to blocking of adjacent channel interferers. An Automatic Gain Control function is also included together with compensation for DC offset.

Chip rate Processing

The Transmit path chip-rate processing supports all Downlink Physical channel types required by UMTS standards including operation in Compressed Mode. For HSDPA traffic up to 15 x SF16 codes can be utilised each with QPSK or 16QAM modulation to support up to 14Mbps peak data rate.

The Receive path chip-rate processing provides a RACH Preamble Detector which supports a single signature programmable from a full set of 16 signatures. To support low spreading factor channels (SF2) Minimum Mean Square Error (MMSE) equalizers are deployed. Rake Receivers with an integral Searcher which can demodulate higher SF DPDCH and associated DPCCH channels each with up to 4 rake fingers. The PC312 will support HSUPA speeds up to 5.76Mbps.

The MMSE, Rake Receiver and Channel Estimation functions achieve all the performance requirements specified by the UMTS standards which are applicable to a low user-speed picocell.

Channel Quality Indicator (CQI) and Hybrid ARQ Acknowledgement indication (ACK) are extracted from the HS-DPCCH channels and provided to the MAC-hs Scheduler function. E-TFCI and the “Happy Bit” are extracted from E-DPCCH channels and provided to the MAC-e Scheduler. Both MAC-hs and MAC-e reside within the PHY.

Chip-rate processing is managed by a Physical Channel Controller which includes algorithms for Rake Finger Management and other functions which maintain QoS targets and ensure efficient utilisation of the physical processing resources.

Symbol Rate Processing

The Symbol rate processing functions implement all the transmit path Channel Coding, HARQ, Multiplexing and Interleaving, and all the receive path Channel Decoding, HARQ, Rate Matching, De-multiplexing and De-interleaving required by the UMTS standards. The PC312 platform delivers totally deterministic processing and resource allocation ensuring the symbol processing can support a completely arbitrary and dynamic mix of voice and data channel types. Hardware accelerators are provided for both Viterbi and Turbo decoding to support up to 8 x 64 bit CS channels (Viterbi) and 4 x 384kbps users together with 14Mbps HSDPA (Turbo).

The Symbol rate processing also includes TFCI decoding and all standards specified BER measurements for the Viterbi and Turbo decoders.

MAC-hs and MAC-e Functionality

The MAC-hs function allocates user data to the HS-DSCH channel. The scheduling algorithm can utilise up to 15 x SF16 codes each with adaptive modulation (either QPSK or 16QAM) to allocate data for up to 8 active users making use of the CQI and ACK information received from each user over the HS-DPCCH uplink channels. The MAC-hs function also manages Hybrid ARQ operation and generates the HS-SCCH channel.

Full MAC-e functionality is also included. HSUPA UE categories 1-3 are supported with minimum spreading factors SF4 and TTIs of both 10ms and 2ms – giving a maximum capacity of up to 5.74Mbps. Each user may have 1.46 Mbps in the uplink.

Radio control API

To support flexible radio configuration and control with the PC8229-333 PHY, Picochip provides Libradio. Libradio is a C library that is used by an application to initialize and configure a radio.

Libradio uses phyAPI to communicate with the Radio Sequencing Engine (RSE) on the Physical Layer (PHY). A sequence of commands and data is sent to the RSE which consists of Serial Peripheral Interface (SPI) read/write commands sent to an external chip and commands for querying or configuring the PHY.

Libradio provides an interface for the application to initialize and configure a radio without getting involved in these command sequences. Radio calibration data can be loaded from calibration files to improve the accuracy of DC offset, transmit power and receiver gain configuration.

A test application, picoradioapp, is also provided that allows the radio to be configured using low level Lua scripts.

Network Monitor Functionality

The PC8210-3x2 and PC8211-3x2 PHY provide the downlink WCDMA and GSM Network Monitor mode of operation by a separate picoArray image. This supports the SON algorithms in the higher layer stack. The PC8210 and PC8211 enables zero-touch provisioning of Femtocells by providing a network monitor function that can be used for both automated cell planning and synchronization.

The PC8210-3x2 WCDMA Network Monitor PHY performs cell search on P-SCH and S-SCH providing System Frame Number, scrambling code index, relative frequency offset, CPICH RSCP and UTRA RSSI measurements for each of the measured cells. Full demodulation and decoding of BCH of specified cells provides SIB information from BCH transport block data.

The PC8211-3x2 enables a femtocell to configure itself as a GSM MS in order to scan for its neighbor cells. The acquired information can be used for cell planning, handout from the femtocell and synchronization to a 2G macrocell BTS. The PC8211-3x2 performs a cell search of neighboring GSM macrocell carriers, and determines relative frequency offset the PLMN color code, the basestation color code and the reduced TDMA frame number. The BCCH function involves a full demodulation and decoding of the BCCH from the specified cells and provides SIB information from BCH transport block data.

The PC8210-3x2 and PC8211-3x2 PHY provide message-based control and data interfaces to higher layers on the host subsystem for the WCDMA/GSM Network Monitor modes.

Specification Summary

Parameter	Value
Specification Version	3GPP FDD Release 6 (Release 8 Home BS)
R99 UL/DL Capacity	8 x 12.2k AMR + SRB or 8 x 32K PS RAB + SRB or 8 x 64k PS RAB + SRB or 4 x 128k PS RAB + SRB or 4 x 384k PS RAB + SRB
Peak HSDPA Data rate	Max single user 14Mbps or 8 users sharing aggregate rate 14Mbps†
Peak HSUPA Data rate	Max single user 1.46Mbps or 8 users sharing aggregate rate 5.76Mbps†
HSUPA TTI support	10ms / 2ms
HSDPA UE categories	1-12
HSUPA UE categories	1-3
Rake Fingers	4 per UL physical channels
Cell Radius	≤ 200m
Maximum UE Speed	10km/h

† Physical layer data rate. Does not include air interface, protocol overhead, backhaul limitations, or limitations due to implementation of higher layer protocols.

SoC Architecture

The PC312 has many functional blocks including an ARM1176JZ-S. Communication between the ARM1176JZ-S processor and the picoArray is through the AXI2pico interface.

The External Bus Interface (EBI) is available to provide access to other external peripherals including Flash memory.

Internal communications in the ARM sub-system is via two AMBA buses: the AMBA eXtended Interface (AXI) and Advanced Peripheral Bus (APB).

The PHY consists of picoArray processors and accelerator logic. The picoArray is used to implement scheduling and a management algorithms in Node-B mode and can be reconfigured to implement network monitoring functions when needed for provisioning and interference mitigation. The picoArray's flexibility allows software upgrades to be applied as necessary in line with product releases, localizations, standardization updates, bug fixes, and performance enhancements.

To minimize cost and power the PC312 has dedicated hardware support for sample, chip and symbol rate PHY processing including turbo decoders, rake receivers, equalizers etc.

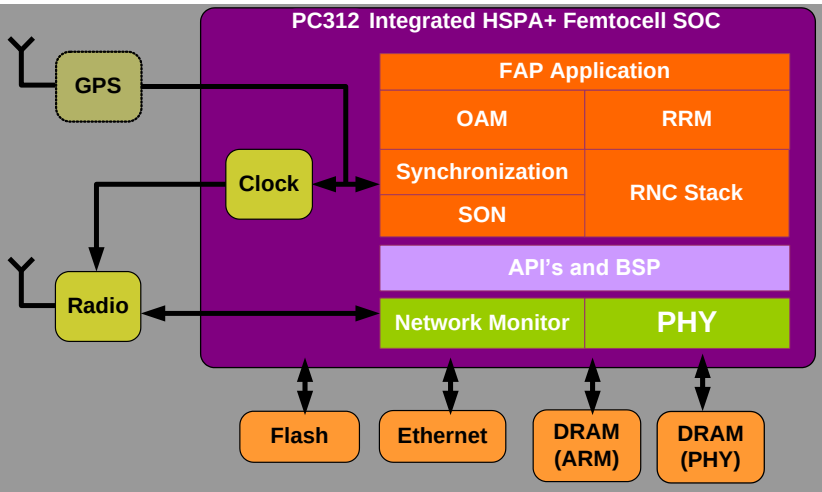


Figure 1 PC312 Femtocell System on Chip Architecture

ARM Sub-System

The ARM sub-system is based around the ARM1176JZ-S 400MHz core from ARM Ltd. This powerful 32-bit RISC processor is highly optimized for low power, high performance, computing needed for RNC stack and Trusted Platform Module (TPM) processing. Being an industry standard core, the ARM1176JZ-S is supported by various openly available tool chains and debuggers. JTAG ports support a simple and familiar development environment.

Figure 1 shows the software stacks needed to execute on the ARM11 to implement a TR25.820 compliant FAP. The PC312 ARM11 sub-system has been architected to aid RNC stack processing, security and the synchronization functions needed for Femtocell operation.

ARM Memory Architecture

The memory architecture supports a full range of memory types, allowing flexible memory map allocation depending upon the particular application requirements. The cache and tightly coupled memory deliver maximum processor performance. The memory types are summarized as follows

- On-chip memory for maximum performance
  - 64kB instruction, 64kB data cache, 32 bits wide
  - 16kB instruction, 16kB data TCM (Tightly Coupled Memory), 32bits wide single cycle access
  - 128kB SRAM, 32 bits wide
- 8 bit External Bus Interface (EBI) to allow access to off-chip memory mapped devices
- SPI NOR flash interface
- DDR2 SDRAM Interfaces

ARM Peripherals

PC312 integrates a number of peripheral blocks allowing both a reduction in total system BOM cost, as well as providing flexible interfaces to application specific sub-systems. The ARM1176JZ-S peripherals are logically mapped into the ARM1176JZ-S memory map, and are configurable by way of dedicated registers per block. The principle ARM1176JZ-S peripheral blocks are summarized as follows:

- General purpose timers (4)
- Watchdog Timer & RTC
- Single UART interface for real time tracing of MAC software
- Ethernet MAC with Reduced MII and IEEE-1588 support
- Reverse MII interface allowing direct connection to MII interfaces of router/WiFi chipsets
- 2 multi-channel DMA controllers
- 8 GPIO
- Vectored Interrupt Controller
- IPsec/SRTP Encryption/decryption engine

- Kasumi ciphering
- SHA1/2 authentication

Security

Secure boot is provided over conventional flash or the MII interface. Only proper encrypted boot code will be decrypted, authenticated and executed. On-chip customer-determined One Time Programmable (OTP) keys provide for encrypted boot and other authentication functions.

On-chip SRTP/IPsec and Kasumi encryption secures the flow of data from the network and wireless interfaces. A cryptographic engine provides support for SHA1, SHA2, AES, DES & 3DES algorithms. Support is also provided for the 3GPP Kasumi security algorithm. An IPsec/SRTP offload engine implements crypto and hashing functions for IPsec (as specified in RFCs 4301-4309) and SRTP (as specified in RFC 3711)

The PC312 implements the TrustZone from ARM to allow creation of hypervisors in an OS for secure key transactions, certificate transactions, and authentication of software processes. On-chip peripherals and memory areas are integrated into the TrustZone regime allowing a higher level of security of access to these areas of the chip.

Packet Based Timing Solutions

The PC312 has support for packet based timing solutions such as IEEE1588 v2 and NTPv3.0 both of which require hardware time-stamping. Clocks can either be generated from an on board NCO or VCXOs controlled via on-chip sigma-delta DACs.

Interfaces

External Bus Interface (EBI) allows connection to off-chip memory mapped devices. An SPI interface will allow the connection to SPI boot Flash memory. The ARM will boot from an internal ROM and copy, decrypt and authenticate the contents of the SPI flash into internal memory prior to execution of the copied code.

A Parallel Asynchronous Interface (PAI) is provided for flexible baseband interfacing to data-converters. The PAI port consists of two 16-bit interfaces with an 80 MSps throughput at 3.3v CMOS levels.

DDR2 SDRAM memory interfaces support the most economical memory solutions.

General Purpose I/O of 24 pins is programmable to support a number of different requirements such as SIM card for authentication, 16 sigma-delta GPIO for AGC, SPI, or I^2C. 3.3v CMOS levels.

JTAG test and debug

Package

21x21 PBGA 396

Power Dissipation

The PC312 has many energy saving features to enable the lowest power FAP implementations in line with the EEC Code of Conduct on Energy Consumption of Broadband Equipment. The target maximum power dissipation is 2.36W.

Related documents and specifications

The following documentation is available on the Picochip support site https://support.picochip.com/

- PC302 / PC312 Datasheet
- PC302 / PC312 Programmers Guide
- PC302 / PC312 HW Design collateral
- PC7302/PC7312 BSP and tools
- PC7312 Development Board designware and documentation
- Libradio User Guide

Contact Information

For more information on the PC312 or related products PC8219-312, PC8210-3x2, PC8211-3x2, PC7312 or other Picochip products, visit the Picochip website www.picochip.com or contact Picochip info@picochip.com

Order Information

Ordering Number	Description
PC312-HSC	8 User HSPA Femtocell SOC

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