Why yet another BTS?

- Population density – small clusters, spread across large area
- The direct “cost” of a BTS is a manageable portion of a traditional site budget. (power, tower, land, backhaul, security, operation/management)
- Open-source hardware – enabling integrated solution and open ecosystem. (work have just started …)
Architecture
OC Gen-1: simplified block diagram

- **GBC**: Application processor, Embedded Controller
- **SDR/SoC**: Baseband processor, TRX (upto 6GHz)
- **FE**: Cellular specific, Analog front-end
Architecture
OC Gen-1: block diagram

- **LED**: LED buzzer
- **GBC**: Computing, Power, Housekeeping, Ethernet SW
- **Debug**: HDMI, USB2/3, Ethernet, ICID
- **Radio**: USB3/PCIe, FPGA, TRX
- **Sync**: GPSDO, OBC
- **GPS/Iridium**: Band-specific, PA, LNA, Filter, Duplexer, coupler, GSM loopback
- **FE**:
Architecture
OC Gen-1: Interfaces

LED

GBC
USB2/3, I2C, PCIE G2
GPIO, +12V, +3.3V

Debug
HDMI, USB
Ethernet, ICID

Sync
GPSDO, OBC

Radio

FE
GSM Loopback

GPS/Iridium
I2C, GPIO, 5V
2RX, 2TX
- DC input: 16-24VDC
- PoE: PD
  (IEEE 802.3at/af/PoE++/Passive PoE)
- PoE: PSE (max. 20W)
- Main power switch
- 2x N-type (two TRX)
- LT4275 PD controller
- LT4274 PSE controller
- Two QC (charge controller): internal battery: Lithium ion (2700mAh) external battery: SLA (65Ah)
- 12V for main rail + housekeeping (own)
- Hard-coded power sequencing
- TI ARM M4, Tiva 120MHz uController
- Manage all power rails and power sequencing, front-end SW, voltage/current sensors
- Ethernet switches, PD/PSE, QC, Sync
- Monitor boot sequence, runs OCWare
- SDR
- UHD-Compatible
- Storage
- TRX/Gain control

- USB2.0
- USB3.0
- I2C
- PCIE G2
- GPIO
- +12V
- +3.3V
Architecture

OCWare

Transport
- UART
- Ethernet
- OBC

Transport Manager
- Gossiper

Subsystem Monitor
- Big Brother

Subsystems
- GPP
- BMS
- RFFE
- Sync
- Power
- ...

TI-RTOS/Tivaware/FreeRTOS
Architecture

Radio

SDR

FX3 Firmware
USB3

FPGA Firmware
UHD/TRX config
Gain/PA control

OCWare
Front-end control