SIEMENS

General Purpose Power Controller (GPPC) PSB 2121

Preminimary Data **CMOS IC**

Type	Ordering Code	Package
PSB 2121-P	Q67100-H8646	P-DIP-16
PSB 2121-T	Q67100-H6032	P-DSO-20 (SMD)

The PSB 2121 is a pulse width modulator circuit designed for fixed-frequency switching regulators with very low power consumption.

In telefony and ISDN systems a high conversion yield is crucial to maintain functionality in all supply conditions via "S" or "U" interfaces. The PSB 2121 design and technology realize high conversion efficiency and low power dissipation.

It should be recognized that the PSB 2121 can also be used in numerous DC/DC conversion systems other than ISDN power supplies.

The PSB 2121 Contains the Following Functional Blocks

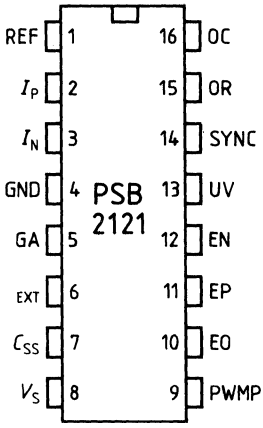
- Undervoltage lockout
- Temperature compensated voltage reference
- Sawtooth oscillator
- Error amplifier
- Pulse width modulator
- Digital current limiting
- Soft start
- Double pulse inhibit
- Power driver

Together with few external components it provides a stable 5 V DC supply for subscriber terminals (TEs) or network terminations (NTs). It can also be programmed for higher output voltages, e.g. to supply S-lines with 40 V.

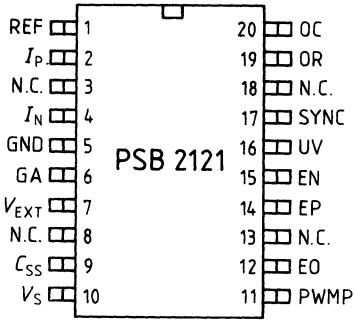
- Switched mode DC/DC-converter
- CCITT ISDN compatible
- Low power dissipation
- Supply voltage range 8 V to 70 V
- Programmable input undervoltage protection
- Programmable overcurrent protection
- Soft start
- Power housekeeping input
- Oscillator synchronization input/output
- High voltage CMOS technology 70 V

Pin Configurations
(top view)

P-DIP-16



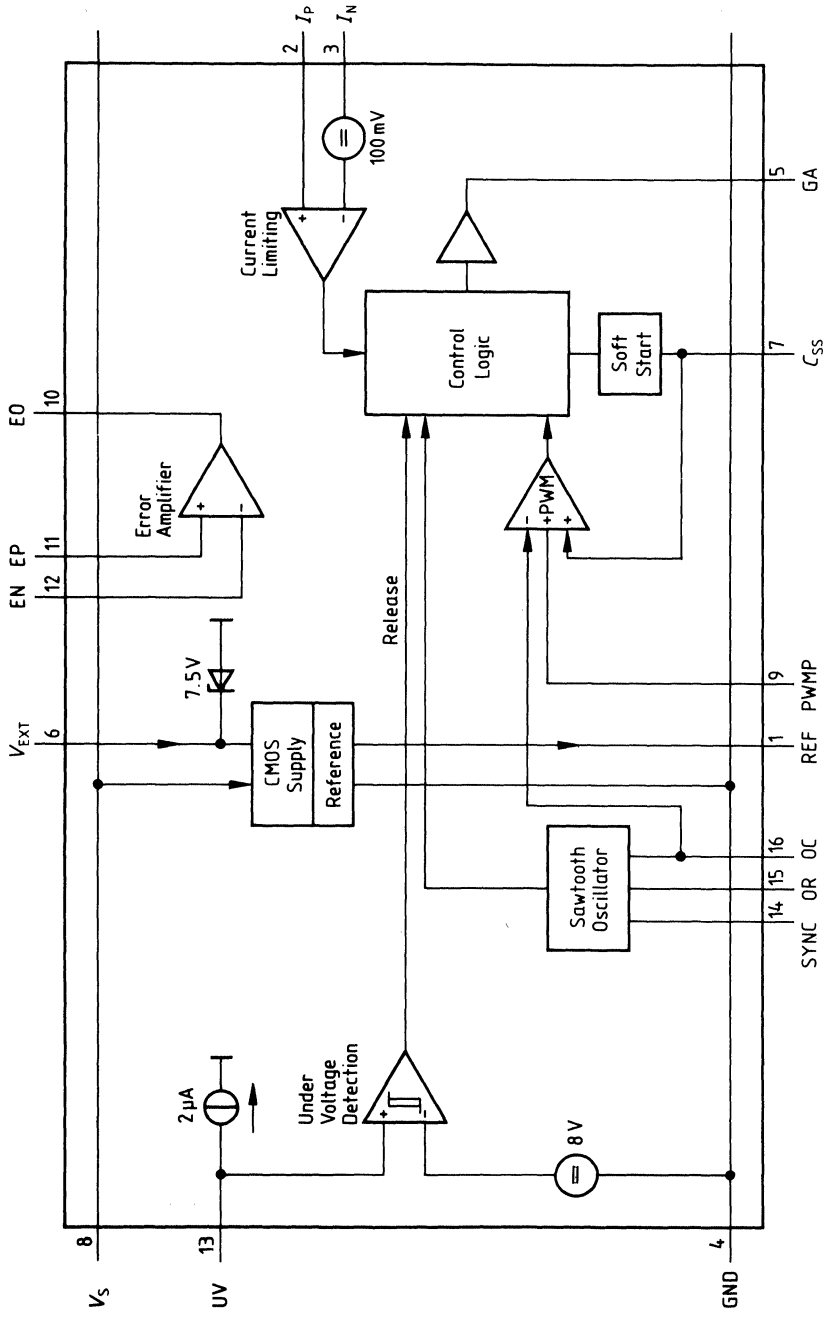
P-DSO-20



Pin Definitions and Functions

Pin No. P-DIP	Symbol	Input (I) Output (O)	Definition	Function
1	REF	O	Reference voltage	Output of the 4.0 V reference voltage.
2	I_P	I	Positive current sense	When the voltage difference between these two pins exceeds 100 mV, the digital current limiting becomes active.
3	I_N	I	Negative current sense	
4	GND	I	Ground	All analog and digital signals are referred to this pin.
5	GA	O	Gate	Totem-pole output driver, has to be connected with the gate of an external power switch.
6	V_{EXT}	I/O	External supply	Output of the internal CMOS supply. Via V_{EXT} the internal CMOS circuits can be supplied from an external DC-supply in order to reduce chip power dissipation.
7	C_{SS}	I	Soft start capacitor	The capacitor at this pin determines the soft start characteristic.
8	V_S	I	Supply voltage	V_S is the positive input voltage.
9	PWMP	I	Pulse width modulator	Non inverting input of the pulse width modulator.
10	EO	O		Error amplifier output.
11	EP	I	Positive voltage sense	Non inverting input of the error amplifier.
12	EN	I	Negative voltage sense	Inverting input of the error amplifier.
13	UV	I	Undervoltage detection	The undervoltage lockout can be programmed via UV.
14	SYNC	I/O	Synchronization	This pin can be used as an input for synchronization of the oscillator to an external frequency, or as an output to synchronize multiple devices.
15	OR	I	R-Oscillator	The external timing components of the ramp generator are attached to OR and OC.
16	OC	I	C-Oscillator	

Figure 1
GPPC Functional Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage (pin V_S) referred to GND	V_S	80	V
Analog input voltage (pins I_P, I_N, PWMP, EP, EN, SYNC, OR, OC) referred to GND	$V_{I\,A}$	6	V
Reference output current (pin REF)	$I_{O\,REF}$	−5	mA
SYNC output current (pin SYNC)	$I_{O\,SYNC}$	−5	mA
Error amplifier output current (pin EO)	$I_{O\,Amp}$	−5	mA
Z-current (pin V_{EXT})	$I_{Z\,EXT}$	2	mA
Output current (pin V_{EXT})	$I_{O\,EXT}$	−5	mA
Driver output current (pin GA)	$I_{D\,R}$	−5	mA
Ambient temperature under bias	T_A	−25 to 85	°C
Storage temperature	T_{stg}	−40 to 125	°C

DC Characteristics

$T_A = 0$ to 70 °C, $V_S = 8$ to 70 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_S		30		µA	$V_{S\,EXT} \geq 6.3$ V
Reference V_{REF}						
Output voltage	$V_{REF\,O}$	3.92	4.0	4.08	V	$T_j = 25$ °C, $I_L = 0$ mA, $V_S = 40$ V
Line regulation	$V_{REF\,Line}$			60	mV	$V_S = 20$ to 60 V $T_j = 25$ °C, $I_L = 0$ mA
Load regulation	$V_{REF\,Load}$		20	40	mV	$I_L = 0.1$ to 0.3 mA $V_S = 40$ V, $T_j = 25$ °C
Temperature stability	$V_{REF\,TS}$		25		mV	0...70 °C
Load current	$I_{REF\,Load}$			0.5	mA	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Oscillator/SYNC/OC						
$f_{OSC} = 20$ kHz, $R_C = 39$ kΩ ± 1%, $R_D = 0$ Ω, $C_r = 1$ nF ± 1%						
Initial accuracy $T_j = 25$ °C			± 10		%	
Voltage stability			1	3	%	
Temperature stability			5		%	
Max. frequency	f_{max}	200			kHz	$R_C = 27$ kΩ $C_r = 39$ pF
Sawtooth peak voltage	V_S		3.2		V	$V_S = 40$ V
Sawtooth valley voltage	V_S		1.8		V	$V_S = 40$ V
H-sync output level	$V_{SYNC\,H}$	2.4		5.25	V	$I_L = 0.5$ mA $V_{EXT} \leq 6.3$ V
L-sync output level	$V_{SYNC\,L}$		0.4	0.8	V	$I_L = 20$ µA
Error Amplifier/EO/EP/EN						
Input offset voltage	V_{IO}		3	10	mV	
Input current	I_I			10	nA	
Common mode range	CMR	1.8		4.5	V	
DC open loop gain	G_{VO}	60	70		dB	
Common mode rejection	k_{CMR}	60	70		dB	
Unity gain bandwidth	f		0.5		MHz	C_L (pin) ≤ 10 pF
Supply voltage rejection	k_{SVR}		70		dB	
H-output voltage	V_{OH}	4			V	$I_L = -100$ µA
L-output voltage	V_{OL}			1	V	$I_L = 10$ µA
Current Limit Comparator I_P/I_N,						
$T_j = 25$ °C						
Sense voltage	V_{Sense}	85	100	115	mV	$V_S = 40$ V
Input bias current	I_I			10	nA	
Input voltage range	V_I	0		1	V	
Response time (signal at GA)	t_{Res}		1	2	µs	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Pulse Width Modulator						
Duty cycle	t_d	0		50	%	
Under Voltage Detection UV						
Start up threshold	V	7	8	9	V	pin UV = V_S
Threshold hysteresis	H_y		0.3		V	pin UV = V_S
Soft Start C_{SS}						
Charging current	C_T	2	4	8	µA	
Output Driver GA $T_j = 25\,°C$						
High output voltage	V_{OH}	4.5			V	$I_{Source} = 5$ mA
Low output voltage	V_{OL}			0.4	V	$I_{Sink} = 5$ mA
Rise time	t_r		130	200	ns	$C_L = 220$ pF
Fall time	t_f		130	200	ns	$C_L = 220$ pF
Output current	I_O			5	mA	
External Supply V_{EXT}						
Output voltage	V_O		6		V	$I_{Source} = 1$ mA
Output current	I_O			2	mA	
Input voltage	V_I	6.0		7.5	V	
Z-current	I_Z			2	mA	
Power Consumption	P_{tot}		5	6	mW	$V_S = 40$ V $f_{OSC} = 20$ kHz $V_{EXT} = 6.3$ V

Application Information

Undervoltage Lockout

The undervoltage lockout circuit protects the PSB 2121 and the power devices from inadequate supply voltage. If V_S is too low, the circuit disables this output driver. This ensures that all control functions have been stabilized in the proper state when the turn on voltage (8 V) is reached, and it prevents from the possibility of start up glitches. The undervoltage lockout is programmable by connecting a Z-diode between V_S and UV from 8 V up to 70 V. If UV is connected to V_S the default undervoltage lockout is 8 V.

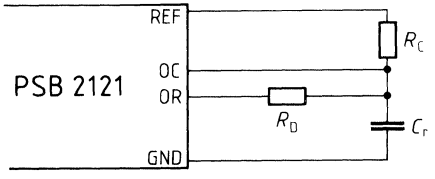
Voltage Reference

The reference regulator of the PSB 2121 is based on a temperature compensated bandgap. This circuitry is fully active at supply voltages above +6.0 V and provides up to 0.5 mA of load current to external circuitry at +4.0 V. This reference has to be buffered by an external capacitor > 0.5 µF.

Oscillator

The oscillator frequency is programmed by three components: R_C, C_r and R_D as shown in **figure 2**. The oscillator timing capacitor C_T is charged by V_{REF} through R_C and discharged by R_D. (R_D is series-connected with an internal 9 kΩ discharge-resistor). So the rise-time and the fall-time of the sawtooth oscillator can be programmed individually.

Figure 2



The PSB 2121 could be synchronized by the rising edge of the SYNC signal, whose frequency must be 10% higher than the free run frequency, determined by the RC-components. The SYNC pin can also be used as a trigger-output. As long as the capacitor of the sawtooth oscillator is discharged, SYNC is high. So multiple devices can be synchronized together by programming one master unit for the desired frequency.

Notice that the frequency of the output driver is half the oscillator frequency.

Soft Start Circuit

The soft start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When the supply voltage is connected to the PSB 2121 the undervoltage lockout circuit holds the soft start capacitor voltage at zero. When the supply voltage reaches normal operating range an internal 4 µA current source will charge the external soft start capacitor. As the soft start voltage ramps up to +5 V, the duty cycle of the PWM linearly increases to whatever value regulation loop requires.

Pulse Width Modulator

The pulse width modulator compares the sawtooth-voltage of the oscillator output with the input signal at PWMP and with the voltage of the external soft start capacitor at C_{SS} **(see figure 1)**.

Error Amplifier

Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance: unity-gain stable.

Control Logic

The control logic inhibits double pulses during one duty cycle and limits the maximum duty cycle to 50%.

Current Limiting

A differential input comparator terminates individual output pulses each time when the sense voltage rises above threshold.

When sense voltage rises to 100 mA above threshold a shutdown signal is sent to the control logic.

CMOS Supply

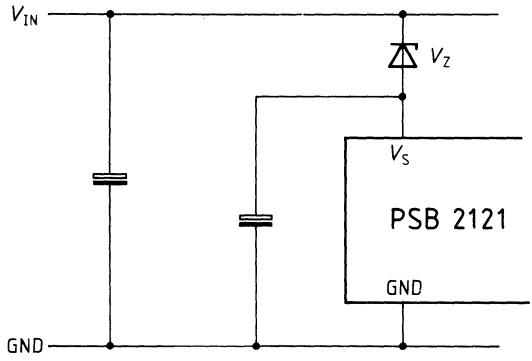
An integrated 6 V linear voltage regulator supplies the internal low-voltage CMOS circuits from the input voltage. This supply voltage is connected to pin V_{EXT} and has to be buffered by an external capacitor (C_{min} = 1 µF). Power dissipation of the linear voltage regulator can be reduced, if an external supply is used for that purpose by connecting it to pin V_{EXT}. If the input voltage at V_{EXT} reaches 6.3 V the internal linear voltage regulator turns off and the internal CMOS circuits are fed from the external voltage. In this case the input current at V_{EXT} is approx. 0.5 mA.

Note: An internal 7.5 V Z-diode protects the V_{EXT} input against overvoltage. The maximum Z-current is 2 mA! So if the external CMOS supply isn't stabilized the input current must be limited (e.g. by a resistor).

Extended Input Voltage Range

Some DC/DC-converter applications require a higher input voltage than the maximum supply voltage of the PSB 2121 which is limited to 70 V. **Figure 3** shows a method to extend the input voltage range by connecting a Z-diode between the input voltage and V_S of the PSB 2121.

Figure 3



If the PSB 2121 is fed via V_{EXT}, the input current at pin V_S is approx. 30 µA. The additional power losses are accordingly 30 µA · V_Z; the minimum input voltage is V_Z + 8 V.