Data Sheet, DS 1, March 2001

Q-SMINT®IX
2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(I**ntelligent e**X**tended)
PEF 81912/81913 Version 1.3

Wired
Communications

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Revision History: **March 2001** DS 1

Previous Version: Preliminary Data Sheet 10.00

Page	Subjects (major changes since last revision)
All	Editorial changes, addition of notes for clarification etc.
Table 1, **Chapter 1.3**	Introduced new versions 81913 with extended performance of the U-interface
Chapter 2.1.1.1	SCI: header description: added to sequences 43_H, 41_H and 49_H: ' Generally, it can be used for any register access to the address range 00_H-$7D_H$.'
Chapter 2.3.2	IOM-2 handler: removed 'U-transceiver (U)' from listing of functional units with programmable time slot and data port.
Figure 12	Figure 'Data Access via CDAx0 and CDAx1 register pairs' corrected: input swap has influence on the input enable (EN_I0,1), too
Chapter 2.5.5.2	C/I commands: removed 'unconditional command' from description C/I-command 'DR'
Chapter 2.5.5.3	LT-S state machine: C/I=command AIL removed (no valid input to the LT-S state machine)
Chapter 2.6.2.1	HDLC: removed from description RBC: '(bytes, which are ready for next read access)' and '(blocks, which have been already read)'.
Chapter 2.6.3.1	HDLC: Possible Error Conditions: added behavioral description in case of an XPR interrupt
Chapter 4	Detailed register description: • U-transceiver Mode Evaluation Timing: clarified description • register ID: reset value of version 1.3 is 01_H (not 00_H) • RSTA.SA1,0: clarified note • CIX1.CODX1: bits 5-0 of C/I-channel 1 (not 7-2) • IOM_CR:TIC_DIS: added for clarification: 'This means that the timeslots TIC, A/B, S/G and BAC are not available any more.'
Chapter 5.1	Absolute Maximum Ratings: Maximum Voltage on VDD: 4.2V (before: 4.6V)
Chapter 5.1	Refined references for ESD requirements:' ...(CDM), EIA/JESD22-A114B (HBM) ---'
Chapter 5.2	Input/output leakage current set to 10µA (before: 1µA)
Table 43	U-transceiver characteristics: enhanced S/N+D for 81913 and threshold level for 81912 and 81913 distinguished

PEF 81912/81913

Revision History:	**March 2001**	DS 1
Previous Version:	Preliminary Data Sheet 10.00	

Page	Subjects (major changes since last revision)
Chapter 5.6.2 **Chapter 5.6.3**	AC-Timing SCI/parallel µC interface: enhanced timing specifications
Chapter 5.6.3	Added restriction for control interval t_{RI}
Chapter 5.6.5	Parameters of the UVD/POR Circuit: defined reduced range of hysteresis: min. 30mV/max. 90mV relaxed upper limit of Detection Threshold to 2.92V (before: 2.9V) defined max. rising VDD for power-on
Chapter 7.2.5	Register summary U-transceiver 4B3T: Reset value of MASKU is FF_H (not 00_H)
Chapter 7.3	External circuitry for T-SMINT updated

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1 Overview

The **PEF 81912 / 81913** (Q-SMINT®IX) offers most features known from the PEB / PEF 8191 [12] and can hence replace the latter in its major applications. However, it does not replace the PEB/PEF 8191 in applications that use the S-transceiver in TE mode.

The Q-SMINT®IX features U-transceiver, S-transceiver, HDLC controller and an IOM®-2 interface on a single chip. A microcontroller interface provides access to both transceivers, the HDLC controller as well as the IOM®-2 interface.

Main target applications of the Q-SMINT®IX are intelligent NT applications which require one single HDLC controller.

Table 1 summarizes the 2nd generation NT products.

Table 1 NT Products of the 2nd Generation

	PEF80912	PEF80913	PEF81912	PEF81913	PEF82912	PEF82913
	Q-SMINT®O		Q-SMINT®IX		Q-SMINT®I	
Package	P-MQFP-44		P-MQFP-64 P-TQFP-64		P-MQFP-64 P-TQFP-64	
Register access	no		U+S+HDLC+ IOM®-2		U+S+ IOM®-2	
Access via	n.a.		parallel (or SCI or IOM®-2)		parallel (or SCI or IOM®-2)	
MCLK, watchdog timer, SDS, BCL, D-channel arbitration, IOM®-2 access and manipulation etc. provided	no		yes		yes	
HDLC controller	no		yes		no	
NT1 mode available	yes (only)		no		no	
Extended U-Performance 20kft	no	yes	no	yes	no	yes

1.1 References

[1] TS 102 080, Transmission and Multiplexing ; ISDN basic rate access; Digital transmission system on metallic local lines, ETSI, November 1998

[2] T1.601-1998 (Revision of ANSI T1.601-1992), ISDN-Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification), ANSI, 1998

[3] ST/LAA/ELR/DNP/822, CNET, France

[4] RC7355E, 2B1Q Generic Physical Layer Specification, British Telecommunications plc., 1997

[5] FZA TS 0095/01:1997-10, Technische Spezifikationen für Netzabschlußgeräte für den ISDN Basisanschluß (NT-BA), Post & Telekom Austria, 1997

[6] pr ETS 300 012 Draft, ISDN; Basic User Network Interface (UNI), ETSI, November 1996

[7] T1.605-1991, ISDN-Basic Access Interface for S and T Reference Points (Layer 1 Specification), ANSI, 1991

[8] I.430, ISDN User-Network Interfaces: Layer 1 Recommendations, ITU, November 1988

[9] IEC-Q, ISDN Echocancellation Circuit, PEB 2091 V4.3, User's Manual 02.95, Siemens AG, 1995

[10] SBCX, S/T Bus Interface Circuit Extended, PEB 2081 V3.4, User's Manual 11.96, Siemens AG, 1996

[11] NTC-Q, Network Termination Controller (2B1Q), PEB / PEF 8091 V1.1, Data Sheet 10.97, Siemens AG, 1997

[12] INTC-Q, Intelligent Network Termination Controller (2B1Q), PEB / PEF 8191 V1.1, Data Sheet 10.97, Siemens AG, 1997

[13] IOM®-2 Interface Reference Guide, Siemens AG, 03.91

[14] SCOUT-S(X), Siemens Codec with S/T-Transceiver, PSB 2138x V1.3, Preliminary Data Sheet 8.99, Infineon Technologies, 1999

[15] PITA, PCI Interface for Telephony/Data Applications V0.3, SICAN GmbH, September 1997

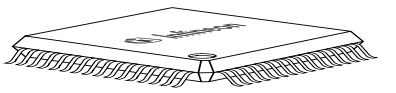
[16] Dual Channel SLICOFI-2, HV-SLIC; DUSLIC; PEB3265, 4265, 4266; Data Sheet DS2, Infineon Technologies, July 2000.

2B1Q Second Gen. Modular ISDN NT (Intelligent eXtended)
Q-SMINT®IX

PEF 81912/81913

Version 1.3

1.2 Features PEF 81912



P-MQFP-64

P-TQFP-64

Features known from the PEB/PEF 8191

- U-transceiver, S-transceiver and HDLC controller on one chip
- Perfectly suited for low-cost intelligent NTs that require one single HDLC controller
- U-interface (2B1Q) conform to ETSI [1], ANSI [2] and CNET [3]:
  - Meets all transmission requirements on all ETSI, ANSI and CNET loops with margin
  - Conform to British Telecom's RC7355E [4]
  - Compliant with ETSI 10 ms micro interruptions
  - MLT input and decode logic (ANSI [2])
- S/T-interface conform to ETSI [6], ANSI [7] and ITU [8]
  - Supports point-to-point and bus configurations
  - Meets and exceeds all transmission requirements
- Activation status LED supported
- BCL, SDS1, SDS2, programmable MCLK, watchdog timer,
- Access to IOM®-2 C/I and Monitor channels
- Power-down mode and reset states (e.g. S-transceiver) for individual circuits
- Automatic D-channel arbitration between S-bus and local HDLC controller
- Parallel or serial µP-interface

Type	Package
PEF 81912/81913	P-MQFP-64
PEF 81912/81913	P-TQFP-64

New Features

- Reduced number of external components for external U-hybrid required
- Optional use of up to 2x20 Ω resistors on the line side of the transformer (e.g. PTCs)
- Pin Uref and the according external capacitor removed
- Improved ESD (2 kV instead of <850 V)
- Inputs accept 3.3 V and 5 V
- I/O (open drain) accepts pull-up to 3.3 V[1)]
- LED signal is programmable but can also automatically indicate the activation status (mode select via 1 bit)
- Pin compatible with T-SMINT®IX (2nd Generation)
- Priority setting (8/10) for off-chip and on-chip HDLC controller
- Improved FIFO structure (SCOUT)
- Enhanced IOM®-2 timeslot access and manipulation (SCOUT)
- HDLC extended transparent mode (SCOUT)
- MCLK can be disabled (SCOUT)
- External Awake ($\overline{\text{EAW}}$)
- Optional: All registers can be read and written to via new Monitor channel concept
- Optional: Implementation of S-transceiver statemachine in software
- Indirect Addressing (SCOUT)
- HDLC access to B-channels, D-channel and any combination of them
- Programmable strobes SDS1/2 are more flexible, e.g. active during several timeslots
- Power-on reset and Undervoltage Detection with no external components
- Lowest power consumption due to:
  - Low power CMOS technology (0.35µ)
  - Newly optimized low-power libraries
  - High output swing on U- and S-line interface leads to minimized power consumption
  - Single 3.3 Volt power supply
- 200 mW (INTC-Q: 295 mW) power consumption with random data over ETSI Loop 2 (external loads on the S and U interface only and no additional external loads).
- 15 mW typical power consumption in power down (INTC-Q: 28 mW)

1.3 Features PEF 81913

The Q-SMINT®IX PEF 81913 provides all features of the PEF 81912. Additionally, a significantly enhanced performance of the U-interface as compared to ETSI [1], ANSI [2] and CNET [3] requirements is guaranteed:

Transparent transmission on 20kft AWG26 with a BER < 10^{-7} (without noise).

1) Pull-ups to 5 V must be avoided. A so-called 'hot-electron-effect' would lead to long term degradation.

1.4 Not Supported are ...

- Integrated U-hybrid
- ’Self test request’ and ’Self test passed’ of U-transceiver
- TE-mode of the S-transceiver
- DECT-link capability
- SRA (capacitive receiver coupling is not suited for S-feeding).
- ’NT-Star’ with star point on the IOM®-2 bus (already not supported in INTC-Q).
- HDLC Automode
- No access to S2-5 channels. Access only to S1 and Q channel as in SCOUT. No selection between transparent and non-auto mode provided.
- The oscillator architecture was changed with respect to the INTC-Q to reduce power consumption. As a consequence, the Q-SMINT®IX always needs a crystal and pin XIN can not be connected to an external clock as it was possible for IEC-Q and NTC-Q. This does not limit the use of the Q-SMINT®IX in NTs since all NT designs use crystals anyway.

1.5 Different are ...

- HDLC naming convention of transparent modes has changed (as in SCOUT). The according bit combination in the MODEH register remains unchanged, hence software compatibility is ensured.

Table 2 HDLC Naming Convention

Old (ICC/INTC-Q)	New	Address comparison
Transparent 1	Transparent 2	TEI
Transparent 2	Transparent 0	none
Transparent 3	Transparent 1	SAPI

1.6 Pin Configuration

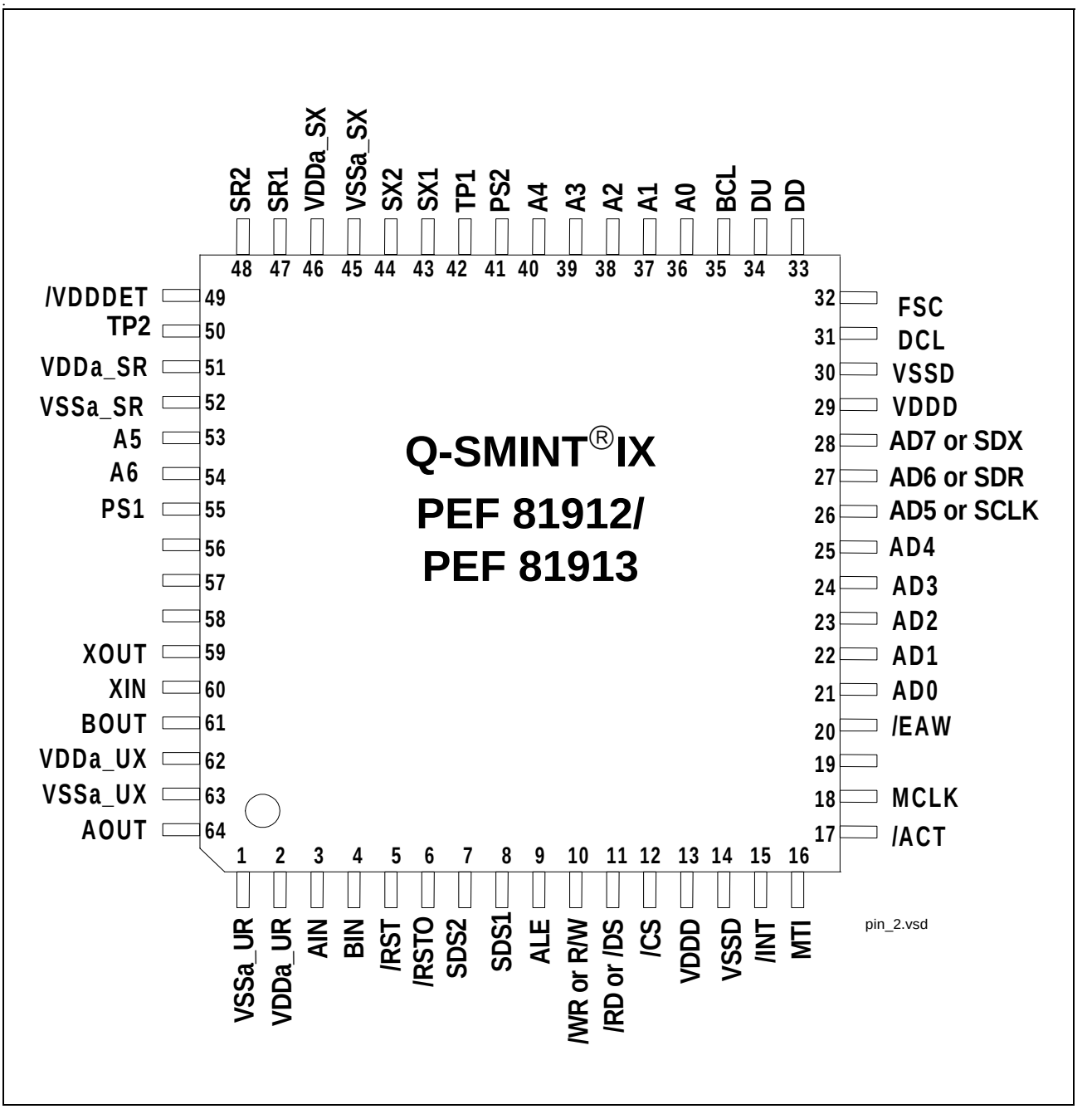


Figure 1 Pin Configuration

1.7 Block Diagram

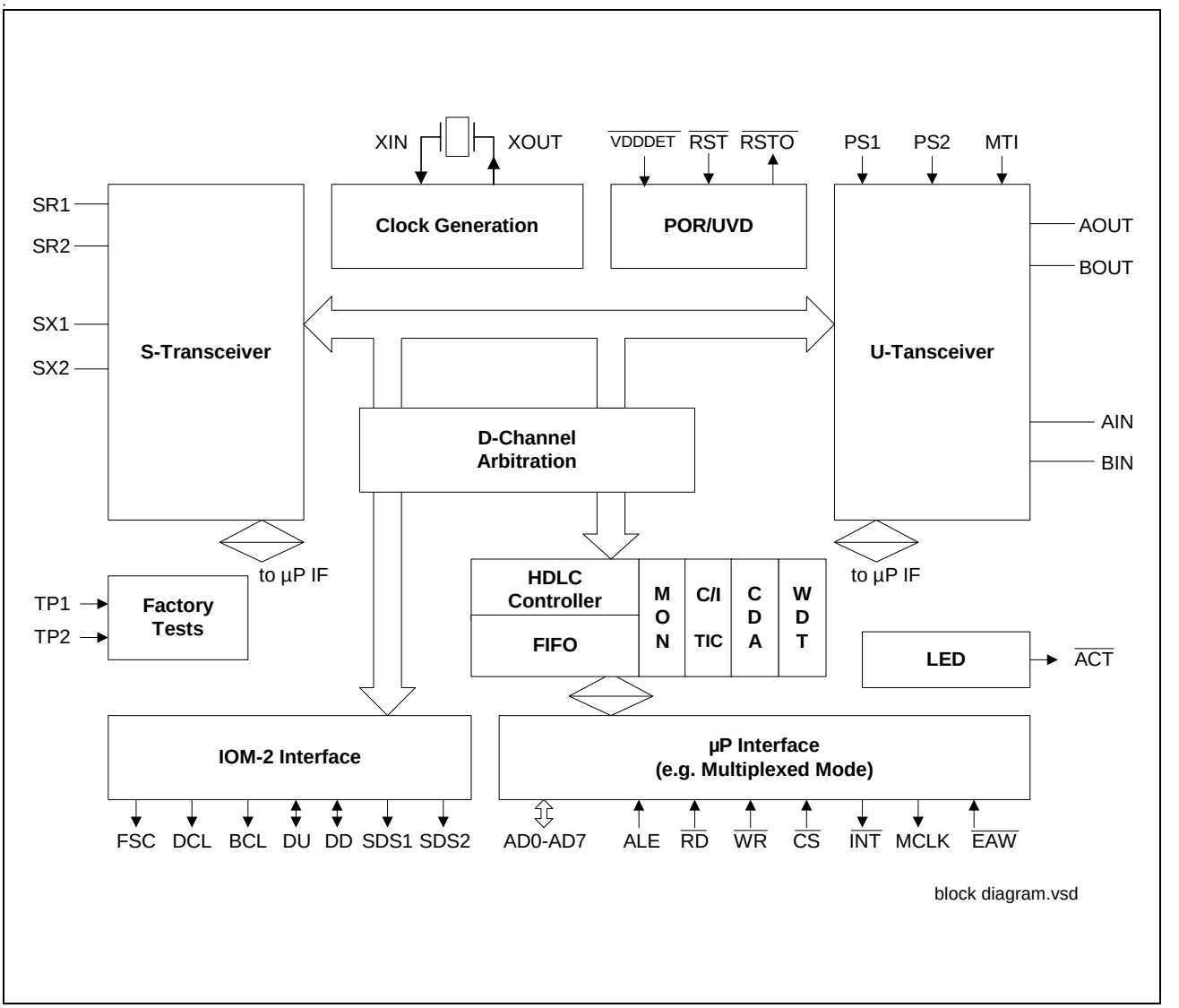


Figure 2 Block Diagram

1.8 Pin Definitions and Functions

Table 3 Pin Definitions and Functions

	Pin	Symbol	Type	Function
	2	VDDa_UR	–	Supply voltage for U-Receiver (3.3 V ± 5 %)
	1	VSSa_UR	–	Analog ground (0 V) U-Receiver
	62	VDDa_UX	–	Supply voltage for U-Transmitter (3.3 V ± 5 %)
	63	VSSa_UX	–	Analog ground (0 V) U-Transmitter
	51	VDDa_SR	–	Supply voltage for S-Receiver (3.3 V ± 5 %)
	52	VSSa_SR	–	Analog ground (0 V) S-Receiver
	46	VDDa_SX	–	Supply voltage for S-Transmitter (3.3 V ± 5 %)
	45	VSSa_SX	–	Analog ground (0 V) S-Transmitter
	29	VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
	30	VSSD	–	Ground (0 V) digital circuits
	13	VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
	14	VSSD	–	Ground (0 V) digital circuits
	32	FSC	O	**Frame Sync:** 8-kHz frame synchronization signal
	31	DCL	O	**Data Clock:** IOM®-2 interface clock signal (double clock): 1.536 MHz
	35	BCL	O	**Bit Clock:** The bit clock is identical to the IOM®-2 data rate (768 kHz)
	33	DD	I/O OD	**Data Downstream:** Data on the IOM®-2 interface
	34	DU	I/O OD	**Data Upstream:** Data on the IOM®-2 interface

Table 3 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	8	SDS1	O	**Serial Data Strobe1:** Programmable strobe signal for time slot and/ or D-channel indication on IOM®-2
	7	SDS2	O	**Serial Data Strobe2:** Programmable strobe signal for time slot and/ or D-channel indication on IOM®-2
	12	$\overline{CS}$	I	**Chip Select:** A low level indicates a microcontroller access to the Q-SMINT®IX
	26	SCLK	I	**Serial Clock:** Clock signal of the SCI interface if a serial interface is selected
	26	AD5	I/O	**Multiplexed Bus Mode:** **Address/data bus** Address/data line AD5 if the parallel interface is selected **Non-Multiplexed Bus Mode:** **Data bus** Data line D5 if the parallel interface is selected
	27	SDR	I	**Serial Data Receive:** Receive data line of the SCI interface if a serial interface is selected
	27	AD6	I/O	**Multiplexed Bus Mode:** **Address/data bus** Address/data line AD6 if the parallel interface is selected **Non-Multiplexed Bus Mode:** **Data bus** Data line D6 if the parallel interface is selected

Table 3 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	28	SDX	OD,O	**Serial Data Transmit:** Transmit data line of the SCI interface if a serial interface is selected
	28	AD7	I/O	**Multiplexed Bus Mode:** **Address/data bus** Address/data line AD7 if the parallel interface is selected **Non-Multiplexed Bus Mode:** **Data bus** Data line D7 if the parallel interface is selected
	21 22 23 24 25	AD0 AD1 AD2 AD3 AD4	I/O I/O I/O I/O I/O	**Multiplexed Bus Mode:** **Address/data bus** Transfers addresses from the microcontroller to the Q-SMINT®IX and data between the microcontroller and the Q-SMINT®IX. **Non-Multiplexed Bus Mode:** **Data bus.** Transfers data between the microcontroller and the Q-SMINT®IX (data lines D0-D4).
	36 37 38 39 40 53 54	A0 A1 A2 A3 A4 A5 A6	I I I I I I I	**Non-Multiplexed Bus Mode:** Address bus transfers addresses from the microcontroller to the Q-SMINT®IX. For indirect address mode only A0 is valid. **Multiplexed Bus Mode** Not used in multiplexed bus mode. In this case A0-A6 should directly be connected to VDD.
	11	$\overline{RD}$	I	**Read** Indicates a read access to the registers (Intel bus mode).
		$\overline{DS}$	I	**Data Strobe** The rising edge marks the end of a valid read or write operation (Motorola bus mode).

Table 3 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	10	$\overline{WR}$ R/$\overline{W}$	I I	**Write** Indicates a write access to the registers (Intel bus mode). **Read/Write** A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode).
	9	ALE	I	**Address Latch Enable** An address on the external address/data bus (multiplexed bus type only) is latched with the falling edge of ALE. ALE also selects the microcontroller interface type (multiplexed or non multiplexed).
	5	$\overline{RST}$	I	**Reset:** Low active reset input. Schmitt-Trigger input with hysteresis of typical 360 mV. Tie to '1' if not used.
	6	$\overline{RSTO}$	OD	**Reset Output:** Low active reset output.
	15	$\overline{INT}$	OD	**Interrupt Request:** $\overline{INT}$ becomes active if the Q-SMINT®IX requests an interrupt.
	18	MCLK	O	**Microcontroller Clock:** Clock output for the microcontroller
	19			Tie to '1'
	20	$\overline{EAW}$	I	**External Awake**: A low level on $\overline{EAW}$ during power down activates the clock generation of the Q-SMINT®IX, i.e. the IOM®-2 interface provides FSC, DCL and BCL for read and write access.[1)]
	43	SX1	O	**S-Bus Transmitter Output (**positive**)**
	44	SX2	O	**S-Bus Transmitter Output (**negative**)**
	47	SR1	I	**S-Bus Receiver Input**

Table 3 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	48	SR2	I	**S-Bus Receiver Input**
	60	XIN	I	**Crystal 1:** Connected to a 15.36 MHz crystal
	59	XOUT	O	**Crystal 2:** Connected to a 15.36 MHz crystal
	64	AOUT	O	**Differential U-interface Output**
	61	BOUT	O	**Differential U-interface Output**
	3	AIN	I	**Differential U-interface Input**
	4	BIN	I	**Differential U-interface Input**
	49	$\overline{\text{VDDDET}}$	I	**VDD Detection:** This pin selects if the V_{DD} detection is active ('0') and reset pulses are generated on pin $\overline{\text{RSTO}}$ or whether it is deactivated ('1') and an external reset has to be applied on pin $\overline{\text{RST}}$.
	16	MTI	I	**Metallic Termination Input.** Input to evaluate Metallic Termination pulses. Tie to '1' if not used.
	55	PS1	I	**Power Status (primary).** The pin status is passed to the overhead bit 'PS1' in the U frame to indicate the status of the primary power supply ('1' = ok).
	41	PS2	I	**Power Status (secondary).** The pin status is passed to the overhead bit 'PS2' in the U frame to indicate the status of the secondary power supply ('1' = ok).
	17	$\overline{\text{ACT}}$	O	**Activation LED.** Indicates the activation status of U- and S-transceiver. Can directly drive a LED (4 mA).
	42	TP1	I	**Test Pin 1.** Used for factory device test. Tie to V_{SS}

Table 3 Pin Definitions and Functions (cont'd)

	Pin	Symbol	Type	Function
	50	TP2	I	**Test Pin 2.** Used for factory device test. Tie to V_{SS}
	56, 57, 58	res		**Reserved**

1) This function of pin $\overline{EAW}$ is different to that defined in Ref. [14]

I: Input

O: Output (Push-Pull)

OD: Output (Open Drain)

1.8.1 Specific Pins

LED Pin $\overline{ACT}$

A LED can be connected to pin **$\overline{ACT}$** to display four different states (off, slow flashing, fast flashing, on). It displays the activation status of the U- and S-transceiver according to **Table 4**. or it is programmable via two bits (LED1 and LED2 in register MODE2).

Table 4 ACT States

Pin $\overline{ACT}$	LED	U_Deactivated	U_Activated	S_Activated
V_{DD}	off	1	x	x
8Hz	8Hz	0	0	x
1Hz	1Hz	0	1	0
GND	on	0	1	1

with:

U_Deactivated: 'Deactivated State' as defined in **Chapter 2.4.10.5**. If the 'Simplified State Machine' is selected: 'Deactivated State' and 'IOM®-2 Awaked'.

U_Activated: 'Synchronized 1', 'Synchronized 2', 'Wait for ACT', 'Transparent', 'Error S/T', 'Pend. Deact. S/T', 'Pend. Deact. U' as defined in **Chapter 2.4.10.5**.

S-Activated: 'Activated State' as defined in **Chapter 2.5.5**.

Note: Optionally, pin $\overline{ACT}$ can drive a second LED with inverse polarity (connect this additional LED to 3.3 V only).

Test Modes

The test patterns on the S-interface (‘2 kHz Single Pulses‘, ‘96 kHz Continuous Pulses‘) and on the U-interface (‘Data Through‘, ‘Send Single Pulses‘) are invoked via C/I codes (TM1, TM2, DT, SSP). Setting SRES.RES_U to ‘1‘ forces the U-transceiver into test mode ‘Quiet Mode‘ (QM), i.e. the U-transceiver is hardware reset.

1.9 System Integration

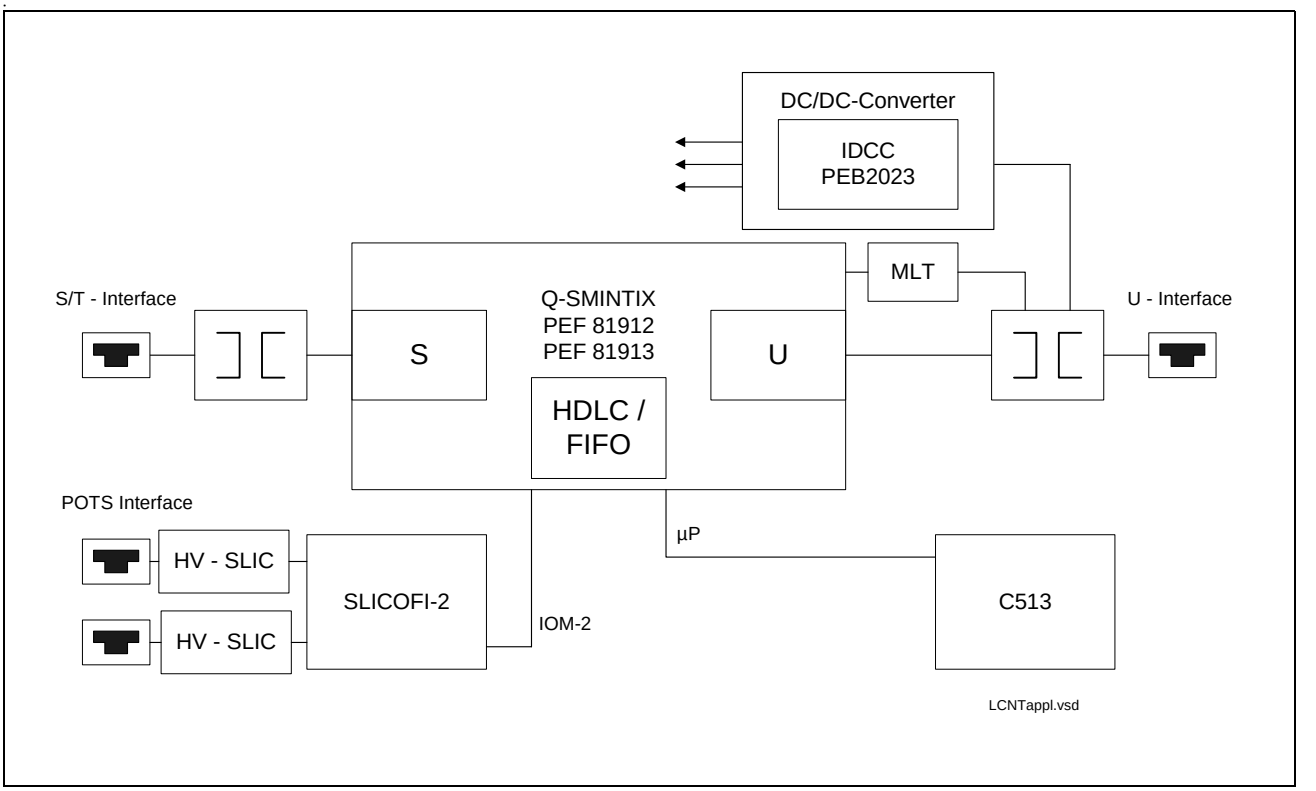


Figure 3 Application Example Q-SMINT®IX: Low Cost Intelligent NT

The U-transceiver, S-transceiver, the IOM®-2 channels and the HDLC-controller can be controlled and monitored via:

a) the parallel or serial microprocessor interface
- Access of on-chip registers via µP interface Address/Data format
- Activation/Deactivation control of U- and S-transceiver via µP interface and C/I handler
- Q-SMINT®IX is Monitor channel master
- TIC bus is transparent on IOM®-2-interface and is used for D-channel arbitration between S-transceiver, on-chip and off-chip HDLC controllers.

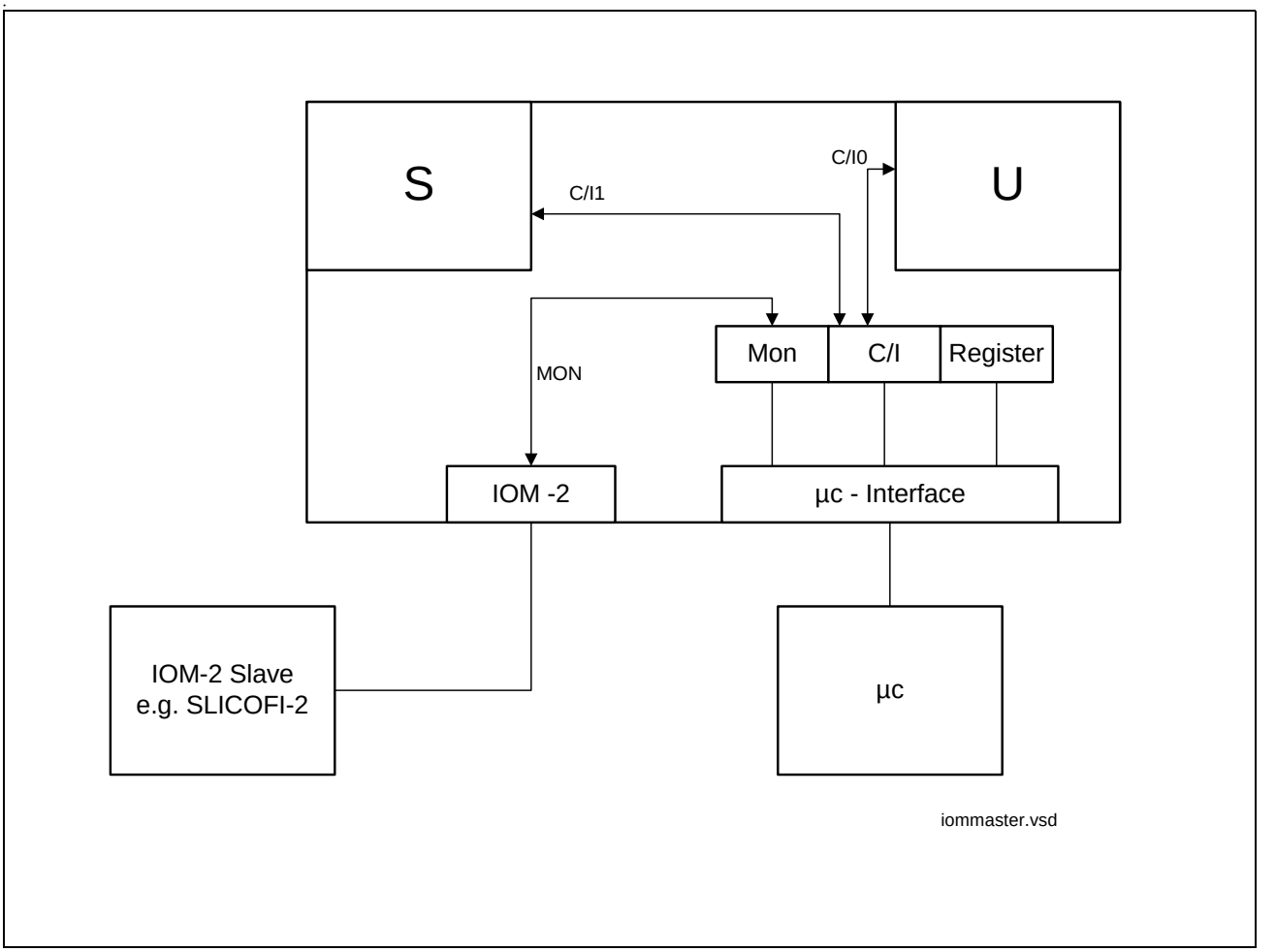


Figure 4 Control via µP Interface

Alternatively, the Q-SMINT®IX can be controlled via

b) the IOM®-2 Interface

- Access of on-chip registers via the Monitor channel with Header/Address/Data format (Device is Monitor slave)
- Activation/Deactivation control of U- and S-transceiver via the C/I channels CI0 and CI1
- TIC bus is transparent on IOM®-2-interface and is used for D-channel arbitration between S-transceiver, on-chip and off-chip HDLC controllers.

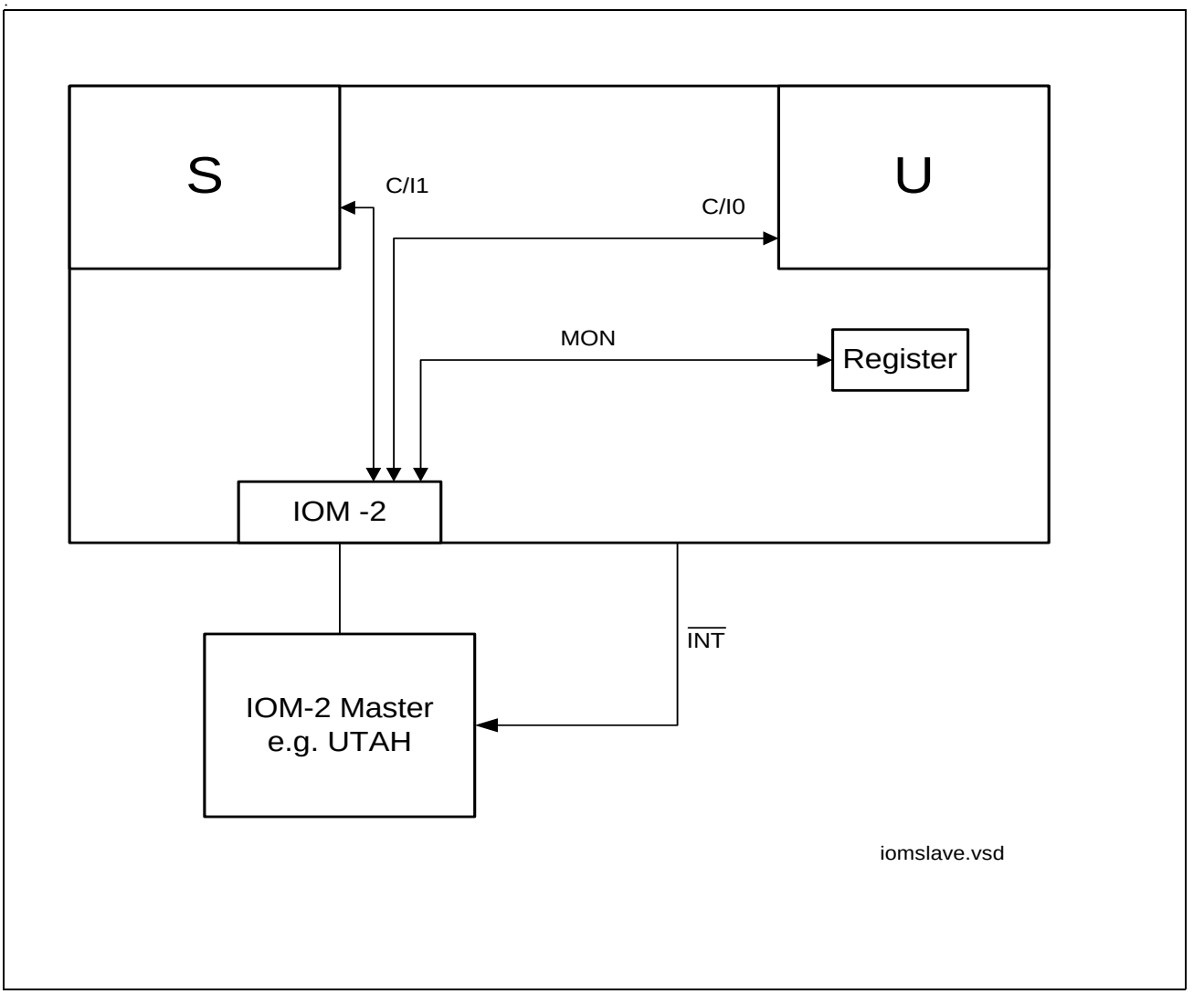


Figure 5 Control via IOM®-2 Interface

2 Functional Description

2.1 Microcontroller Interfaces

The Q-SMINT®IX supports either a serial or a parallel microcontroller interface. For applications where no controller is connected to the Q-SMINT®IX microcontroller interface, register programming is done via the IOM®-2 MONITOR channel from a master device. In such applications the Q-SMINT®IX operates in the IOM®-2 slave mode (refer to the corresponding chapter of the IOM®-2 MONITOR handler).
The interface selections are all done by pinstrapping. The possible interface selections are listed in **Table 5**. The selection pins are evaluated when the reset input $\overline{RST}$ is released. For the pin levels stated in the tables the following is defined:
'High':dynamic pin value which must be 'High' when the pin level is evaluated
V_{DD}, V_{SS}:static 'High' or 'Low' level (tied to V_{DD}, V_{SS})

Table 5 Interface Selection for the Q-SMINT®IX

PINS		Serial /Parallel Interface	PINS		Interface Type/Mode
WR (R/W)	RD (DS)		CS	ALE	
'High'	'High'	**Parallel**	'High'	V_{DD}	Motorola
				V_{SS}	Siemens/Intel Non-Mux
				edge	Siemens/Intel Mux
V_{SS}	V_{SS}	**Serial**	'High'	V_{SS}	Serial Control Interface(SCI)
			V_{SS}	V_{SS}	IOM®-2 MONITOR Channel (Slave Mode)

Note: For a selected interface mode which does not require all pins (e.g. address pins) the unused pins must be tied to V_{DD}.

The microcontroller interface also consists of a microcontroller clock generation at pin MCLK, an interrupt request at pin $\overline{INT}$, a reset input pin $\overline{RST}$ and a reset output pin $\overline{RSTO}$.
The interrupt request pin $\overline{INT}$ (open drain output) becomes active if the Q-SMINT®IX requests an interrupt.

2.1.1 Serial Control Interface (SCI)

The serial control interface (SCI) is compatible to the SPI interface of Motorola and to the Siemens C510 family of microcontrollers.
The SCI consists of 4 lines: SCLK, SDX, SDR and $\overline{CS}$. Data is transferred via the lines SDR and SDX at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of a serial access to the registers. The Q-SMINT®IX latches incoming data at the rising edge of SCLK and shifts out at the falling edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. Data is transferred in groups of 8 bits with the MSB first.

Pad mode of SDX can be selected ’open drain’ or ’push-pull’ by programming MODE2.PPSDX.

Figure 6 shows the timing of a one byte read/write access via the serial control interface.

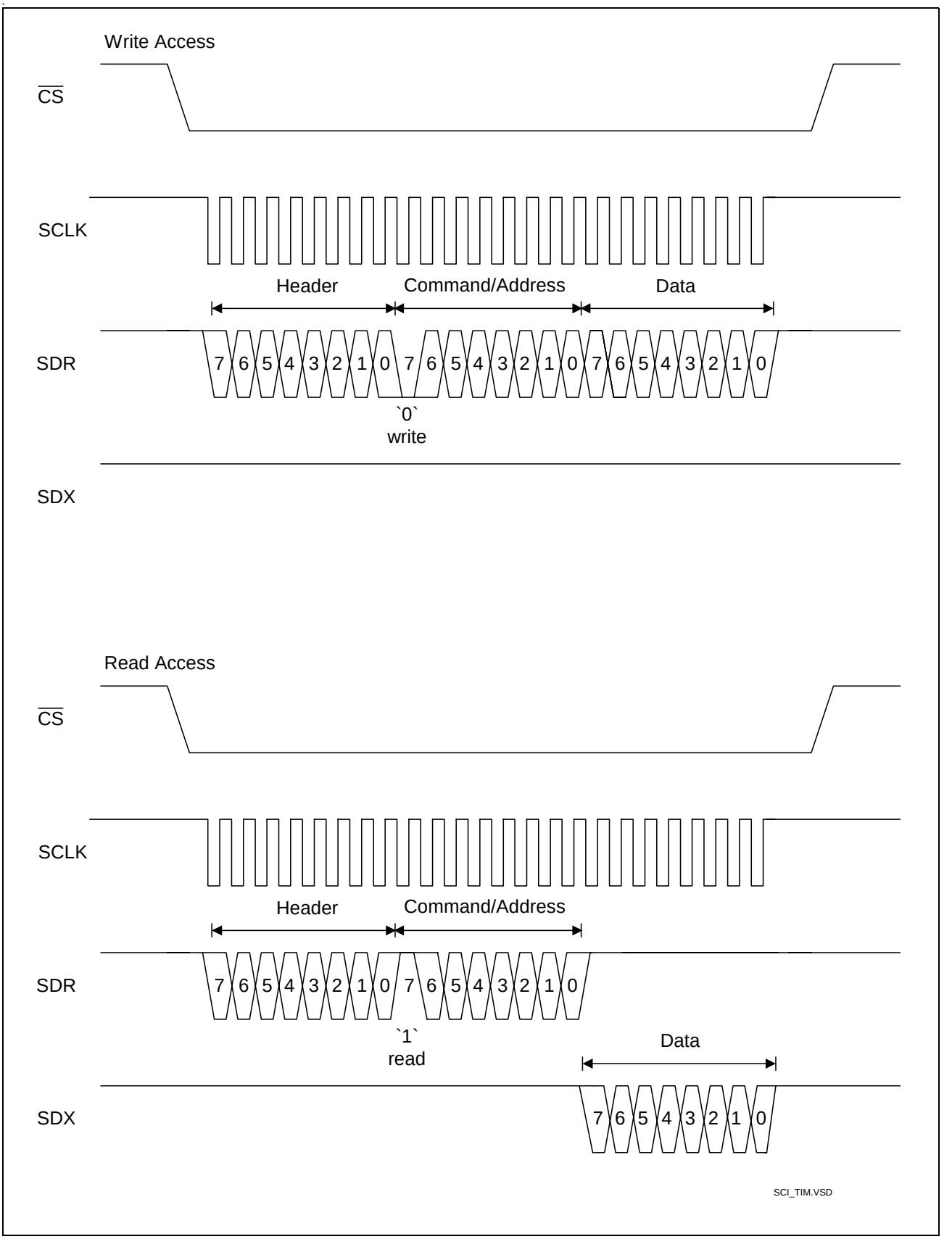


Figure 6 Serial Control Interface Timing

2.1.1.1 Programming Sequences

The basic structure of a read/write access to the Q-SMINT®IX registers via the serial control interface is shown in **Figure 7**.

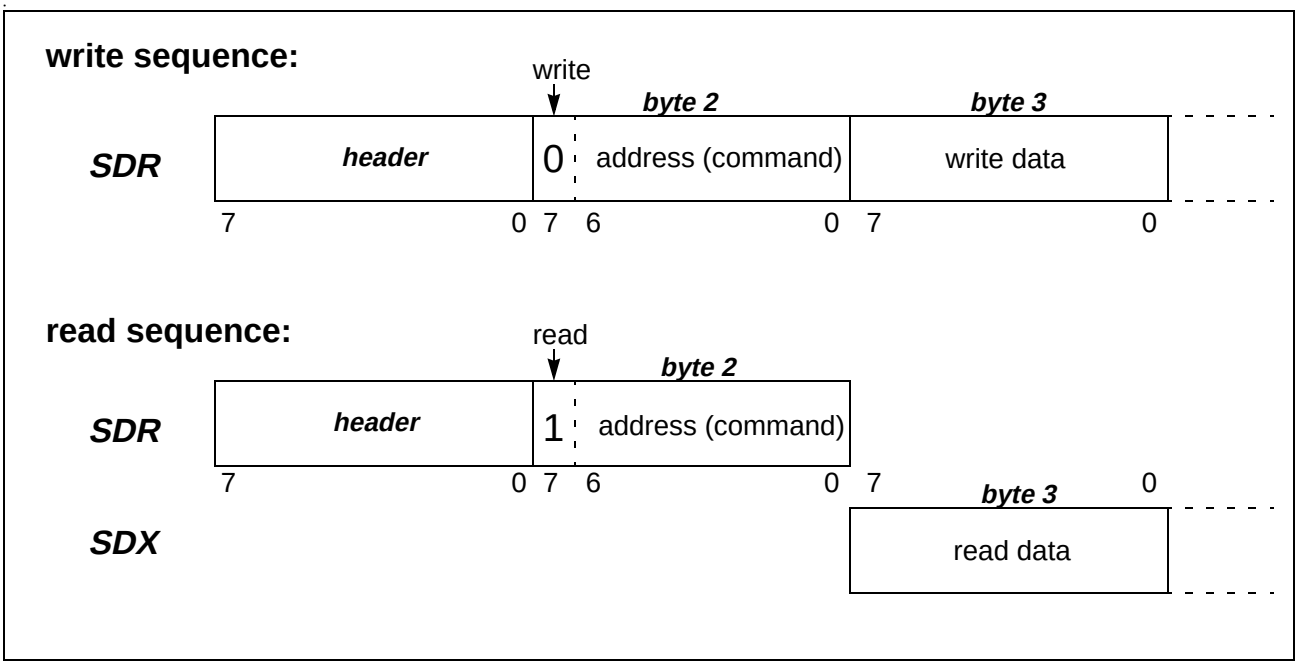


Figure 7 Serial Command Structure

A new programming sequence starts with the transfer of a header byte. The header byte specifies different programming sequences allowing a flexible and optimized access to the individual functional blocks of the Q-SMINT®IX.
The possible sequences are listed in **Table 6** and are described after that.

Table 6 Header Byte Code

Header Byte	Sequence	Sequence Type	Access to
40_H	Adr-Data-Adr-Data	non-interleaved	Address Range 00_H-$7F_H$
48_H		interleaved	
43_H	Adr-Data-Data-Data	Read-/Write-only	Address Range 00_H-$7F_H$
41_H		non-interleaved	
49_H		interleaved	

Header 40_H: Non-interleaved A-D-A-D Sequences

The non-interleaved A-D-A-D sequences give direct read/write access to the address range 00_H-$7F_H$ and can have any length. In this mode SDX and SDR can be connected together allowing data transmission on one line.
Example for a read/write access with header 40_H:

SDR	header	wradr	wrdata	rdadr		rdadr		wradr	wrdata	
SDX					rddata		rddata			

Header 48_H: Interleaved A-D-A-D Sequences

The interleaved A-D-A-D sequences give direct read/write access to the address range 00_H-$7F_H$ and can have any length. This mode allows a time optimized access to the registers by interleaving the data on SDX and SDR.
Example for a read/write access with header 48_H:

SDR	header	wradr	wrdata	rdadr	rdadr	wradr	wrdata			
SDX					rddata	rddata				

Header 43_H: Read-/Write- only A-D-D-D Sequence

This mode (header 43_H) can be used for a fast access to the HDLC FIFO data. Any address (rdadr, wradr) in the range between 00_H-$1F_H$ gives access to the current FIFO location selected by an internal pointer which is automatically incremented with every data byte following the first address byte. Generally, it can be used for any register access to the address range 00_H-$7D_H$. The sequence can have any length and is terminated by the rising edge of $\overline{CS}$.

Example for a write access with header 43_H:

SDR	header	wradr	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	
SDX										

Example for a read access with header 43_H:

SDR	header	rdadr								
SDX			rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	

Header 41_H: Non-interleaved A-D-D-D Sequence

This sequence (header 41_H) allows in front of the A-D-D-D write access a non-interleaved A-D-A-D read access. This mode is useful for reading status information before writing to the HDLC XFIFO. Generally, it can be used for any register access to the address range 00_H-$7D_H$. The termination condition of the read access is the reception of the wradr. The sequence can have any length and is terminated by the rising edge of $\overline{CS}$.

Example for a read/write access with header 41_H:

SDR	header	rdadr		rdadr		wradr	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)
SDX			rddata		rddata				

Header 49_H: Interleaved A-D-D-D Sequence

This sequence (header 49_H) allows in front of the A-D-D-D write access an interleaved A-D-A-D read access. This mode is useful for reading status information before writing to the HDLC XFIFO. Generally, it can be used for any register access to the address range 00_H-$7D_H$. The termination condition of the read access is the reception of the wradr. The sequence can have any length and is terminated by the rising edge of $\overline{CS}$.

Example for a read/write access with header 49_H:

SDR	header	rdadr	rdadr	wradr	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)		
SDX			rddata	rddata					

2.1.2 Parallel Microcontroller Interface

The 8-bit parallel microcontroller interface with address decoding on chip allows an easy and fast microcontroller access.

The parallel interface of the Q-SMINT®IX provides three types of µP busses which are selected via pin ALE. The bus operation modes with corresponding control pins are listed in **Table 7**.

Table 7 Bus Operation Modes

	Bus Mode	Pin ALE	Control Pins
(1)	Motorola	V_{DD}	$\overline{CS}$, R/$\overline{W}$, $\overline{DS}$
(2)	Siemens/Intel non-multiplexed	V_{SS}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$
(3)	Siemens/Intel multiplexed	Edge	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

Note: For a selected interface mode which does not require all pins (e.g. address pins) the unused pins must be tied to V_{DD}.

A read/write access to the Q-SMINT®IX registers can be done in **multiplexed or non-multiplexed** mode.
In non-multiplexed mode the register address must be applied to the address bus (A0-A6) for the data access via the data bus (D0-D7).
In multiplexed mode the address on the address bus (AD0-AD7) is latched in by ALE before a read/write access via the address/data bus is performed.

The Q-SMINT®IX provides two different ways to address the register contents which can be selected with the AMOD bit in the MODE2 register. The address mode after reset is the indirect address mode (AMOD = ’0’). Reprogramming into the direct address mode (AMOD = ’1’) has to take place in the indirect address mode. **Figure 8** illustrates both register addressing modes.

Direct address mode (AMOD = ’1’): The register address to be read or written is directly set in the way described above.

Indirect address mode (AMOD = ’0’):

- non-muxed: only the LSB of the address bus (A0)
- muxed: only the LSB of the address-data bus (AD0)

gets evaluated to address a virtual ADDRESS (0_H) and a virtual DATA (1_H) register.

Every access to a target register consists of:

- a write access (muxed or non-muxed) to ADDRESS to store the target register´s address, as well as
- a read access (muxed or non-muxed) from DATA to read from the target register or
- a write access (muxed or non-muxed) to DATA to write to the target register

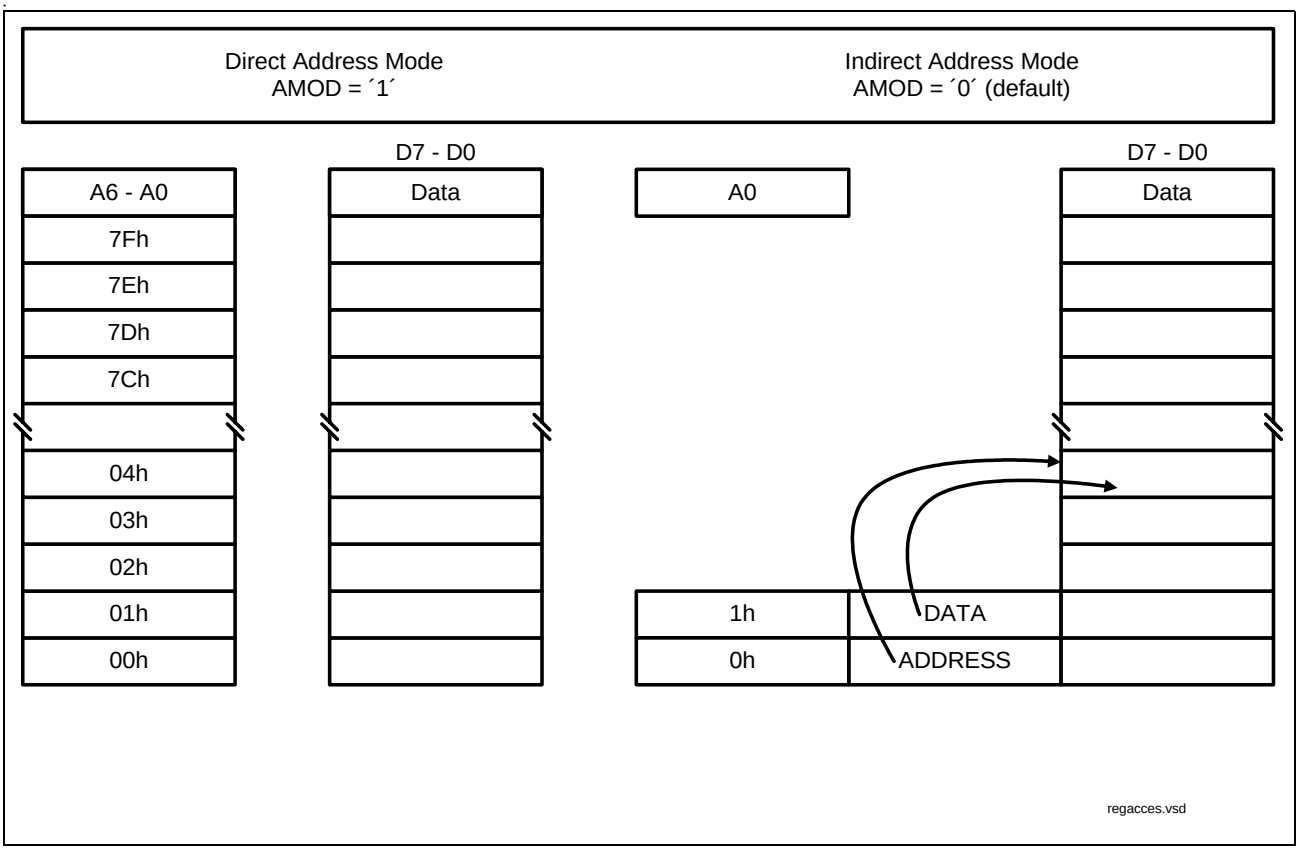


Figure 8 Direct/Indirect Register Address Mode

2.1.3 Microcontroller Clock Generation

The microcontroller clock is derived from the unregulated 15.36 MHz clock from the oscillator and provided by the pin MCLK. Five clock rates are selectable by a programmable prescaler which is controlled by the bits MODE1.MCLK and MODE1.CDS corresponding to the following table.

Table 8 MCLK Frequencies

MODE1. MCLK Bits		MCLK frequency with MODE1.CDS = ’0’	MCLK frequency with MODE1.CDS = ’1’
0	0	3.84 MHz	7.68 MHz
0	1	0.96 MHz	1.92 MHz
1	0	7.68 MHz	15.36 MHz
1	1	disabled	disabled

The clock rate is changed after $\overline{CS}$ becomes inactive.

2.2 Reset Generation

Figure 9 shows the organization of the reset generation of the Q-SMINT®IX.

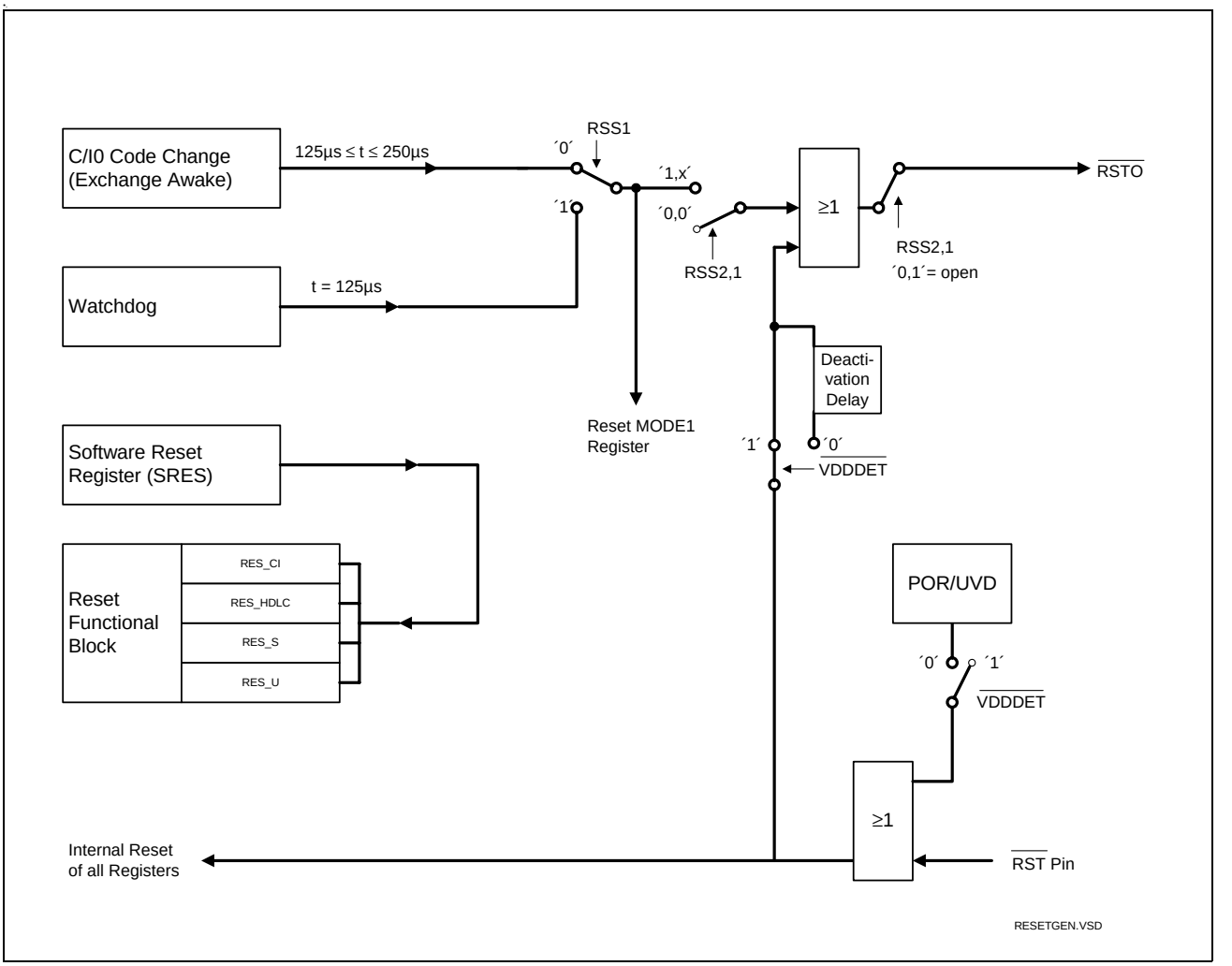


Figure 9 Reset Generation of the Q-SMINT®IX[1)]

Reset Source Selection

The internal reset sources C/I code change and Watchdog timer can be output at the low active reset pin $\overline{\text{RSTO}}$. These reset sources can be selected with the RSS2,1 bits in the MODE1 register according to **Table 9**.

1) The 'OR'-gates shall illustrate in a symbolic way, that 'source A active' or 'source B active' is forwarded. The real polarity of the different sources is not considered.

The internal reset sources set the MODE1 register to its reset value.

Table 9 Reset Source Selection

RSS2 Bit 1	RSS1 Bit 0	C/I Code Change	Watchdog Timer	POR/UVD[1] and $\overline{\text{RST}}$
0	0	--	--	x
0	1	/RSTO disabled (= high impedance)		
1	0	x	--	x
1	1	--	x	x

1) POR/UVD can be enabled/disabled via pin $\overline{\text{VDDDET}}$

- **C/I Code Change (Exchange Awake)**
  A change in the downstream C/I channel (C/I0) generates a reset pulse of 125 µs ≤ t ≤ 250 µs.
- **Watchdog Timer**

After the selection of the watchdog timer (RSS = ’11’) an internal timer is reset and started. During every time period of 128 ms the microcontroller has to program the WTC1- and WTC2 bits in the following sequence to reset and restart the watchdog timer:

	WTC1	WTC2
1.	1	0
2.	0	1

Otherwise the timer expires and a WOV-interrupt (ISTA Register) together with a reset out pulse on pin $\overline{\text{RSTO}}$ of 125 µs is generated.
Deactivation of the watchdog timer is only possible with a hardware reset (including expiration of the watchdog timer).

As in the SCOUT-S, the watchdog timer is clocked with the IOM®-2 clocks and works only if the internal IOM®-2 clocks are active. Hence, the power consumption is minimized in state power down.

Software Reset Register (SRES)

Several main functional blocks of the Q-SMINT®IX can be reset separately by software setting the corresponding bit in the SRES register. This is equivalent to a hardware reset of the corresponding functional block. The reset state is activated as long as the bit is set to ’1’.

External Reset Input

At the $\overline{RST}$ input an external reset can be applied forcing the Q-SMINT®IX in the reset state. This external reset signal is additionally fed to the $\overline{RSTO}$ output.

After release of an external reset, the µC has to wait for min. $t_{\mu C}$ before it starts read or write access to the Q-SMINT®IX (see **Table 45**).

Reset Ouput

If $\overline{VDDDET}$ is active, then the deactivation of a reset output on $\overline{RSTO}$ is delayed by t_{DEACT} (see **Table 46**).

Reset Generation

The Q-SMINT®IX has an on-chip reset generator based on a Power-On Reset (POR) and Under Voltage Detection (UVD) circuit (see **Table 46**). The POR/UVD requires no external components.

The POR/UVD circuit can be disabled via pin $\overline{VDDDET}$.

The requirements on V_{DD} ramp-up during power-on reset are described in **Chapter 5.6.5**.

Clocks and Data Lines During Reset

During reset the data clock (DCL), the bit clock (BCL), the microcontroller clock[1)] (MCLK) and the frame synchronization (FSC) keep running.

During reset DD and DU are high; with the exception of:

- The output C/I code from the U-Transceiver on DD IOM®-2 channel 0 is 'DR' = 0000 (Value after reset of register UCIR = '00_H')
- The output C/I code from the S-Transceiver on DU IOM®-2 channel 1 is 'TIM' = 0000.

1) during a Power-On/UVD Reset, the microcontroller clock MCLK is not running, but starts running as soon as timer t_{DEAC} is started.

2.3 IOM®-2 Interface

The Q-SMINT®IX supports the IOM®-2 interface in terminal mode (DCL=1.536 MHz) according to the IOM®-2 Reference Guide [13].

2.3.1 IOM®-2 Functional Description

The IOM®-2 interface consists of four lines: FSC, DCL, DD, DU and optionally BCL. The rising edge of FSC indicates the start of an IOM®-2 frame. The DCL and the BCL clock signals synchronize the data transfer on both data lines DU and DD. The DCL is twice the bit rate, the BCL rate is equal to the bit rate. The bits are shifted out with the rising edge of the first DCL clock cycle and sampled at the falling edge of the second clock cycle. With BCL the bits are shifted out with the rising edge and sampled with the falling edge of the single clock cycle.

The IOM®-2 interface can be enabled/disabled with the DIS_IOM bit in the IOM_CR register.

The FSC signal is an 8 kHz frame sync signal. The number of PCM timeslots on the receive and transmit lines is determined by the frequency of the DCL clock (or BCL), with the 1.536 MHz (BCL=768 kHz) clock 3 channels consisting of 4 timeslots each are available.

IOM®-2 Frame Structure of the Q-SMINT®IX

The frame structure on the IOM®-2 data ports (DU,DD) of the Q-SMINT®IX with a DCL clock of 1.536 MHz (or BCL=768 kHz) and if TIC bus is not disabled (IOM_CR.TIC_DIS) is shown in **Figure 10.**

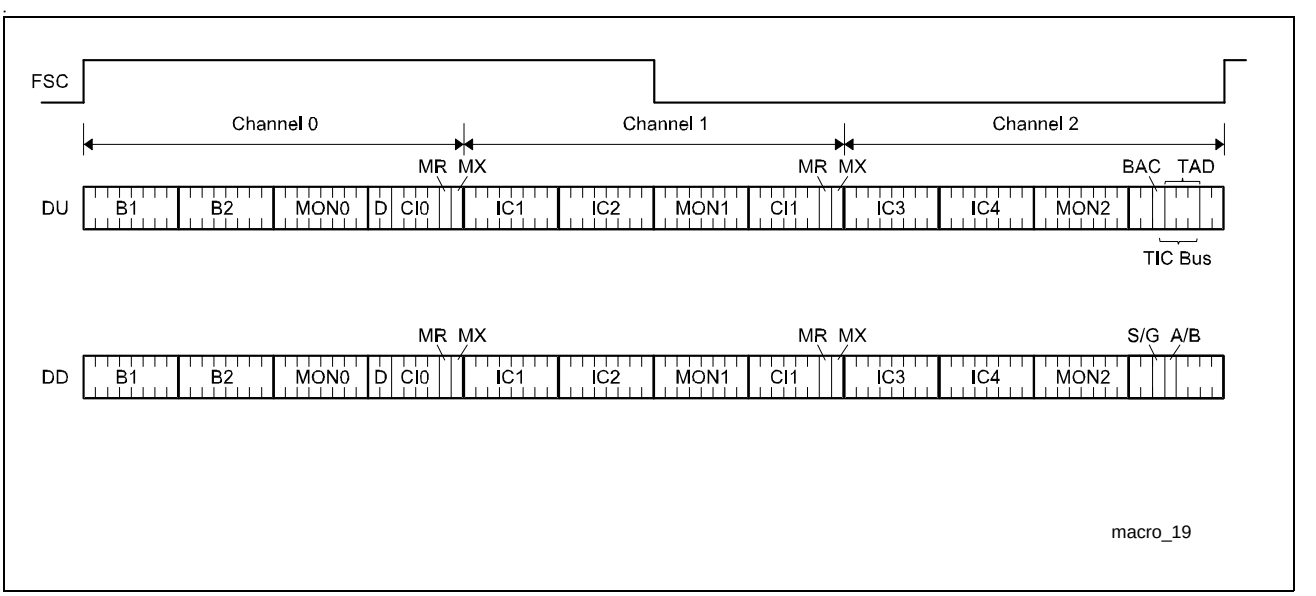


Figure 10 IOM®-2 Frame Structure of the Q-SMINT®IX

The frame is composed of three channels

- Channel 0 contains 144-kbit/s of user and signaling data (2B + D), a MONITOR programming channel (MON0) and a command/indication channel (CI0) for control and programming of e.g. the U-transceiver.
- Channel 1 contains two 64-kbit/s intercommunication channels (IC), a MONITOR programming channel (MON1) and a command/indication channel (CI1) for control and programming of e.g. the S-transceiver.
- Channel 2 is used for D-channel access mechanism (TIC-bus, S/G bit). Additionally, channel 2 supports further IC and MON channels.

2.3.2 IOM®-2 Handler

The IOM®-2 handler offers a great flexibility for handling the data transfer between the different functional units of the Q-SMINT®IX and voice/data devices connected to the IOM®-2 interface. Additionally it provides a microcontroller access to all time slots of the IOM®-2 interface via the four controller data access registers (CDA).

The PCM data of the functional units

- S-transceiver (S) and the
- Controller data access (CDA)

can be configured by programming the time slot and data port selection registers (TSDP). With the TSS bits (Time Slot Selection) the PCM data of the functional units can be assigned to each of the 12 PCM time slots of the IOM®-2 frame. With the DPS bit (Data Port Selection) the output of each functional unit is assigned to DU or DD respectively. The input is assigned vice versa. With the control registers (CR) the access to the data of the functional units can be controlled by setting the corresponding control bits (EN, SWAP).

The IOM®-2 handler also provides access to the

- U and S transceiver
- MONITOR channel
- C/I channels (CI0,CI1)
- TIC bus (TIC) and
- D- and/or B-channel for HDLC control

The access to these channels is controlled by the registers S_CR, HCI_CR and MON_CR.
The IOM®-2 interface with the two Serial Data Strobes (SDS1,2) is controlled by the control registers IOM_CR, SDS1_CR and SDS2_CR.

The following **Figure 11** shows the architecture of the IOM®-2 handler.

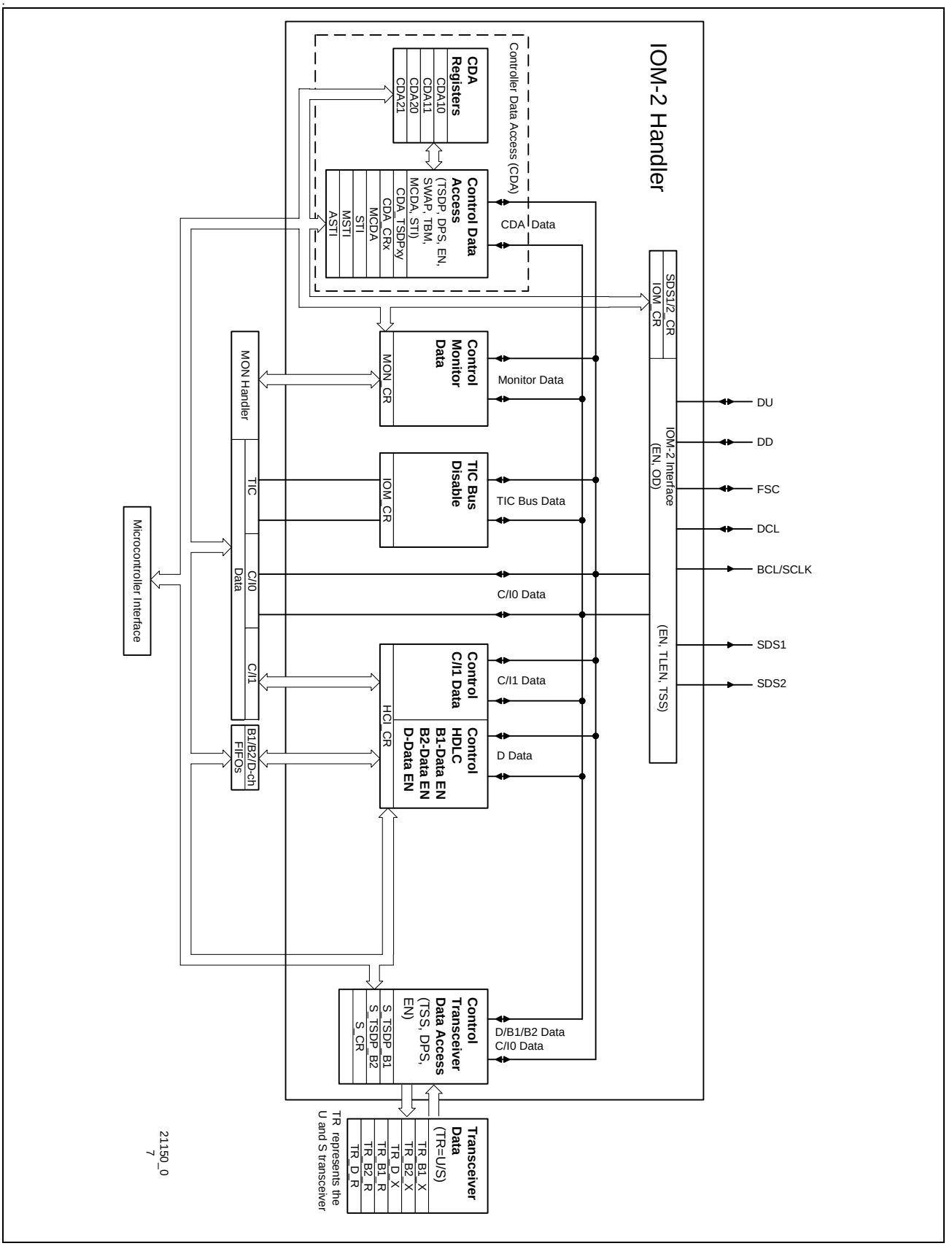


Figure 11 Architecture of the IOM®-2 Handler

2.3.2.1 Controller Data Access (CDA)

The four controller data access registers (CDA10, CDA11, CDA20, CDA21) provide microcontroller access to the 12 IOM®-2 time slots and more:

- looping of up to four independent PCM channels from DU to DD or vice versa over the four CDA registers
- shifting or switching of two independent PCM channels to another two independent PCM channels on both data ports (DU, DD). Between reading and writing the data can be manipulated (processed with an algorithm) by the microcontroller. If this is not the case a switching function is performed.
- monitoring of up to four time slots on the IOM®-2 interface simultaneously
- microcontroller read and write access to each PCM channel

The access principle, which is identical for the two channel register pairs CDA10/11 and CDA20/21, is illustrated in **Figure 12**. The index variables x,y used in the following description can be 1 or 2 for x, and 0 or 1 for y. The prefix 'CDA_' from the register names has been omitted for simplification.

To each of the four CDAxy data registers a TSDPxy register is assigned by which the time slot and the data port can be determined. With the TSS (Time Slot Selection) bits a time slot from 0...11 can be selected. With the DPS (Data Port Selection) bit the output of the CDAxy register can be assigned to DU or DD respectively. The time slot and data port for the output of CDAxy is always defined by its own TSDPxy register. The input of CDAxy depends on the SWAP bit in the control registers CRx.
If the SWAP bit = '0' (swap is disabled) the time slot and data port for the input and output of the CDAxy register is defined by its own TSDPxy register.
If the SWAP bit = '1' (swap is enabled) the input port and time slot of the CDAx0 is defined by the TSDP register of CDAx1 and the input port and time slot of CDAx1 is defined by the TSDP register of CDAx0. The input definition for time slot and data port CDAx0 are thus swapped to CDAx1 and for CDAx1 swapped to CDAx0. The output timeslots are not affected by SWAP.

The input and output of every CDAxy register can be enabled or disabled by setting the corresponding EN (-able) bit in the control register CDAx_CR. If the input of a register is disabled the output value in the register is retained.

Usually one input and one output of a functional unit (transceiver, HDLC controller, CDA register) is programmed to a timeslot on IOM®-2 (e.g. for B-channel transmission in upstream direction the S-transceiver writes data onto IOM®-2 and the U-transceiver reads data from IOM®-2). For monitoring data in such cases a CDA register is programmed as described below under "Monitoring Data". Besides that none of the IOM®-2 timeslots must be assigned more than one input and output of any functional unit.

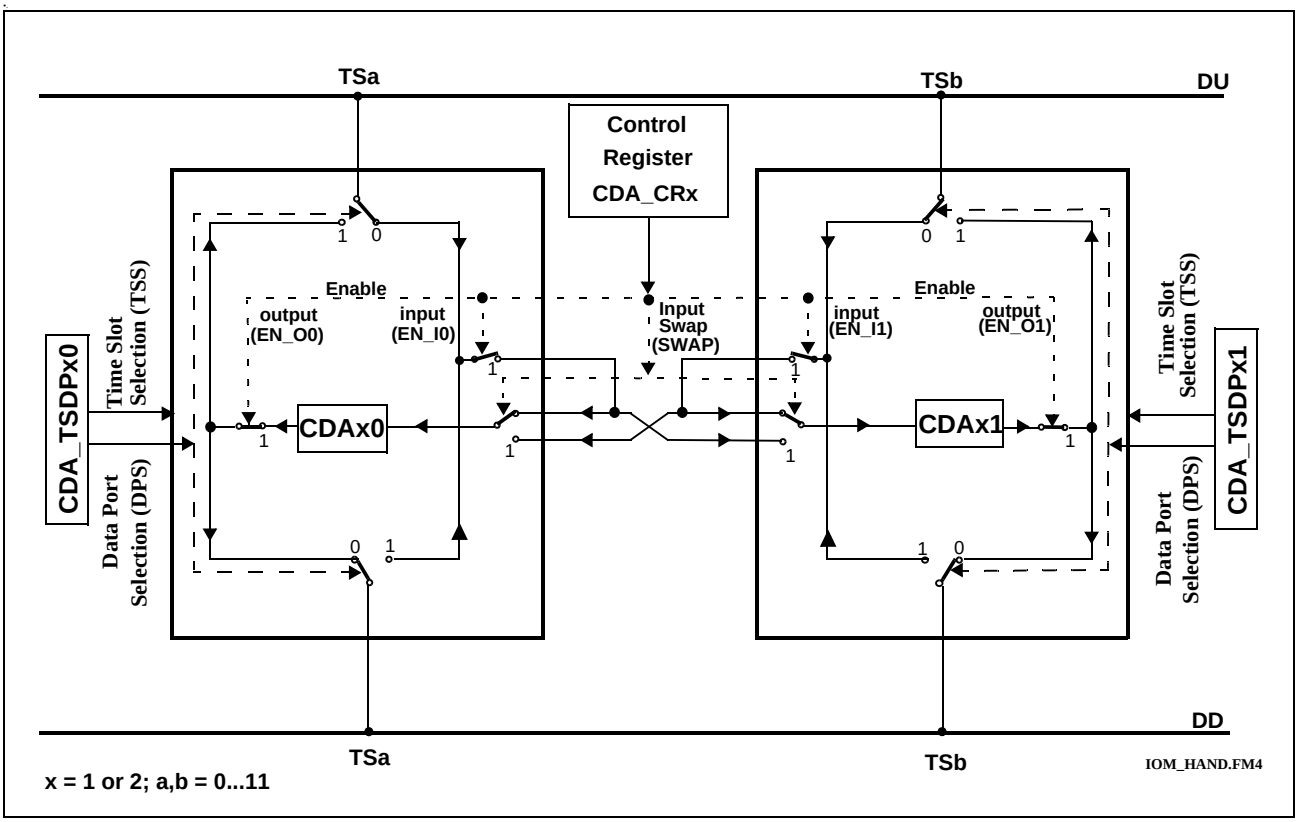


Figure 12 Data Access via CDAx0 and CDAx1 register pairs

Looping and Shifting Data

Figure 13 gives examples for typical configurations with the above explained control and configuration possibilities with the bits TSS, DPS, EN and SWAP in the registers TSDPxy or CDAx_CR:

a) looping IOM®-2 time slot data from DU to DD or vice versa (SWAP = ’0’)

b) shifting data from TSa to TSb and TSc to TSd in both transmission directions (SWAP = ’1’)

c) switching data from TSa to TSb and looping from DU to DD or switching TSc to TSd and looping from DD to DU .

TSa is programmed in TSDP10, TSb in TSDP11, TSc in TSDP20 and TSd in TSDP21.

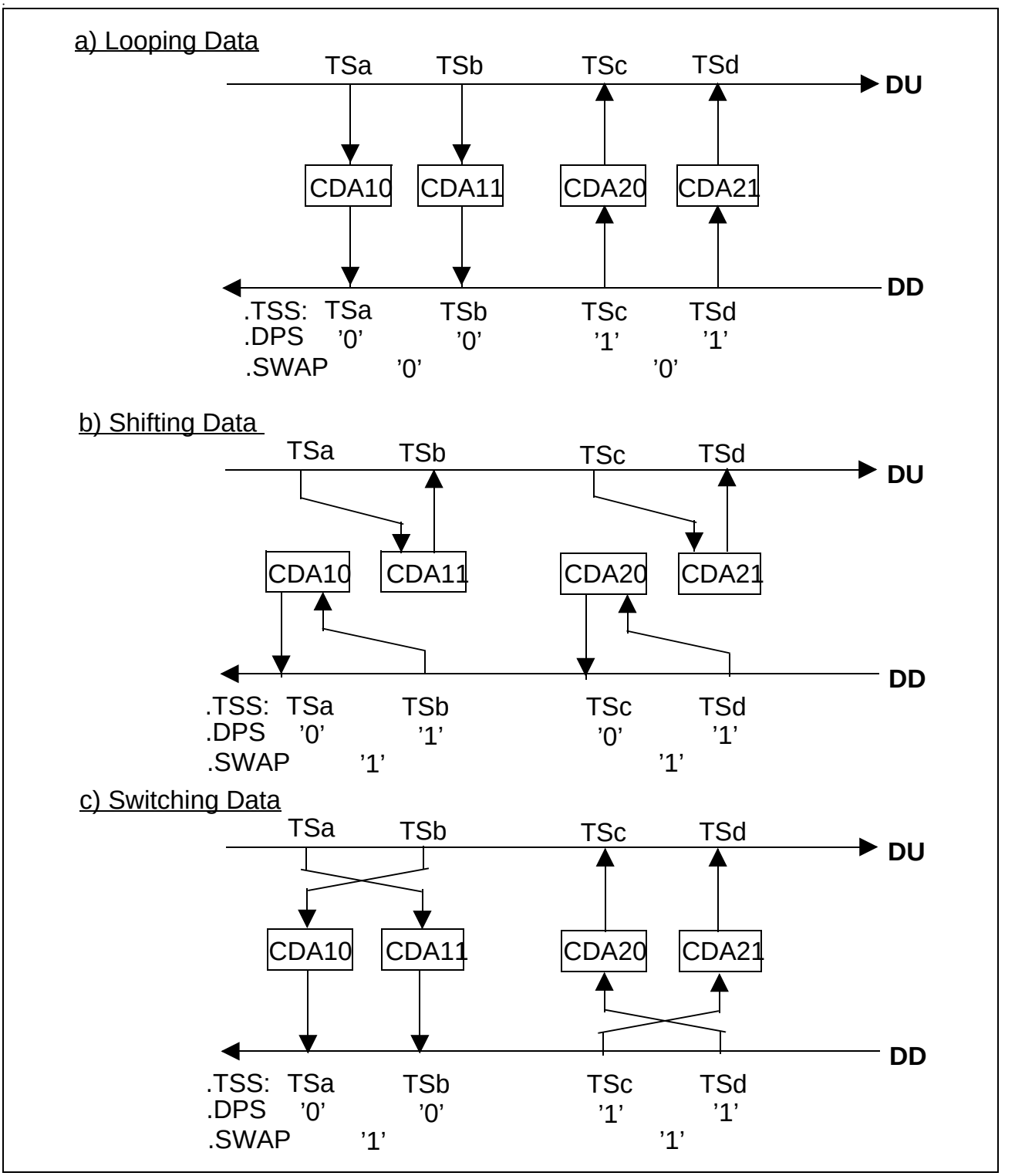


Figure 13 Examples for Data Access via CDAxy Registers

a) Looping Data
b) Shifting (Switching) Data
c) Switching and Looping Data

Figure 14 shows the timing of looping TSa from DU to DD via CDAxy register. TSa is read in the CDAxy register from DU and is written one frame later on DD.

Figure 15 shows the timing of shifting data from TSa to TSb on DU(DD). In **Figure 15**a) shifting is done in one frame because TSa and TSb didn't succeed directly one another (a = 0...9 and b ≥ a+2). In **Figure 15**b) shifting is done from one frame to the following frame. This is the case when the time slots succeed one other (b = a+1) or b is smaller than a (b < a).

At looping and shifting the data can be accessed by the controller between the synchronous transfer interrupt (STI) and the status overflow interrupt (STOV). STI and STOV are explained in the section 'Synchronous Transfer'. If there is no controller intervention the looping and shifting is done autonomously.

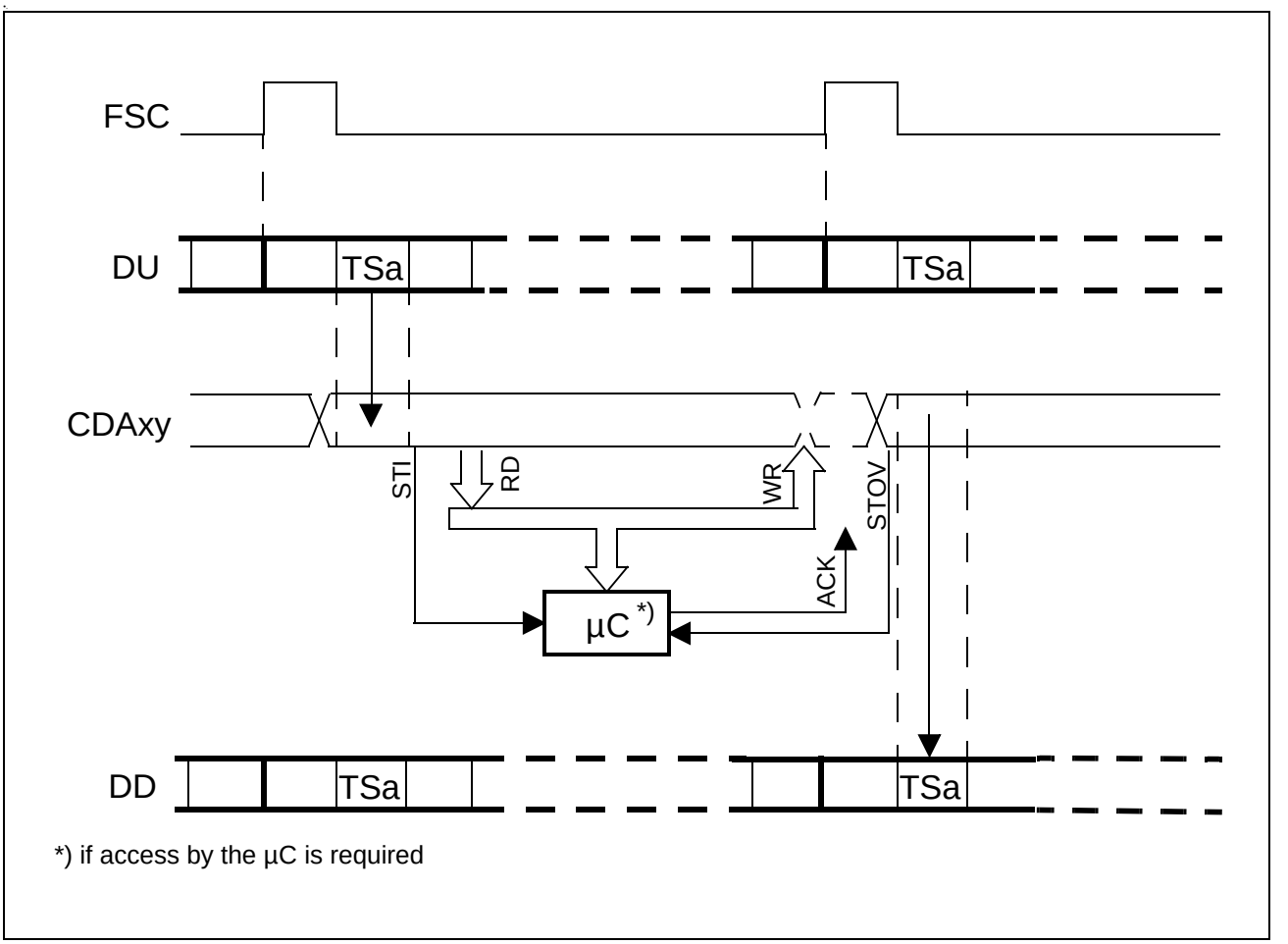


Figure 14 Data Access when Looping TSa from DU to DD

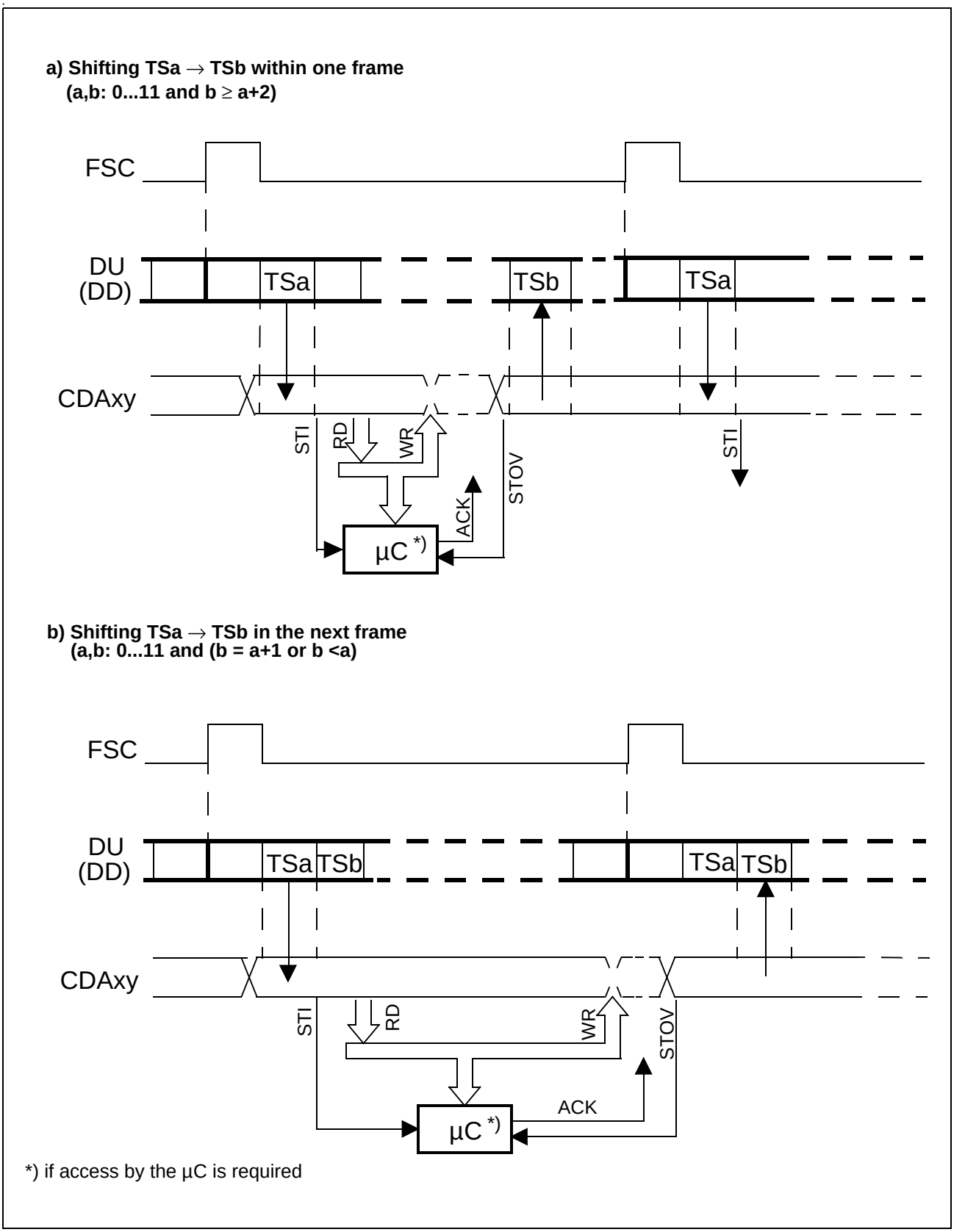


Figure 15 Data Access when Shifting TSa to TSb on DU (DD)

Monitoring Data

Figure 16 gives an example for monitoring of two IOM®-2 time slots each on DU or DD simultaneously. For monitoring on DU and/or DD the channel registers with even numbers (CDA10, CDA20) are assigned to time slots with even numbers TS(2n) and the channel registers with odd numbers (CDA11, CDA21) are assigned to time slots with odd numbers TS(2n+1). The user has to take care of this restriction by programming the appropriate time slots.

This mode is only valid if two blocks (e.g. both transceivers) are programmed to these timeslots and communicating via IOM®-2.

However, if only one block is programmed to this timeslot the timeslots for CDAx0 and CDAx1 can be programmed completely independently.

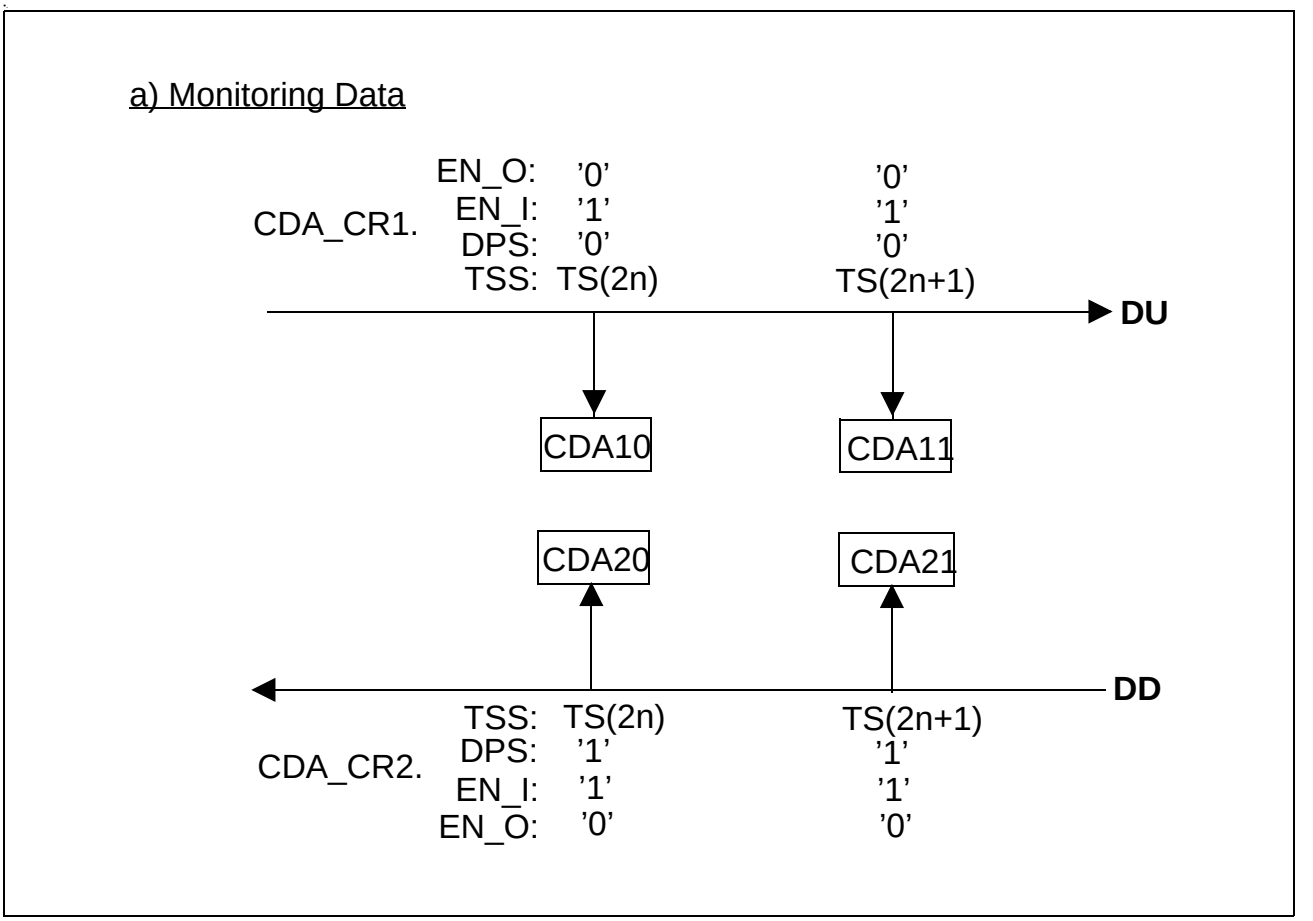


Figure 16 Example for Monitoring Data

Monitoring TIC Bus

Monitoring the TIC bus (TS11) is handled as a special case. The TIC bus can be monitored with the registers CDAx0 by setting the EN_TBM (Enable TIC Bus Monitoring) bit in the control registers CRx. The TSDPx0 must be set to 08_h for monitoring from DU or 88_h for monitoring from DD. By this it is possible to monitor the TIC bus (TS11) and the odd numbered D-channel (TS3) simultaneously on DU and DD.

Synchronous Transfer

While looping, shifting and switching the data can be accessed by the controller between the synchronous transfer interrupt (STI) and the synchronous transfer overflow interrupt (STOV).

The microcontroller access to each of the CDAxy registers can be synchronized by means of four programmable synchronous transfer interrupts (STIxy)[1] and synchronous transfer overflow interrupts (STOVxy)[2] in the STI register.
Depending on the DPS bit in the corresponding TSDPxy register the STIxy is generated two (for DPS='0') or one (for DPS='1') BCL clock after the selected time slot (CDA_TSDPxy.TSS). One BCL clock is equivalent to two DCL clocks.
In the following description the index xy_0 and xy_1 are used to refer to two different interrupt pairs (STI/STOV) out of the four CDA interrupt pairs (STI10/STOV10, STI11/ STOV11, STI20/STOV20, STI21/STOV21).

A $STOVxy_0$ is related to its $STIxy_0$ and is only generated if $STIxy_0$ is enabled and not acknowledged. However, if $STIxy_0$ is masked, the STOVxy0 is generated for any other STIxy1 which is enabled and not acknowledged.

Table 10 gives some examples for that. It is assumed that a STOV interrupt is only generated because a STI interrupt was not acknowledged before.

In example 1 only the $STIxy_0$ is enabled and thus $STIxy_0$ is only generated. If no STI is enabled, no interrupt will be generated even if STOV is enabled (example 2).
In example 3 $STIxy_0$ is enabled and generated and the corresponding $STOVxy_0$ is disabled. $STIxy_1$ is disabled but its $STOVxy_1$ is enabled, and therefore $STOVxy_1$ is generated due to $STIxy_0$. In example 4 additionally the corresponding $STOVxy_0$ is enabled, so $STOVxy_0$ and $STOVxy_1$ are both generated due to $STIxy_0$.
In example 5 additionally the $STIxy_1$ is enabled with the result that $STOVxy_0$ is only generated due to $STIxy_0$ and $STOVxy_1$ is only generated due to $STIxy_1$.

Compared to the previous example $STOVxy_0$ is disabled in example 6, so $STOVxy_0$ is not generated and $STOVxy_1$ is only generated for $STIxy_1$ but not for $STIxy_0$.

---

1) In order to enable the STI interrupts the input of the corresponding CDA register has to be enabled. This is also valid if only a synchronous write access is wanted. The enabling of the output alone does not effect an STI interrupt.

2) In order to enable the STOV interrupts the output of the corresponding CDA register has to be enabled. This is also valid if only a synchronous read access is wanted. The enabling of the input alone does not effect an interrupt.

Table 10 Examples for Synchronous Transfer Interrupts

Enabled Interrupts (Register MSTI)		Generated Interrupts (Register STI)		
STI	**STOV**	**STI**	**STOV**	
xy_0	-	xy_0	-	Example 1
-	xy_0	-	-	Example 2
xy_0	xy_1	xy_0	xy_1	Example 3
xy_0	xy_0 ; xy_1	xy_0	xy_0 ; xy_1	Example 4
xy_0 ; xy_1	xy_0 ; xy_1	xy_0 xy_1	xy_0 xy_1	Example 5
xy_0 ; xy_1	xy_1	xy_0 xy_1	- xy_1	Example 6
xy_0 ; xy_1	xy_0 ; xy_1 ; xy_2	xy_0 xy_1	xy_0 ; xy_2 xy_1 ; xy_2	Example 7

Compared to example 5 in example 7 a third STOVxy_2 is enabled and thus STOVxy2 is generated additionally for both STIxy_0 and STIxy_1.

A STOV interrupt is not generated if all stimulating STI interrupts are acknowledged.

A STIxy must be acknowledged by setting the ACKxy bit in the ASTI register two BCL clock (for DPS='0') or one BCL clocks (for DPS='1') before the time slot which is selected for the appropriate STIxy. The interrupt structure of the synchronous transfer is shown in **Figure 17**.

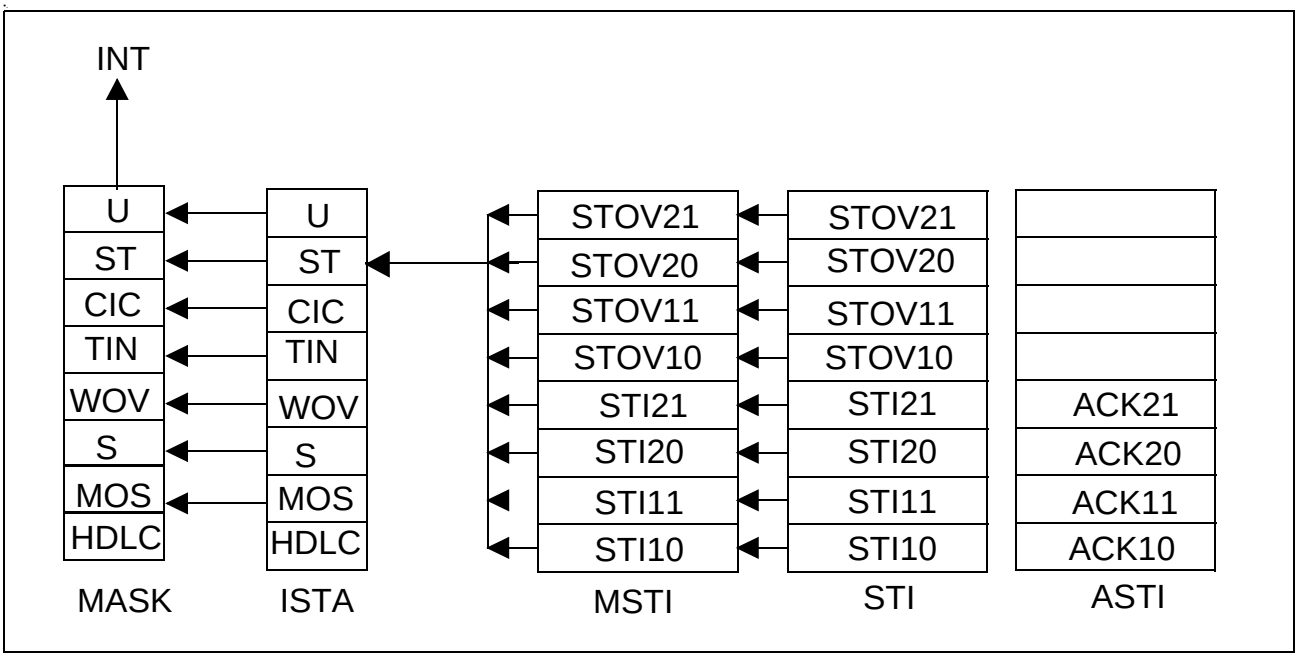


Figure 17 Interrupt Structure of the Synchronous Data Transfer

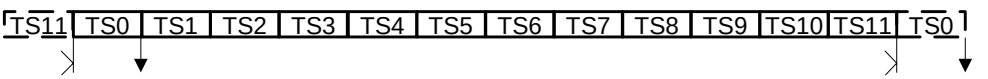
Figure 18 shows some examples based on the timeslot structure. Figure a) shows at which point in time a STI and STOV interrupt is generated for a specific timeslot. Figure b) is identical to example 3 above, figure c) corresponds to example 5 and figure d) shows example 4.

: STI interrupt generated

: STOV interrupt generated for a not acknowledged STI interrupt

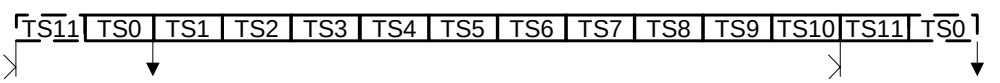
a) Interrupts for data access to time slot 0 (B1 after reset), MSTI.STI10 and MSTI.STOV10 enabled

xy:	10	11	21	20
CDA_TDSPxy.TSS:	TS0	TS1	TS5	TS11
MSTI.STIxy:	'0'	'1'	'1'	'1'
MSTI.STOVxy:	'0'	'1'	'1'	'1'



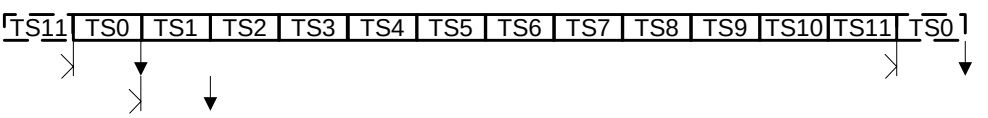
b) Interrupts for data access to time slot 0 (B1 after reset), STOV interrupt used as flag for "last possible CDA access"; MSTI.STI10 and MSTI.STOV20 enabled

xy:	10	11	21	20
CDA_TDSPxy.TSS:	TS0	TS1	TS5	TS11
MSTI.STIxy:	'0'	'1'	'1'	'1'
MSTI.STOVxy:	'1'	'1'	'1'	'0'



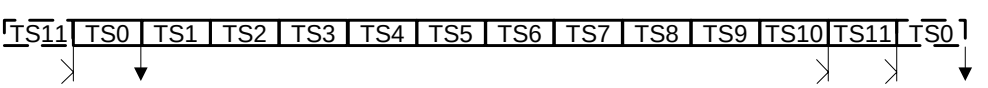
c) Interrupts for data access to time slot 0 and 1 (B1 and B2 after reset), MSTI.STI10, MSTI.STOV10, MSTI.STI11 and MSTI.STOV11 enabled

xy:	10	11	21	20
CDA_TDSPxy.TSS:	TS0	TS1	TS5	TS11
MSTI.STIxy:	'0'	'0'	'1'	'1'
MSTI.STOVxy:	'0'	'0'	'1'	'1'



d) Interrupts for data access to time slot 0 (B1 after reset), STOV20 interrupt used as flag for "last possible CDA access", STOV10 interrupt used as flag for "CDA access failed"; MSTI.STI10, MSTI.STOV10 and MSTI.STOV20 enabled

xy:	10	11	21	20
CDA_TDSPxy.TSS:	TS0	TS1	TS5	TS11
MSTI.STIxy:	'0'	'1'	'1'	'1'
MSTI.STOVxy:	'0'	'1'	'1'	'0'



sti_stov.vsd

Figure 18 Examples for the Synchronous Transfer Interrupt Control with one STIxy enabled

2.3.2.2 Serial Data Strobe Signal

For time slot oriented standard devices at the IOM®-2 interface, the Q-SMINT®IX provides two independent data strobe signals SDS1 and SDS2.

The two strobe signals can be generated with every 8-kHz-frame and are controlled by the registers SDS1/2_CR. By programming the TSS bits and three enable bits (ENS_TSS, ENS_TSS+1, ENS_TSS+3) a data strobe can be generated for the IOM®-2 time slots TS, TS+1 and TS+3 (bit7,6) and the combinations of them.

The data strobes for TS and TS+1 are always 8 bits long (bit7 to bit0) whereas the data strobe for TS+3 is always 2 bits long (bit7, bit6).

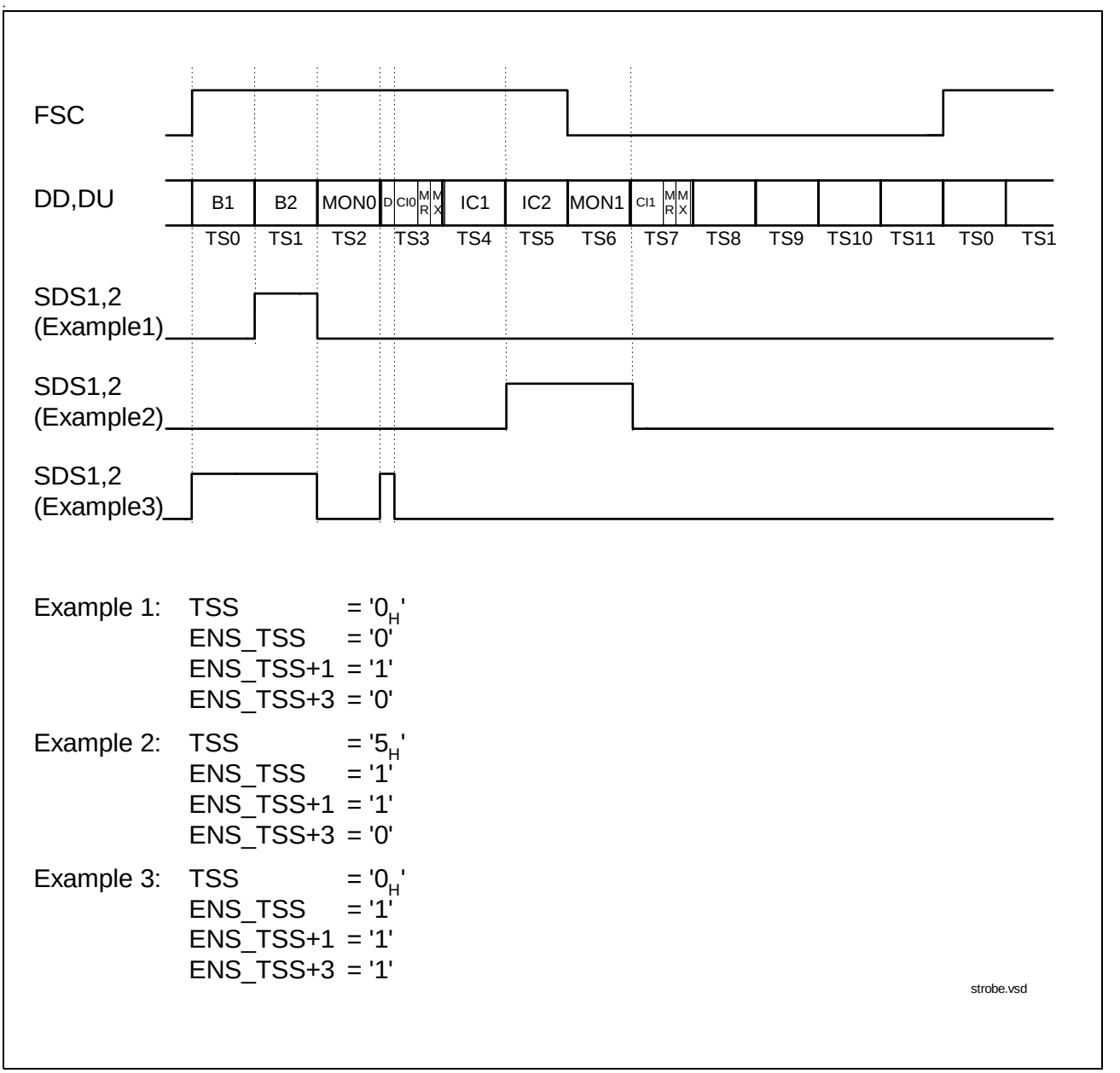


Figure 19 Data Strobe Signal Generation

Figure 19 shows three examples for the generation of a strobe signal. In example 1 the SDS is active during channel B2 on IOM®-2, whereas in the second example during IC2 and MON1. The third example shows a strobe signal for 2B+D channels which is used e.g. at an IDSL (144 kbit/s) transmission.

2.3.3 IOM®-2 Monitor Channel

The IOM®-2 MONITOR channel is utilized for information exchange between the Q-SMINT®IX and other devices in the MONITOR channel.

The MONTIOR channel data can be controlled by the bits in the MONITOR control register (MON_CR). For the transmission of the MONITOR data one of the 3 IOM®-2 channels can be selected by setting the MONITOR channel selection bits (MCS) in the MONITOR control register (MON_CR).

The DPS bit in the same register selects between an output on DU or DD respectively and with EN_MON the MONITOR data can be enabled/disabled. The default value is MONITOR channel 0 (MON0) enabled and transmission on DD.

The MONITOR channel of the Q-SMINT®IX can be used in the following applications (refer also to **Figure 4** and **Figure 5**):

- As a **master device** the Q-SMINT®IX can program and control other devices (e.g. PSB 2161) attached to the IOM®-2, which therefore, do not need a microcontroller interface.
- As a **slave device** the Q-SMINT®IX is programmed and controlled from a master device on IOM®-2 (e.g. UTAH). This is used in applications where no microcontroller is connected directly to the Q-SMINT®IX.

The MONITOR channel operates according to the IOM®-2 Reference Guide [13].

Note: In contrast to the INTC-Q, the Q-SMINT®IX *does neither issue nor react on Monitor commands (MON0,1,2,8). Instead, the Q-SMINT®*IX *operated in IOM®-2 slave mode must be programmed via new MONITOR channel concept (see **Chapter 2.3.3.4**), which provides full register access. The Monitor time out procedure is available. Reporting of the Q-SMINT®*IX *is performed via interrupts.*

2.3.3.1 Handshake Procedure

The MONITOR channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MONITOR Channel Receive (MR) and MONITOR Channel Transmit (MX) bits. Data is placed onto the MONITOR channel and the MX bit is activated. This data will be transmitted once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The MONITOR channel protocol is described In the following section and **Figure 22** shall illustrate this. The relevant control and status bits for transmission and reception are listed in **Table 11** and **Table 12**.

Table 11 Transmit Direction

Control/ Status Bit	Register	Bit	Function
Control	MOCR	MXC	MX Bit Control
		MIE	Transmit Interrupt (MDA, MAB, MER) Enable
Status	MOSR	MDA	Data Acknowledged
		MAB	Data Abort
	MSTA	MAC	Transmission Active

Table 12 Receive Direction

Control/ Status Bit	Register	Bit	Function
Control	MOCR	MRC	MR Bit Control
		MRE	Receive Interrupt (MDR) Enable
Status	MOSR	MDR	Data Received
		MER	End of Reception

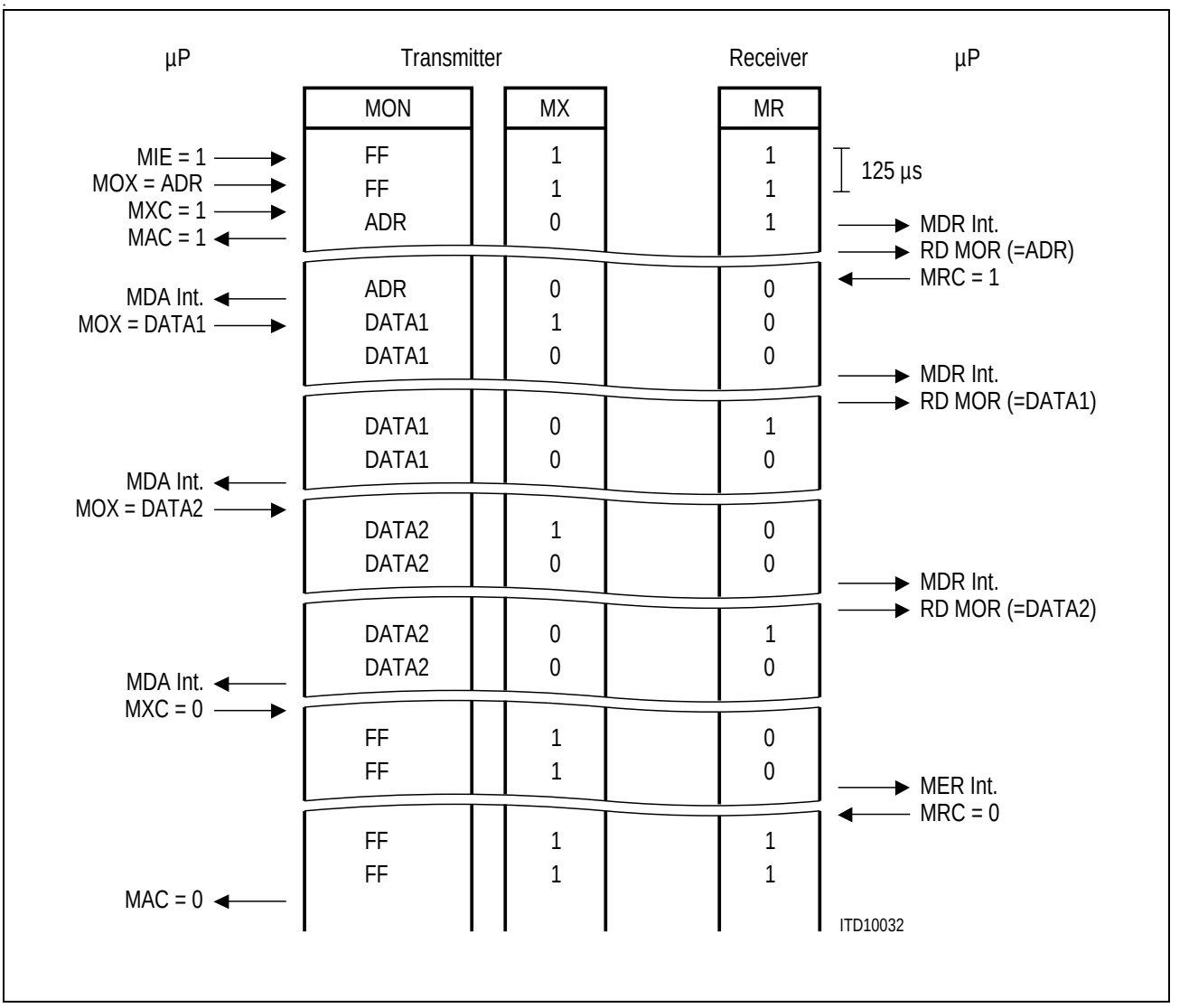


Figure 20 MONITOR Channel Protocol (IOM®-2)

Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a ’0’ in the MONITOR Channel Active MAC status bit.

After having written the MONITOR Data Transmit (MOX) register, the microprocessor sets the MONITOR Transmit Control bit MXC to ’1’. This enables the MX bit to go active (0), indicating the presence of valid MONITOR data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the MONITOR byte in its MONITOR Receive MOR register and generates a MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the MONITOR Receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to ’1’ to enable the receiver to store succeeding MONITOR channel bytes and acknowledge them according to the MONITOR channel protocol.

In addition, it enables other MONITOR channel interrupts by setting MONITOR Interrupt Enable (MIE) to ’1’.

As a result, the first MONITOR byte is acknowledged by the receiving device setting the MR bit to ’0’. This causes a MONITOR Data Acknowledge MDA interrupt status at the transmitter.

A new MONITOR data byte can now be written by the microprocessor in MOX. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the MONITOR channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the MONITOR byte in MOR and generates a new MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate a MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send. Note that the MONITOR channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the MONITOR Transmit Control bit MXC to ’0’. This enforces an inactive (’1’) state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a MONITOR Channel End of Reception MER interrupt status is generated by the receiver when the MX bit is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the MONITOR Channel Active MAC bit return to ’0’.

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to ’0’. An aborted transmission is indicated by a MONITOR Channel Data Abort MAB interrupt status at the transmitter.

The MONITOR transfer protocol rules are summarized in the following section

- A pair of MX and MR in the inactive state for two or more consecutive frames indicates an **idle state** or an **end of transmission**.
- A **start of a transmission** is initiated by the transmitter by setting the MXC bit to ’1’ enabling the internal MX control. The receiver acknowledges the received first byte by setting the MR control bit to ’1’ enabling the internal MR control.
- The internal MX, MR control indicates or acknowledges a new byte in the MON slot by toggling MX, MR from the active to the inactive state for one frame.
- Two frames with the MR-bit set to inactive indicate a receiver request for **abort**.
- The transmitter can **delay a transmission** sequence by sending the same byte continuously. In that case the MX-bit remains active in the IOM®-2 frame following the first byte occurrence. Delaying a transmission sequence is only possible while the receiver MR-bit and the transmitter MX-bit are active.

- Since a **double last-look criterion** is implemented the receiver is able to receive the MON slot data at least twice (in two consecutive frames), the receiver waits for the acknowledge of the reception of two identical bytes in two successive frames.
- To control this handshake procedure a collision detection mechanism is implemented in the transmitter. This is done by making a **collision check** per bit on the transmitted MONITOR data and the MX bit.
- Monitor data will be transmitted repeatedly until its reception is acknowledged or the transmission time-out timer expires.
- Two frames with the MX bit in the inactive state indicates the **end of a message** (EOM).
- Transmission and reception of monitor messages can be performed simultaneously. This feature is used by the device to send back the response before the transmission from the controller is completed (the device does not wait for EOM from controller).

2.3.3.2 Error Treatment

In case the device does not detect identical monitor messages in two successive frames, transmission is not aborted. Instead the device will wait until two identical bytes are received in succession.

A transmission is aborted by the device if

- an error in the MR handshaking occurs
- a collision on the IOM®-2 bus of the MONITOR data or MX bit occurs
- the transmission time-out timer expires

A reception is aborted by the device if

- an error in the MX handshaking occurs or
- an abort request from the opposite device occurs

MX/MR Treatment in Error Case

In the master mode the MX/MR bits are under control of the microcontroller through MXC or MRC, respectively. An abort is indicated by an MAB interrupt or MER interrupt, respectively.

In the slave mode the MX/MR bits are under control of the device. An abort is always indicated by setting the MX/MR bit inactive for two or more IOM®-2 frames. The controller must react with EOM.

Figure 21 shows an example for an abort requested by the receiver, **Figure 22** shows an example for an abort requested by the transmitter and **Figure 23** shows an example for a successful transmission.

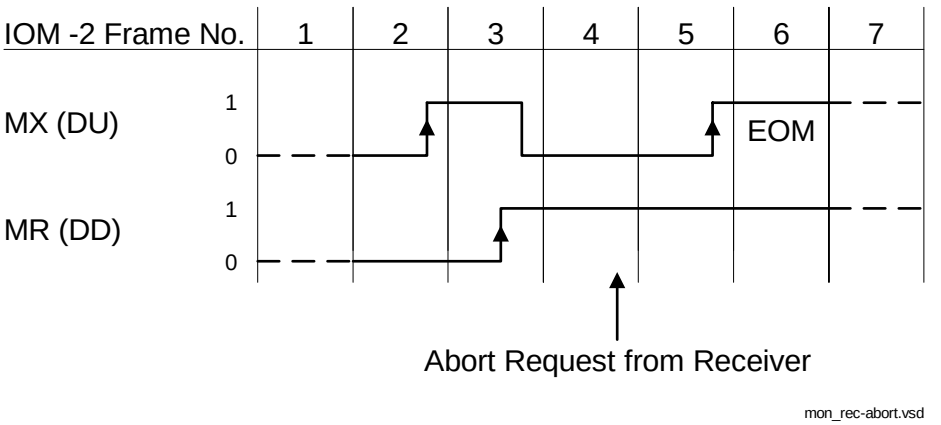


Figure 21 Monitor Channel, Transmission Abort requested by the Receiver

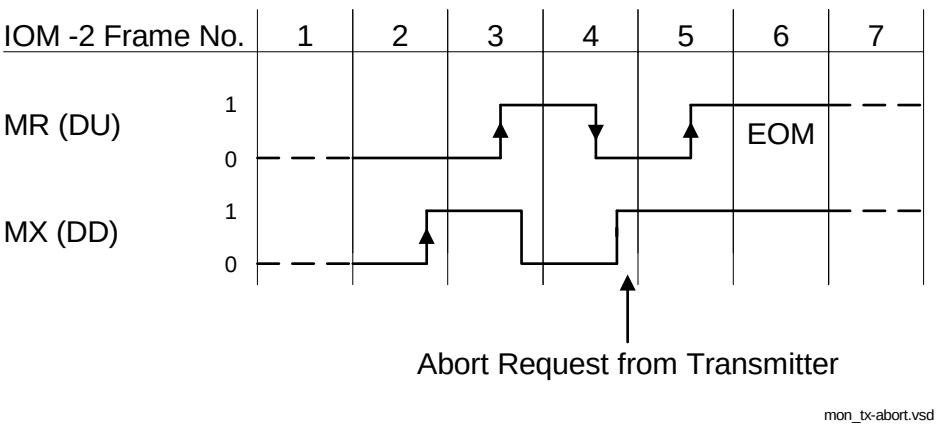


Figure 22 Monitor Channel, Transmission Abort requested by the Transmitter

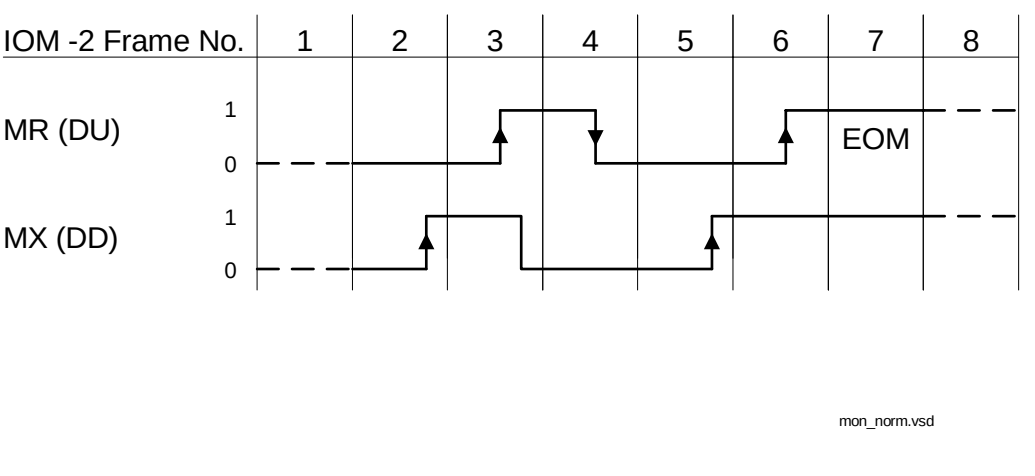


Figure 23 Monitor Channel, Normal End of Transmission

2.3.3.3 MONITOR Channel Programming as a Master Device

The master mode is selected by default if one of the microcontroller interfaces is selected. The monitor data is written by the microcontroller in the MOX register and transmitted via IOM®-2 DD(DU) line to the programmed/controlled device e.g. ARCOFI-BA PSB 2161. The transfer of the commands in the MON channel is regulated by the handshake protocol mechanism with MX, MR.

2.3.3.4 MONITOR Channel Programming as a Slave Device

MONITOR slave mode can be selected by pinstrapping the microcontroller interface pins according to **Table 5**. All programming data required by the device is received in the MONITOR time slot on the IOM®-2 and is transferred to the MOR register. The transfer of the commands in the MON channel is regulated by the handshake protocol mechanism with MX, MR which is described in the previous **Chapter 2.3.3.1**.
The first byte of the MONITOR message must contain in the higher nibble the MONITOR channel address code which is ’1000’ for the Q-SMINT®IX. The lower nibble distinguishes between a programming command and an identification command.

Identification Command

In order to be able to identify unambiguously different hardware designs of the Q-SMINT®IX by software, the following identification command is used:

DU 1st byte value	1	0	0	0	0	0	0	0
DU 2nd byte value	0	0	0	0	0	0	0	0

The Q-SMINT®IX responds to this identification sequence by sending a identification sequence:

DD 1st byte value	1	0	0	0	0	0	0	0
DD 2nd byte value	0	0	DESIGN					<IDENT>

DESIGN: six bit code, specific for each device in order to identify differences in operation (see **“ID - Identification Register” on Page 198**).

This identification sequence is usually done once, when the Q-SMINT®IX is connected for the first time. This function is used so that the software can distinguish between different possible hardware configurations. However this sequence is not compulsory.

Programming Sequence

The programming sequence is characterized by a ’1’ being sent in the lower nibble of the received address code. **The data structure after this first byte is equivalent to the structure of the serial control interface described in chapter Chapter 2.1.1**.

DU 1st byte value	1	0	0	0	0	0	0	1
DU 2nd byte value	Header Byte							
DU 3rd byte value	R/W	Command/ Register Address						
DU 4th byte value	Data 1							
DU (nth + 3) byte value	Data n							

All registers can be read back when setting the R/W bit to ’1’. The Q-SMINT®IX responds by sending his IOM®-2 specific address byte (81_h) followed by the requested data.

Note: Application Hint:

It is not allowed to disable the MX- and MR-control in the programming device at the same time! First, the MX-control must be disabled, then the µC has to wait for an End of Reception before the MR-control may be disabled. Otherwise, the Q-SMINT® IX does not recognize an End of Reception.

2.3.3.5 Monitor Time-Out Procedure

To prevent lock-up situations in a MONITOR transmission a time-out procedure can be enabled by setting the time-out bit (TOUT) in the MONITOR configuration register (MCONF). An internal timer is always started when the transmitter must wait for the reply of the addressed device or for transmit data from the microcontroller. After 40 IOM®-2 frames (5 ms) without reply the timer expires and the transmission will be aborted with an EOM (End of Message) command by setting the MX bit to ’1’ for two consecutive IOM®-2 frames.

2.3.3.6 MONITOR Interrupt Logic

Figure 24 shows the interrupt structure of the MONITOR handler. The MONITOR Data Receive interrupt status MDR has two enable bits, MONITOR Receive interrupt Enable (MRE) and MR bit Control (MRC). The MONITOR channel End of Reception MER, MONITOR channel Data Acknowledged MDA and MONITOR channel Data Abort MAB interrupt status bits have a common enable bit MONITOR Interrupt Enable MIE.

MRE set to “0” prevents the occurrence of MDR status, including when the first byte of a packet is received. When MRE is set to “1” but MRC is set to “0”, the MDR interrupt status is generated only for the first byte of a receive packet. When both MRE and MRC are set to “1”, MDR is always generated and all received MONITOR bytes - marked by a 1-to-0 transition in MX bit - are stored. Additionally, a MRC set to “1” enables the control of the MR handshake bit according to the MONITOR channel protocol.

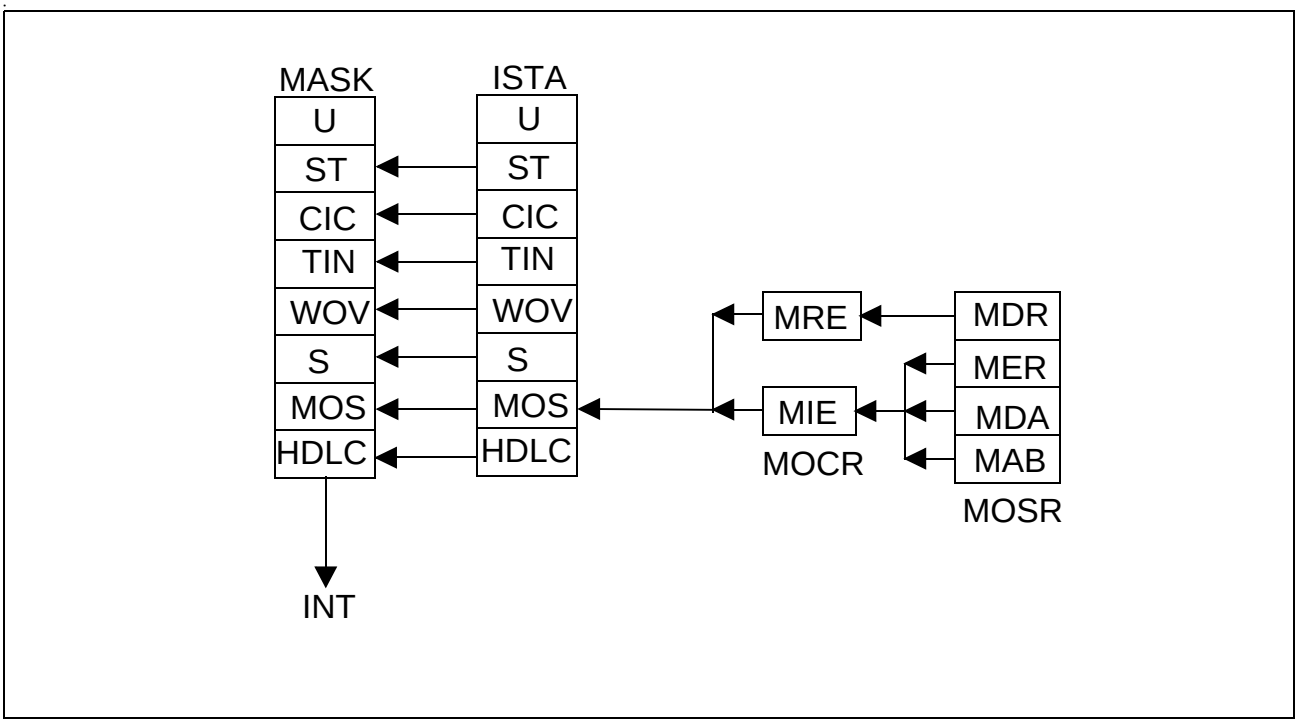


Figure 24 MONITOR Interrupt Structure

2.3.4 C/I Channel Handling

The Command/Indication channel carries real-time status information between the Q-SMINT®IX and another device connected to the IOM®-2.

1) C/I0 channel lies in IOM®-2 channel 0 and access may be arbitrated via the TIC bus access protocol. In this case the arbitration is done in IOM®-2 channel 2.

The C/I0 channel is accessed via register CIR0 (received C/I0 data from DD) and register CIX0 (transmitted C/I0 data to DU). The C/I0 code is four bits long.
In the receive direction, the code from layer-1 is continuously monitored, with an interrupt being generated any time a change occurs (ISTA.CIC).

C/I0 only: a new code must be found in two consecutive IOM®-2 frames to be considered valid and to trigger a C/I code change interrupt status (double last look criterion).

In the transmit direction, the code written in CIX0 is continuously transmitted in C/I0.

2) A second C/I channel (called C/I1) lies in IOM®-2 channel 1 and is used to convey real time status information of the on-chip S-transceiver or an external device. The C/I1 channel consists of four or six bits in each direction. The width can be changed from 4 bit to 6 bit by setting bit CIX1.CICW.

In 4-bit mode 6-bits are written whereby the higher 2 bits must be set to “1” and 6-bits are read whereby only the 4 LSBs are used for comparison and interrupt generation (i.e. the higher two bits are ignored).

The C/I1 channel is accessed via registers CIR1 and CIX1. The connection of CIR1 and CIX1 to DD and DU, respectively, can be selected by setting bit HCI_CR.DPS_CI1. A change in the received C/I1 code is indicated by an interrupt status without double last look criterion.

CIC Interrupt Logic

Figure 25 shows the CIC interrupt structure.

The two corresponding status bits CIC0 and CIC1 are read in CIR0 register. CIC1 can be individually disabled by clearing the enable bit CI1E in the CIX1 register. In this case the occurrence of a code change in CIR1 will not be displayed by CIC1 until the corresponding enable bit has been set to one.
Bits CIC0 and CIC1 are cleared by a read of CIR0.
An interrupt status is indicated every time a valid new code is loaded in CIR0 or CIR1. The CIR0 is buffered with a FIFO size of two. If a second code change occurs in the received C/I channel 0 before the first one has been read, immediately after reading of CIR0 a new interrupt will be generated and the new code will be stored in CIR0. If several consecutive codes are detected, only the first and the last code are obtained at the first and second register read, respectively.

For CIR1 no FIFO is available. The actual code of the received C/I channel 1 is always stored in CIR1.

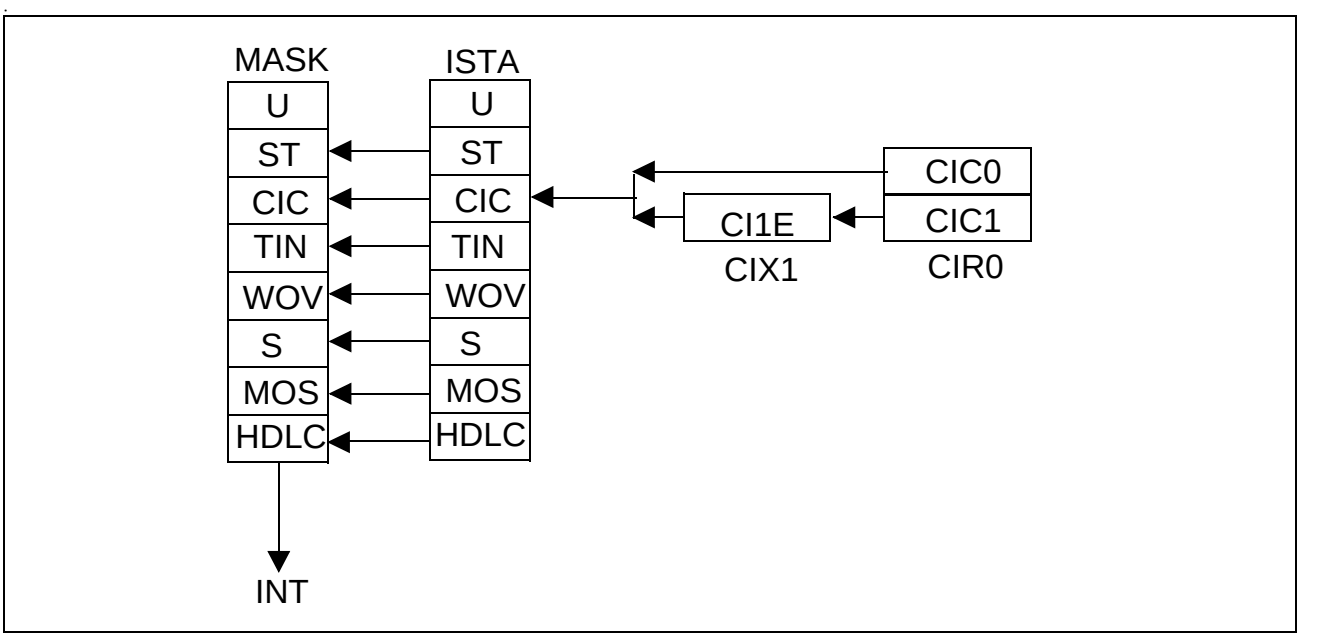


Figure 25 CIC Interrupt Structure

2.3.5 D-Channel Access Control

The upstream D-channel is arbitrated between the S-bus, the internal HDLC controller and external HDLC controllers via the TIC bus (S/G, BAC, TBA bits) according to the

IOM®-2 Reference Guide[1]. Further to the implementation in the INTC-Q it is possible, to set the priority (8 or 10) of all HDLC-controllers connected to IOM®-2, which is particularly useful for use of the Q-SMINT®IX together with the UTAH.

2.3.5.1 Application Example for D-Channel Access Control

Figure 26 shows a scenario for the local D-channel arbitration between the S-bus and the microcontroller.

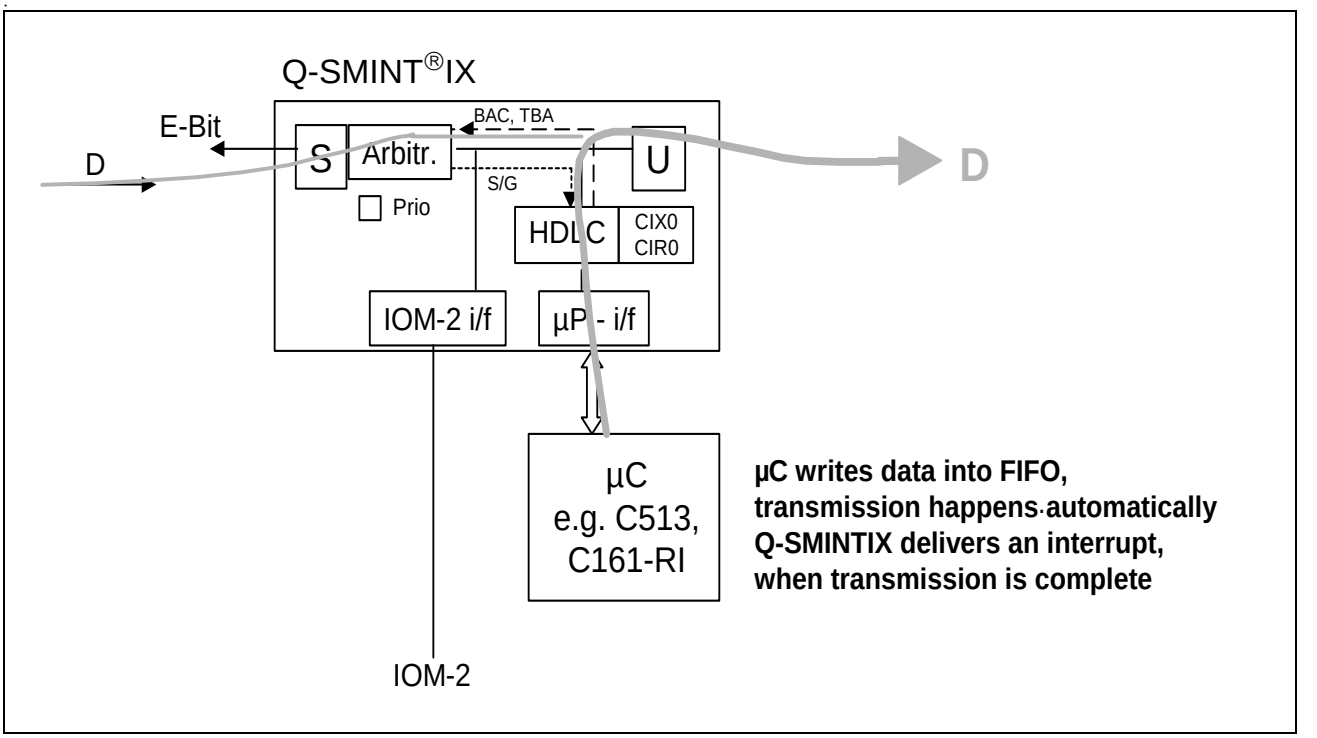


Figure 26 D-Channel Arbitration: µC has no HDLC and no Direct Access to TIC Bus

2.3.5.2 TIC Bus Handling

The TIC bus is implemented to organize the access to the C/I0-channel and to the D-channel from up to 7 D-channels HDLC controllers. The arbitration mechanism must be activated by setting MODEH.DIM2-0=00x.

The arbitration mechanism is implemented in the last octet in IOM®-2 channel 2 of the IOM®-2 interface (see **Figure 27**). An access request to the TIC bus may either be generated by software (µC access to the C/I0-channel via CIX0 register) or by an internal or an external D-channel HDLC controller (transmission of an HDLC frame in the D-channel). A software access request to the bus is effected by setting the BAC bit in register CIX0 to '1' (resulting in BAC = '0' on IOM®-2).

[1] The A/B-bit is not supported by the U-transceiver

In the case of an access request by the Q-SMINT®IX, the Bus Accessed-bit BAC (bit 5 of last octet of CH2 on DU, see **Figure 27**) is checked for the status "bus free“, which is indicated by a logical ’1’. If the bus is free, the Q-SMINT®IX transmits its individual TIC bus address TAD programmed in the CIX0 register (CIX0.TBA2-0). While being transmitted the TIC bus address TAD is compared bit by bit with the value read back on DU. If a sent bit set to ’1’ is read back as ’0’ because of the access of an external device with a lower TAD, the Q-SMINT®IX withdraws immediately from the TIC bus, i.e. the remaining TAD bits are not transmitted. The TIC bus is occupied by the device which sends and reads back its address error-free. If more than one device attempt to seize the bus simultaneously, the one with the lowest address values wins. This one will set BAC=0 on TIC bus and starts D-channel transmission in the same frame.

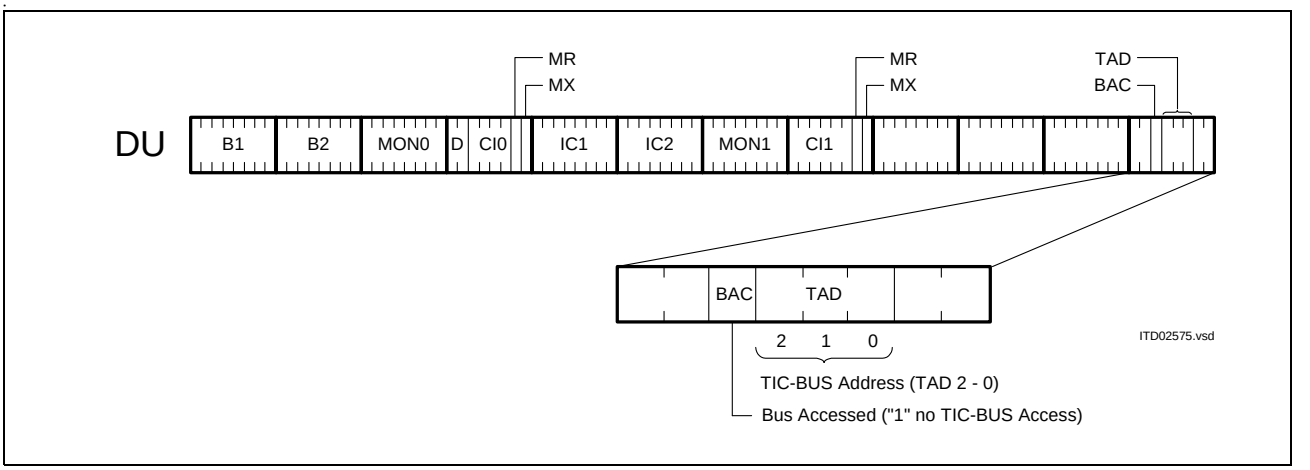


Figure 27 Structure of Last Octet of Ch2 on DU

When the TIC bus is seized by the Q-SMINT®IX, the bus is identified to other devices as occupied via the DU Ch2 Bus Accessed-bit state ’0’ until the access request is withdrawn. After a successful bus access, the Q-SMINT®IX is automatically set into a lower priority class, that is, a new bus access cannot be performed until the status "bus free" is indicated in two successive frames.

If none of the devices connected to the IOM®-2 interface request access to the D and C/I0 channels, the TIC bus address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I0 channels.

Note: Bit BAC (CIX0 register) should be reset by the µC when access is no more requested, to grant other devices access to the D and C/I0 channels.

2.3.5.3 Stop/Go Bit Handling

The availability of the DU D channel is indicated in bit 5 "Stop/Go" (S/G) of the last octet in DD channel 2 (**Figure 28**). The arbitration mechanism must be activated by setting MODEH.DIM2-0=0x1.

S/G = 1 : stop
S/G = 0 : go

The Stop/Go bit is available to other layer-2 devices connected to the IOM®-2 interface to determine if they can access the D channel in upstream direction.

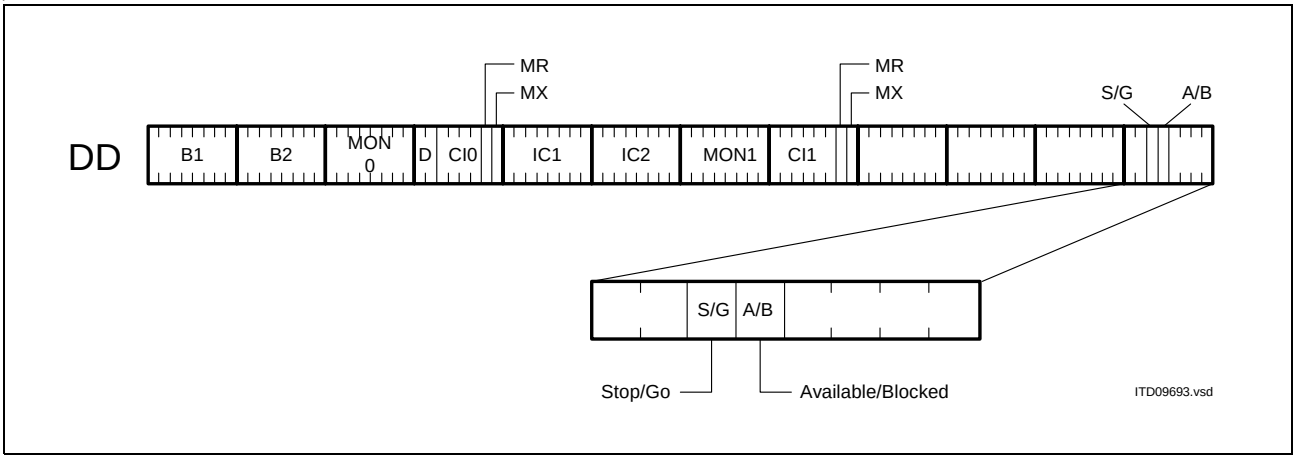


Figure 28 Structure of Last Octet of Ch2 on DD

2.3.5.4 D-Channel Arbitration

In intelligent NT applications (selected via register S_MODE.MODE2-0) the Q-SMINT®IX has to share the upstream D-channel with one or more D-channel controllers on the IOM®-2 interface and with all connected TEs on the S interface.

The S-transceiver incorporates an elaborate state machine for D-channel priority handling on IOM®-2 (**Chapter 2.3.5.5**). For the access to the D-channel a similar arbitration mechanism as on the S interface (writing D-bits, reading back E-bits) is performed for all D-channel sources on IOM®-2. Due to this an equal and fair access is guaranteed for all D-channel sources on both the S interface and the IOM®-2 interface. The access to the upstream D-channel is handled via the S/G bit for the HDLC controllers and via E-bit for all connected terminals on S (E-bits are inverted to block the terminals on S). Furthermore, if more than one HDLC source is requesting D-channel access on IOM®-2 the TIC bus mechanism is used (see **Chapter 2.3.5.2**).

The arbiter permanently counts the “1s” in the upstream D-channel on IOM®-2. If the necessary number of “1s” is counted and an HDLC controller on IOM®-2 requests upstream D-channel access (BAC bit is set to 0), the arbiter allows this D-channel controller immediate access and blocks other TEs on S (E-bits are inverted). Similar as on the S-interface the priority for D-channel access on IOM®-2 can be configured to 8 or 10 (S_CMD.DPRIO).

The configuration settings of the Q-SMINT®IX in intelligent NT applications are summarized in **Table 13**.

Table 13 Q-SMINT®IX Configuration Settings in Intelligent NT Applications

Functional Block	Configuration Description	Configuration Setting
Layer 1	Select Intelligent NT mode	S-Transceiver Mode Register: S_MODE.MODE0 = 0 (NT state machine) or S_MODE.MODE0 = 1 (LT-S state machine) S_MODE.MODE1 = 1 S_MODE.MODE2 = 1
Layer 2	Enable S/G bit and TIC bus evaluation	D-channel Mode Register: MODEH.DIM2-0 = 001

Note: For mode selection in the S_MODE register the MODE1/2 bits are used to select intelligent NT mode, MODE0 selects NT or LT-S state machine.

With the configuration settings shown above the Q-SMINT®IX in intelligent NT applications provides for equal access to the D-channel for terminals connected to the S-interface and for D-channel sources on IOM®-2.

2.3.5.5 State Machine of the D-Channel Arbiter

Figure 29 gives a simplified view of the state machine of the D-channel arbiter. CNT is the number of ’1’ on the IOM®-2 D-channel and BAC corresponds to the BAC-bit on IOM®-2. The number n depends on configuration settings (selected priority 8 or 10) and the condition of the previous transmission, i.e. if an abort was seen (n = 8 or 10, respectively) or if the last transmission was successful (n = 9 or 11, respectively).

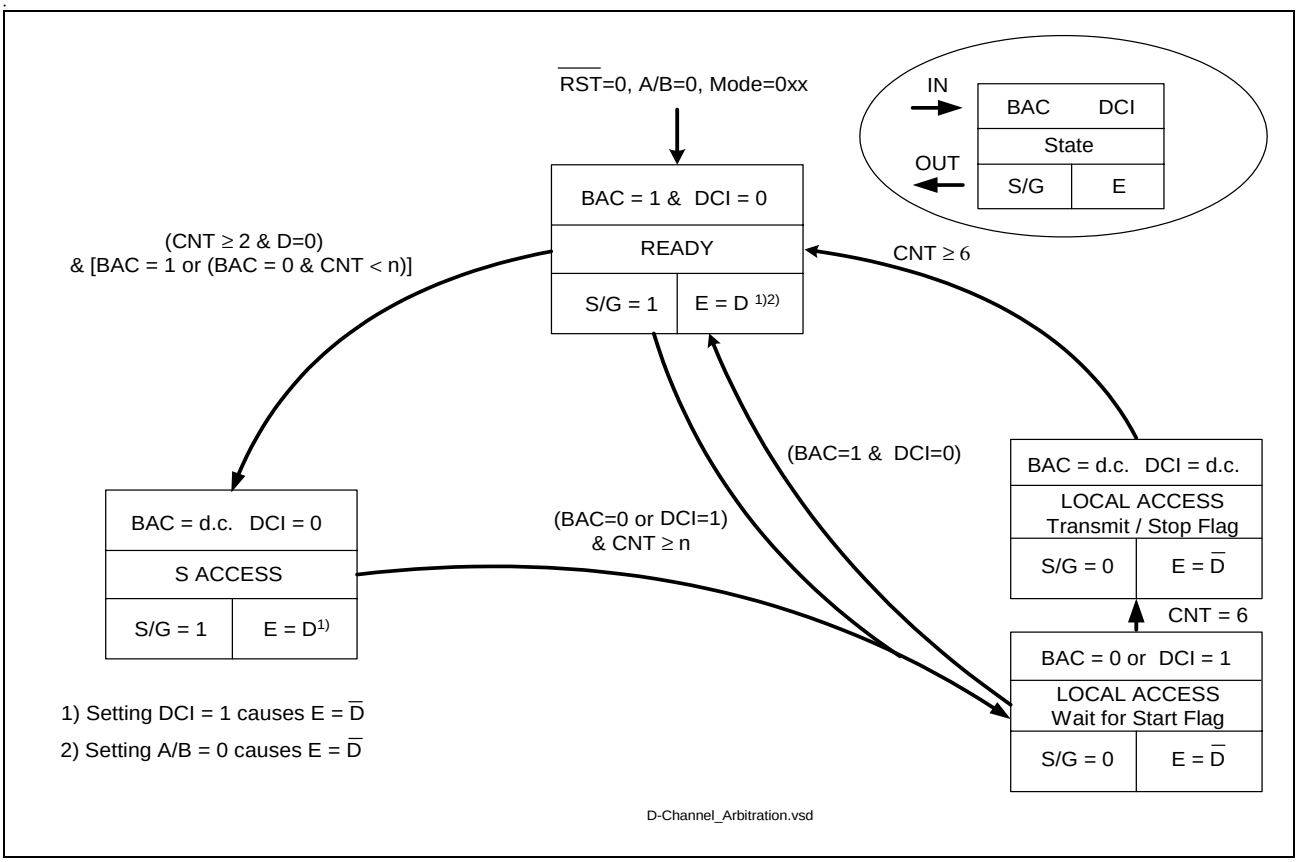


Figure 29 State Machine of the D-Channel Arbiter (Simplified View)[1)]

Table 14 lists the major differences of the D-channel arbiter´s state machine between Q-SMINT®IX and INTC-Q [12]

Table 14 Major Differences D-Channel Arbiter INTC-Q and Q-SMINT®IX

	INTC-Q	Q-SMINT®IX
State 'IDLE' (S/G=0, E=D)	Automatically entered from state 'READY' or 'S ACCESS' after CNT=n	Not available, initial state is 'READY' (S/G=1, E=D)
BAC-bit	Ignored	Local HDLC must tie BAC = '0' to enter state 'LOCAL ACCESS'
D-channel inhibit	Not possible	S-MODE.DCH_INH Alternative to BAC-bit to enter state 'LOCAL ACCESS'

1) If the S-transceiver is reset by SRES.RES_S = '1' or disabled by S_CONF0.DIS_TR = '1', then the D-channel arbiter is in state Ready (S/G = '1'), too. The S/G evaluation of the HDLC has to be disabled in this case; otherwise, the HDLC is not able to send data.

1. Local D-Channel Controller Transmits Upstream

In the initial state (’Ready’ state) neither the local D-channel sources nor any of the terminals connected to the S-bus transmit in the D-channel.

The Q-SMINT®IX S-transceiver thus receives BAC = “1” (IOM®-2 DU line) and transmits S/G = “1” (IOM®-2 DD line). The access will then be established according to the following procedure:

- Local D-channel source verifies that BAC bit is set to ONE (currently no bus access).
- Local D-channel source issues TIC bus address and verifies that no controller with higher priority requests transmission (TIC bus access must always be performed even if no other D-channel sources are connected to IOM®-2).
- Local D-channel source issues BAC = “0” to block other sources on IOM®-2 and to announce D-channel access.
- Q-SMINT®IX S-transceiver pulls S/G bit to ZERO (’Local Access’ state) as soon as CNT ≥ n (see note) to allow sending D-channel data from the entitled source.
  Q-SMINT®IX S-transceiver transmits inverted echo channel (E bits) on the S-bus to block all connected S-bus terminals (E = $\overline{D}$).
- Local D-channel source commences with D data transmission on IOM®-2 as long as it receives S/G = “0”.
- After D-channel data transmission is completed the controller sets the BAC bit to ONE.
- Q-SMINT®IX S-transceiver transmits non-inverted echo (E = D).
- Q-SMINT®IX S-transceiver pulls S/G bit to ONE (’Ready’ state) to block the D-channel controller on IOM®-2.

Note: If right after D-data transmission the D-channel arbiter goes to state ’Ready’ and the local D-channel source wants to transmit again, then it may happen that the leading ’0’ of the start flag is written into the D-channel before the D-channel source recognizes that the S/G bit is pulled to ’1’ and stops transmission. In order to prevent unintended transitions to state ’S-Access’, the additional condition CNT ≥ 2 is introduced. As soon as CNT ≥ n, the S/G bit is set to ’0’ and the D-channel source may start transmission again (if TIC bus is occupied). This allows an equal access for D-channel sources on IOM®-2 and on the S interface.

2. Terminal Transmits D-Channel Data Upstream

The initial state is identical to that described in the last paragraph. When one of the connected S-bus terminals needs to transmit in the D-channel, access is established according to the following procedure:

- S-transceiver recognizes that the D-channel on the S-bus is active via D = ’0’.
- S-transceiver transfers S-bus D-channel data transparently through to the upstream IOM®-2 bus.

2.3.6 Activation/Deactivation of IOM®-2 Interface

The deactivation procedure of the IOM®-2 interface is shown in Figure 30. After detecting the code DI (Deactivation Indication) the Q-SMINT®IX responds by transmitting DC (Deactivation Confirmation) during subsequent frames and stops the timing signals after the fourth frame. The clocks stop at the end of the C/I-code in IOM®-2 channel 0.

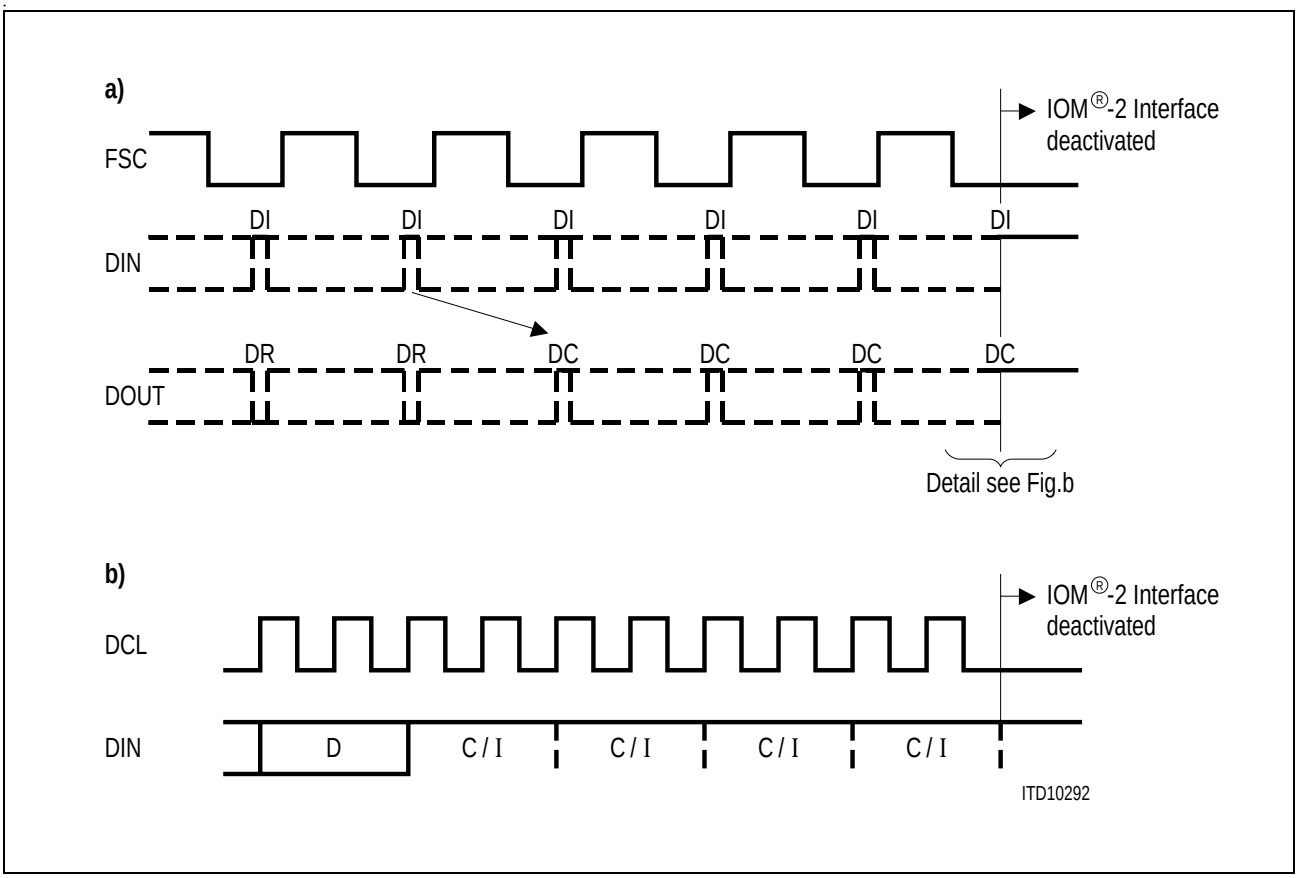


Figure 30 Deactivation of the IOM®-2 Clocks

Conditions for Power-Down

If none of the following conditions is true, the IOM®-2 interface can be switched off, reducing power consumption to a minimum.

- S-transceiver is not in state 'Deactivated'
- Signal $\overline{\text{INFO0}}$ on the S-interface
- Uk0-transceiver is not in state 'Deactivated'
- Pin DU is low (either at the IOM®-2 interface or via IOM_CR.SPU)
- External pin $\overline{\text{EAW}}$ External Awake is low
- Bit MODE 1.CFS = '0'
- Stop on the correct place in the IOM®-2 frame. DCL must be low during power down (stop on falling edge of DCL) (see **Figure 30**).

A deactivated IOM®-2 can be reactivated by one of the following methods:

- Pulling pin DU line low:
  - directly at the IOM®-2 interface
  - via the µP interface with "Software Power Up" (IOM_CR:SPU bit)
- Pulling pin $\overline{\text{EAW}}$ ‘External Awake‘ low
- Setting ‘Configuration Select‘ MODE1:CFS bit = ’0’
- Level detection at the S-interface
- Activation from the U-interface

2.4 U-Transceiver

The state machine of the U-Transceiver is based on the NT state machine in the PEB / PEF 8191 documentation [12].

Note: 'Self test request' and 'Self test passed' are not executed by the U-transceiver

The U-transceiver is configured and controlled via the registers described in **Chapter 4.11**. The U-transceiver is always in IOM®-2 channel 0. It is possible to select between a state machine that simplifies programming (see **Chapter 2.4.10.6**) and the state machine as known from the PEB / PEF 8091 (see **Chapter 2.4.10.2**).

2.4.1 2B1Q Frame Structure

Transmission on the U_{2B1Q}-interface is performed at a rate of 80 kbaud. The code used is reducing two bits to one quaternary symbol (2B1Q).

Data is grouped together into U-superframes of 12 ms each. Each superframe consists of eight basic frames which begin with a synchronization word and contain 222 bits of information. The first basic frame of a superframe starts with an inverted synchword (ISW) compared to the other basic frames (SW). The structure of one U-superframe is illustrated in **Figure 31** and **Figure 32**.

ISW	**1. Basic Frame**	**SW**	**2. Basic Frame**	**. . .**	**SW**	**8. Basic Frame**
<---12 ms--->						

Figure 31 U-Superframe Structure

(I) SW **(Inverted) Synch Word** **18 Bit (9 Quat)**	**12 × 2B + D** **User Data** **216 Bits (108 Quat)**	**M1 – M6** **Maintenance Data** **6 Bits (3 Quat)**
<---1,5 ms--->		

Figure 32 U-Basic Frame Structure

Out of the 222 information bits 216 contain 2B + D data from 12 IOM®-frames, the remaining 6 bits are used to transmit maintenance information. Thus 48 maintenance bits are available per U-superframe. They are used to transmit two EOC-messages (24 bit), 12 Maintenance (overhead) bits and one checksum (12 bit).

Table 15 U-Superframe Format

		Fram-ing	2B + D	Overhead Bits (M1 – M6)					
	Quat Positions	1 – 9	10 – 117	118 s	118 m	119 s	119 m	120 s	120 m
	Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B + D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B + D	EOC a1	EOC a2	EOC a3	ACT/ ACT	1	1
	2	SW	2B + D	EOC dm	EOC i1	EOC i2	DEA / PS1	1	FEBE
	3	SW	2B + D	EOC i3	EOC i4	EOC i5	SCO/ PS2	CRC1	CRC2
	4	SW	2B + D	EOC i6	EOC i7	EOC i8	1/ NTM	CRC3	CRC4
	5	SW	2B + D	EOC a1	EOC a2	EOC a3	1/ CSO	CRC5	CRC6
	6	SW	2B + D	EOC dm	EOC i1	EOC i2	1	CRC7	CRC8
	7	SW	2B + D	EOC i3	EOC i4	EOC i5	UOA / SAI	CRC9	CRC 10
	8	SW	2B + D	EOC i6	EOC i7	EOC i8	AIB / NIB	CRC 11	CRC 12
2,3…									
						LT- to NT dir. >	/	< NT- to LT dir.	

– ISW Inverted Synchronization Word (quad): – 3 – 3 + 3 + 3 + 3 – 3 + 3 – 3 – 3
– SW Synchronization Word (quad): + 3 + 3 – 3 – 3 – 3 + 3 – 3 + 3 + 3
– CRC Cyclic Redundancy Check
– EOC Embedded Operation Channel
  a = address bit
  d/m = data / message bit
  i = information (data / message)
– ACT Activation bit
  ACT = (1) –> Layer 2 ready for communication

–	DEA	Deactivation bit	DEA = (0) –> LT informs NT that it will turn off
–	CSO	Cold Start Only	CSO = (1) –> NT-activation with cold start only
–	UOA	U-Only Activation	UOA = (0) –> U-only activated
–	SAI	S-Activity Indicator	SAI = (0) –> S-interface is deactivated
–	FEBE	Far-end Block Error	FEBE = (0) –> Far-end block error occurred
–	PS1	Power Status Primary Source	PS1 = (1) –> Primary power supply ok
–	PS2	Power Status Secondary Source	PS2 = (1) –> Secondary power supply ok
–	NTM	NT-Test Mode	NTM = (0) –> NT busy in test mode
–	AIB	Alarm Indication Bit	AIB = (0) –> Interruption (according to ANSI)
–	NIB	Network Indication Bit	NIB = (1) –> no function (reserved for network use)
–	SCO	Start on Command only bit	
–	1	(currently not defined by ANSI/ETSI)	

can be accessed by the system interface for proprietary use

The principle signal flow is depicted in **Figure 33** and **Figure 34**. The data is first grouped in bits that are covered by the CRC and bits that are not. After the CRC generation the bits are arranged in the proper sequence according to the 2B1Q frame format, encoded and finally transmitted.

In receive direction the data is first decoded, descrambled, deframed and handed over for further processing.

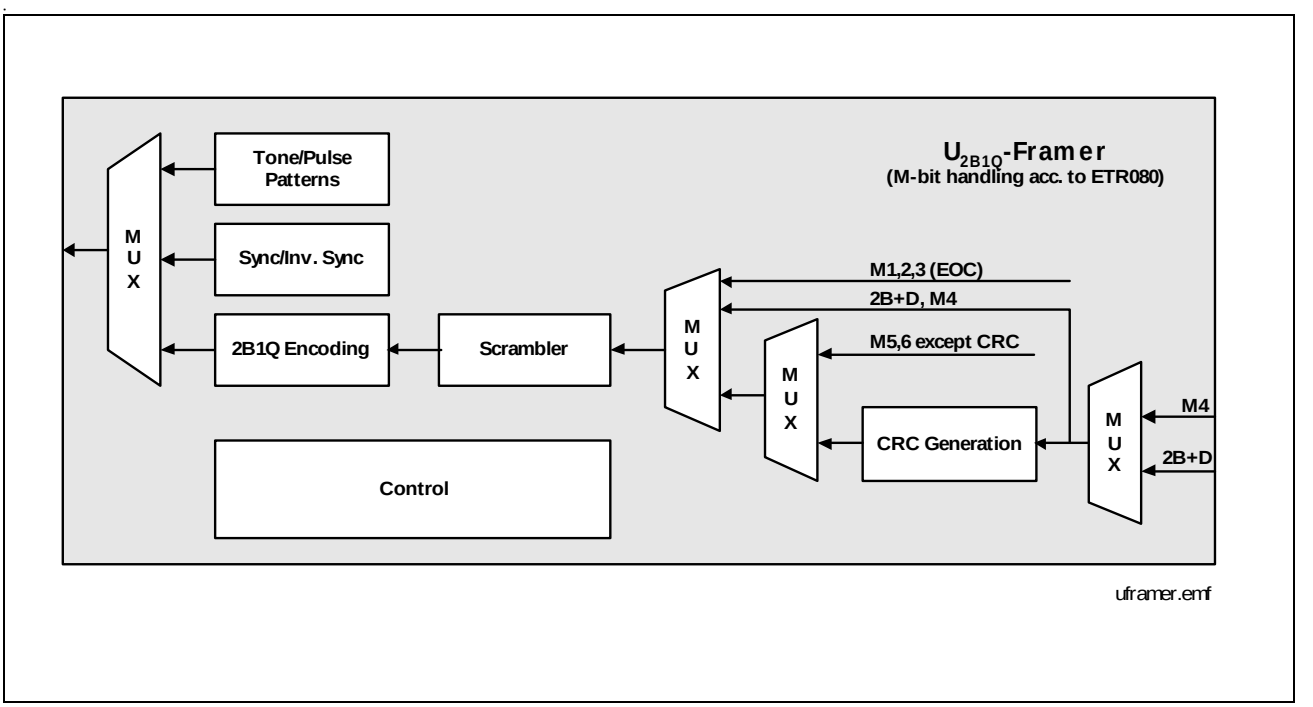


Figure 33 U_{2B1Q} Framer - Data Flow Scheme

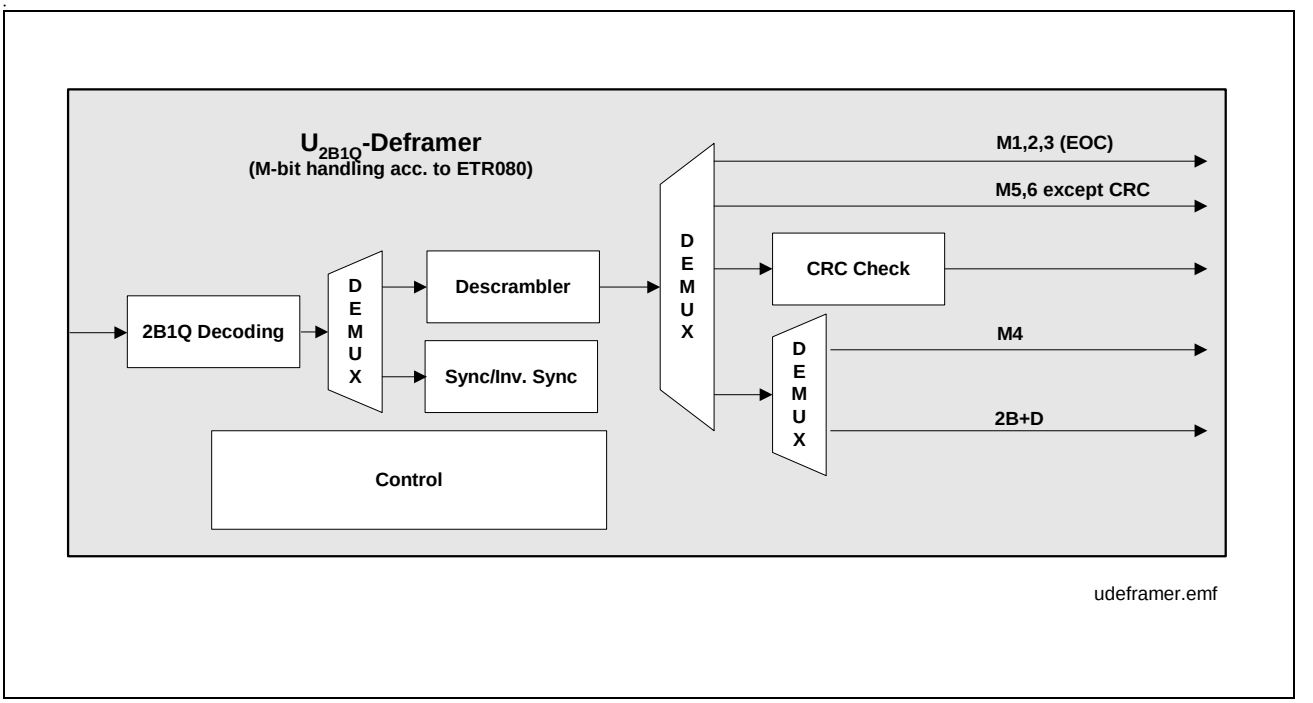


Figure 34 U_{2B1Q} Deframer - Data Flow Scheme

2.4.2 Maintenance Channel

The last three symbols (6 bits) of each basic frame are used as M (Maintenance)-channel for the exchange of operation and maintenance data between the network and the NT. Approved M-bit data is first processed and then reported to the µC by interrupt requests. The verification method is programmed in the MFILT register (see **Chapter 4.11.2**).

EOC-data is inserted into the U-frame at the positions M1, M2 and M3 (**Table 15**) thereby permitting the transmission of two complete EOC-messages (2× 12 bits) within one U-superframe (see **Chapter 2.4.3**).

M4 bits are used to communicate status and maintenance functions between the transceivers. The meaning of a bit position is dependent upon the direction of transmission (upstream/downstream) and the operation mode (NT/LT). See **Table 15** for the different meaning of the M4 bits. For details see **Chapter 2.4.4**.

The M5 and M6 bits contain the FEBE bit and the CRC bits. For details see **Chapter 2.4.6**.

2.4.2.1 Reporting to the µC Interface

The maintenance channel information is exchanged with external devices via the appropriate registers. Received maintenance channel information is reported to the µC by an interrupt.

2.4.2.2 Access from the µC Interface

The maintenance data to be transmitted can be programmed by writing the internal EOCW/M4W/M56W registers.

2.4.2.3 Availability of Maintenance Channel Information

Transmission of the Maintenance channel data is only possible if a superframe is transmitted and the M-bits are transparent (M-Bits are “normal” in **Table 25**). In other states all maintenance bits are clamped to high.

Reception of the Maintenance channel data is enabled by the state machine in the following states:

Table 16 Enabling the Maintenance Channel (Receive Direction)

Synchronized1
Synchronized2
Wait for ACT
Transparent
Error S/T
Pend. Deac. S/T
Pend. Deac. U
Analog Loop Back

Reporting and execution of maintenance information is only sensible if the Q-SMINT®IX is synchronous. Filters are provided to avoid meaningless reporting.

Reset values are applied to the maintenance bits before the state machine enters one of the states in **Table 16**.

2.4.2.4 M-Bit Register Access Timing

Since the maintenance data must be put into and read from the U-frame in time there is the need for synchronization if M-Bit data is exchanged via the µC-interface. Below the timing is given for the access to the M-Bit read and write registers.

The **write access timing** is depicted in **Figure 35**. Timing references for a write access are the 6 ms and 12 ms interrupts which are accommodated in the ISTAU register. An active 6 ms interrupt signals that from this event there is a time frame of 3 basic frames duration (4.5 ms) for the write access to the EOCW register.

The 12 ms interrupt serves as time reference for the write access to the M4W and M56W registers. From the point of time the 12 ms interrupt goes active there is a time window of 7 basic frames to overwrite the register values. The programmed data will be sent out with the next U-superframe.

Note that the point of time when the 6 ms and 12 ms interrupts are generated within basic frame #1 and #5 is not fixed and may vary.

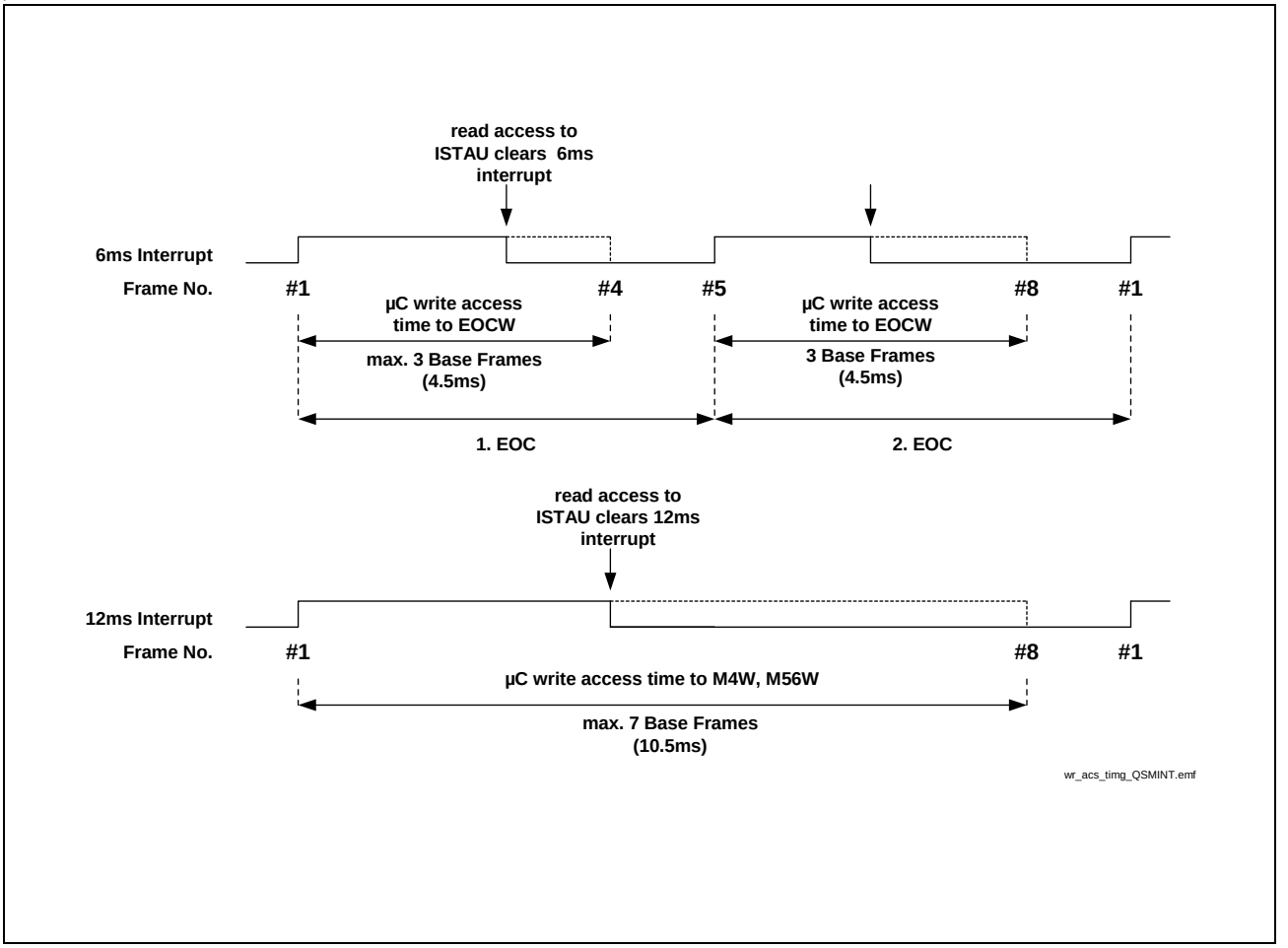


Figure 35 Write Access Timing

The **read access timing** is illustrated in **Figure 36**. An interrupt source of the same name is associated with each read register (EOCR, M4R, M56R). An EOC interrupt indicates that the value of the EOCR register has been changed and updated. So do the M4 and M56 interrupts. Note that unlike the 6 ms and 12 ms interrupts the ’read’ interrupts are only generated on change of the register value and do not occur periodically.

The EOC, M4 and M56 interrupt bits are all accommodated in the ISTAU register.

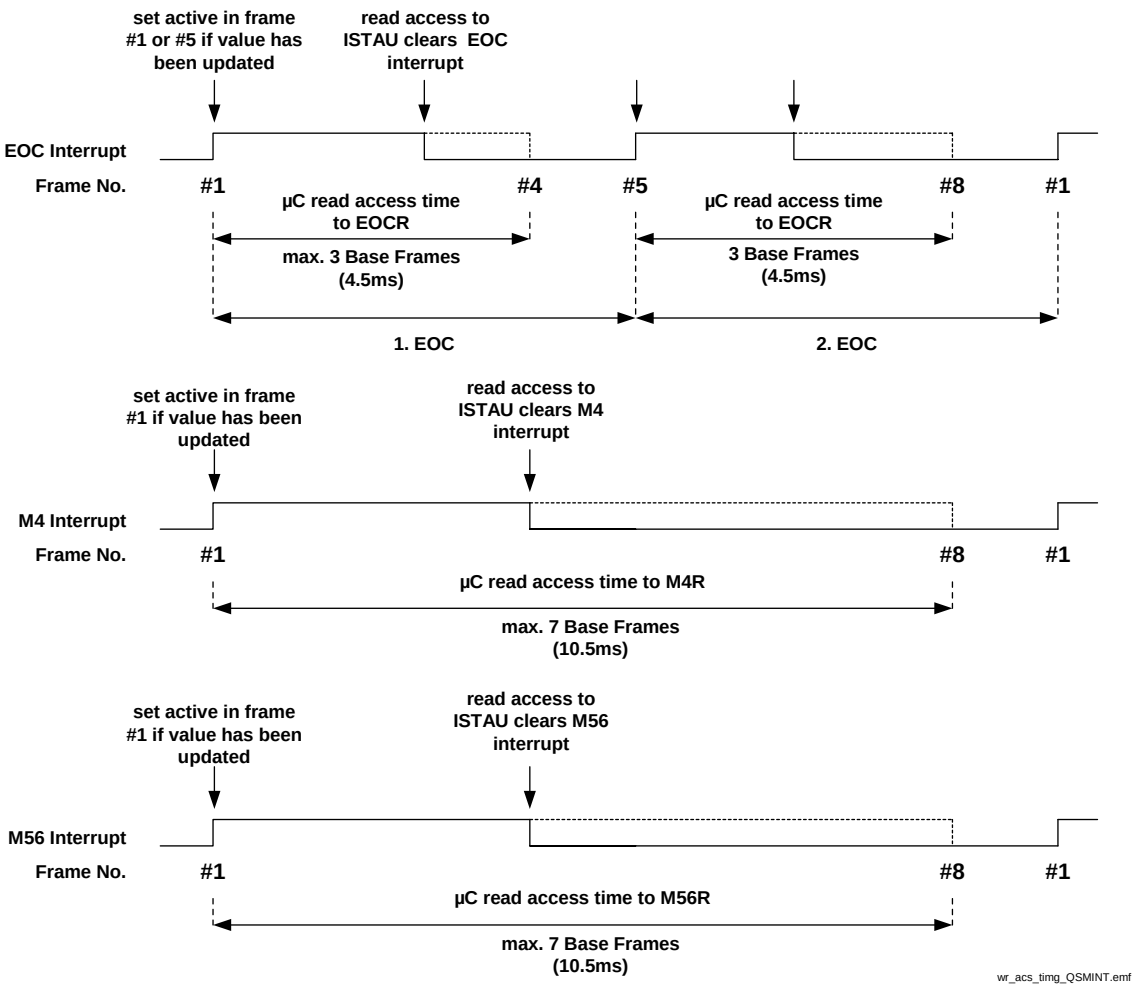


Figure 36 Read Access Timing

2.4.3 Processing of the EOC

2.4.3.1 EOC Commands

The EOC command consists of an address field, a data/message indicator and an eight-bit information field. With the address field the destination of the transmitted message/ data is defined. Addresses are defined for the NT, 6 repeater stations and broadcasting.

The data/message indicator needs to be set to (1) to indicate that the information field contains a message. If set to (0), numerical data is transferred to the NT. Currently no numerical data transfer to or from the NT is required.

Table 17 Coding of EOC-Commands

EOC					
Address Field	**Data/ Message Indicator**	**Information**	**O (rigin) D (estination)**		**Message**
a1a2a3	**d/m**	**i1 i2 i3 i4 i5 i6 i7 i8**	**LT**	**NT**	
0 0 0	x				NT
111	x				Broadcast
0 01 1 10	x				Repeater stations No. 1 – No. 6
	0				Data
	1				Message
	1	0 1 0 1 0 0 0 0	O	D	LBBD
	1	0 1 0 1 0 0 0 1	O	D	LB1
	1	0 1 0 1 0 0 1 0	O	D	LB2
	1	0 1 0 1 0 0 1 1	O	D	RCC
	1	0 1 0 1 0 1 0 0	O	D	NCC
	1	1 1 1 1 1 1 1 1	O	D	RTN
	1	0 0 0 0 0 0 0 0	D/O	O/D	H
	1	1 0 1 0 1 0 1 0	D	O	UTC

Table 18 Usage of Supported EOC-Commands

Hex-code			**Function**
i1-i8	**D**	**U**	
00	H	H	**Hold**. Provokes no change. The device issues Hold if no NT or broadcast address is used or if the d/m indicator is set to (0).
50	LBBD		**Close complete loop-back (B1, B2, D)**. If this command is detected in NT EOC auto mode the C/I-code ARL is issued by the Q-SMINT®IX U-transceiver.

Table 18 Usage of Supported EOC-Commands(cont'd)

Hex-code			Function
i1-i8	D	U	
51	LB1		**Closes B1 loop-back in NT**. All B1-channel data will be looped back within the Q-SMINT®IX U-transceiver. The bits LB1 and U/IOM® are set in the register LOOP.
52	LB2		**Closes B2 loop-back in NT**. All B2-channel data will be looped back within the Q-SMINT®IX U-transceiver. The bits LB2 and U/IOM® are set in the register LOOP.
53	RCC		**Request corrupt CRC**. Upon receipt the Q-SMINT®IX transmits corrupted (= inverted) CRCs upstream. This allows to test the near end block error counter on the LT-side. The far end block error counter at the Q-SMINT®IX-side is stopped and Q-SMINT®IX-error indications are retained.
54	NCC		**Notify of corrupt CRC**. Upon receipt of NCC the Q-SMINT®IX-block error counters (near-end only) are disabled and error indications are retained. This prevents wrong error counts while corrupted CRCs are sent.
AA		UTC	**Unable to comply**. Message sent instead of an acknowledgment if an undefined EOC-command or d/m bit=0 was received by the Q-SMINT®IX.
FF	RTN		**Return to normal**. With this command all previously sent EOC-commands will be released. The EOCW register is reset to its initial state (FF_H).
XX		ACK	**Acknowledge**. If a defined and correctly addressed EOC-command was received by the Q-SMINT®IX, the Q-SMINT®IX replies by echoing back the received command.

2.4.3.2 EOC Processor

The on-chip EOC-processor is responsible for the correct insertion and extraction of EOC-data on the U-interface. The EOC-processor can be programmed either to auto mode or to transparent modes (see **Chapter 2.4.3.3**).

Figure 37 shows the registers and pins that are involved when EOC data is transmitted and received.

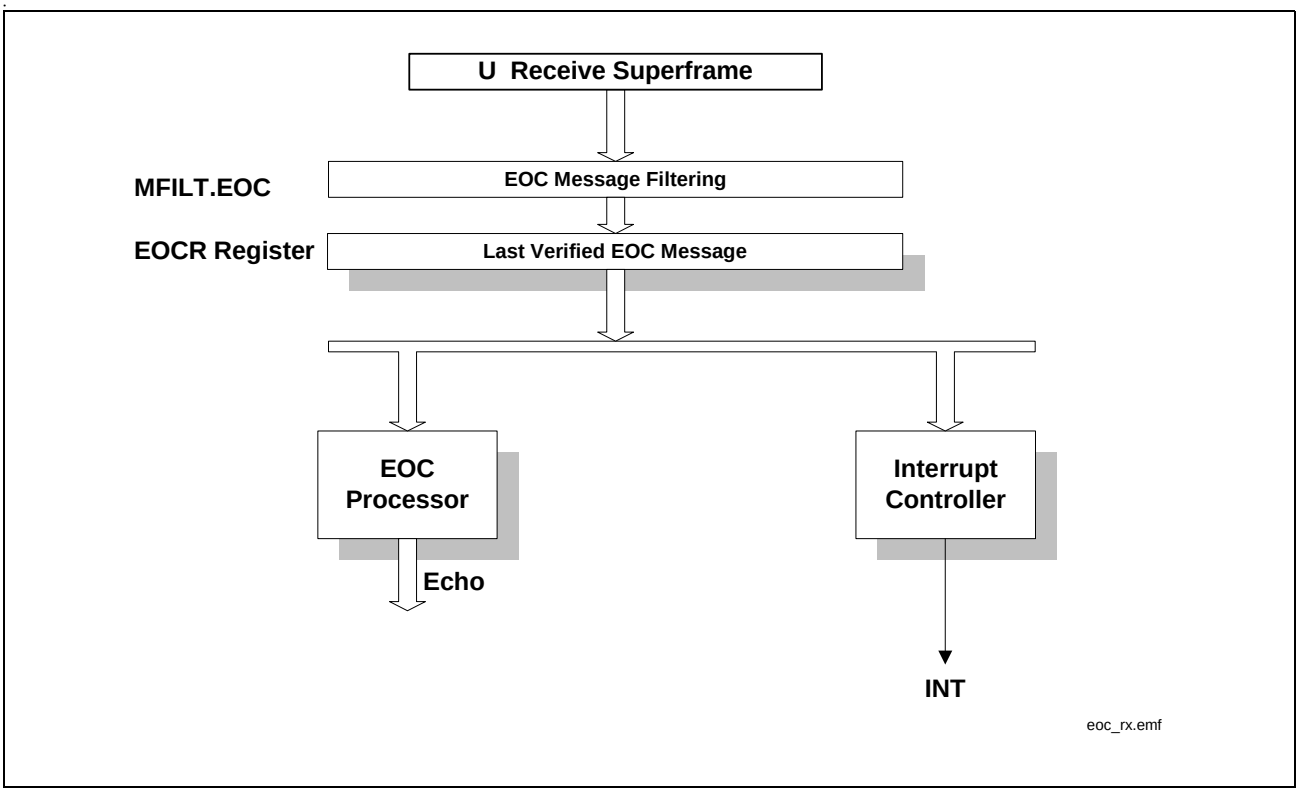


Figure 37 EOC Message Reception

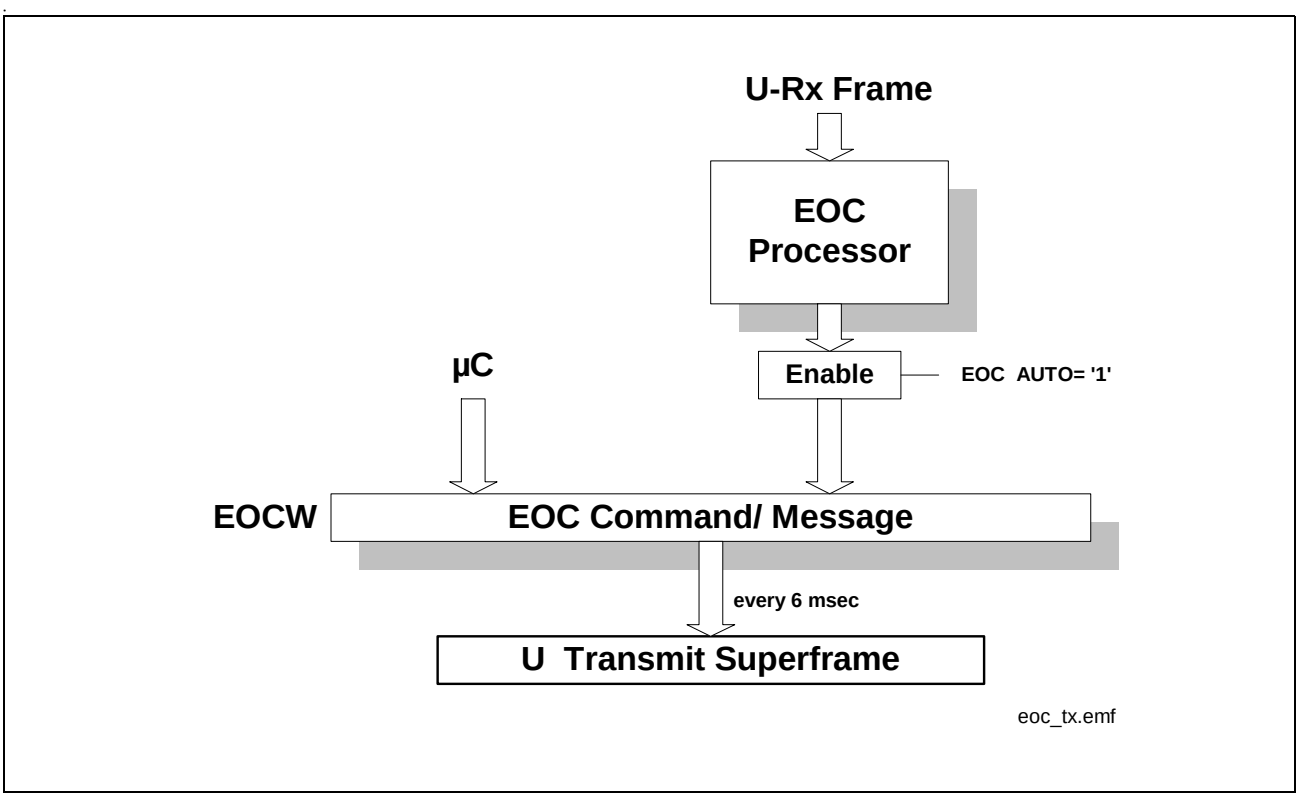


Figure 38 EOC Command/Message Transmission

2.4.3.3 EOC Operating Modes

The EOC operating modes are programmable in the MFILT register (see **Chapter 4.11.2**)

EOC Auto Mode

- **Acknowledgement:** All received EOC-frames are echoed back to the exchange immediately without triple-last-look. If an address other than $(000)_B$ or $(111)_B$ is received, a HOLD message with address $(000)_B$ is returned. However there is an exception: The Q-SMINT®IX will send a 'UTC' after three consecutive receptions of d/m = 0 or after an undefined command.
- **Latching:** All detected EOC-commands, i.e. LBBD, RCC etc., are latched. Multiple subsequent valid EOC-commands are executed in parallel, as long as they are not disabled with the EOC 'RTN' command or a deactivation.
- **Reporting:** With the triple-last-look criterion fulfilled the new EOC-command will be reported by an interrupt, independently of the address used and the status of the d/m indicator. The triple last look criterion implies that the new verified message is different to the last TLL-verified message.
- **Execution:** The EOC-commands listed in **Table 17** will be executed automatically by the U-transceiver if they were addressed correctly (000_B or 111_B) and the d/m bit was set to message (1). The execution of a command is performed only after the "triple-last-look" criterion is met.

EOC Transparent Mode 6 ms

- **Acknowledgement:** There is no automatic acknowledgement in transparent mode. Therefore the external µC has to perform the EOC-Procedure. 2 msec must be available for the report and the subsequent access of the transmit EOC data of the next outgoing EOC-frame.
- **Latching:** No latching is performed due to no execution.
- **Reporting:** The received EOC-frame is reported to the µC by an interrupt every 6 ms. Verification, acknowledgment and execution of the received command have to be initiated by an external controller. The µC can program back all defined test functions (close/open loops, send corrupted CRCs). In the transmit direction, the last written EOC-code from the µC is used.
- **Execution:** No automatic execution in transparent modes. The appropriate actions can be programmed by the µC.

Transparent mode with 'On Change bit' active

- **Acknowledgment:** There is no automatic acknowledgement in transparent mode. For details see above.
- **Latching:** No latching is performed due to no execution.

– **Reporting:** This mode is almost identical to the Transparent Mode 6 ms. But a report to the µC by an interrupt takes place only, if a change in the EOC message has been detected.
– **Execution:** No automatic execution in transparent modes. The appropriate actions can be programmed by the µC.

Transparent mode with TLL active

– **Acknowledgement:** There is no automatic acknowledgment in transparent mode. For details see above.
– **Latching:** No latching is performed due to no execution.
– **Reporting:** This mode is almost identical to the Transparent Mode 6 ms. But a report to the µC by an interrupt takes place only, if the new EOC command has been detected in at least three consecutive EOC messages.
– **Execution:** No automatic execution in transparent modes. The appropriate actions can be programmed by the µC.

2.4.3.4 Examples for different EOC modes

General

In the following examples some letters like A,B,C are used to symbolize EOC command. There are also particular EOC commands mentioned which indicate special system behavior (e.g. UTC, H). The examples are shown in tables.

EOC Automode

Table 19 EOC Auto Mode

remarks	immediately akcn.			immediately akcn.			NO report to system interface	wrong address -> H					undef. command or d/m=0					
input from µC	Access to EOCW register has direct impact on EOC TX.																	
EOC TX	A	A	A	B	A	A	A	H	H	H	D	D	UTC	UTC	A	D	D	UTC
EOC RX	A	A	A	B	A	A	A	C	C	C	D	D	D	D	A	D	D	D
report to µC			A							C			D					D

- A, B: EOC commands with correct address, d/m bit = 1 and defined command.
- C: EOC command with wrong address. Immediately acknowledged with H.
- D: EOC command which is not defined or d/m bit = 0. Acknowledgement after TLL with UTC.

Transparent mode 6 ms)

Table 20 Transparent mode 6 ms

remarks													
input from µC	A				B			C			D		
EOC TX	A	A	A	A	B	B	B	C	C	C	D	D	D
EOC RX	C	A	B	C	C	A	A	A	A	B	B	B	B
report to µC	C	A	B	C	C	A	A	A	A	B	B	B	B

Transparent mode '@change'

Table 21 Transparent mode '@change'

remarks													
input from µC	A				B			C				D	
EOC TX	A	A	A	A	B	B	B	C	C	C	C	D	D
EOC RX	C	A	B	C	C	A	A	A	A	A	B	B	B
report to µC		A	B	C		A					B		

Transparent mode TLL

Table 22 Transparent mode TLL

remarks				saturation					single EOC 'B' interrupts TLL							saturnation	
input from µC	A				B					C				D			
EOC TX	A	A	A	A	B	B	B	B	B	C	C	C	C	D	D	D	D
EOC RX	C	C	C	C	C	A	A	A	B	A	A	A	B	B	B	B	B
report to µC			C					A				A			B		

2.4.4 Processing of the Overhead Bits M4, M5, M6

2.4.4.1 M4 Bit Reporting to the µC

Four different validation modes can be selected and take effect on a **per bit base**. Only if the received M4 bit change has been approved by the programmed filter algorithm a report to the µC is triggered. The following filter algorithms are provided and can be programmed in the MFILT register:

- On Change
- **Triple-Last-Look (TLL)** coverage
- **CRC** coverage

Note that unlike the M4 bits the M56 bits are not included in the CRC generation!

- **CRC and TLL** coverage

2.4.4.2 M4 Bit Reporting to State Machine

Some M4 bits, ACT, DEA and UOA, have two destinations, the state machine and the µC. Regarding these bits Triple-Last-Look (TLL) is applied by default before the changed status is input to the state machine. Via the MFILT register the user can decide whether the M4 bits which are input to the state machine shall be approved

- by **TLL** (default setting, since TLL is a Bellcore requirement) or
- by the same verification mode as selected for reporting to the µC.

The reset values before activation are ACT=0, DEA=1, UOA=0.

2.4.4.3 M5, M6 Bit Reporting to the µC

By default changes in the received spare bits M51, M52, and M61 are reported to the µC only if no CRC violation has been detected. However the user has the choice to program one of the following two options in the MFILT register (for details see **Chapter 4.11.2**):

- Same validation algorithm is applied to M5 and M6 bits as programmed for M4 bits
- **On Change**

In transmit direction these bits are set by default to ’1’ if they are not explicitly set by an µC access (via M56W register).

2.4.4.4 Summary of M4, M5, M6 Bit Reporting

Figure 39 summarizes again the various filtering options that are provided for the several maintenance channel bits.

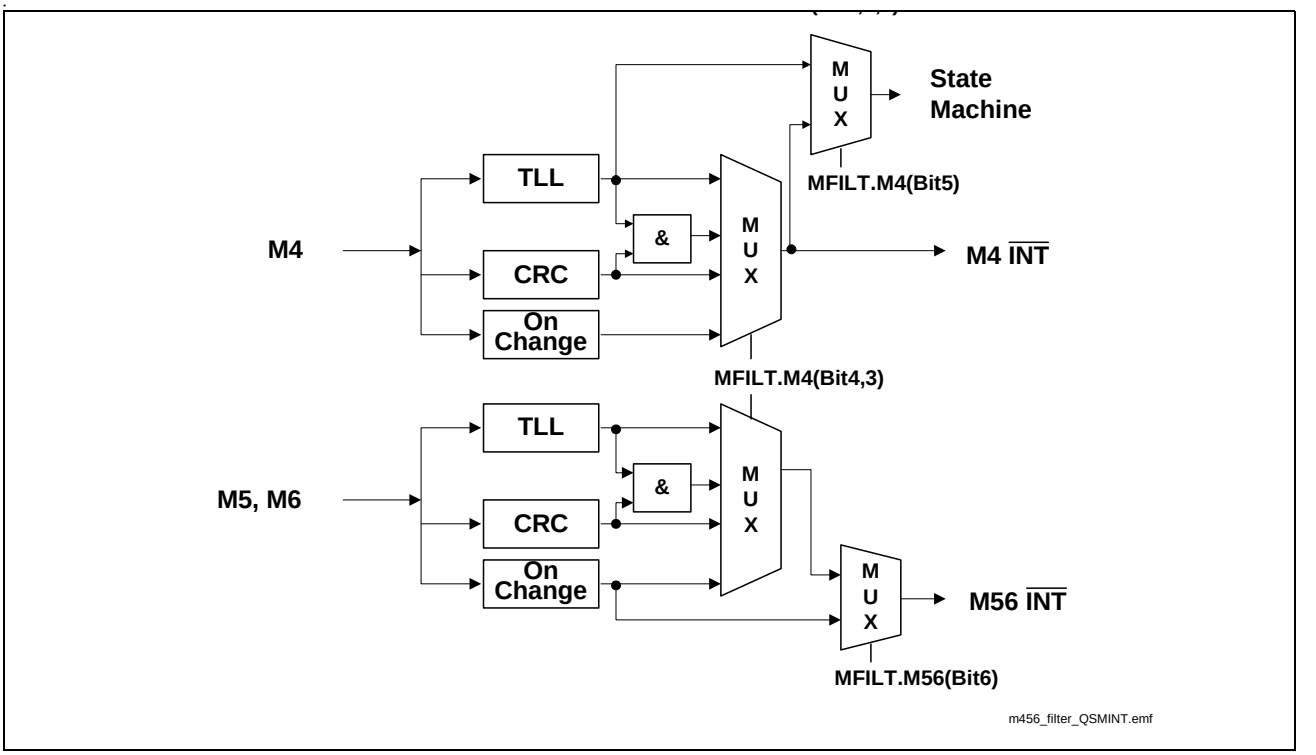


Figure 39 Maintenance Channel Filtering Options

Figure 40 illustrates the point of time when a detected M4, M5, M6 bit change is reported to the µC and when it is reported to the state machine:

- **towards the µC** reports are always sent after one complete U-superframe was received,
- whereas **towards the state machine** M4-bit changes (ACT, DEA, UOA, SAI) are instantly passed on as soon as they were approved. In context of Figure 40 this means that a verified ACT bit change is already reported at the end of basic frame #1 instead of the end of basic frame #8.

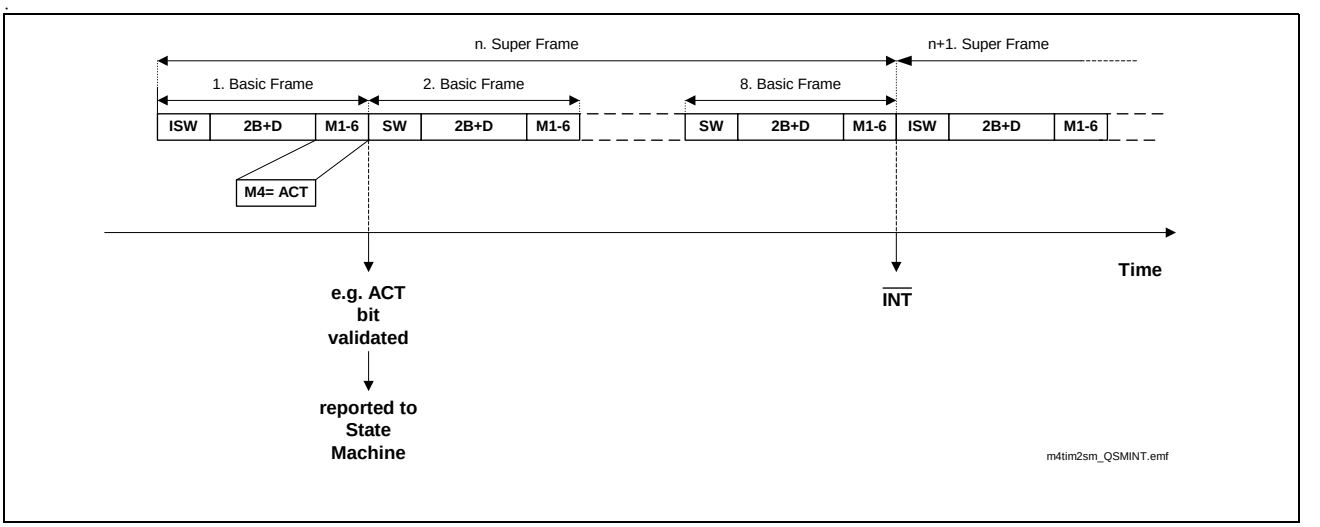


Figure 40 M4 Bit Report Timing (Statemachine vs. µC)

However, if the same filter is selected towards the state machine as programmed towards the µC, the user has to be aware that if CRC mode is active, the state machine is informed at the end of the next U-superframe.

2.4.5 M4, M5, M6 Bit Control Mechanisms

Figure 41 and **Figure 42** show the control mechanisms that are provided for M4, M5 and M6 bit data:

Via the **M4WMASK** register the user can selectively program which M4 bits are externally controlled and which are set by the internal state machine or dedicated pins (PS1, PS2). If one M4WMASK bit is set to ’0’ then the M4 bit value in the U-transmit frame is determined by the bit value at the corresponding bit position in the M4W register.

Note: By bit 6 in the M4WMASK register it can be selected whether SAI is set by the state machine or by µC access and whether the value of the received UOA bit is reported to the state machine or UOA= ’1’ is signalled.

Via the **M4RMASK** register the user can selectively program which M4 bit changes shall cause an report to the µC.

The **M4W** register latches the M4 bits that are sent with the next available U-superframe.

The **M4R** register contains the last validated M4 bit data.

The default value of M51, M52 and M61 can be overwritten at any time by use of register **M56W**. **M56R** latches the last received and verified M5, M6 bit data.

The control of the FEBE bit is performed by the CRC-Processor, see **Chapter 2.4.6**.

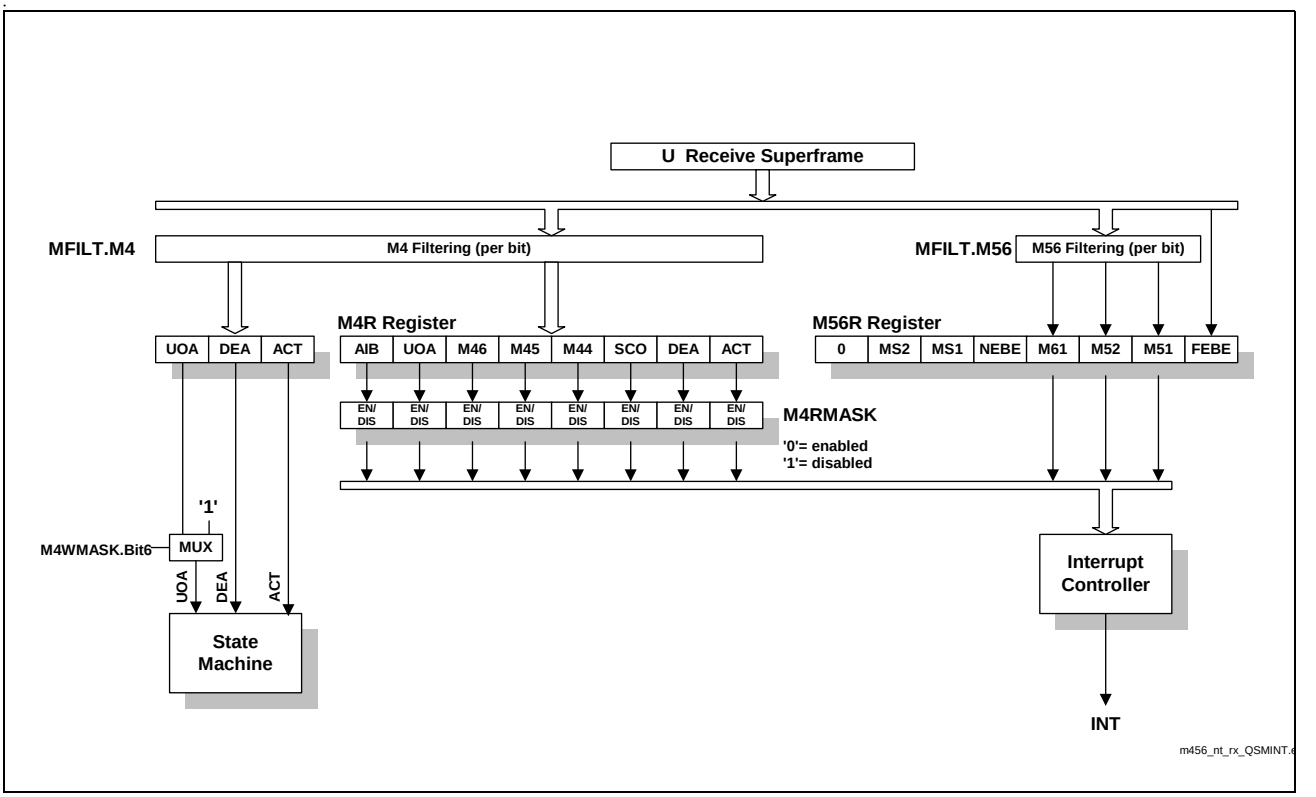


Figure 41 M4, M5, M6 Bit Control in Receive Direction

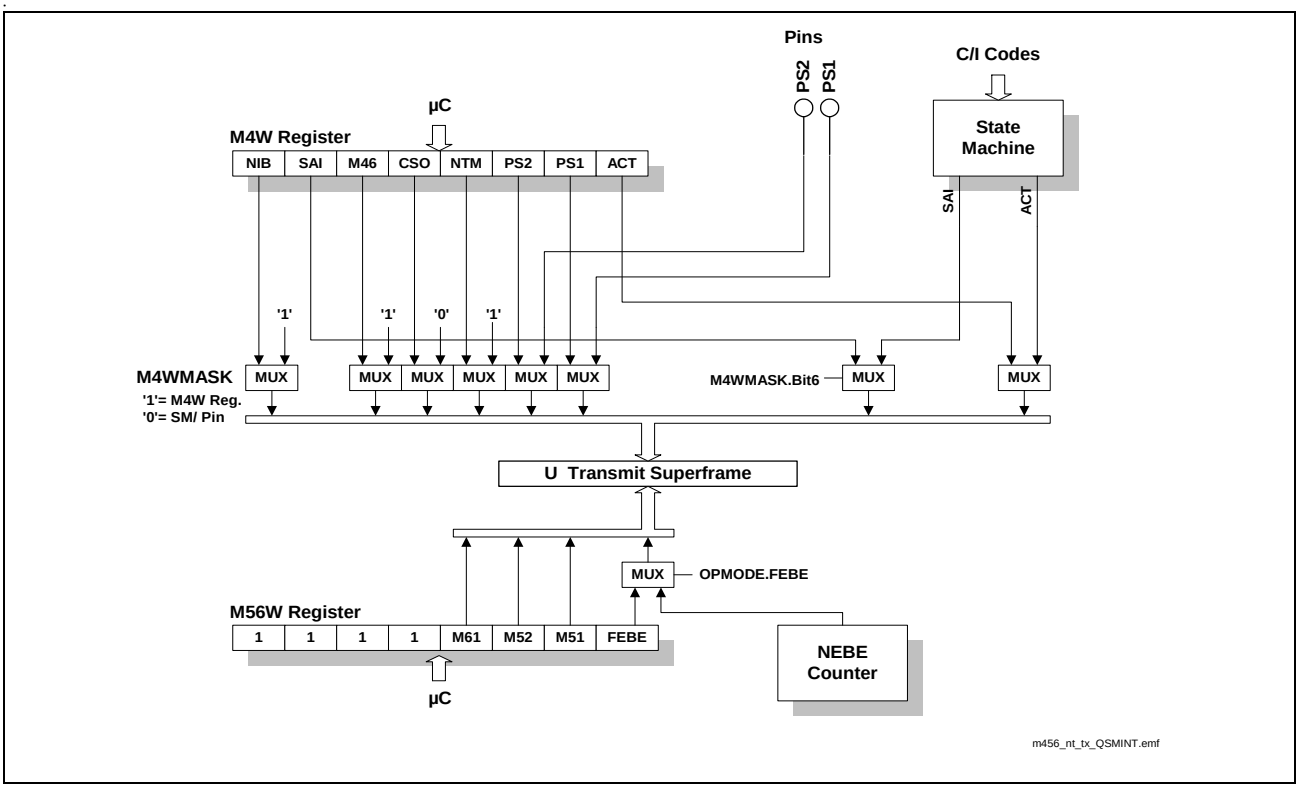


Figure 42 M4, M5, M6 Bit Control in Transmit Direction

2.4.6 Cyclic Redundancy Check / FEBE bit

An error monitoring function is implemented covering the 2B + D and M4 data transmission of a U-superframe by a Cyclic Redundancy Check (CRC).

The computed polynomial is:

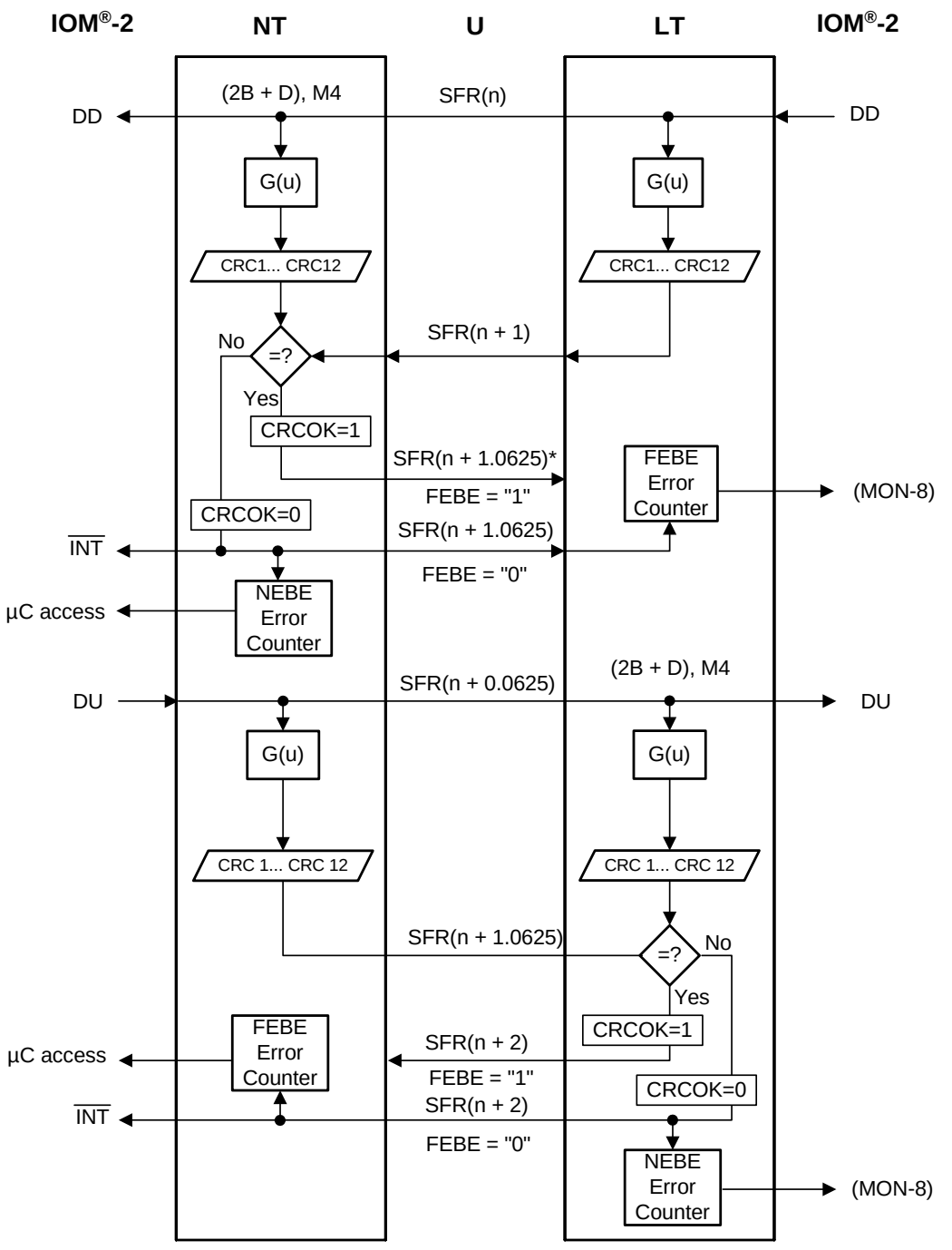
$$G(u) = u^{12} + u^{11} + u^3 + u^2 + u + 1$$

(+ modulo 2 addition)

The check digits (CRC bits CRC1, CRC2, …, CRC12) generated are transmitted in the U-superframe. The receiver will compute the CRC of the received 2B + D and M4 data and compare it with the received CRC-bits generated by the transmitter.

A CRC-error will be indicated to both sides of the U-interface, as a NEBE (Near-end Block Error) on the side where the error is detected, as a FEBE (Far-end Block Error) on the remote side. The FEBE-bit will be placed in the next available U-superframe transmitted to the originator.

Figure 43 illustrates the CRC-process.



*0.0625 of a SFR is the 60 Quats offset of the NT transmit data.

crc_QSMINT.emf

Figure 43 CRC-Process

2.4.7 Block Error Counters

The U-transceiver provides internal counters for far-end and near-end block errors. This allows a comfortable surveillance of the transmission quality at the U-interface. In addition, the occurrence of near-end errors, far-end errors, and the simultaneous occurrence of both errors are reported to the µC by an interrupt at the beginning of the following receive-superframe.

A block error is detected each time when the calculated checksum (CRC) of the received data does not correspond to the control checksum transmitted in the successive superframe. One block error thus indicates that one U-superframe has not been transmitted correctly. No conclusion with respect to the number of bit errors is therefore possible.

2.4.7.1 Near-End and Far-End Block Error Counter

A near-end block error (NEBE) indicates that the error has been detected in the receive direction (i.e. NEBE in the NT = LT => NT error). Each detected NEBE-error increments the 8-bit NEBE-counter. When reaching the maximum count, counting is stopped and the counter value reads (FF_H).

A far-end block error identifies errors in transmission direction (i.e. FEBE in the NT = NT => LT-error). FEBE errors are processed in the same manner as NEBE-errors.

The FEBE and NEBE counter values can be read in registers FEBE and NEBE. The counter is cleared after read. The counters are also reset to 00_H in all states except the states listed in **Table 16**.

2.4.7.2 Testing Block Error Counters

Figure 44 illustrates how near- and far-end block error counters can be tested. Transmission errors are simulated with artificially corrupted CRCs. With two commands the cyclic redundancy checksum can be inverted in the upstream and downstream direction. A third command offers to invert single FEBE-bits.

- **EOC Command NCC:**
  Requests the Q-SMINT®IX to notify corrupted CRCs.
  The functional behavior of the Q-SMINT®IX and the NEBE-counter depends on the mode selected:
  – EOC auto mode:
  NEBE-detection stopped: no NEBE interrupt generated and NEBE-counter disabled
  – EOC transparent mode
  NEBE-detection enabled: NEBE interrupt generated and NEBE-counter enabled
- **EOC Command RCC:**
  Requests the Q-SMINT®IX to send corrupt CRCs. After issuing RCC near-end block errors will be registered on the LT-side.

The functional behavior of the Q-SMINT®IX and the FEBE-counter depends on the mode selected:

– EOC auto mode:
The Q-SMINT®IX will react with a permanently inverted upstream CRC.
FEBE-detection stopped: no FEBE interrupt generated and FEBE-counter disabled

– EOC transparent mode
The external µC must react on RCC by programming TEST.CCRC = ’1’.
FEBE-detection enabled: FEBE interrupt generated and FEBE-counter enabled

- **EOC command RTN:**
Disables all previously sent EOC commands.
- **M56W.FEBE**
By setting / resetting M56W.FEBE (M56W.FEBE can only be set and controlled externally if OPMODE.FEBE is set to ’1’), the FEBE bit of the next available U-frame can be set / reset . Therefore, it is possible to predict exactly the FEBE-counter value.

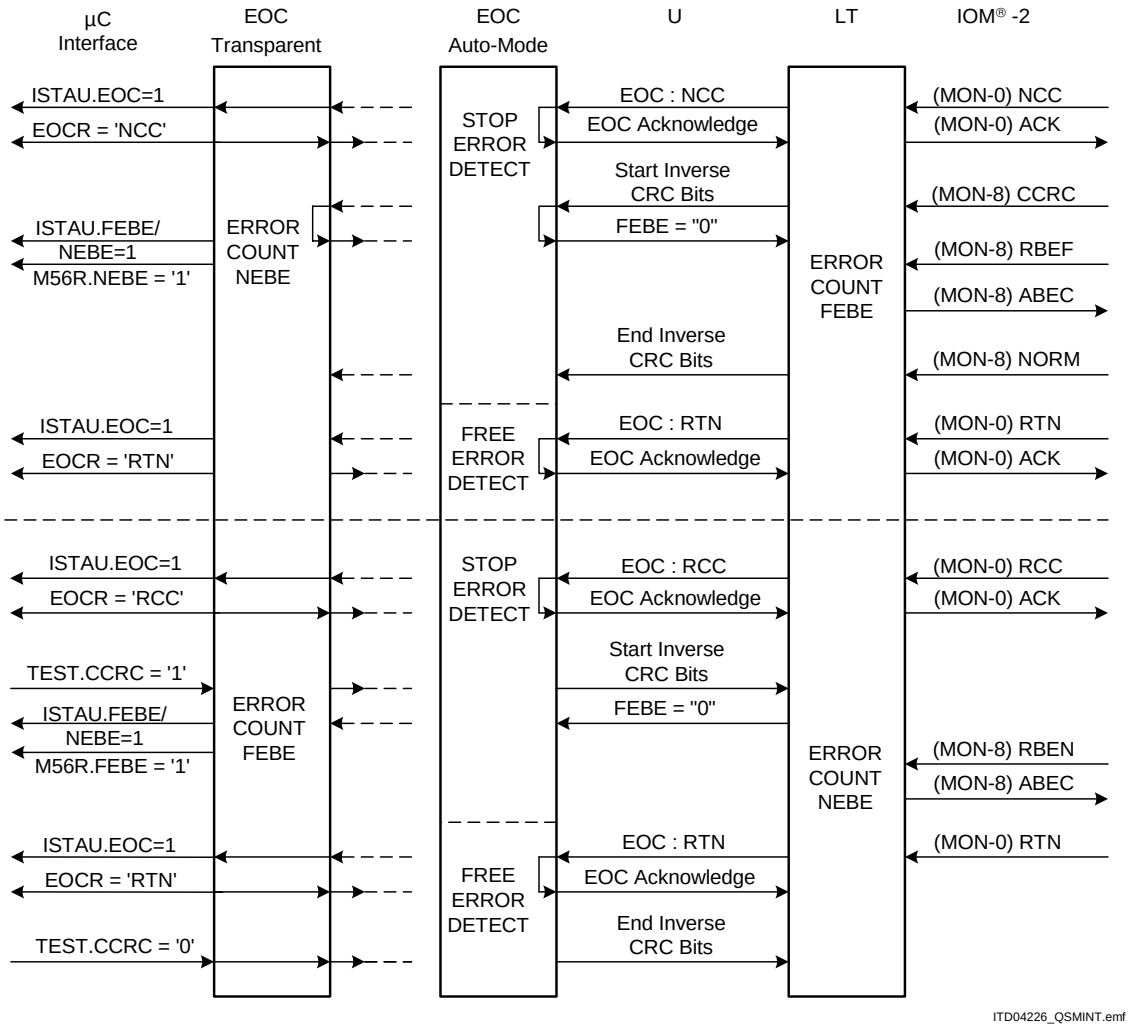


Figure 44 Block Error Counter Test

2.4.8 Scrambling/ Descrambling

The scrambling algorithm ensures that no sequences of permanent binary 0s or 1s are transmitted. The scrambling / descrambling process is controlled fully by the Q-SMINT®IX . Hence, no influence can be taken by the user.

2.4.9 C/I Codes

The operational status of the U-transceiver is controlled by the Control/Indicate channel (C/I-channel).

Table 23 presents all defined C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM®-2-frames (double last-look criterion).

Note: Unconditional C/I-Commands must be applied for at least 4 IOM®-2 frames for reliable recognition by the U-transceiver.

Commands have to be applied continuously on DU until the command is validated by the U-transceiver and the desired action has been initiated. Afterwards the command may be changed.

An indication is issued permanently by the U-transceiver on DD until a new indication needs to be forwarded. Because a number of states issue identical indications it is not possible to identify every state individually.

Table 23 U - Transceiver C/I Codes

Code	IN	OUT
0000	TIM	DR
0001	RES	–
0010	–	–
0011	–	–
0100	EI1	EI1
0101	SSP	–
0110	DT	–
0111	–	PU
1000	AR	AR
1001	–	–
1010	ARL	ARL
1011	–	–
1100	AI	AI
1101	–	–
1110	–	AIL
1111	DI	DC

AI: Activation Indication

AIL: Activation Indication Loop

AR: Activation Request

ARL: Activation Request Local Loop

DC: Deactivation Confirmation

DI: Deactivation Indication

DR: Deactivation Request

DT: Data Through test mode

EI1: Error Indication 1

PU: Power-Up

RES: Reset

SSP: Send Single Pulses test mode

TIM: Timing request

2.4.10 State Machines for Line Activation / Deactivation

2.4.10.1 Notation

The state machines control the sequence of signals at the U-interface that are generated during the start-up procedure. The informations contained in the following state diagrams are:

– State name
– U-signal transmitted
– Overhead bits transmitted
– C/I-code transmitted
– Transition criteria
– Timers

Figure 45 shows how to interpret the state diagrams.

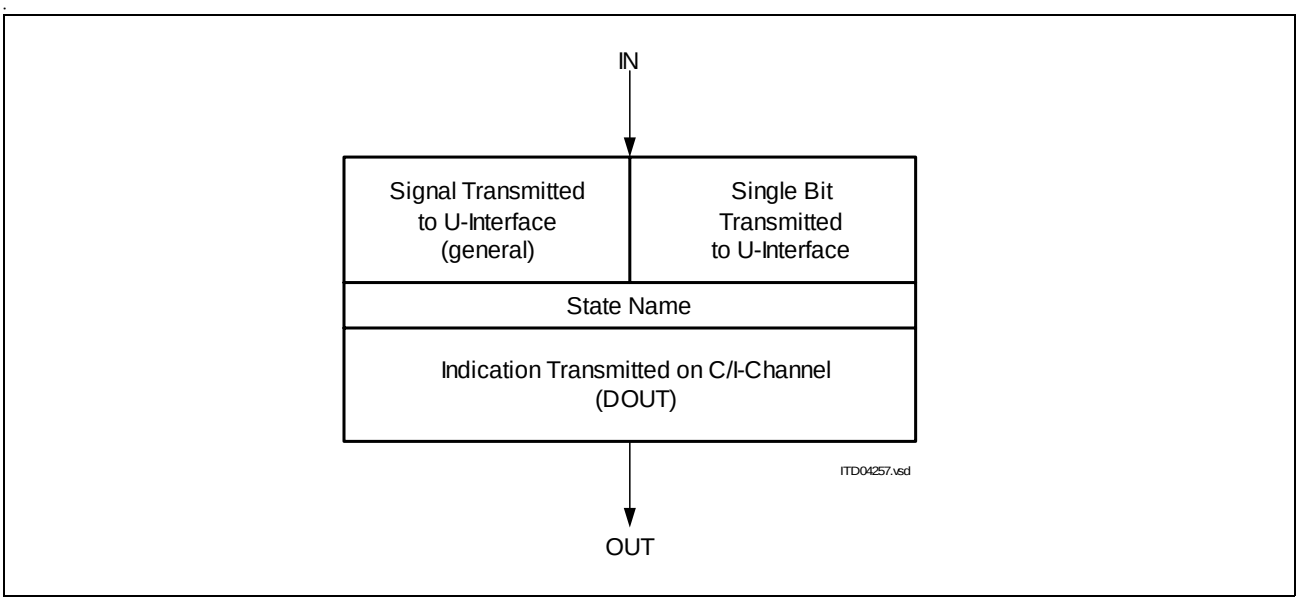


Figure 45 Explanation of State Diagram Notation

Combinations of transition criteria are possible. Logical “AND” is indicated by “&” (TN & DC), logical “OR” is written “or” and for a negation “/” is used. The start of a timer is indicated with “TxS” (“x” being equivalent to the timer number). Timers are always started when entering the new state. The action resulting after a timer has expired is indicated by the path labelled “TxE”.

2.4.10.2 Standard NT State Machine (IEC-Q / NTC-Q Compatible)

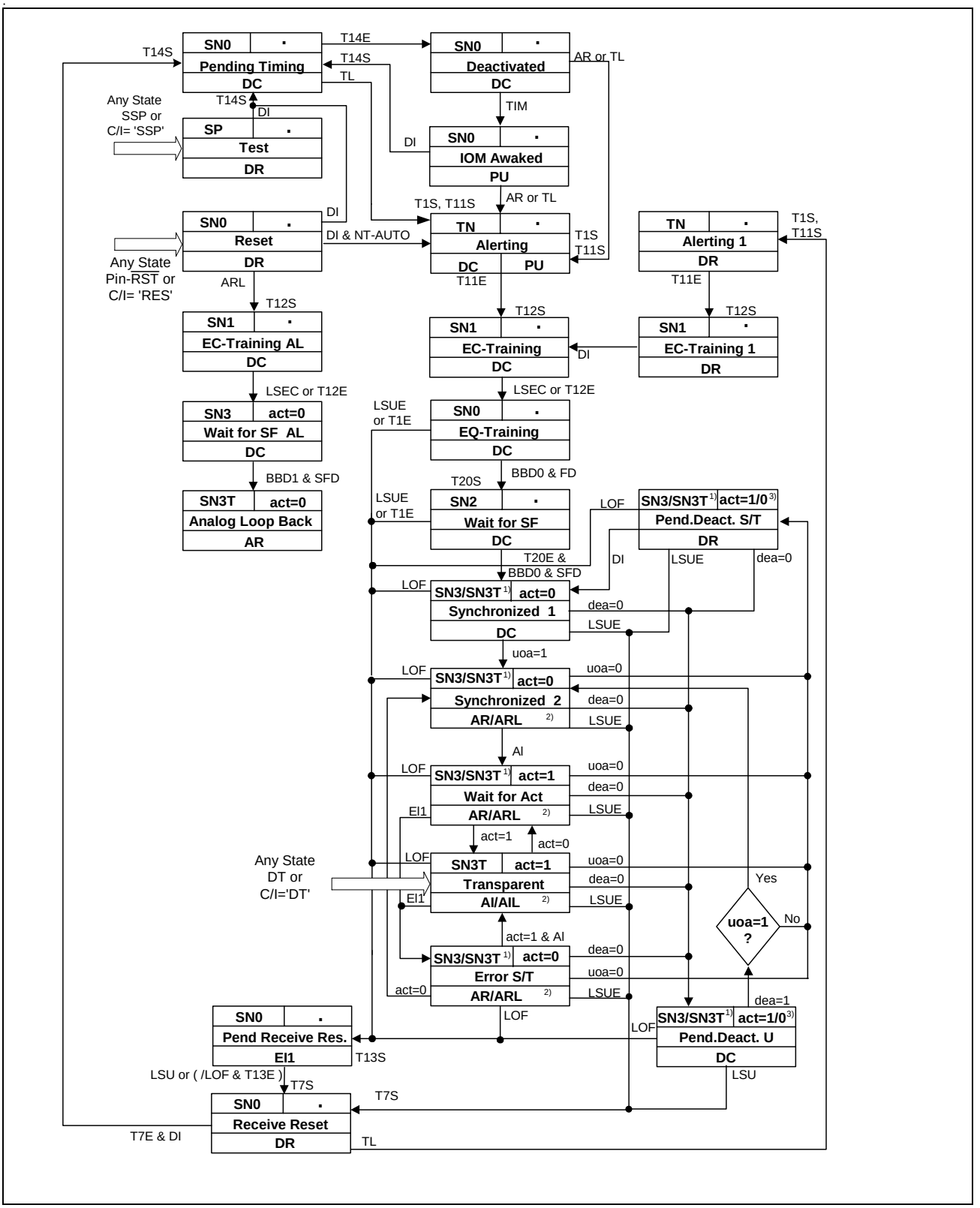


Figure 46 Standard NT State Machine (IEC-Q / NTC-Q Compatible) (Footnotes: see "Dependence of Outputs" on Page 91)

*Note: The test modes 'Data Through' (DT) and 'Send Single Pulses' (SSP) are invoked via C/I codes 'DT' and 'SSP' according to **Table 23**. Setting SRES.RES_U to '1' forces the U-transceiver into test mode 'Quiet Mode' (QM), i.e. the U-transceiver is hardware reset.*
*If the Metallic Loop Termination is used, then the U-transceiver is forced into the states 'Reset' and 'Transparent' by valid pulse streams on pin MTI according to **Table 30**.*

Note: If the state machine is in state 'Deactivated' and the IOM®-2 clocks are not running, then the transitions to 'IOM®-2 Awaked' or 'Alerting' can be invoked by writing directly the corresponding C/I-code to register UCIW via the µC interface.

2.4.10.3 Inputs to the U-Transceiver:

C/I-Commands:

AI — Activation Indication
The downstream device issues this indication to announce that its layer-1 is available. The U-transceiver informs the LT side by setting the "ACT" bit to "1".

AR — Activation Request
The U-transceiver is requested to start the activation process by sending the wake-up signal TN.

ARL — Activation Request Local Loop-back
The U-transceiver is requested to operate an analog loop-back (close to the U-interface) and to begin the start-up sequence by sending SN1 (without starting timer T1). This command may be issued only after the U-transceiver has been HW- or SW-reset. This eases that the EC- and EQ-coefficient updating algorithms converge correctly. The ARL-command has to be issued continuously as long as the loop-back is required.

DI — Deactivation Indication
This indication is used during a deactivation procedure to inform the U-transceiver that it may enter the deactivated (power-down) state.

DT — Data Through
This unconditional command is used for test purposes only and forces the U-transceiver into the "Transparent" state.

EI1 — Error Indication 1
The downstream device indicates an error condition (loss of frame alignment or loss of incoming signal). The U-transceiver informs the LT-side by setting the ACT-bit to "0" thus indicating that transparency has been lost.

RES — Reset
Unconditional command which resets the U-transceiver.

SSP — Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface.

TIM Timing
The U-transceiver is requested to enter state 'IOM®-2 Awaked'.

U-Interface Events:

ACT = 0/1 ACT-bit received from LT-side.
- ACT = 1 requests the U-transceiver to transmit transparently in both directions. In the case of loop-backs, however, transparency in both directions of transmission is established when the receiver is synchronized.
- ACT = 0 indicates that layer-2 functionality is not available.

DEA = 0/1 DEA-bit received from the LT-side
- DEA = 0 informs the U-transceiver that a deactivation procedure has been started by the LT-side.
- DEA = 1 reflects the case when DEA = 0 was detected by faults due to e.g. transmission errors and allows the U-transceiver to recover from this situation.

UOA = 0/1 UOA-bit received from network side
- UOA = 0 informs the U-transceiver that only the U-interface is to be activated. The S/T-interface must be deactivated.
- UOA = 1 requests the S/T-interface (if present) to activate.

Timers

The start of timers is indicated by TxS, the expiry by TxE. **Table 24** shows which timers are used:

Table 24 Timers Used

Timer	Duration (ms)	Function	State
T1	15000	Supervisor for start-up	
T7	40	Hold time	Receive reset
T11	9	TN-transmission	Alerting
T12	5500	Supervisor EC-converge	EC-training
T13	15000	Frame synchronization	Pend. receive reset
T14	0.5	Hold time	Pend. timing
T20	10	Hold time	Wait for SF

2.4.10.4 Outputs of the U-Transceiver:

The following signals and indications are issued on IOM®-2 (C/I-indications) and on the U-interface (predefined U-signals):

C/I-Indications

AI — Activation Indication
The U-transceiver has established transparency of transmission. The downstream device is requested to establish layer-1 functionality.

AIL — Activation Indication Loopback
The U-transceiver has established transparency of transmission. The downstream device is requested to establish a loopback #2.

AR — Activation Request
The downstream device is requested to start the activation procedure.

ARL — Activation Request Loop-back
The U-transceiver has detected a loop-back 2 command in the EOC-channel and has established transparency of transmission in the direction IOM®-2 to U-interface. The downstream device is requested to start the activation procedure and to establish a loopback #2.

DC — Deactivation Confirmation
Idle code on the IOM®-2-interface.

DR — Deactivation Request
The U-transceiver has detected a deactivation request command from the LT-side for a complete deactivation or a S/T only deactivation. The downstream device is requested to start the deactivation procedure.

EI1 — Error Indication 1
The U-transceiver has entered a failure condition caused by loss of framing on the U-interface or expiry of timer T1.

Signals on U-Interface

The signals SNx, TN and SP transmitted on the U-interface are defined in **Table 25**.

Table 25 U-Interface Signals

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
TN [1)]	± 3	± 3	± 3	± 3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal
SN3T	present	present	normal	normal
Test Mode				
SP [2)]	test signal	test signal	test signal	test signal

Note: [1] Alternating ± 3 symbols at 10 kHz.

Note: [2] 4 Options for the test signal can be selected by register TEST:
A 40 kHz signal composed by alternating +/-3 or +/-1 transmit pulses.
A series of single pulses spaced at intervals of 1.5 ms; Either alternating +/-1 or +/-3 pulses can be selected.

Input Signals of the State Machine and related U-Signals

The table below summarizes the input signals that control the NT state machine and that are extracted from the U-interface signal sequences.

LOF	**Loss of framing** This condition is fulfilled if framing is lost for 573 ms.
LSEC	**Loss of signal behind echo canceller** Internal Signal which indicates that the echo canceller has converged
LSU	**Loss of Signal on U-Interface** This signal indicates that a loss of signal level for a duration of 3 ms has been detected on the U-interface. This short response time is relevant in all cases where the NT waits for a response (no signal level) from the LT-side.
LSUE	**Loss of Signal on U-Interface - Error condition** After a loss of signal has been noticed, a 588 ms timer is started. When it has elapsed , the LSUE-criterion is fulfilled. This long response time (see also LSU) is valid in all cases where the NT is not prepared to lose signal level i.e. the LT has stopped transmission because of loss of framing, an unsuccessful activation, or the transmission line is interrupted.
FD	**Frame Detected**
SFD	**Super Frame Detected**
BBD0 / BBD1	**BBD0/1 Detected** These signals are set if either ’1' (BBD1) or ’0' (BBD0) were detected in 4 subsequent basic frames. It is used as a criterion that the receiver has acquired frame synchronization and both its EC- and EQ-coefficients have converged. BBD0 corresponds to the received signal SL2 in case of a normal activation, BBD1 corresponds to the internally received signal SN3 in case of analog loop back.
TL	**Awake tone detected** The U-transceiver is requested to start an activation procedure.

Signals on IOM®-2

The Data (B+B+D) is set to all ’1’s in all states besides the states listed in **Table 16**.

Dependence of Outputs

- Outputs denoted with 1) in **Figure 46**:
  Signal output on U_{k0} depends on the received EOC command and on the history of the state machine according to **Table 26**:

Table 26 Signal Output on U_{k0}

EOC Command	History of the State Machine	Signal output on U_{k0}
received ’LBBD’	no influence	SN3T
received no ’LBBD’ or ’RTN’ after an ’LBBD’	state ’Transparent’ has not been reached previously during this activation procedure	SN3
	state ’Transparent’ has been reached previously during this activation procedure	SN3T

- Outputs denoted with 2) in **Figure 46**:
  C/I-code output depends on received EOC-command ’LBBD’ according to **Table 27**:

Table 27 C/I-Code Output

EOC Command	Synchronized 2	Wait for Act	Transparent	Error S/T
received no ’LBBD’ or ’RTN’ after an ’LBBD’	AR	AR	AI	AR
received ’LBBD’	ARL	ARL	AIL	ARL

- Outputs denoted with 3) in **Figure 46**:
  In States ’Pend. Deact. S/T’ and ’Pend. Deact. U’ the ACT-bit output depends on its value in the previous state.
- The value of the issued SAI-bit depends on the received C/I-code: DI and TIM lead to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity of the downstream device.
- If state Alerting is entered from state Deactivated, then C/I-code ’PU’ is issued, else C/I-code ’DC’ is issued.

2.4.10.5 Description of the NT-States

The following states are used:

Alerting

The wake-up signal TN is transmitted for a period of T11 either in response to a received wake-up signal TL or to start an activation procedure on the LT-side.

Alerting 1

“Alerting 1” state is entered when a wake-up tone was received in the “Receive Reset” state and the deactivation procedure on the NT-side was not yet finished. The transmission of wake-up tone TN is started.

Analog Loop-Back

Transparency is achieved in both directions of transmission. This state can be left by making use of any unconditional command.

Deactivated

Only in state Deactivated the device may enter the power-down mode.

EC Training

The signal SN1 is transmitted on the U-interface to allow the NT-receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled.

EC-Training 1

The “EC-Training 1” state is entered if transmission of signal SN1 has to be started and the deactivation procedure on the NT-side is not yet finished.

EC-Training AL

The signal SN1 is transmitted on the U-interface to allow the NT-receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled.

EQ-Training

The receiver waits for signal SL1 or SL2 to be able to update the AGC, to recover the timing phase, to detect the synch-word (SW), and to update the EQ-coefficients.

Error S/T

The downstream device is in an error condition (EI1). The LT-side is informed by setting the ACT-bit to “0” (loss of transparency on the NT-side).

IOM®-2-Awaked

The U-transceiver is deactivated, but may not enter the power-down mode.

Pending Deactivation of S/T

The U-transceiver has received the UOA-bit at zero after a complete activation of the S/T-interface. The U-transceiver requests the downstream device to deactivate by issuing DR.

Pending Deactivation of U-Interface

The U-transceiver waits for the receive signal level to be turned off (LSU) to start the deactivation procedure.

Pending Receive Reset

The “Pending Receive Reset” state is entered upon detection of loss of framing on the U-interface or expiry of timer T1. This failure condition is signalled to the LT-side by turning off the transmit level (SN0). The U-transceiver then waits for a response (no signal level LSU) from the LT-side.

Pending Timing

In the NT-mode the pending timing state assures that the C/I-channel code DC is issued four times before entering the ’Deactivated’ state.

Receive Reset

In state ’Receive Reset’ a reset of the Uk0-receiver is performed, except in case that state ’Receive Reset’ was entered from state ’Pend. Deact. U’. Timer T7 assures that no activation procedure is started from the NT-side for a minimum period of time of T7. This gives the LT a chance to activate the NT.

Reset

In state ’Reset’ a software-reset is performed.

Synchronized 1

State ’Synchronized 1’ is the fully active state of the U-transceiver, while the downstream device is deactivated.

Synchronized 2

In this state the U-transceiver has received UOA = 1. This is a request to activate the downstream device.

Test

The test signal SP is issued as long as C/I=SSP is applied. For further details see **Table 25**.

Transparent

This state is entered upon the detection of ACT = 1 received from the LT-side and corresponds to the fully active state.

Wait for ACT

Upon the receipt of AI, the NT waits for a response (ACT = 1) from the LT-side.

Wait for SF

The signal SN2 is sent on the U-interface and the receiver waits for detection of the superframe.

Wait for SF AL

This state is entered in the case of an analog loop-back and allows the receiver to update the AGC, to recover the timing phase, and to update the EQ-coefficients.

2.4.10.6 Simplified NT State Machine

As an alternative to the activation/deactivation state machine of the U-transceiver known from the IEC-Q [9], a more software friendly state machine can be selected.

In the early days of ISDN, the activation and deactivation procedure in a NT was completely determined by the U- and S-transceiver state machines without a microcontroller being necessary. Intelligent NTs or U-terminals require a microcontroller and software. In this case the software controls both the S-and the U-transceiver state machine.

The simplified U-transceiver state machine was developed to better address the needs and requirements of software running on the microcontroller. The simplified state machine offers the following advantages:

– the software can tell whether the IOM®-2 clocks are active or powered down via the received C/I code
– From the received C/I code the software always knows, what it is expected to do and what options it has. The software does not have to backtrack older C/I codes.

– unnecessary C/I changes at irrelevant state transitions are omitted, hence the number of interrupts is reduced.

All advantages can be offered by the following minor changes to the existing state machine:

Table 28 Changes to achieve Simplified NT State Machine

Change	State	Standard NT State Machine	Simplified NT State Machine
Change of Transmitted C/I -Code			
	Alerting	DC/PU	PU
	EC-Training	DC	PU
	EQ-Training	DC	PU
	Wait for SF	DC	PU
	Synchronized 1	DC	PU
	Pend. Receive Res.	EI1	DR
	Pend. Deact. U.	DC	DR
	Wait for SF AL	DC	DR
	EC-Training AL	DC	DR
	all other States	no changes	
Changed State Transition Criteria			
	Alerting 1 to Alerting	DI	DI or TIM
	EC-Training 1 to EC-Training	DI	DI or TIM
	Pend. Deact. S/T to Synchron. 1	DI	DI or TIM
	all other transition criterias	no changes	
New State Transitions			
	Receive Reset to IOM®-2 Awaked	none	T7E & TIM
	Reset to IOM®-2 Awaked	none	TIM

Table 28 Changes to achieve Simplified NT State Machine(cont'd)

Change	State	Standard NT State Machine	Simplified NT State Machine
	Test to IOM®-2 Awaked	none	TIM
Not Supported State Transitions			
	Reset to Alerting	DI & NTAUTO	none
	all other transitions	no changes	

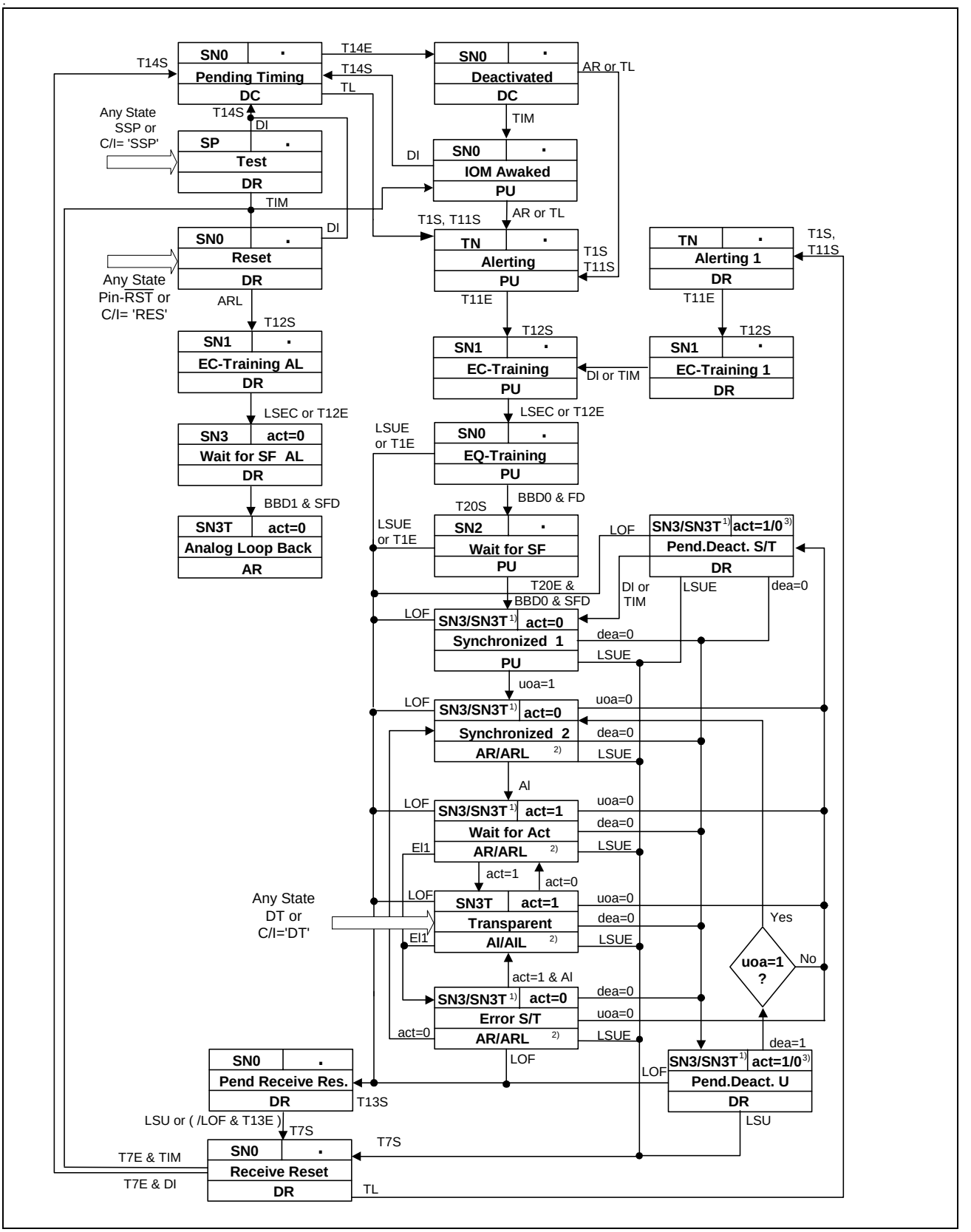


Figure 47 Simplified NT State Machine

Table 29 Appearance of the State Machine to the Software

C/I ind.	Meaning	Options		U-transparent
DR	LT has decided to deactivate or activation was lost: – after an activation or – after an activation attempt or – after reset	DI TIM	Acknowledge and give permission to turn off the clocks Acknowledge, clocks will stay active	no
DC	four IOM®-2 frames with C/I code DC are issued before permission to turn off the clocks	TIM AR any other C/I-code	turn on clocks start U-activation no action, permission to turn off the clocks will be given	no
PU	clocks are on; U-interface is not transparent but may be synchronous (e.g. U-only activation)	any C/I-code	no action, clocks will remain on	no
AR	used during activation. U-interface is synchronous and is waiting for an ok from the downstream device	AI	accept that activation can continue, layer 2 of the downstream device is ready. Then wait for CI/ indication AI	no
AI	U-interface transparent	-- EI1 or act=0	no action, transmit data report problem on downstream device	yes

2.4.11 Metallic Loop Termination

For North American applications a maintenance controller according to ANSI T1.601 section 6.5 is implemented. The maintenance pulse stream from the U-interface Metallic Loop Termination circuit (MLT) is fed to pin MTI, usually via an optocoupler. It is digitally filtered for 20 ms and decoded independently on the polarity by the maintenance controller according to **Table 30**. Therefore, the maintenance controller is capable of detecting the DC and AC signaling format. The Q-SMINT®IX automatically sets the U-transceiver in the proper state and issues an interrupt. The state selected by the MLT is indicated via two bits.

The Q-SMINT®IX reacts on a valid pulse stream independently of the current U-transceiver state. This includes the power-down state.

A test mode is valid for 75 seconds. If during the 75 seconds a valid pulse sequence is detected the 75 s timer starts again. After expiry of the 75 s timer the MLT maintenance controller goes back to normal operation.

Table 30 ANSI Maintenance Controller States

Number of counted pulses	ANSI maintenance controller state	U-transceiver State Machine
<= 5	ignored	no impact
6	Quiet Mode	transition to state 'Reset' start timer 75s
7	ignored	no impact
8	Insertion Loss Measurement	transition to state 'Transparent' start timer 75s
9	ignored	no impact
10	normal operation	transition to state 'Reset'
>= 11	ignored	no impact

Figure 48 shows examples for pulse streams with inverse polarity selecting Quiet Mode.

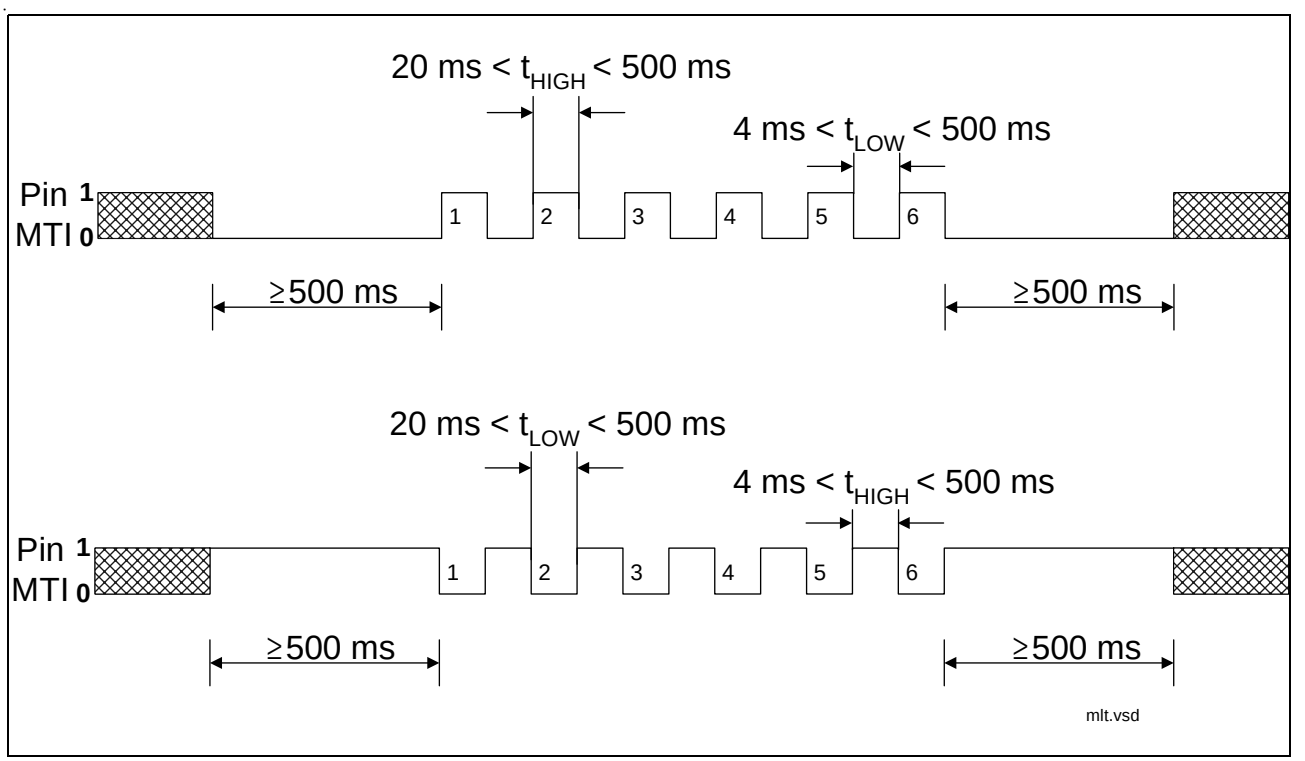


Figure 48 Pulse Streams Selecting Quiet Mode

2.4.12 U-Transceiver Interrupt Structure

The U-Interrupt Status register (ISTAU) contains the interrupt sources of the U-Transceiver (**Figure 49**). Each source can be masked by setting the corresponding bit of the U-Interrupt Mask register (MASKU) to ’1’. Such masked interrupt status bits are not indicated when ISTAU is read and do not generate an interrupt request.

The ISTAU register is cleared on read access. The interrupt sources of the ISTAU register (UCIR, EOCR, M4R, M56R) need not be evaluated.

When at time t1 an interrupt source generates an interrupt, all further interrupts are collected. Reading the ISTAU register clears all interrupts set before t1, even if masked. All interrupts, which are flagged after t1 remain active. After the ISTAU read access, the next unmasked interrupt will generate the next interrupt at time t2. After t2 it is possible to reprogram the MASKU register, so that all interrupts, which arrived between t1 and t2 are accessible.

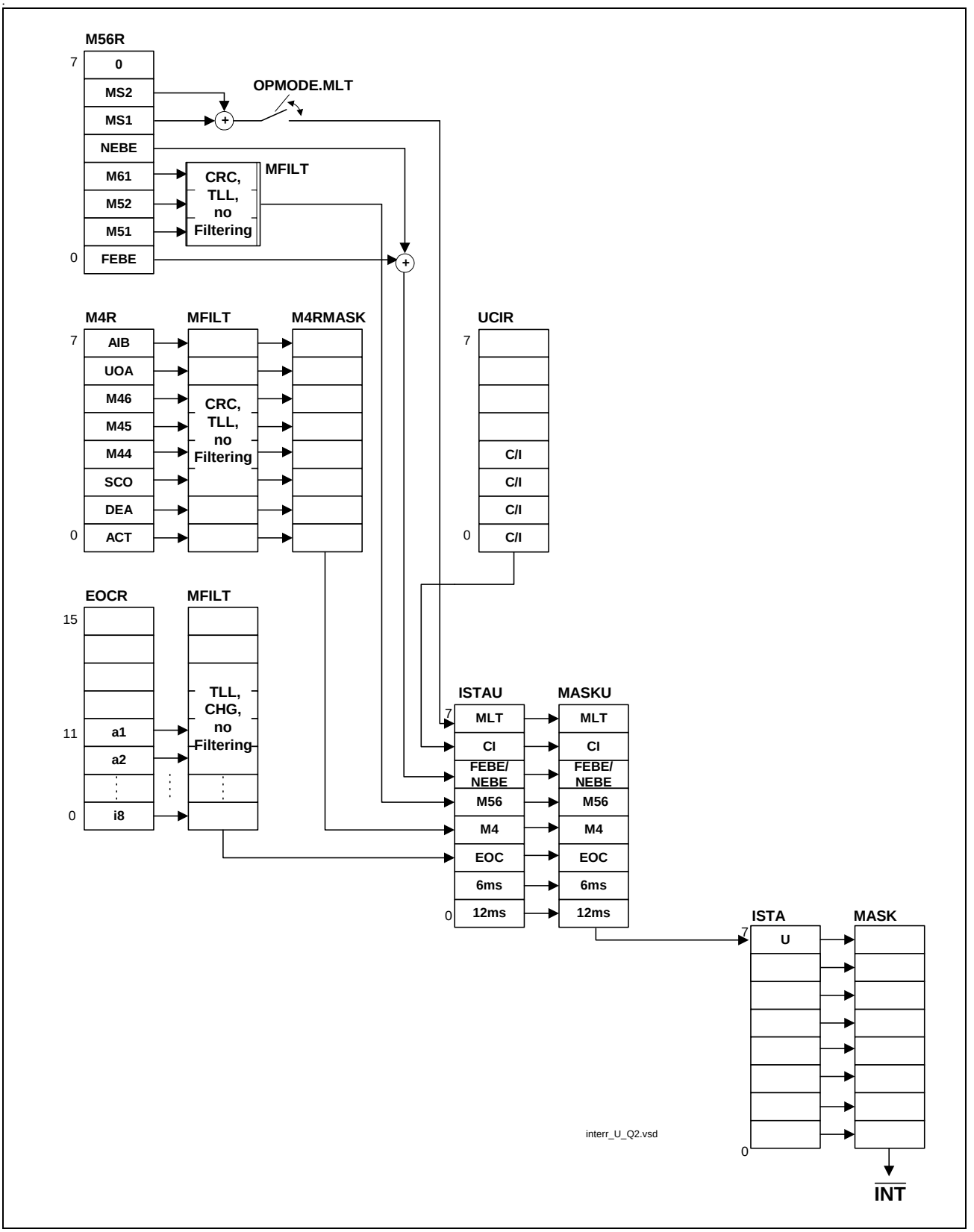


Figure 49 Interrupt Structure U-Transceiver

2.5 S-Transceiver

The S-Transceiver offers the NT and LT-S mode state machines described in the User's Manual V3.4 [10].

The S-transceiver lies in IOM®-2 channel 1 (default) and is configured and controlled via the registers described in **Chapter 4.7**. The state machine is set to NT mode (default) but can be set to LT-S mode via register programming.

The TE mode (S-transceiver TE mode, U-transceiver disabled) is not supported.

2.5.1 Line Coding, Frame Structure

Line Coding

The following figure illustrates the line code. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with two exceptions:
For the required frame structure a code violation is indicated by two consecutive pulses of the same polarity. These two pulses can be adjacent or separated by binary ONEs.
In bus configurations a binary ZERO always overwrites a binary ONE.

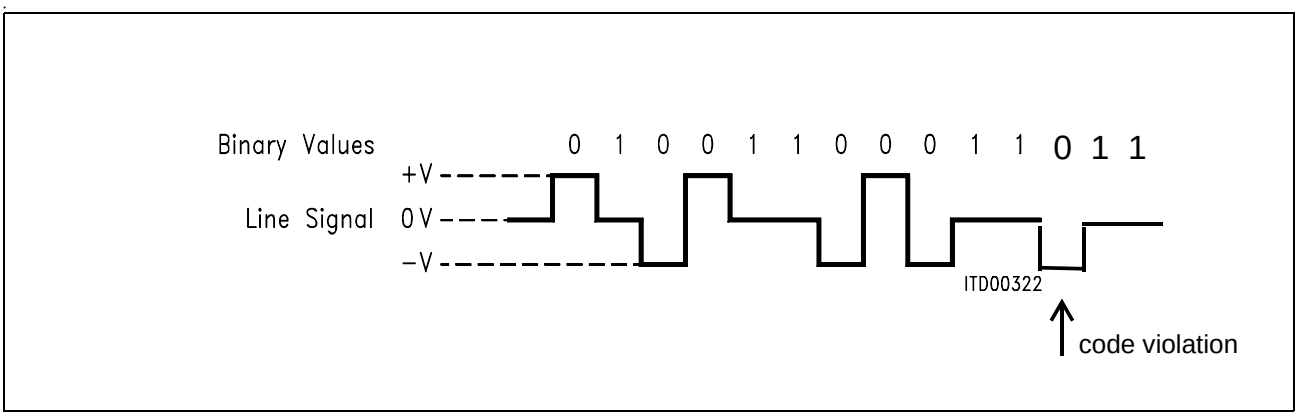


Figure 50 S/T -Interface Line Code

Frame Structure

Each S/T frame consists of 48 bits at a nominal bit rate of 192 kbit/s. For user data (B1+B2+D) the frame structure applies to a data rate of 144 kbit/s (see **Figure 50**).
In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

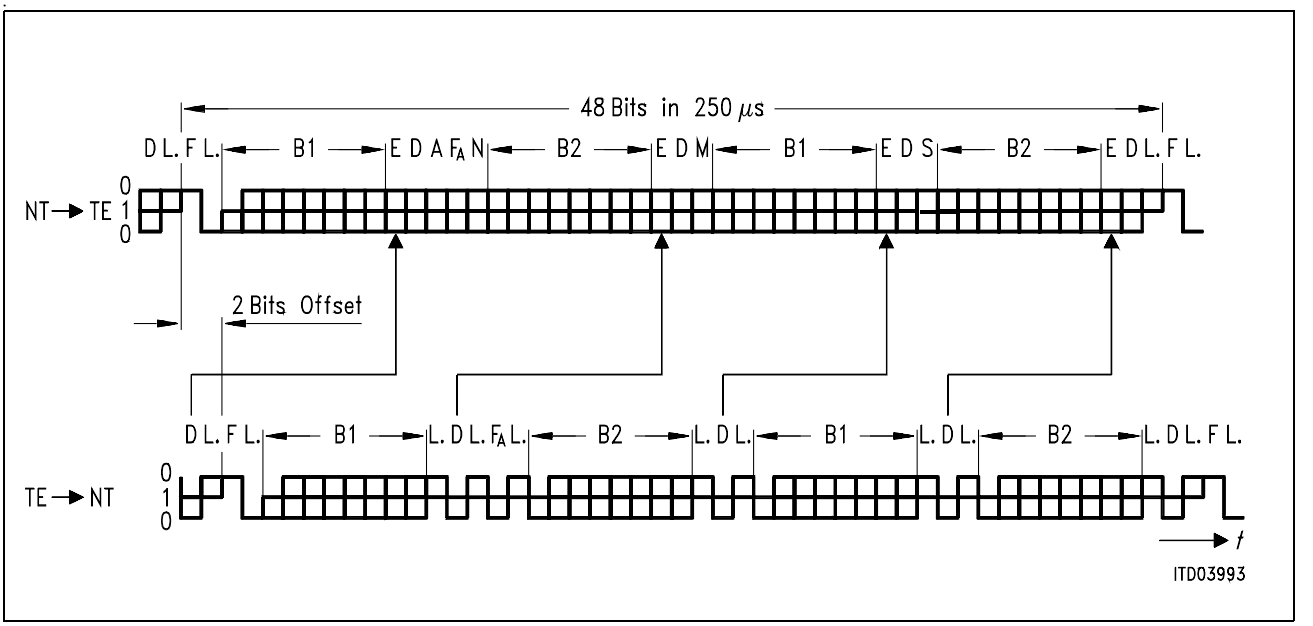


Figure 51 Frame Structure at Reference Points S and T (ITU I.430)

– F	Framing Bit	F = (0b) → identifies new frame (always positive pulse, always code violation)
– L.	D.C. Balancing Bit	L. = (0b) → number of binary ZEROs sent after the last L. bit was odd
– D	D-Channel Data Bit	Signaling data specified by user
– E	D-Channel Echo Bit	E = D → received E-bit is equal to transmitted D-bit
– F_A	Auxiliary Framing Bit	See section 6.3 in ITU I.430
– N		N = $\overline{F_A}$
– B1	B1-Channel Data Bit	User data
– B2	B2-Channel Data Bit	User data
– A	Activation Bit	A = (0b) → INFO 2 transmitted A = (1b) → INFO 4 transmitted
– S	S-Channel Data Bit	S_1 channel data (see note below)
– M	Multiframing Bit	M = (1b) → Start of new multi-frame

Note: The ITU I.430 standard specifies S1 - S5 for optional use.

2.5.2 S/Q Channels, Multiframing

According to ITU recommendation I.430 a multi-frame provides extra layer-1 capacity in the TE-to-NT direction through the use of an extra channel between the TE and NT (Q-channel). The Q bits are defined to be the bits in the F_A bit position.

In the NT-to-TE direction the S-channel bits are used for information transmission.

The S- and Q-channels are accessed via µC by reading/writing the SQR or SQX bits in the S/Q channel registers (SQRR, SQXR).

Table 31 shows the S and Q bit positions within the multi-frame.

Table 31 S/Q-Bit Position Identification and Multi-Frame Structure

Frame Number	NT-to-TE F_A Bit Position	NT-to-TE M Bit	NT-to-TE S Bit	TE-to-NT F_A Bit Position
1	ONE	ONE	S11	Q1
2	ZERO	ZERO	S21	ZERO
3	ZERO	ZERO	S31	ZERO
4	ZERO	ZERO	S41	ZERO
5	ZERO	ZERO	S51	ZERO
6	ONE	ZERO	S12	Q2
7	ZERO	ZERO	S22	ZERO
8	ZERO	ZERO	S32	ZERO
9	ZERO	ZERO	S42	ZERO
10	ZERO	ZERO	S52	ZERO
11	ONE	ZERO	S13	Q3
12	ZERO	ZERO	S23	ZERO
13	ZERO	ZERO	S33	ZERO
14	ZERO	ZERO	S43	ZERO
15	ZERO	ZERO	S53	ZERO
16	ONE	ZERO	S14	Q4
17	ZERO	ZERO	S24	ZERO
18	ZERO	ZERO	S34	ZERO
19	ZERO	ZERO	S44	ZERO
20	ZERO	ZERO	S54	ZERO
1	ONE	ONE	S11	Q1
2	ZERO	ZERO	S21	ZERO

The S-transceiver starts multiframing if SQXR1.MFEN is set.

After multi-frame synchronization has been established in the TE, the Q data will be inserted at the upstream (TE → NT) F_A bit position by the TE in each 5th S/T frame, the S data will be inserted at the downstream (NT → TE) S bit position in each 5th S/T frame (see **Table 31**). Access to S2-S5-channel is not supported.

Interrupt Handling for Multi-Framing

To trigger the microcontroller for a multi-frame access an interrupt can be generated once per multi-frame (SQW) or if the received Q-channel have changed (SQC).
In both cases the microcontroller has access to the multiframe within the duration of one multiframe (5 ms).

The start of a multiframe can not be synchronized to an external signal.

2.5.3 Data Transfer between IOM®-2 and S_0

In the state G3 (Activated) or if the internal layer-1 statemachine is disabled and XINF of register S_CMD is programmed to '011' the B1, B2 and D bits are transferred transparently from the S/T to the IOM®-2 interface and vice versa. In all other states '1's are transmitted to the IOM®-2 interface.

Note: In intelligent NT or intelligent LT-S mode the D-channel access can be blocked by the IOM®-2 D-channel handler.

2.5.4 Loopback 2

C/I commands ARL and AIL close the analog loop as close to the S-interface as possible. ETSI refers to this loop under 'loopback 2'. ETSI requires, that B1, B2 and D channels have the same propagation delay when being looped back.

The D-channel Echo bit is set to bin. 0 during an analog loopback (i.e. loopback 2). The loop is transparent.

Note: After C/I-code AIL has been recognized by the S-transceiver, zeros are looped back in the B and D-channels (DU) for four frames.

2.5.5 Control of S-Transceiver / State Machine

The S-transceiver activation/ deactivation can be controlled by an internal statemachine via the IOM®-2 C/I-channel or by software via the µC interface directly. In the default state the internal layer-1 statemachine of the S-transceiver is used. By setting the L1SW bit in the S_CONF0 register the internal statemachine can be disabled and the layer-1 transmit commands, which are normally generated by the internal statemachine can be written directly into the S_CMD register or the received status read out from the S_STA register, respectively. The S-transceiver layer-1 control flow is shown in **Figure 52**.

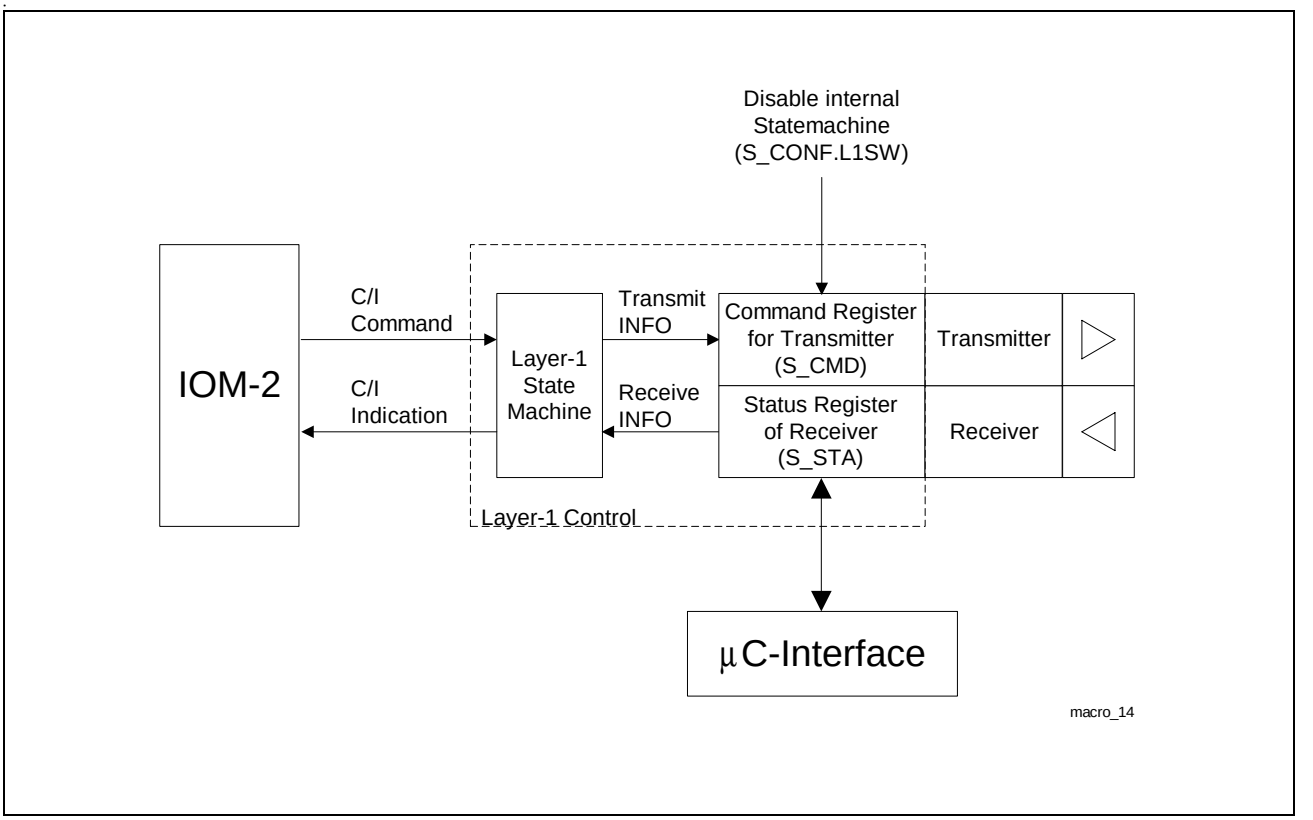


Figure 52 S-Transceiver Control

The state diagram notation is given in **Figure 53**.

The information contained in the state diagrams are:

– state name
– Signal received from the line interface (INFO)
– Signal transmitted to the line interface (INFO)
– C/I code received (commands)
– C/I code transmitted (indications)
– transition criteria

The transition criteria are grouped into:

– C/I commands
– Signals received from the line interface (INFOs)
– Reset

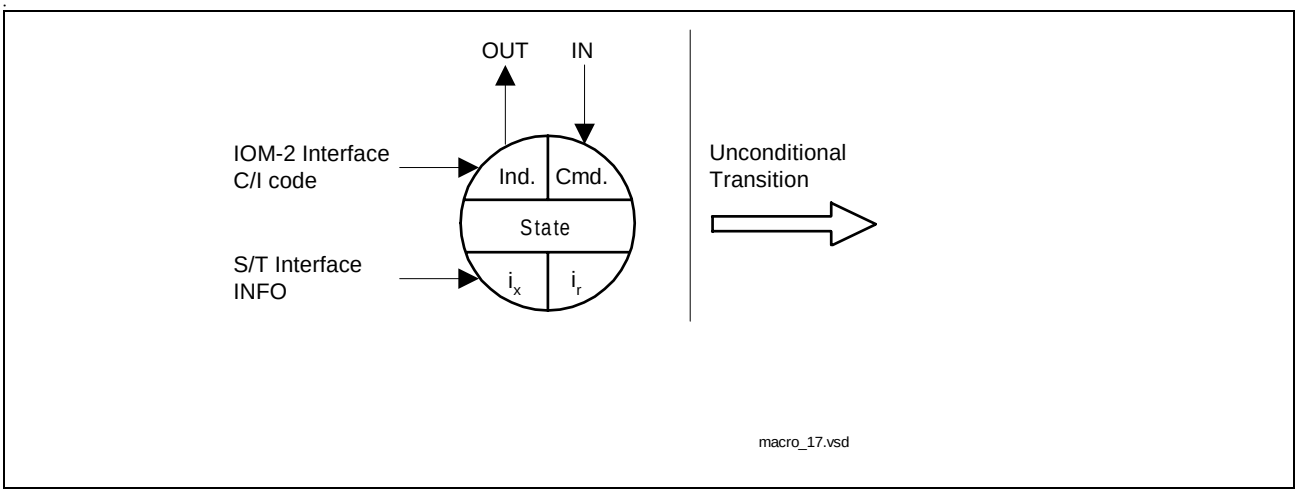


Figure 53 State Diagram Notation

As can be seen from the transition criteria, combinations of multiple conditions are possible as well. A “∗” stands for a logical AND combination. And a “+” indicates a logical OR combination.

Test Signals

- 2 kHz Single Pulses (TM1)

  One pulse with a width of one bit period per frame with alternating polarity.
- 96 kHz Continuous Pulses (TM2)

  Continuous pulses with a pulse width of one bit period.

Note: The test signals TM1 and TM2 are invoked via C/I codes ‘TM1‘ and ‘TM2‘ according to ***Chapter 2.5.5.1****.*

External Layer-1 Statemachine

Instead of using the integrated layer-1 statemachine it is also possible to implement the layer-1 statemachine completely in software.

The internal layer-1 statemachine can be disabled by setting the L1SW bit in the S_CONF0 register to ’1’.

The transmitter is completely under control of the microcontroller via register S_CMD.

The status of the receiver is stored in register S_STA and has to be evaluated by the microcontroller. This register is updated continuously. If not masked a RIC interrupt is generated by any change of the register contents. The interrupt is cleared after a read access to this register.

Reset States

After an active signal on the reset pin $\overline{\text{RST}}$ the S-transceiver state machine is in the reset state.

C/I Codes in Reset State

In the reset state the C/I code 0000 (TIM) is issued. This state is entered either after a hardware reset ($\overline{RST}$) or with the C/I code RES.

C/I Codes in Deactivated State

If the S-transceiver is in state ‘Deactivated‘ and receives $\overline{i0}$, the C/I code 0000 (TIM) is issued until expiration of the 8 ms timer. Otherwise, the C/I code 1111 (DI) is issued.

2.5.5.1 C/I Codes

The table below presents all defined C/I0 codes. A command needs to be applied continuously until the desired action has been initiated. Indications are strictly state orientated. Refer to the state diagrams in the following sections for commands and indications applicable in various states.

Code				LT-S		NT	
				Cmd	**Ind**	**Cmd**	**Ind**
0	0	0	0	DR	TIM	DR	TIM
0	0	0	1	RES	–	RES	–
0	0	1	0	TM1	–	TM1	–
0	0	1	1	TM2	–	TM2	–
0	1	0	0	–	RSY	RSY	RSY
0	1	0	1	–	–	–	–
0	1	1	0	–	–	–	–
0	1	1	1	–	–	–	–
1	0	0	0	AR	AR	AR	AR
1	0	0	1	–	–	–	–
1	0	1	0	ARL	–	ARL	–
1	0	1	1	–	CVR	–	CVR
1	1	0	0	–	AI	AI	AI
1	1	0	1	–	–	–	–
1	1	1	0	–	–	AIL	–
1	1	1	1	DC	DI	DC	DI

Receive Infos on S/T

I0	INFO 0 detected
$\overline{I0}$	Level detected (signal different to I0)
I3	INFO 3 detected
$\overline{I3}$	Any INFO other than INFO 3

Transmit Infos on S/T

I0	INFO 0
I2	INFO 2
I4	INFO 4
It	Send Single Pulses (TM1). Send Continuous Pulses (TM2).

2.5.5.2 State Machine NT Mode

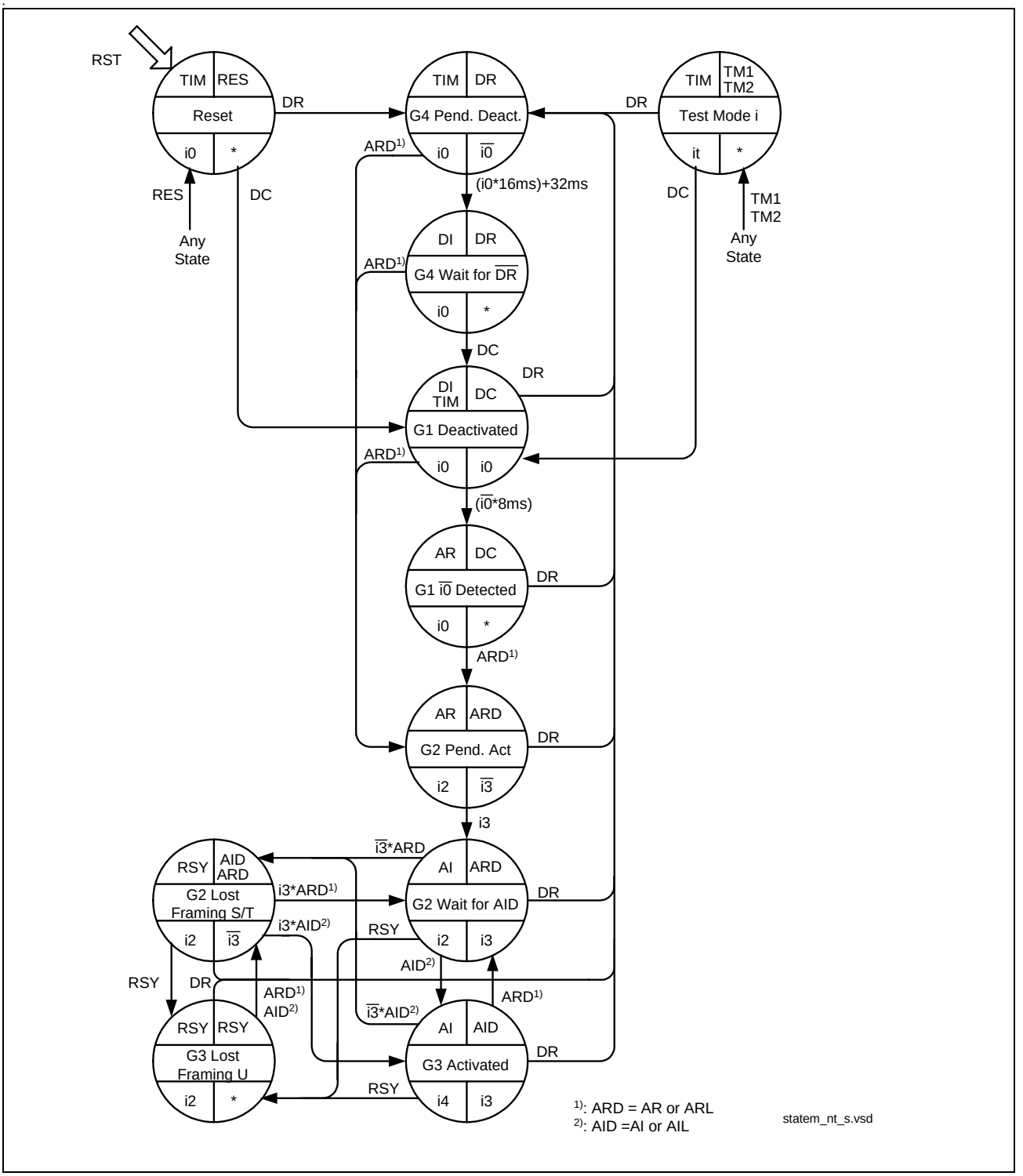


Figure 54 State Machine NT Mode

Note: State 'Test Mode' can be entered from any state except from state 'Test Mode' itself, i.e. C/I-code 'TMi' must not be followed by C/I-code 'TMj' directly.

G1 Deactivated

The S-transceiver is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel. Activation is possible from the S/T interface and from the IOM®-2 interface.

G1 $\overline{\text{I0}}$ Detected

An $\overline{\text{INFO 0}}$ is detected on the S/T-interface, translated to an “Activation Request” indication in the C/I channel. The S-transceiver is waiting for an AR command, which normally indicates that the transmission line upstream is synchronized.

G2 Pending Activation

As a result of the ARD command, an INFO 2 is sent on the S/T-interface. INFO 3 is not yet received. In case of ARL command, loop 2 is closed.

G2 wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the S-transceiver waits for a “switch-through” command AID from the device upstream.

G3 Activated

INFO 4 is sent on the S/T-interface as a result of the “switch through” command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

G2 Lost Framing S/T

This state is reached when the transceiver has lost synchronism in the state G3 activated.

G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the transmission line, the S-transceiver transmits INFO 2.

G4 Pending Deactivation

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state “G4 wait for DR”) is issued by the transceiver when:

either INFO0 is received for a duration of 16 ms

or an internal timer of 32 ms expires.

G4 wait for $\overline{DR}$

Final state after a deactivation request. The S-transceiver remains in this state until DC is issued.

Unconditional States

Test Mode TM1

Send Single Pulses

Test Mode TM2

Send Continuous Pulses

C/I Commands

Command	Abbr.	Code	Remark
Deactivation Request	DR	0000	Deactivation Request. Initiates a complete deactivation by transmitting INFO 0.
Reset	RES	0001	Reset of state machine. Transmission of Info0. No reaction to incoming infos. RES is an unconditional command.
Send Single Pulses	TM1	0010	Send Single Pulses.
Send Continuous Pulses	TM2	0011	Send Continuous Pulses.
Receiver not Synchronous	RSY	0100	Receiver is not synchronous
Activation Request	AR	1000	Activation Request. This command is used to start an activation.
Activation Request Loop	ARL	1010	Activation request loop. The transceiver is requested to operate an analog loop-back close to the S/T-interface.
Activation Indication	AI	1100	Activation Indication. Synchronous receiver, i.e. activation completed.

Command	Abbr.	Code	Remark
Activation Indication Loop	AIL	1110	Activation Indication Loop
Deactivation Confirmation	DC	1111	Deactivation Confirmation. Transfers the transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

Indication	Abbr.	Code	Remark
Timing	TIM	0000	Interim indication during deactivation procedure.
Receiver not Synchronous	RSY	0100	Receiver is not synchronous.
Activation Request	AR	1000	$\overline{\text{INFO 0}}$ received from terminal. Activation proceeds.
Illegal Code Ciolation	CVR	1011	Illegal code violation received. This function has to be enabled in S_CONF0.EN_ICV.
Activation Indication	AI	1100	Synchronous receiver, i.e. activation completed.
Deactivation Indication	DI	1111	Timer (32 ms) expired or INFO 0 received for a duration of 16 ms after deactivation request.

2.5.5.3 State Machine LT-S Mode

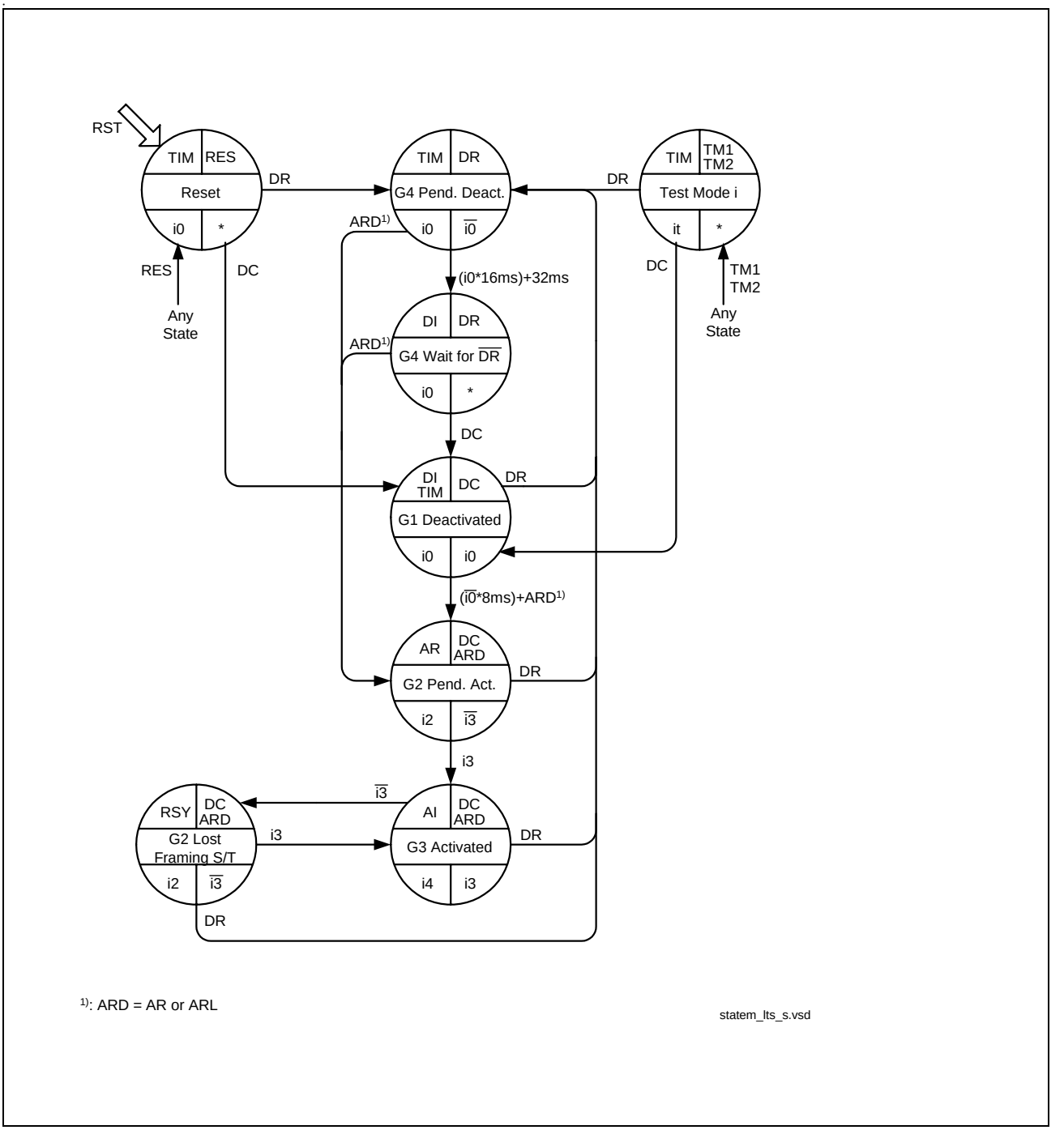


Figure 55 State Machine LT-S Mode

Note: State 'Test Mode' can be entered from any state except from state 'Test Mode' itself, i.e. C/I-code 'TMi' must not be followed by C/I-code 'TMj' directly.

G1 deactivated

The S-transceiver is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel. Activation is possible from the S/T interface and from the IOM®-2 interface.

G2 pending activation

As a result of an $\overline{\text{INFO 0}}$ detected on the S/T line or an ARD command, the S-transceiver begins transmitting INFO 2 and waits for reception of INFO 3. The timer to supervise reception of INFO 3 is to be implemented in software. In case of an ARL command, loop 2 is closed.

G3 activated

Normal state where INFO 4 is transmitted to the S/T-interface. The transceiver remains in this state as long as neither a deactivation nor a test mode is requested, nor the receiver looses synchronism.

When receiver synchronism is lost, INFO 2 is sent automatically. After reception of INFO 3, the transmitter keeps on sending INFO 4.

G2 lost framing

This state is reached when the S-transceiver has lost synchronism in the state G3 activated.

G4 pending deactivation

This state is triggered by a deactivation request DR. It is an unstable state: indication DI (state “G4 wait for DR.”) is issued by the S-transceiver when:

either INFO0 is received for a duration of 16 ms,

or an internal timer of 32 ms expires.

G4 wait for $\overline{\text{DR}}$

Final state after a deactivation request. The transceiver remains in this state until DC is issued.

Unconditional States

Test mode - TM1

Single alternating pulses are sent on the S/T-interface.

Test mode - TM2

Continuous alternating pulses are sent on the S/T-interface.

Command	Abbr.	Code	Remark
Deactivation Request	DR	0000	DR - Deactivation Request. Initiates a complete deactivation by transmitting INFO 0.
Reset	RES	0001	Reset of state machine. Transmission of Info0. No reaction to incoming infos. RES is an unconditional command.
Send Single Pulses	TM1	0010	Send Single Pulses.
Send Continuous Pulses	TM2	0011	Send Continuous Pulses.
Activation Request	AR	1000	Activation Request. This command is used to start an activation.
Activation Request Loop	ARL	1010	Activation request loop. The transceiver is requested to operate an analog loop-back close to the S/T-interface.
Deactivation Confirmation	DC	1111	Deactivation Confirmation. Transfers the transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

Indication	Abbr.	Code	Remark
Timing	TIM	0000	Interim indication during activation procedure in G1.
Receiver not Synchronous	RSY	0100	Receiver is not synchronous
Activation Request	AR	1000	$\overline{\text{INFO 0}}$ received from terminal. Activation proceeds.
Illegal Code Ciolation	CVR	1011	Illegal code violation received. This function has to be enabled in S_CONF0.EN_ICV.
Activation Indication	AI	1100	Synchronous receiver, i.e. activation completed.
Deactivation Indication	DI	1111	Timer (32 ms) expired or INFO 0 received for a duration of 16 ms after deactivation request

2.5.6 S-Transceiver Enable / Disable

The layer-1 part of the S-transceiver can be enabled/disabled with the two bits S_CONF0.DIS_TR and S_CONF2.DIS_TX.
If DIS_TX=’1’ the transmit buffers are disabled. The receiver will monitor for incoming data in this configuration. By default the transmitter is disabled (DIS_TX = ’1’).
If the transceiver is disabled (DIS_TR = ’1’, DIS_TX = don’t care) all layer-1 functions are disabled including the level detection circuit of the receiver. In this case the power consumption of the S-transceiver is reduced to a minimum.

2.5.7 Interrupt Structure S-Transceiver

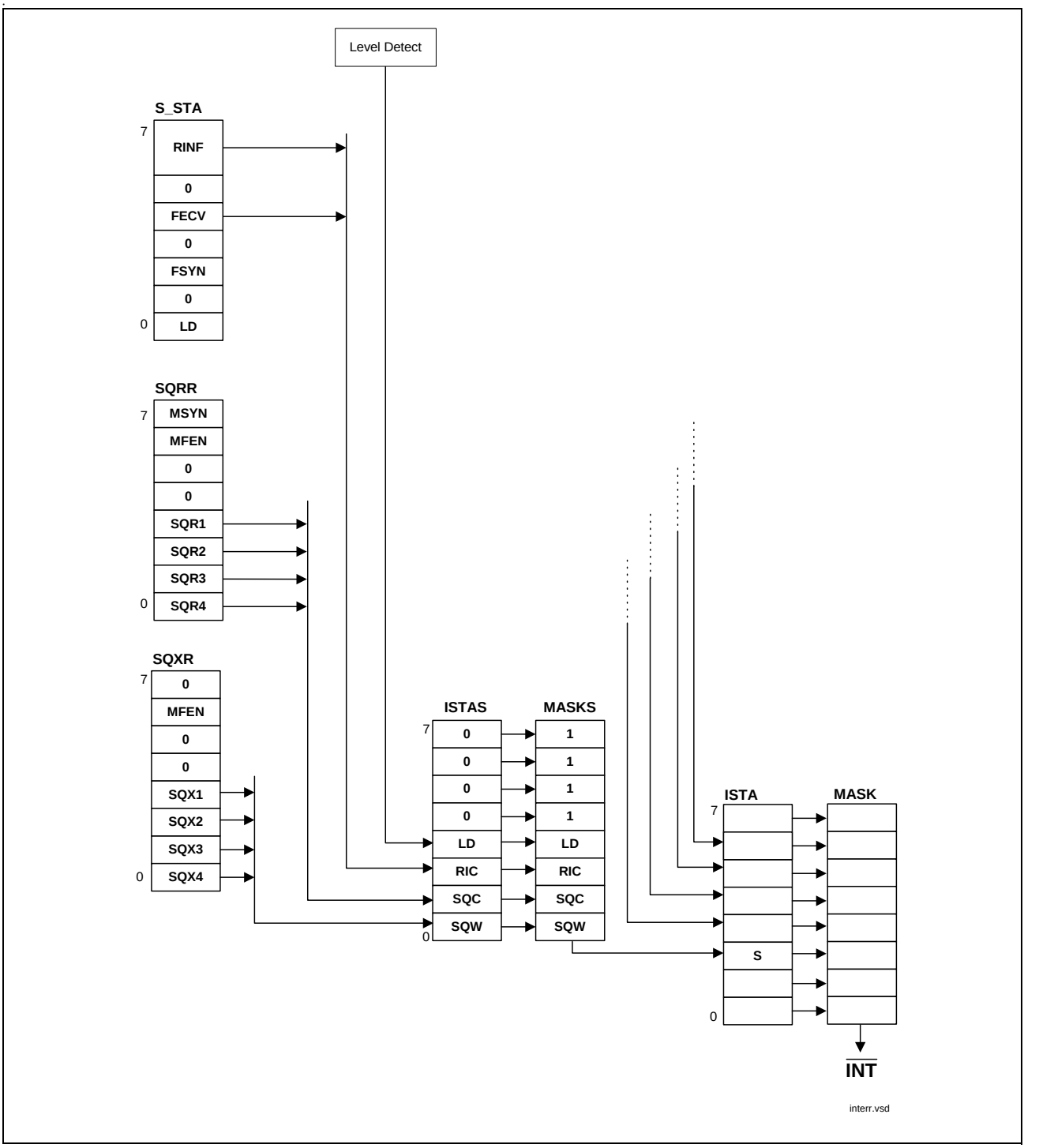


Figure 56 Interrupt Structure S-Transceiver

2.6 HDLC Controller

The Q-SMINT®IX contains a HDLC controller which can be used for the layer-2 functions of the D- channel protocol (LAPD) or B-channel protocols. By setting the enable HDLC channel bits (EN_D, EN_B1H, EN_B2H) in the HCI_CR register the HDLC controller can access the D or B-channels or any combination of them e.g. 18 bit IDSL data (2B+D).

The HDLC transceiver in the Q-SMINT®IX performs the framing functions used in HDLC based communication: flag generation/recognition, bit stuffing, CRC check and address recognition.

The HDLC controller contains a 64 byte FIFO in both receive and transmit direction which is implemented as a cyclic buffer. The transceivers read and write data sequentially with constant data rate, whereas the data transfer between FIFO and µC interface uses a block oriented protocol with variable block sizes.

2.6.1 Message Transfer Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be programmed in a flexible way to satisfy different system requirements.
The structure of a LAPD two-byte address is shown below.

High Address Byte			Low Address Byte	
SAPI1, 2, SAPG	C/R	0	TEI 1, 2, TEIG	EA

For the address recognition the Q-SMINT®IX contains four programmable registers for individual SAPI and TEI values (SAP1, 2 and TEI1, 2), plus two fixed values for the “group” SAPI (SAPG = ’FE’ or ’FC’) and TEI (TEIG = ’FF’).
The received C/R bit is excluded from the address comparison. EA is the address field extension bit which is set to ’1’ according to the LAPD protocol.

There are 5 different operating modes which can be selected via the mode selection bits MDS2-0 in the MODEH register:

Non-Auto Mode (MDS2-0 = ’01x’)

Characteristics: Full address recognition with one-byte (MDS = ’010’) or two-byte (MDS = ’011’) address comparison

All frames with valid addresses are accepted and the bytes following the address are transferred to the µP via RFIFO. Additional information is available in RSTA.

Transparent mode 0 (MDS2-0 = ’110’).

Characteristics: no address recognition

Every received frame is stored in RFIFO (first byte after opening flag to CRC field). Additional information can be read from RSTA.

Transparent mode 1 (MDS2-0 = ’111’).

Characteristics: SAPI recognition

A comparison is performed on the first byte after the opening flag with SAP1, SAP2 and “group” SAPI (FE_H/FC_H). In the case of a match, all the following bytes are stored in RFIFO. Additional information can be read from RSTA.

Transparent mode 2 (MDS2-0 = ’101’).

Characteristics: TEI recognition

A comparison is performed only on the second byte after the opening flag, with TEI1, TEI2 and group TEI (FF_H). In case of a match the rest of the frame is stored in the RFIFO. Additional information is available in RSTA.

Extended transparent mode (MDS2-0 = ’100’).

Characteristics: fully transparent

In extended transparent mode fully transparent data transmission/reception without HDLC framing is performed i.e. without FLAG generation/recognition, CRC generation/check and bitstuffing mechanism. This allows user specific protocol variations.
Also refer to **Chapter 2.6.5**.

2.6.2 Data Reception

2.6.2.1 Structure and Control of the Receive FIFO

The 64-byte cyclic RFIFO buffer has variable FIFO block sizes (thresholds) of 4, 8, 16 or 32 bytes which can be selected by setting the corresponding RFBS bits in the EXMR register. The variable block size allows an optimized HDLC processing concerning frame length, I/O throughput and interrupt load.
The transfer protocol between HDLC FIFO and microcontroller is block orientated with the microcontroller as master. The control of the data transfer between the CPU and the Q-SMINT®IX is handled via interrupts (Q-SMINT®IX → Host) and commands (Host → Q-SMINT®IX).

There are three different interrupt indications in the ISTAH register concerned with the reception of data:

– **RPF (Receive Pool Full)** interrupt, indicating that a data block of the selected length (EXMR.RFBS) can be read from RFIFO. The message which is currently received exceeds the block size so further blocks will be received to complete the message.

– **RME** (**R**eceive **M**essage **E**nd) interrupt, indicating that the reception of one message has been completed and the message has been stored in the RFIFO.
  Either
  – a short message has been received
    (message length ≤ the defined block size (EXMR.RFBS) or
  – the last part of a long message has been received
    (message length > the defined block size (EXMR.RFBS)).
– **RFO** (**R**eceive **F**rame **O**verflow) interrupt, indicating that a complete frame could not be stored in RFIFO and is therefore lost as the RFIFO is occupied. This occurs if the host fails to respond quick enough to RPF/RME interrupts since previous data was not read by the host.

There are two control commands that are used with the reception of data:

– **RMC** (**R**eceive **M**essage **C**omplete) command, telling the Q-SMINT®IX that a data block has been read from the RFIFO and the corresponding FIFO space can be released for new receive data.
– **RRES** (**R**eceiver **R**eset) command, resetting the HDLC receiver and clearing the receive FIFO of any data (e.g. used before start of reception). It has to be used after a change of the message transfer mode. RRES does not clear pending interrupt indications of the receiver, but have to be be cleared by reading these interrupts.

Note: The significant interrupts and commands are underlined as only these are usually used during a normal reception sequence.

The following description of the receive FIFIO operation is illustrated in **Figure 57** for a RFIFO block size (threshold) of 16 and 32 bytes.

The RFIFO requests service from the microcontroller by setting a bit in the ISTAH register, which causes an interrupt (RPF, RME, RFO). The microcontroller then reads status information (RBCH,RBCL), data from the RFIFO and changes the RFIFO block size (EXMR.RFBS). A block transfer is completed by the microcontroller via a receive message complete (CMDR.RMC) command. This causes the space of the transferred bytes being released for new data and in case the frame was complete (RME) the reset of the receive byte counter RBC (RBCH,RBCL).[1)]
The total length of the frame is contained in the RBCH and RBCL registers which contain a 12 bit number (RBC11...0), so frames up to 4095 byte length can be counted. If a frame is longer than 4095 bytes, the RBCH.OV (overflow) bit will be set. The least significant bits of RBCL contain the number of valid bytes in the last data block indicated by RME (length of last data block ≤ selected block size). **Table 32** shows which RBC bits contain the number of bytes in the last data block or number of complete data blocks,

1) If RMC is omitted, then no new interrupt can be generated.

respectively. If the number of bytes in the last data block is ’0’ the length of the last received block is equal to the block size.

Table 32 Receive Byte Count with RBC11...0 in the RBCH and RBCL registers

EXMR.RFBS bits	Selected block size	Number of	
		complete data blocks in	bytes in the last data block in
’00’	32 byte	RBC11...5	RBC4...0
’01’	16 byte	RBC11...4	RBC3...0
’10’	8 byte	RBC11...3	RBC2...0
’11’	4 byte	RBC11...2	RBC1...0

The transfer block size (EXMR.RFBS) is 32 bytes by default. If it is necessary to react to an incoming frame within the first few bytes the microcontroller can set the RFIFO block size to a smaller value. Each time a CMDR.RMC or CMDR.RRES command is issued, the RFIFO access controller sets its block size to the value specified in EXMR.RFBS, so the microcontroller has to write the new value for RFBS before the RMC command. When setting an initial value for RFBS before the first HDLC activities, a RRES command must be issued afterwards.

The RFIFO can hold any number of frames fitting in the 64 bytes independent on RFBS. At the end of a frame, the RSTA byte is always inserted.

All generated interrupts are inserted together with all additional information into a wait line to be individually passed to the host. For example if several data blocks have been received to be read by the host and the host acknowledges the current block, a new RPF or RME interrupt from the wait line is immediately generated to indicate new data.

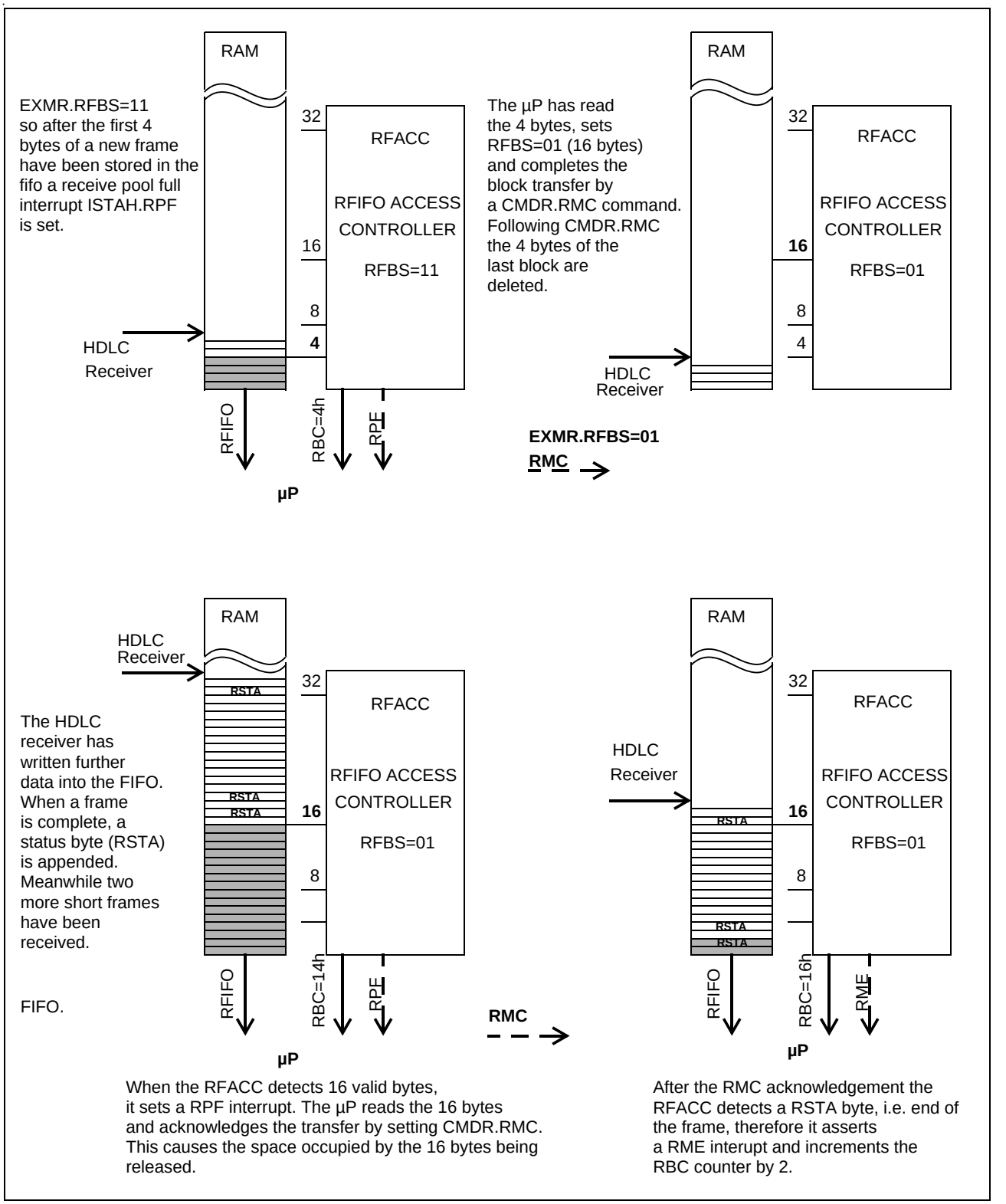


Figure 57 RFIFO Operation

Possible Error Conditions during Reception of Frames

If parts of a frame get lost because the receive FIFO is full, the Receive Data Overflow (RDO) byte in the RSTA byte will be set. If a complete frame is lost, i.e. if the FIFO is full when a new frame is received, the receiver will assert a Receive Frame Overflow (RFO) interrupt.

The microcontroller sees a cyclic buffer, i.e. if it tries to read more data than available, it reads the same data again and again. On the other hand, if it does not read or does not want to read all data, they are deleted anyway after the RMC command.

If the microcontroller tries to read data without a prior RME or RPF interrupt, the content of the RFIFO would not be corrupted, but new data is only transferred to the host as long as new valid data is available in the RFIFO, otherwise the last data is read again and again.

The general procedures for a data reception sequence are outlined in the flow diagram in **Figure 58**.

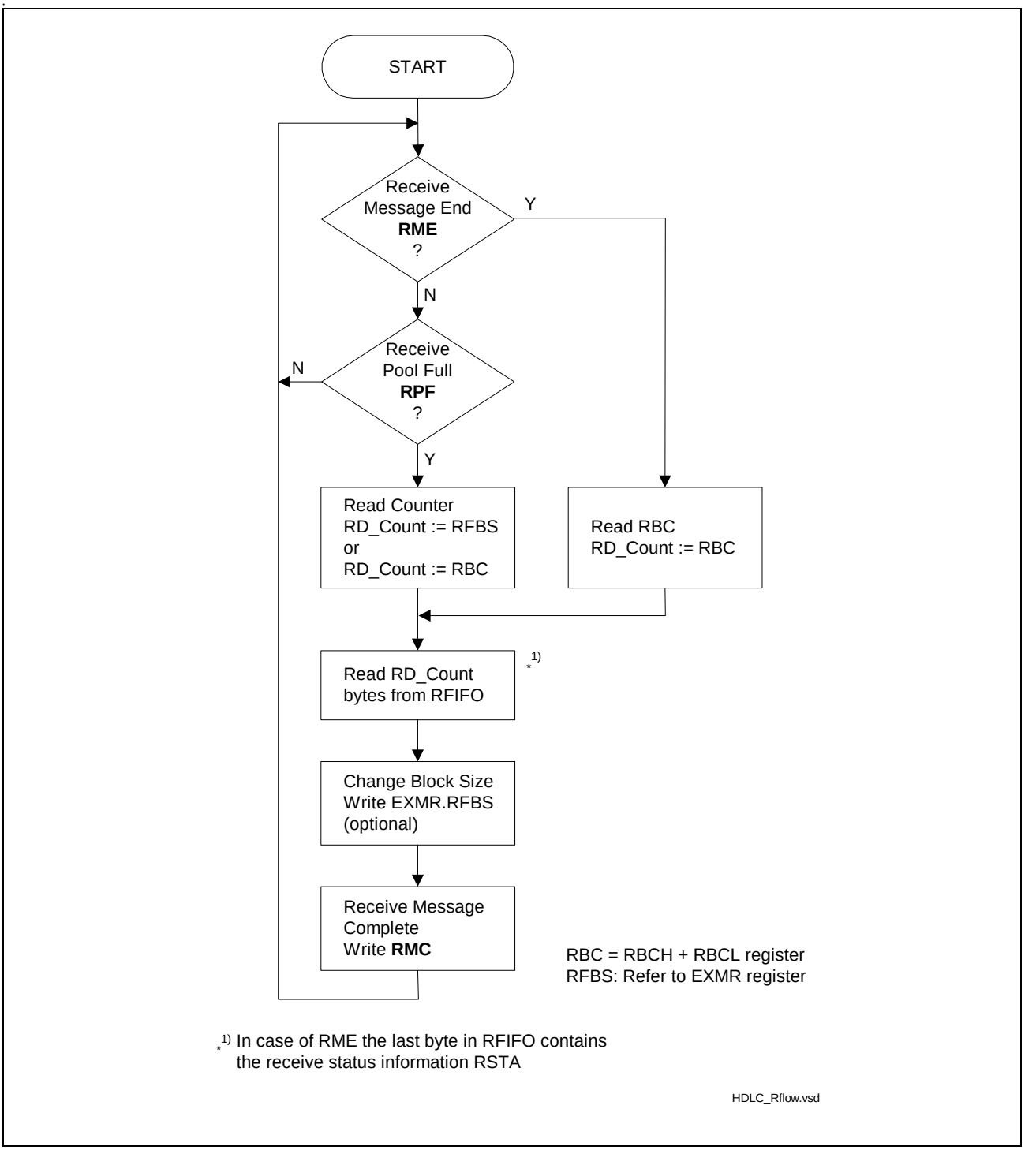


Figure 58 Data Reception Procedures

Figure 59 gives an example of an interrupt controlled reception sequence, supposed that a long frame (68 byte) followed by two short frames (12 byte each) are received. The FIFO threshold (block size) is set to 32 bytes (EXMR.RFBS = ’00’) in this example:

- After 32 bytes have been received off frame 1 a RPF interrupt is generated to indicate that a data block can be read from the RFIFO.

- The host reads the first data block from RFIFO and acknowledges the reception by RMC. Meanwhile the second data block is received and stored in RFIFO.
- The second 32 byte block is indicated by RPF which is read and acknowledged by the host as described before.
- The reception of the remaining 4 bytes are indicated by RME (i.e. the receive status in RSTA register is always appended to the end of a frame).
- The host gets the number of received bytes (COUNT = 5) from RBCL/RBCH and reads out the RFIFO and optionally the status register RSTA. The frame is acknowledged by RMC.
- The second frame is received and indicated by RME interrupt.
- The host gets the number of bytes (COUNT = 13) from RBCL/RBCH and reads out the RFIFO and status registers. The RFIFO is acknowledged by RMC.
- The third frame is transferred in the same way.

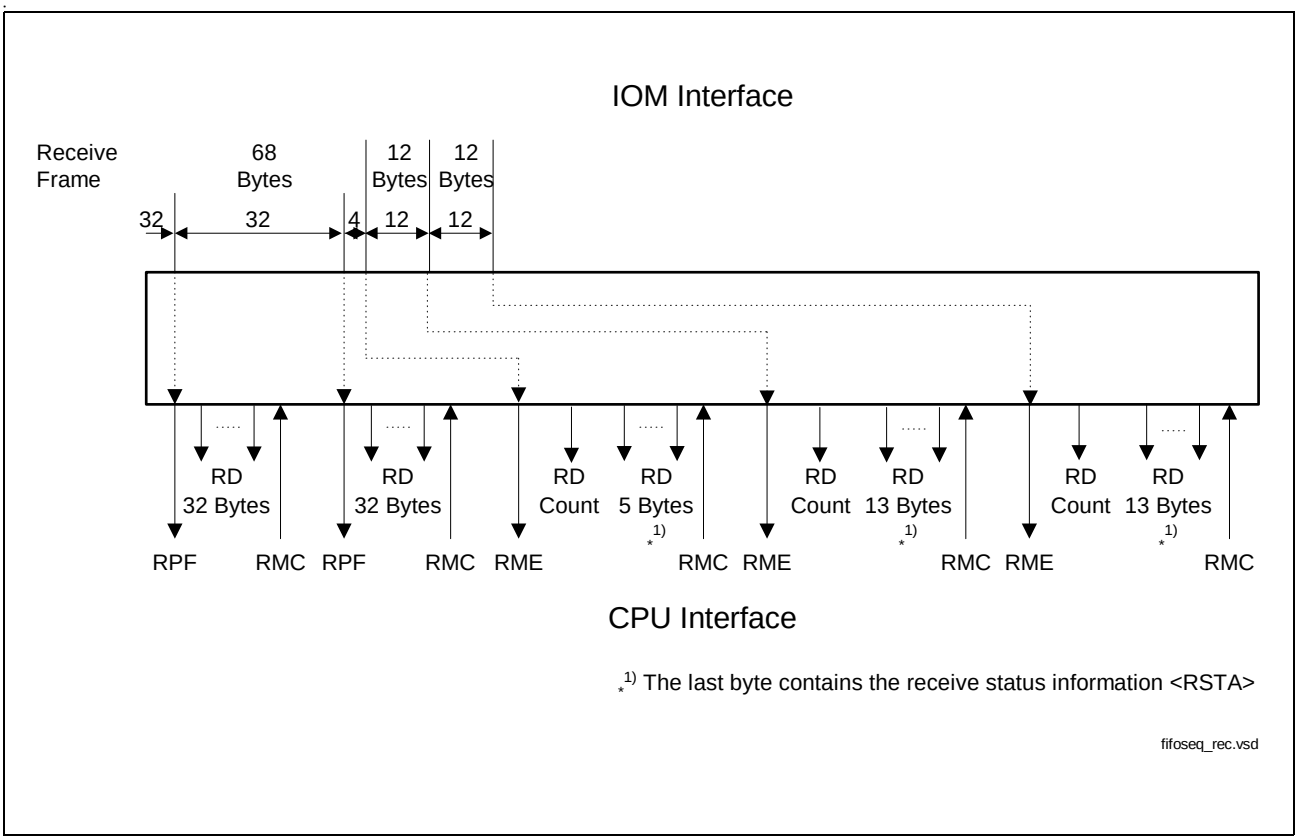


Figure 59 Reception Sequence Example

2.6.2.2 Receive Frame Structure

The management of the received HDLC frames as affected by the different operating modes (see **Chapter 2.6.1**) is shown in **Figure 60**.

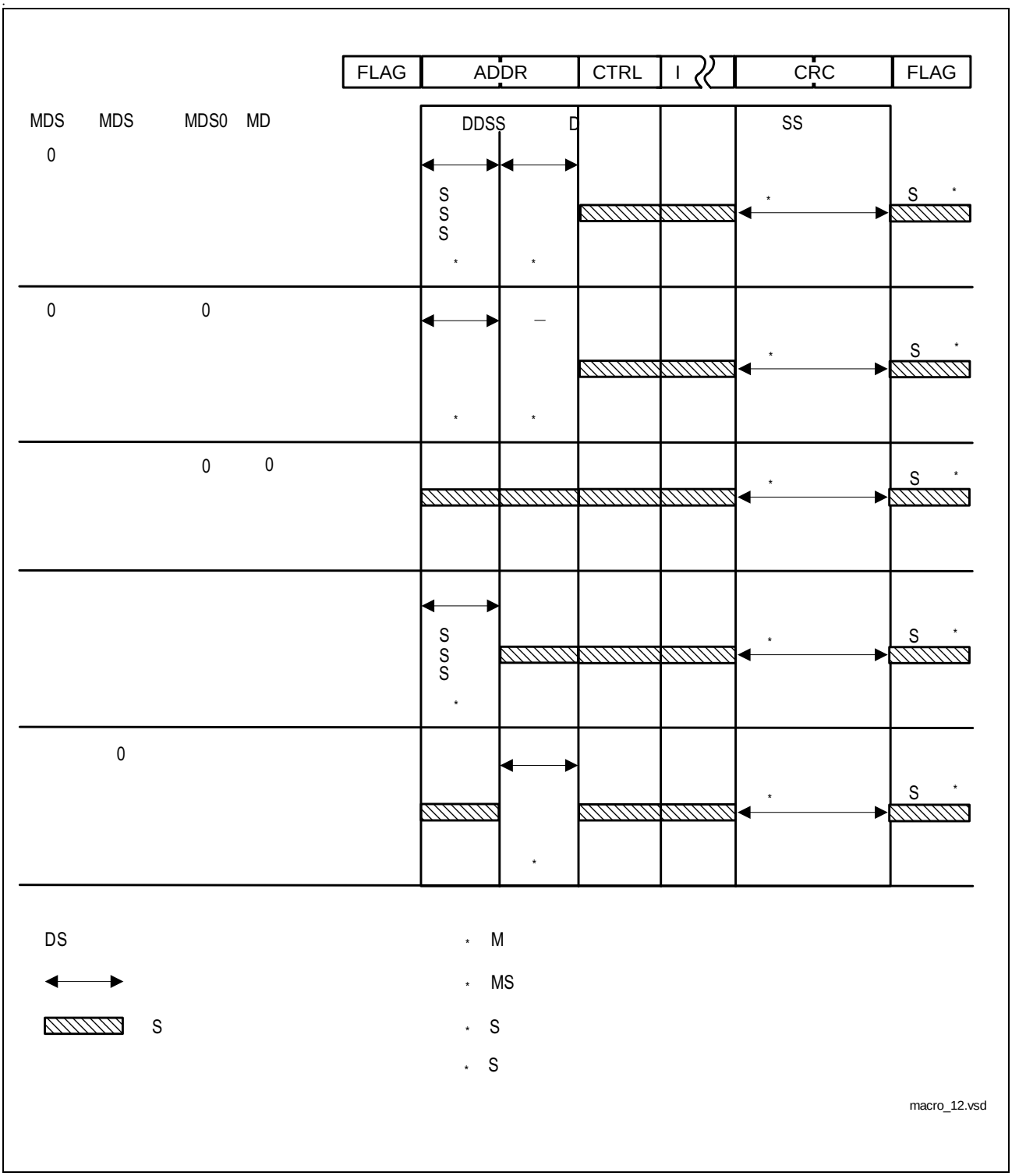


Figure 60 Receive Data Flow

Note: The figure shows all modes except the extended transparent mode as this mode uses no typical frame structure or address recognition. Data is transferred purely transparent.

The Q-SMINT®IX indicates to the host that a new data block can be read from the RFIFO by means of a RPF interrupt (see previous chapter). User data is stored in the RFIFO and information about the received frame is available in the RSTA, RBCL and RBCH registers which are listed in **Table 33**.

Table 33 Receive Information at RME Interrupt

Information	Register	Bit	Mode
Type of frame (Command/ Response)	RSTA	C/R	Non-auto mode, 2-byte address field Transparent mode 1
Recognition of SAPI	RSTA	SA1, 0	Non-auto mode, 2-byte address field Transparent mode 1
Recognition of TEI	RSTA	TA	All except transparent mode 0 and 1
Result of CRC check (correct/incorrect)	RSTA	CRC	All
Valid Frame	RSTA	VFR	All
Abort condition detected (yes/no)	RSTA	RAB	All
Data overflow during reception of a frame (yes/no)	RSTA	RDO	All
Number of bytes received in RFIFO	RBCL	RBCx-0	All (see **Table 32**)
Message length	RBCL RBCH	RBC11-0	All
RFIFO Overflow	RBCH	OV	All

The RSTA register is appended as last byte to the end of a frame.

2.6.3 Data Transmission

2.6.3.1 Structure and Control of the Transmit FIFO

The 64-byte cyclic XFIFO buffer has variable FIFO block sizes (thresholds) of 16 or 32 bytes, selectable by the XFBS bit in the EXMR register.

There are three different interrupt indications in the ISTAH register concerned with the transmission of data:

– **XPR** (**T**ransmit **P**ool **R**eady) interrupt, indicating that a data block of up to 16 or 32 bytes (block size selected via EXMR:XFBS) can be written to the XFIFO.
  A XPR interrupt is generated either
  – after a XRES (Transmitter Reset) command (which is issued for example for frame abort) or
  – when a data block from the XFIFO is transmitted and the corresponding FIFO space is released to accept further data from the host.
– **XDU** (**T**ransmit **D**ata **U**nderrun) interrupt, indicating that the transmission of the current frame has been aborted (seven consecutive ’1’s are transmitted) as the XFIFO holds no further transmit data. This occurs if the host fails to respond to a XPR interrupt quick enough.
– **XMR** (**T**ransmit **M**essage **R**epeat) interrupt, indicating that the transmission of the complete last frame has to be repeated as a collision on the S bus has been detected while the first data bytes have already been overwritten with new data. So the XFIFO does not hold the first data bytes of the frame (the HDLC transmitter is stopped if a collision on the S bus has been detected).
  The occurrence of a XDU or XMR interrupt clears the XFIFO and a XPR interrupt is issued together with a XDU or XMR interrupt, respectively. Data cannot be written to the XFIFO as long as a XDU/XMR interrupt is pending.

Three different control commands are used for transmission of data:

– **XTF** (**T**ransmit **T**ransparent **F**rame) command, telling the Q-SMINT®IX that up to 16 or 32 bytes (according to selected block size) have been written to the XFIFO and should be transmitted. A start flag is generated automatically.
– **XME** (**T**ransmit **M**essage **E**nd) command, telling the Q-SMINT®IX that the last data block written to the XFIFO completes the corresponding frame and should be transmitted. This implies that according to the selected mode a frame end (CRC + closing flag) is generated and appended to the frame.
– **XRES** (**T**ransmitter **R**eset) command, resetting the HDLC transmitter and clearing the transmit FIFO of any data. After a XRES command the transmitter always sends an abort sequence, i.e. this command can be used to abort a transmission. XRES does not clear pending interrupt indications of the transmitter, but has to be be cleared by reading these interrupts.

Optionally two additional status conditions can be read by the host:

– **XDOV** (**T**ransmit **D**ata **O**verflow), indicating that the data block size has been exceeded, i.e. more than 16 or 32 bytes were entered and data was overwritten.
– **XFW** (**T**ransmit **F**IFO **W**rite Enable), indicating that data can be written to the XFIFO. This status flag may be polled instead of or in addition to XPR.

Note: The significant interrupts and commands are underlined as only these are usually used during a normal transmission sequence.

The XFIFO requests service from the microcontroller by setting a bit in the ISTAH register, which causes an interrupt (XPR, XDU, XMR). The microcontroller can then read the status register STAR (XFW, XDOV), write data in the FIFO and it may optionally change the transmit FIFO block size (EXMR.XFBS) if required.
The instant of the initiation of a transmit pool ready (XPR) interrupt after different transmit control commands is listed in **Table 34**.

Table 34 XPR Interrupt (availability of the XFIFO) after XTF, XME Commands

CMDR.	Transmit pool ready (XPR) interrupt initiated...
XTF	as soon as the selected buffer size in the FIFO is available
XTF & XME	after the successful transmission of the closing flag. The transmitter always sends an abort sequence
XME	as soon as the selected buffer size in the FIFO is available, two consecutive frames share flags (endflag = startflag of next frame).

When setting XME the transmitter appends the FCS and the endflag at the end of the frame. When XTF & XME have been set, the XFIFO is locked until successful transmission of the current frame, so a consecutive XPR interrupt also indicates successful transmission of the frame, whereas after XME the XPR interrupt is asserted as soon as there is space for one data block in the XFIFO.

The transfer block size is 32 bytes by default, but sometimes, if the microcontroller has a high computational load, it is useful to increase the maximum reaction time for a XPR interrupt. The maximum reaction time is:
t_{max} = (XFIFO size - XFBS) / data transmission rate
With a selected block size of 16 bytes indicates a XPR interrupt when there are still 48 bytes (64 bytes - 16 bytes) to be transmitted. With a 32 bytes block size the XPR is initiated when there are still 32 bytes (64 bytes - 32 bytes), i.d. the maximum reaction time for the smaller block size is 50 % higher with the trade-off of a doubled interrupt load. A selected block size of 32 or 16 bytes respectively always indicates the available space in the XFIFO. So any number of bytes smaller than the selected XFBS may be stored in the FIFO during one “write block“ access cycle.

Similar to RFBS for the receive FIFO, a new setting of XFBS takes effect after the next XTF,XME or XRES command. XRES resets the XFIFO.

The XFIFO can hold any number of frames fitting in the 64 bytes.

Possible Error Conditions during Transmission of Frames

If the transmitter sees an empty FIFO, i.e. if the microcontroller does not react quickly enough to a XPR interrupt, a XDU (transmit data underrun) interrupt will be raised. If the HDLC channel becomes unavailable during transmission the transmitter tries to repeat the current frame as specified in the LAPD protocol. This is impossible after the first data block has been sent (16 or 32 bytes), in this case a XMR transmit message repeat interrupt is set and the microcontroller has to send the whole frame again.

If the host fails to respond to a Transmit Pool Ready (XPR) interrupt quickly enough, then transmission of the current frame is aborted, a Transmit Data Underrun (XDU) interrupt is generated and an Abort Sequence (seven consecutive ’1’) shall be transmitted. If the µC requests transmission of a new frame during a certain time window after the XDU interrupt, then the Abort Sequence may be overwritten by the Start Flag of this new frame. However, the Abort Sequence is transmitted correctly by waiting 8 IOM-2 frames before the µC requests transmission of a new frame:

- Read from address 20_H (register ISTAH): 14_H (XPR and XDU interrupt active)
- Wait for 1 ms (e.g. by use of the internal timer of the Q-SMINTIX)
- Write new frame to XFIFO

Both XMR and XDU interrupts cause a reset of the XFIFO. The XFIFO is locked while a XMR or XDU interrupt is pending, i.e. all write actions of the microcontroller will be ignored as long as the microcontroller has not read the ISTAH register with the set XDU, XMR interrupts.

If the microcontroller writes more data than allowed (16 or 32 bytes) , then the data in the XFIFO will be corrupted and the STAR.XDOV bit is set. If this happens, the microcontroller has to abort the transmission by CMDR.XRES and start new.

The general procedures for a data transmission sequence are outlined in the flow diagram in **Figure 61**.

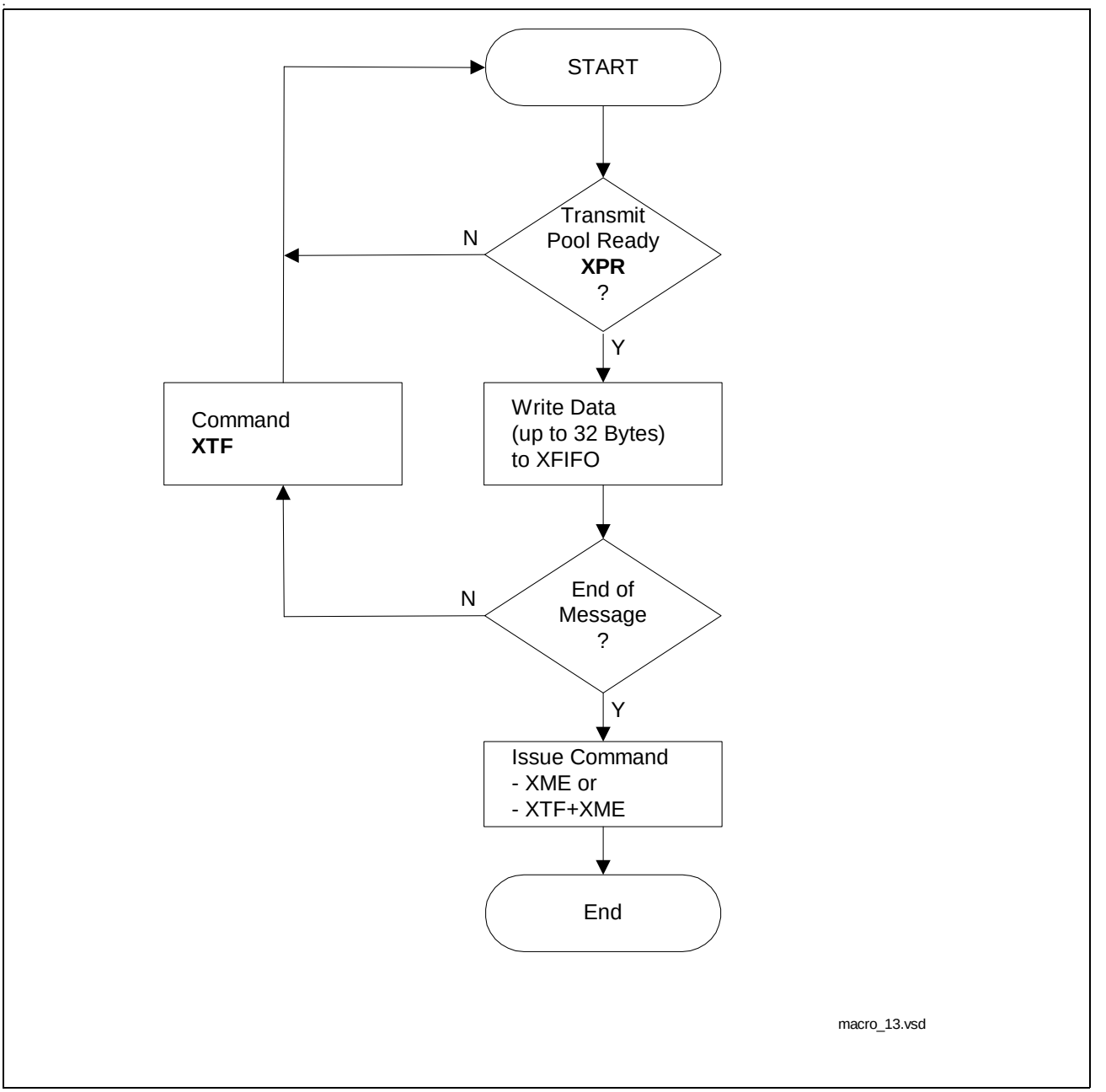


Figure 61 Data Transmission Procedure

The following description gives an example for the transmission of a 76 byte frame with a selected block size of 32 byte (EXMR:XFBS=0):

- The host writes 32 bytes to the XFIFO, issues a XTF command and waits for a XPR interrupt in order to continue with entering data.
- The Q-SMINT®IX immediately issues a XPR interrupt (as remaining XFIFO space is not used) and starts transmission.
- Due to the XPR interrupt the host writes the next 32 bytes to the XFIFO, followed by the XTF command, and waits for XPR.

- As soon as the last byte of the first block is transmitted, the Q-SMINT®IX issues a XPR interrupt (XFIFO space of first data block is free again) and continues transmitting the second block.
- The host writes the remaining 12 bytes of the frame to the XFIFO and issues the XTF command together with XME to indicate that this is the end of frame.
- After the last byte of the frame has been transmitted the Q-SMINT®IX releases a XPR interrupt and the host may proceed with transmission of a new frame.

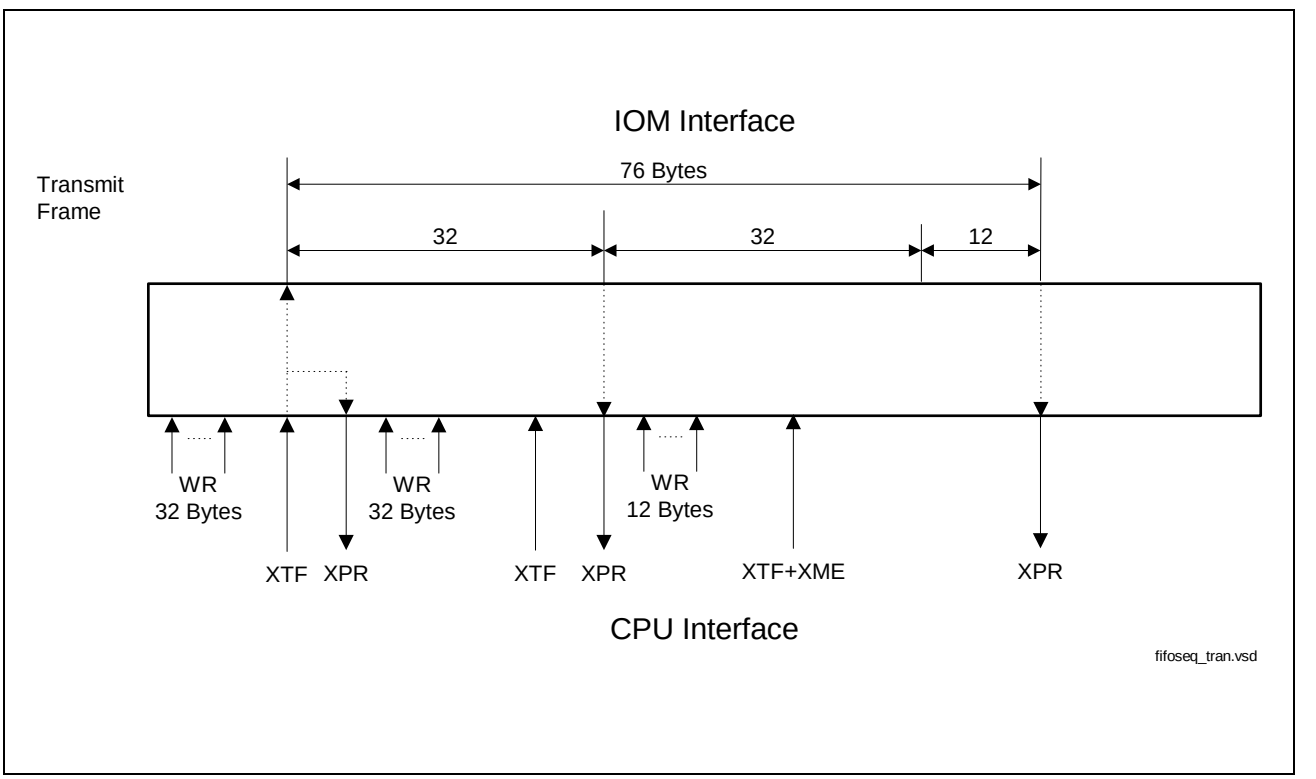


Figure 62 Transmission Sequence Example

2.6.3.2 Transmit Frame Structure

The transmission of transparent frames (XTF command) is shown in **Figure 63**.

For transparent frames, the whole frame including address and control field must be written to the XFIFO. The host configures whether the CRC is generated and appended to the frame (default) or not (selected in EXMR.XCRC).

Further, the host selects the interframe time fill signal which is transmitted between HDLC frames (EXMR:ITF). One option is to send continuous flags (’01111110’), or an idle sequence (continuous ’1’s are transmitted), which is used if D-channel access handling (collision resolution on the S bus) is required for example. Reprogramming of ITF takes effect only after the transmission of the current frame has been completed or after a XRES command.

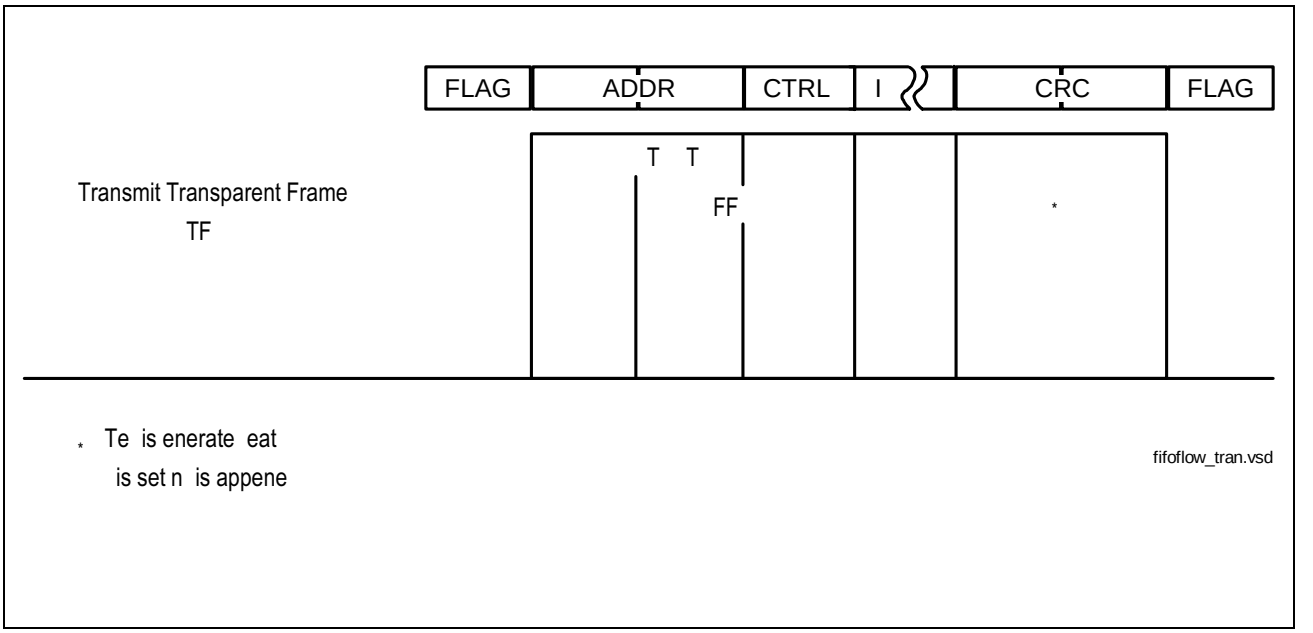


Figure 63 Transmit Data Flow

2.6.4 Access to IOM®-2 channels

By setting the enable HDLC data bits (EN_D, EN_B1H, EN_B2H) in the HCI_CR register the HDLC controller can access the D, B1, B2 channels or any combination of them (e.g. 18 bit IDSL data (2B+D). In all modes (except extended transparent mode) sending works always frame aligned, i.e. it starts with the first selected channel whereas reception looks for a flag anywhere in the serial data stream.

2.6.5 Extended Transparent Mode

This non-HDLC mode is selected by setting MODEH.MDS2-0 to ’100’. In extended transparent mode fully transparent data transmission/reception without HDLC framing is performed i.e. without FLAG generation/recognition, CRC generation/check, bitstuffing mechanism. This allows user specific protocol variations.

Transmitter

The transmitter sends the data out of the FIFO without manipulation. Transmission is always IOM®-2-frame aligned and byte aligned, i.e. transmission starts in the first selected channel (B1, B2, D, according to the setting of register HCI_CR in the IOM®-2 Handler) of the next IOM®-2 frame.

The FIFO indications and commands are the same as in other modes.

If the microcontroller sets XTF & XME the transmitter responds with a XPR interrupt after sending the last byte, then it returns to its idle state (sending continuous ‘1’).

If the collision detection is enabled (MODEH.DIM = ’0x1’) the stop go bit (S/G) can be used as a clear-to-send indication as in any other mode. If the S/G bit is set to ’1’ (stop) during transmission the transmitter responds always with a XMR (transmit message repeat) interrupt and stops transmission.

If the microcontroller fails to respond to a XPR interrupt in time and the transmitter runs out of data then it will assert a XDU (transmit data underrun) interrupt.

Receiver

The reception is IOM®-2-frame aligned and byte aligned, like transmission, i.e. reception starts in the first selected channel (B1, B2, D, according to the setting of register HCI_CR in the IOM®-2 Handler) of the next IOM®-2 frame. The FIFO indications and commands are the same as in others modes.

All incoming data bytes are stored in the RFIFO. If the FIFO is full a RFO interrupt is asserted (EXMR.SRA = ’0’).

Note: In the extended transparent mode the EXMR register has to be set to ’xxx00000‘

2.6.6 Timer

The timer provides two modes (**Table 35**), a count down timer interrupt, i.e. an interrupt is generated only once after expiration of the selected period, and a periodic timer interrupt, which means an interrupt is generated continuously after every expiration of that period.

Table 35 Timer

Address	Register	Modes	Period
04_H	TIMR	Periodic	64 ... 2048 ms
		Count Down	2.048 ... 14.336 s

When the programmed period has expired an interrupt is generated (ISTA.TIN).

The host controls the timer by setting bit CMDR.STI to start the timer and by writing register TIMR to stop the timer. After time period T1 an interrupt is generated continuously if CNT=7 or a single interrupt is generated after timer period T if CNT<7 (**Figure 64**).

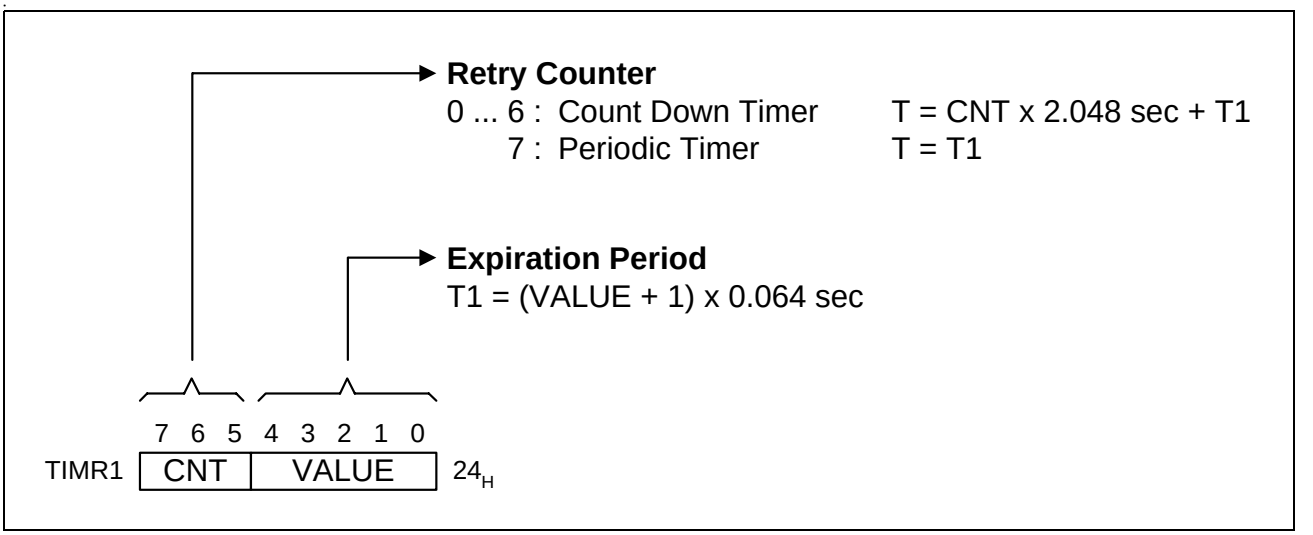


Figure 64 Timer Register

2.6.7 HDLC Controller Interrupts

All interrupt sources from the ISTAH register are combined (ORed) to a single HDLC controller interrupt signal hint. Each of the interrupt sources can individually be masked in the MASKH register. A masked interrupt is not indicated in the ISTAH register but remains internally stored and pending until the interrupt is unmasked and read by the host.

The individual interrupt sources of the HDLC controller during reception and transmission of data are explained in **Chapter 2.6.2.1** or **Chapter 2.6.3.1** respectively. The HDLC controller interrupts XDU and XMR have a special impact on the internal functions. E.g. the transmitter of the HDLC controller is locked if a data underrun condition occurs and the ISTAH.XDU is not read (the interrupt can only be read if unmasked), same applies for XMR.

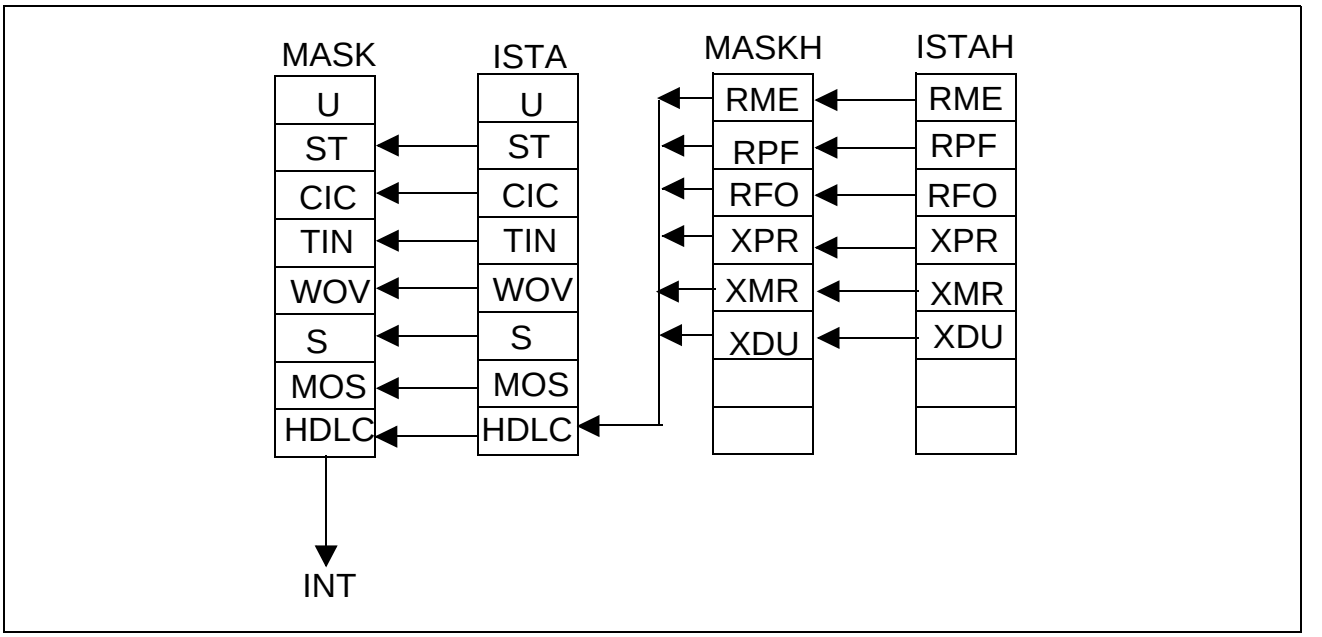


Figure 65 Interrupt Status Registers of the HDLC Controller

2.6.8 Test Function

The Q-SMINT®IX provides test and diagnostic functions for the HDLC controller:

Digital loop via TLP (Test Loop, TMH register) command bit (**Figure 66**): The TX path of the HDLC controller is still connected to IOM®-2 but it is internally connected with the RX path. All incoming data from the IOM®-2 is ignored. This is used for testing HDLC functionality excluding layer 1 (U-transceiver (loopback between XFIFO and RFIFO).

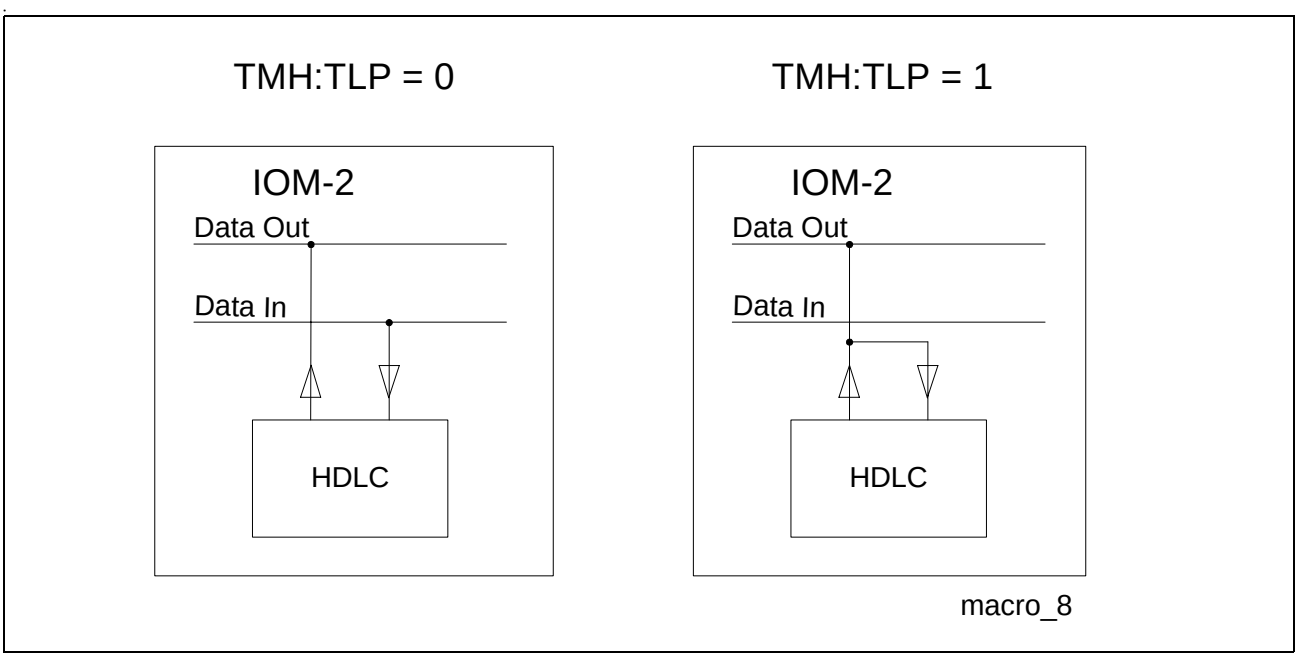


Figure 66 Layer 2 Test Loops

2.6.9 Reset Behavior

After reset all pointers to the FIFOs are set to “0”, the XPR interrupt is set to “1” but cannot be read by the host as it is masked, i.e. it must be unmasked so it can be read.

3 Operational Description

3.1 Layer 1 Activation/Deactivation

3.1.1 Complete Activation Initiated by Exchange

Figure 67 depicts the procedure if activation has been initiated by the exchange side (LT).

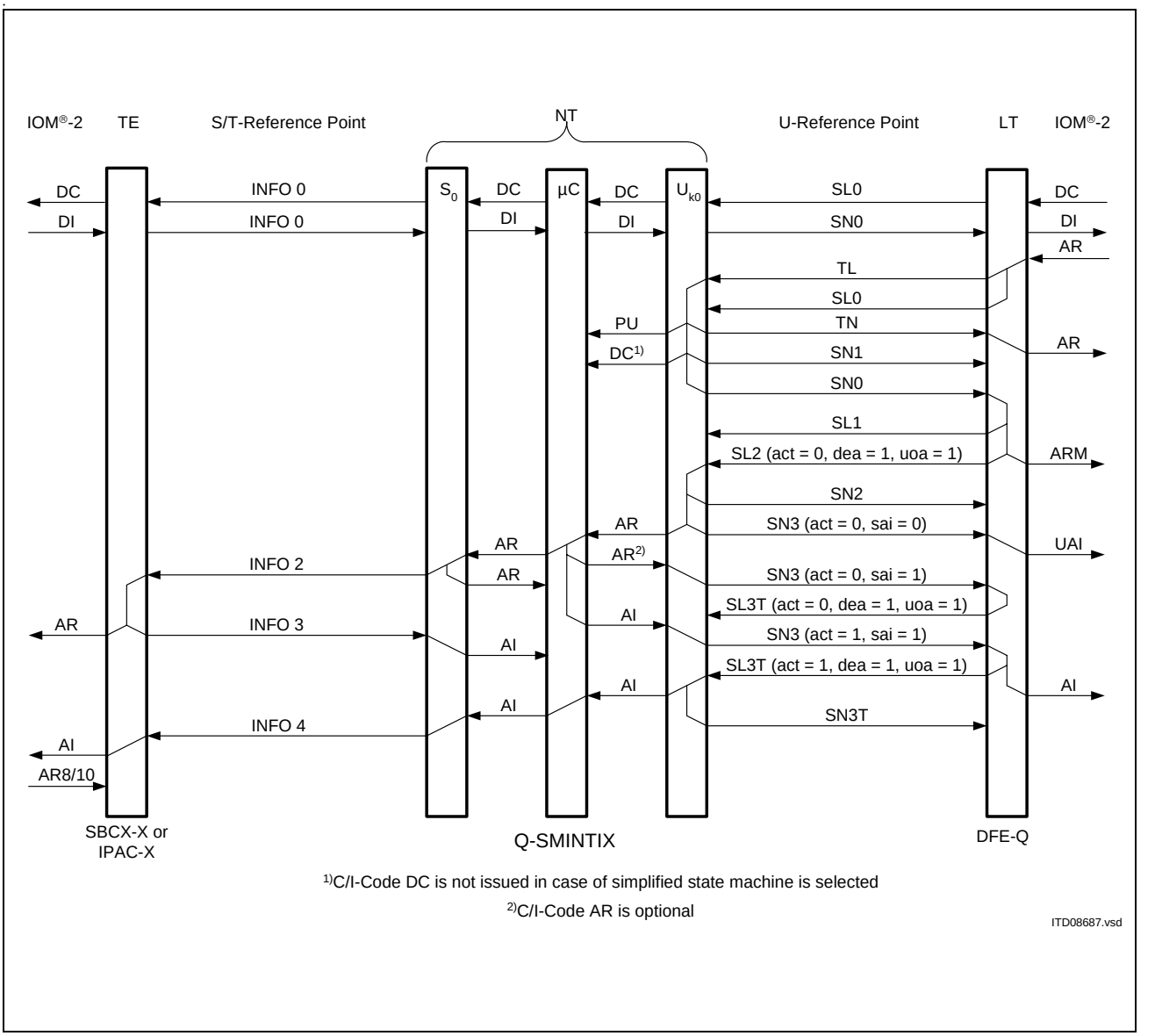


Figure 67 Complete Activation Initiated by Exchange

3.1.2 Complete Activation Initiated by TE

Figure 68 depicts the procedure if activation has been initiated by the terminal side (TE).

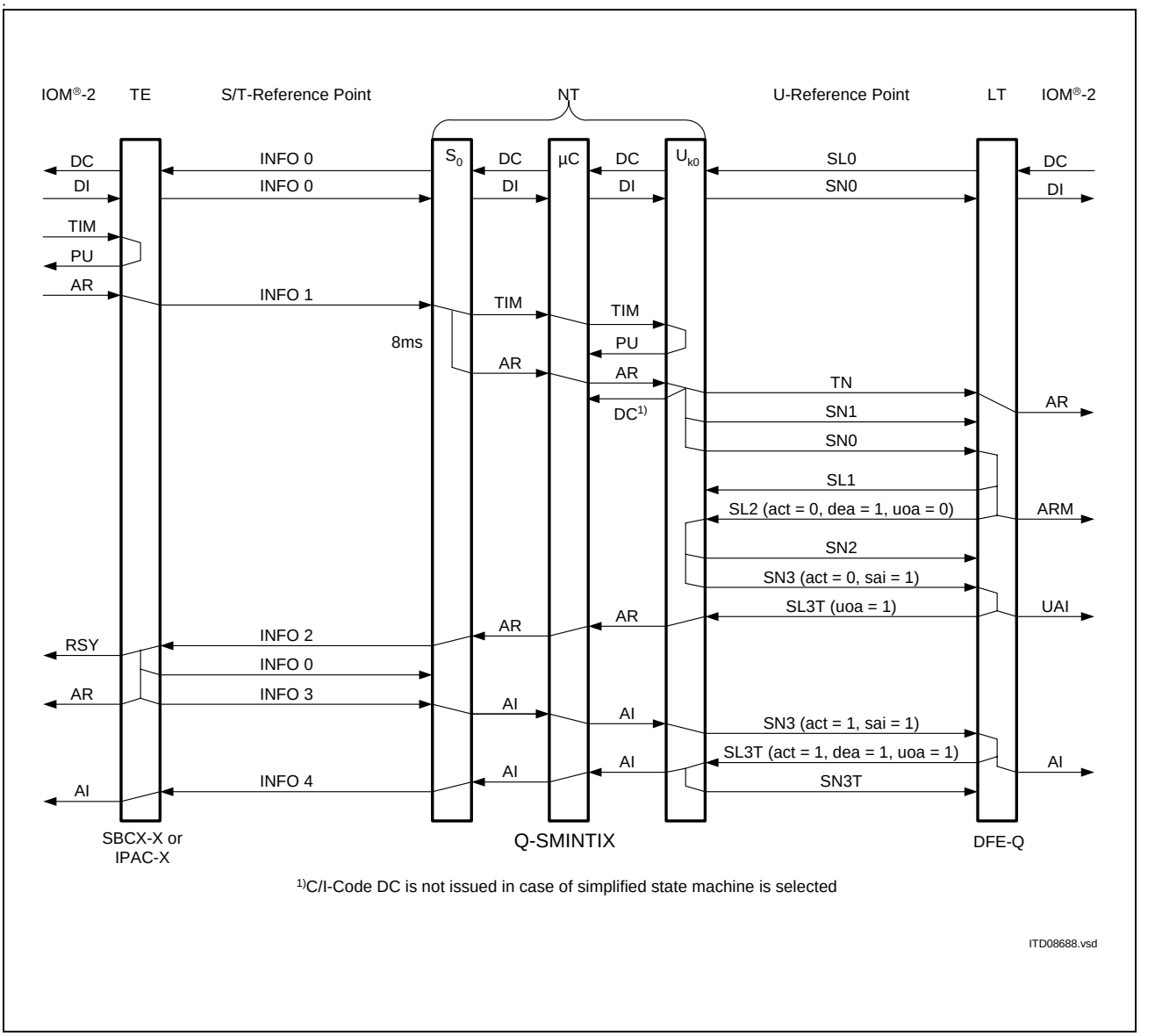


Figure 68 Complete Activation Initiated by TE

3.1.3 Complete Activation Initiated by NT

Figure 69 depicts the procedure if activation has been initiated by the Q-SMINT®IX itself (e.g. after hook-off of a local analog phone).

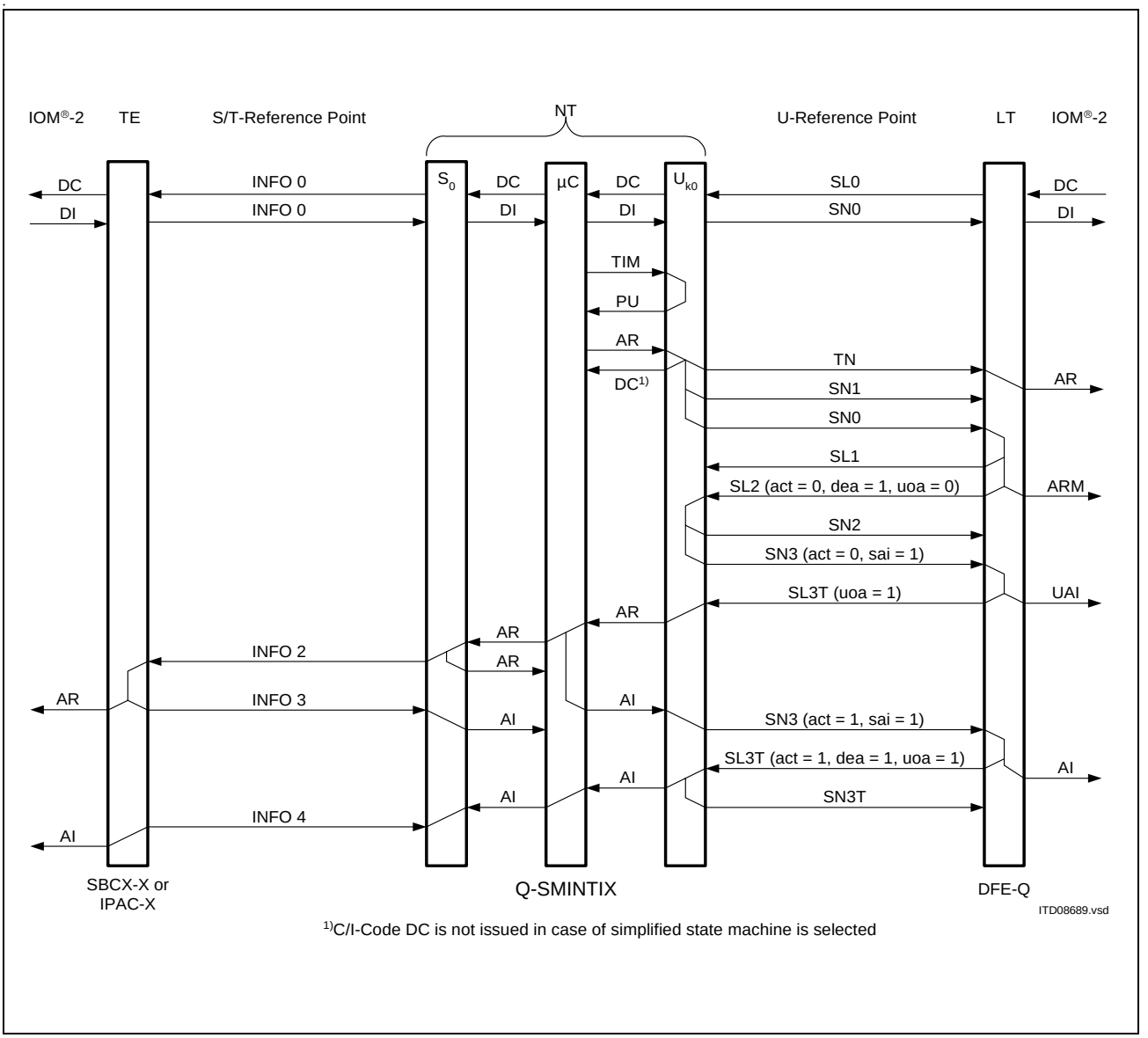


Figure 69 Complete Activation Initiated by Q-SMINT®IX

3.1.4 Complete Deactivation

Figure 70 depicts the procedure if deactivation has been initiated. Deactivation of layer 1 is always initiated by the exchange.

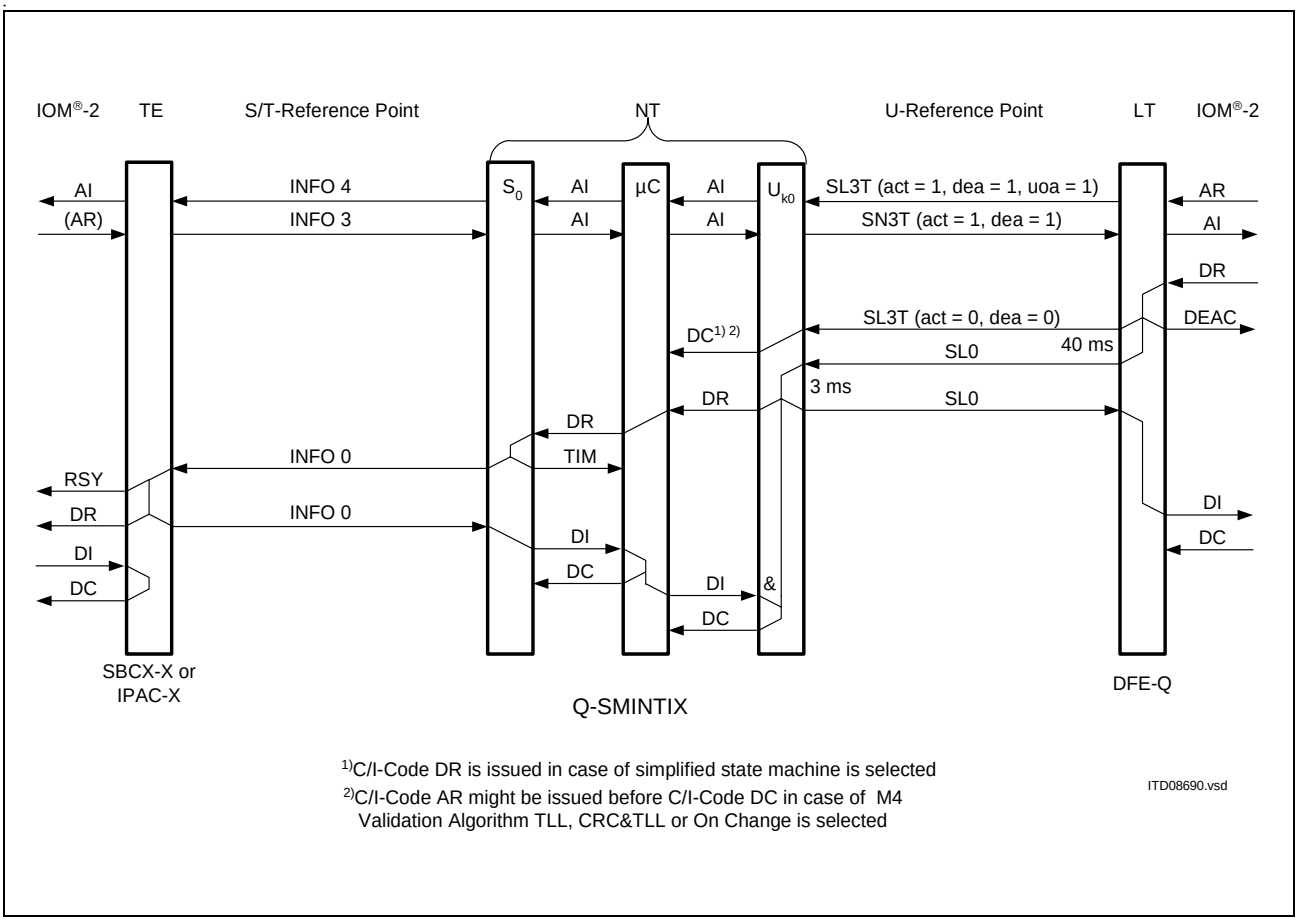


Figure 70 Complete Deactivation Initiated by Exchange

3.1.5 Loop 2

Figure 71 depicts the procedure if loop 2 is closed and opened.

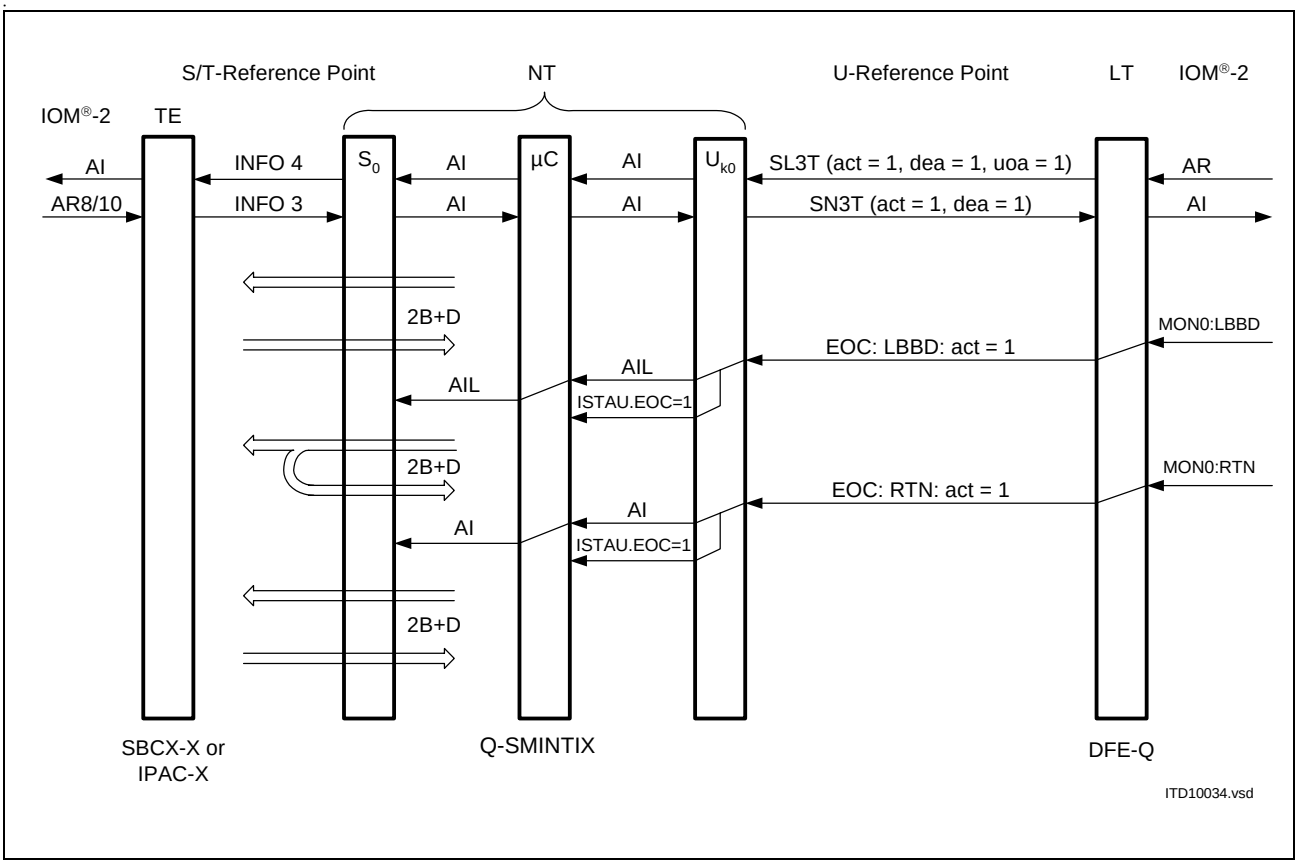


Figure 71 Loop 2

3.2 Layer 1 Loopbacks

Test loopbacks are specified by the national PTTs in order to facilitate the location of defect systems. Four different loopbacks are defined. The position of each loopback is illustrated in **Figure 72**.

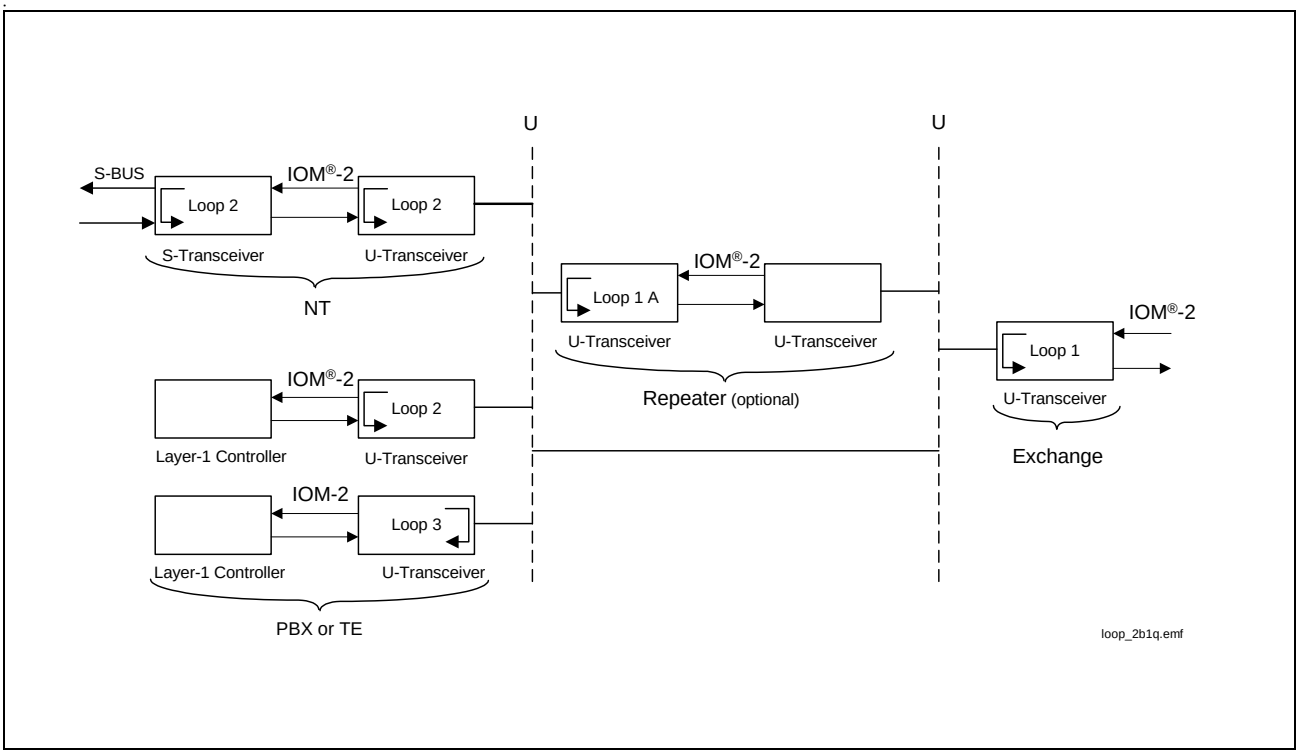


Figure 72 Test Loopbacks

Loopbacks #1, #1A and #2 are controlled by the exchange. Loopback #3 is controlled locally on the remote side. All four loopback types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner. Only the data looped back internally is processed; signals on the receive pins are ignored. The propagation delay of actually looped B and D channels data must be identical in all loopbacks.

Besides the remote controlled loopback stimulation via the EOC channel, the Q-SMINT®IX features also direct loopback control via its register set.

3.2.1 Analog Loopback U-Transceiver (No. 3)

Loopback #3 is closed by the U-transceiver as near to the U-interface as possible, i.e. the loop is closed in the analog part by short circuiting the output to the input. The signal on the line is ignored in this state. For this reason it is also called analog loopback. All analog signals will still be passed on to the U-interface.

Before an analog loopback is closed by the appropriate C/I-command ARL (activation request loopback 3), the U-transceiver shall have been reset.

In order to open an analog loopback correctly, force the U-transceiver into the RESET state. This ensures that the echo coefficients and equalizer coefficients will converge correctly when activating anew.

3.2.2 Analog Loop-Back S-Transceiver

The Q-SMINT®IX provides test and diagnostic functions for the S/T interface:

The **internal local loop** (internal Loop A) is activated by a C/I command ARL or by setting the bit LP_A (Loop Analog) in the S_CMD register if the layer-1 statemachine is disabled.
The transmit data of the transmitter is looped back internally to the receiver. The data of the IOM®-2 input B- and D-channels are looped back to the output B- and D-channels.
The S/T interface level detector is enabled, i.e. if a level is detected this will be reported by the Resynchronization Indication (RSY) but the loop function is not affected.
Depending on the DIS_TX bit in the S_CONF2 register the internal local loop can be transparent or non transparent to the S/T line.

The **external local loop (external Loop A)** is activated in the same way as the internal local loop described above. Additionally the EXLP bit in the S_CONF0 register has to be programmed and the loop has to be closed externally as described in **Figure 73**.
The S/T interface level detector is disabled.

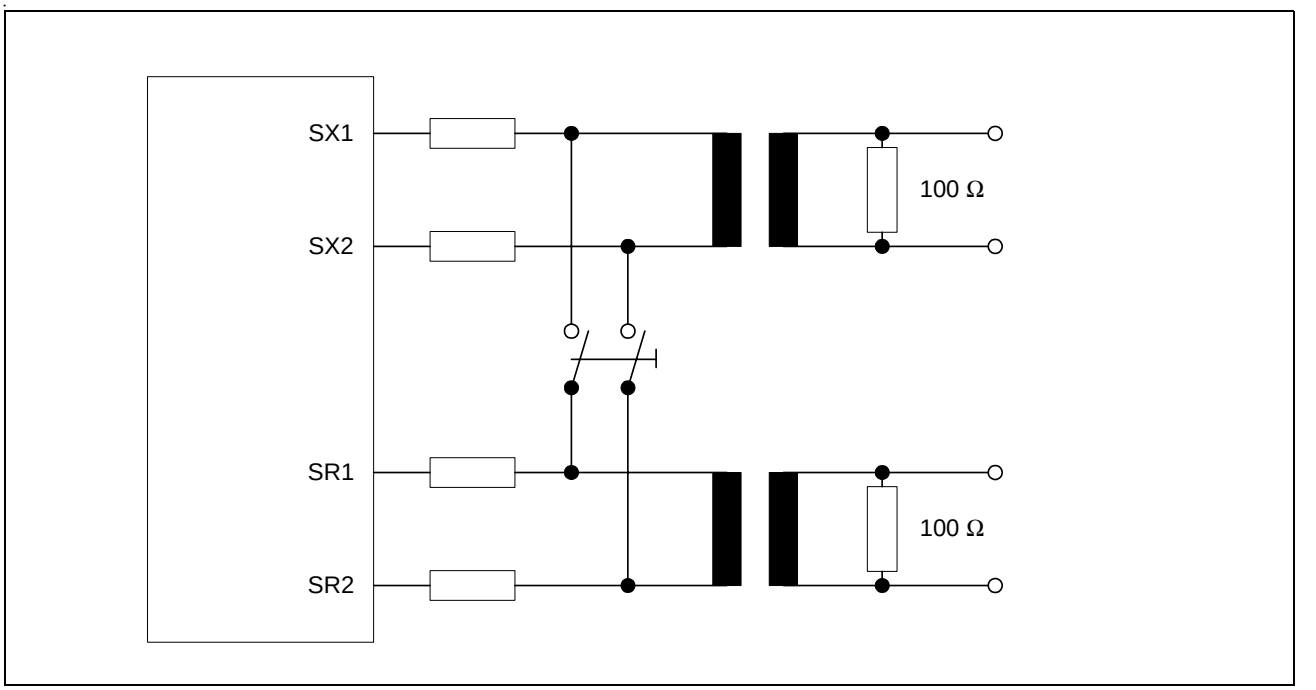


Figure 73 External Loop at the S/T-Interface

3.2.3 Loopback No.2

For loopback #2 several alternatives exist. Both the type of loopback and the location may vary. The following loopback types belong to the loopback-#2 category:

- complete loopback (B1,B2,D), in the U-transceiver
- complete loopback (B1,B2,D), in a downstream device
- B1-channel loopback, always performed in the U-transceiver
- B2-channel loopback, always performed in the U-transceiver

All loop variations performed by the U-transceiver are closed as near to the internal IOM®-2 interface as possible.

Normally loopback #2 is controlled by the exchange. The maintenance channel is used for this purpose. All loopback functions are latched. This allows channel B1 and channel B2 to be looped back simultaneously.

3.2.3.1 Complete Loopback

When receiving the request for a complete loopback, the U transceiver passes it on to the downstream device, e.g. the S-bus transceiver. This is achieved by issuing the C/I-code AIL in the “Transparent” state or C/I = ARL in states different than “Transparent” (note: this holds true only for the EOC automode). The U transceiver may be commanded to close the complete loopback itself.

Figure 74 illustrates the two options.

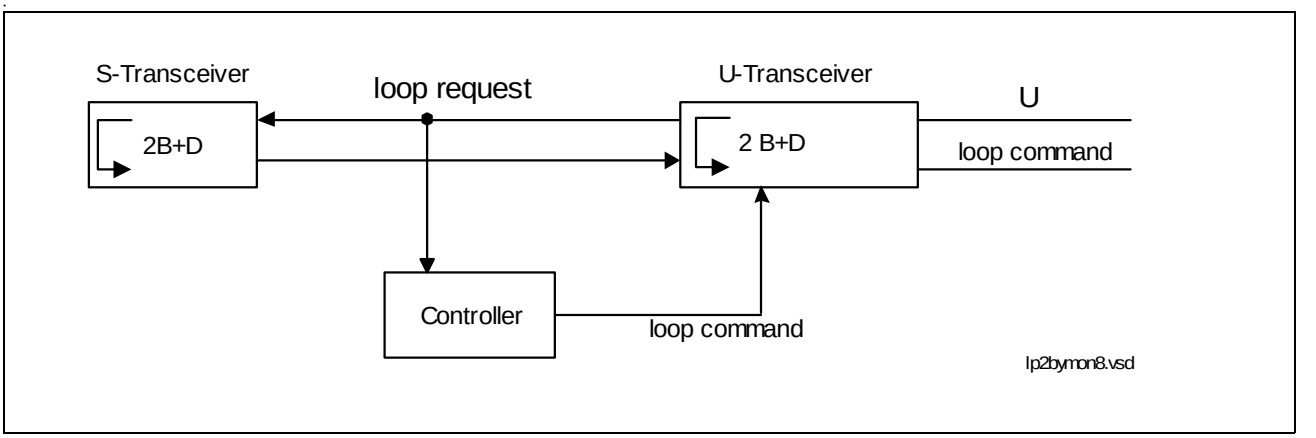


Figure 74 Complete Loopback Options in NT-Mode

The complete loopback is either opened under control of the exchange via the maintenance channel or locally controlled via the µC. No reset is required for loopback #2. The line stays active and is ready for data transmission.

3.2.3.2 Loopback No.2 - Single Channel Loopbacks

Single channel loopbacks are always performed directly in the U-Transceiver. No difference between the B1-channel and the B2-channel loopback control procedure exists.

3.2.4 Local Loopbacks Featured By the LOOP Register

Besides the standardized remote loopbacks the U-transceiver features additional local loopbacks for enhanced test and debugging facilities. The local loopbacks that are featured by register LOOP are shown in **Figure 75**. They are closed in the U-transceiver itself and can be activated regardless of the current operational status.

By the LOOP register it can be configured whether the loopback is closed only for the B1 and/or B2 or for 2B+D channels and whether the loopback is closed towards the internal IOM®-2 interface or towards the U-Interface.

By default the loopbacks are set to transparent mode. In transparent mode the data is both passed on and looped back. In non-transparent mode the data is not forwarded but substituted by 1s (idle code).

Besides the loopbacks in the system interface an additional digital loopback (DLB), the Framer/ Deframer loopback, is featured. It allows to test most digital functions of the U-transceiver besides the signal processing blocks.

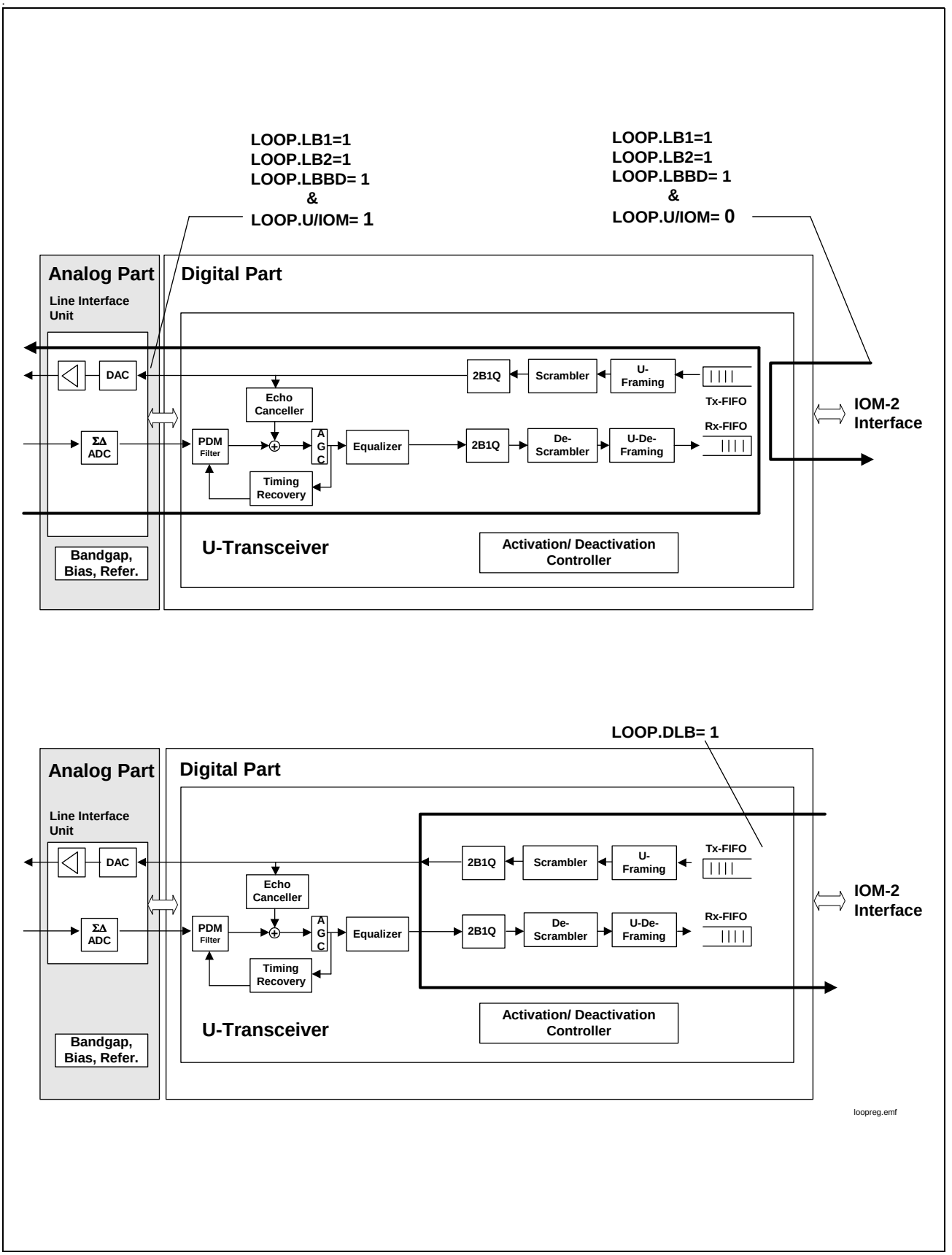


Figure 75 Loopbacks Featured by Register LOOP

3.3 External Circuitry

3.3.1 Power Supply Blocking Recommendation

The following blocking circuitry is suggested.

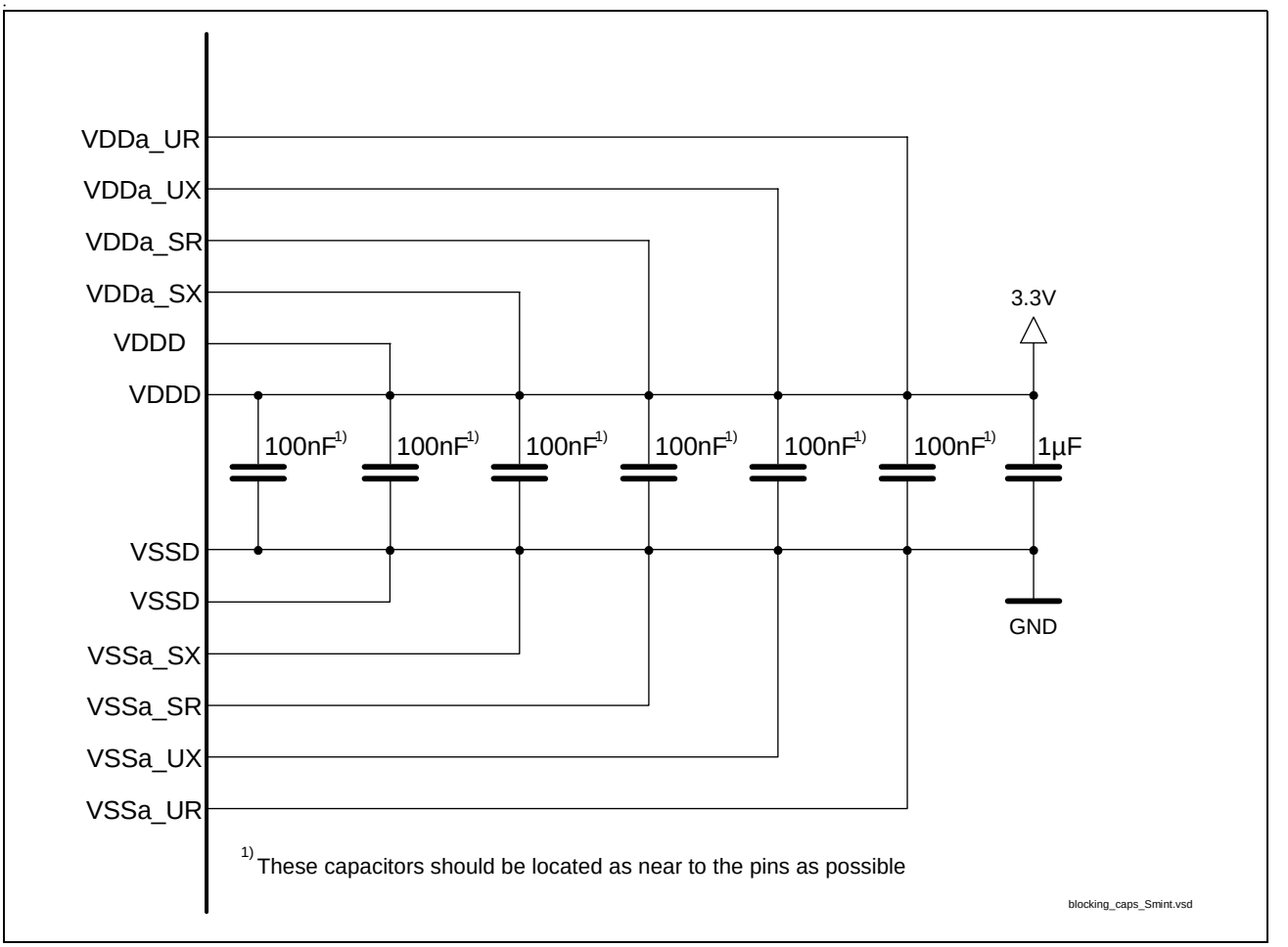


Figure 76 Power Supply Blocking

3.3.2 U-Transceiver

The Q-SMINT®IX is connected to the twisted pair via a transformer. **Figure 77** shows the recommended external circuitry. The recommended protection circuitry is not displayed.

Note: The integrated hybrid as specified for Version 1.1 is no more available in Version 1.3 and an external hybrid is required.

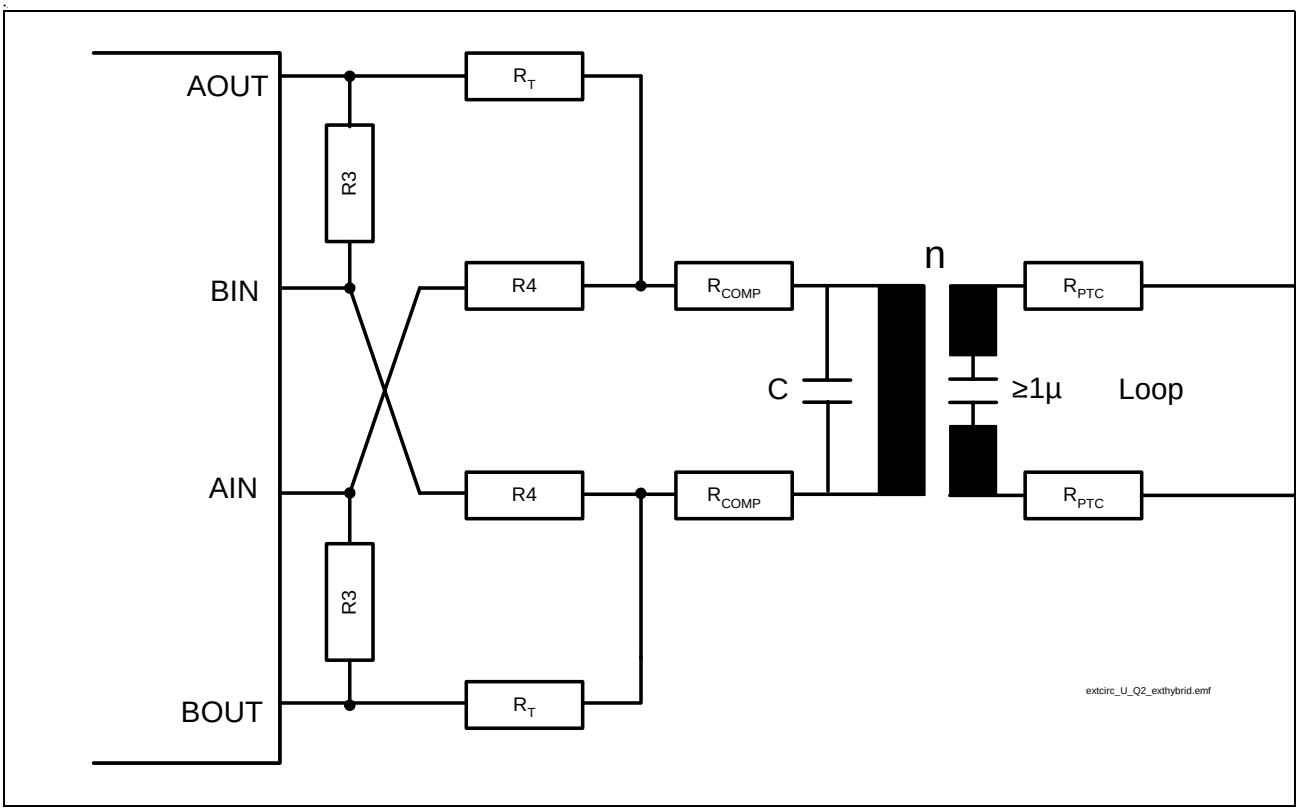


Figure 77 External Circuitry U-Transceiver

U-Transformer Parameters

The following **Table 36** lists parameters of typical U-transformers:

Table 36 U-Transformer Parameters

U-Transformer Parameters	Symbol	Value	Unit
U-Transformer ratio; Device side : Line side	n	1 : 2	
Main inductance of windings on the line side	L_H	14.5	mH
Leakage inductance of windings on the line side	L_S	<75	µH
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	100	pF
DC resistance of the windings on device side	R_B	2.5[1)]	Ω
DC resistance of the windings on line side	R_L	5[1)]	Ω

[1)] R_B / R_L according to equation[2]

Resistors of the External Hybrid R3, R4 and R_T

R3 = 1.3 kΩ

R4 = 1.0 kΩ

R_T = 9.5 Ω

Resistors on the Line Side R_{PTC} / Chip Side R_T

Optional use of up to 2x20 Ω resistors ($2xR_{PTC}$) on the line side of the transformer requires compensation resistors R_{COMP} depending on R_{PTC}:

$$2R_{PTC} + 8R_{COMP} = 40\ \Omega \quad (1)$$

$$2R_{PTC} + 4(2R_{COMP} + 2R_T + R_{OUT} + R_B) + R_L = 135\ \Omega \quad (2)$$

R_B, R_L : see **Table 36**
R_{OUT} : see **Table 43**

27 nF Capacitor C

To achieve optimum performance the 27 nF capacitor should be MKT. A Ceramic capacitor is not recommended.

Tolerances

- Rs: ±1%
- C=27 nF: ±10-20%
- L=14.5 mH: ±10%

3.3.3 S-Transceiver

In order to comply to the physical requirements of ITU recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the S-transceiver needs some additional circuitry.

S-Transformer Parameters

The following **Table 37** lists parameters of a typical S-transformer:

Table 37 S-Transformer Parameters

Transformer Parameters	Symbol	Value	Unit
Transformer ratio; Device side : Line side	n	2 : 1	
Main inductance of windings on the line side	L_H	typ. 30	mH
Leakage inductance of windings on the line side	L_S	typ. <3	µH
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	typ. <100	pF
DC resistance of the windings on device side	R_B	typ. 2.4	Ω
DC resistance of the windings on line side	R_L	typ. 1.4	Ω

Transmitter

The **transmitter** requires external resistors R_{stx} = 47Ω in order to adjust the output voltage to the pulse mask (nominal 750 mV according to ITU I.430, to be tested with the test mode “TM1”) on the one hand and in order to meet the output impedance of minimum 20 Ω on the other hand (to be tested with the testmode ’Continuous Pulses’) on the other hand.

Note: The resistance of the S-transformer must be taken into account when dimensioning the external resistors R_{stx}. If the transmit path contains additional components (e.g. a choke), then the resistance of these additional components must be taken into account, too.

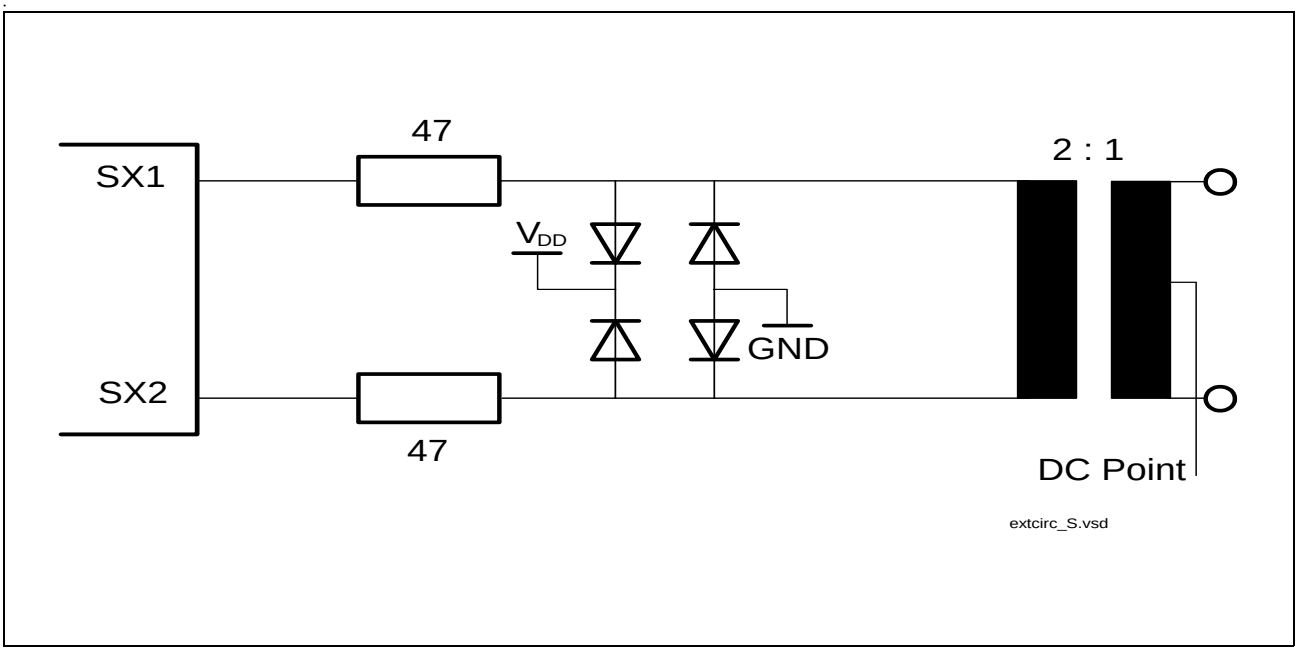


Figure 78 External Circuitry S-Interface Transmitter

Receiver

The **receiver** of the S-transceiver is symmetrical. 10 kΩ overall resistance are recommended in each receive path. It is preferable to split the resistance into two resistors for each line. This allows to place a high resistance between the transformer and the diode protection circuit (required to pass 96 kHz input impedance test of ITU I.430 [8] and ETS 300012-1). The remaining resistance (1.8 kΩ) protects the S-transceiver itself from input current peaks.

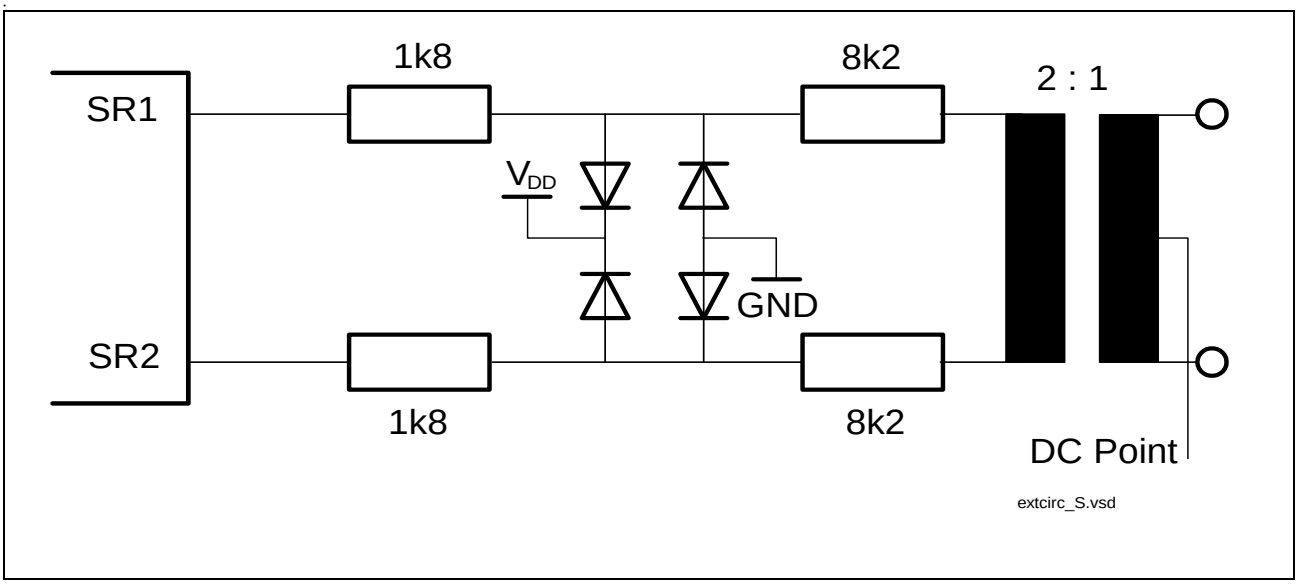


Figure 79 External Circuitry S-Interface Receiver

3.3.4 Oscillator Circuitry

Figure 80 illustrates the recommended oscillator circuit.

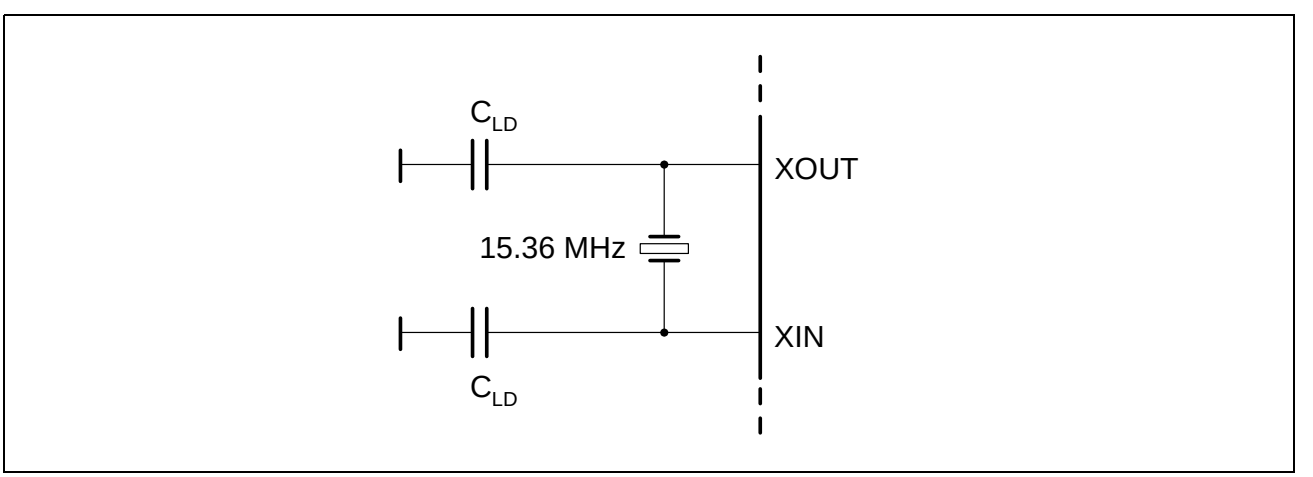


Figure 80 Crystal Oscillator

Table 38 Crystal Parameters

Parameter	Symbol	Limit Values	Unit
Frequency	f	15.36	MHz
Frequency calibration tolerance		+/-60	ppm
Load capacitance	C_L	20	pF
Max. resonance resistance	R1	20	Ω
Max. shunt capacitance	C_0	7	pF
Oscillator mode		fundamental	

External Components and Parasitics

The load capacitance C_L is computed from the external capacitances C_{LD}, the parasitic capacitances C_{Par} (pin and PCB capacitances to ground and V_{DD}) and the stray capacitance C_{IO} between XIN and XOUT:

$$C_L = \frac{(C_{LD} + C_{Par}) \times (C_{LD} + C_{Par})}{(C_{LD} + C_{Par}) + (C_{LD} + C_{Par})} + C_{IO}$$

For a specific crystal the total load capacitance is predefined, so the equation must be solved for the external capacitances C_{LD}, which is usually the only variable to be determined by the circuit designer. Typical values for the capacitances C_{LD} connected to the crystal are 22 - 33 pF.

3.3.5 General

- low power LEDs
- MLT input supports
  - APC13112
  - AT&T LH1465AB
  - discrete as proposed by Infineon

4 Register Description

4.1 Address Space

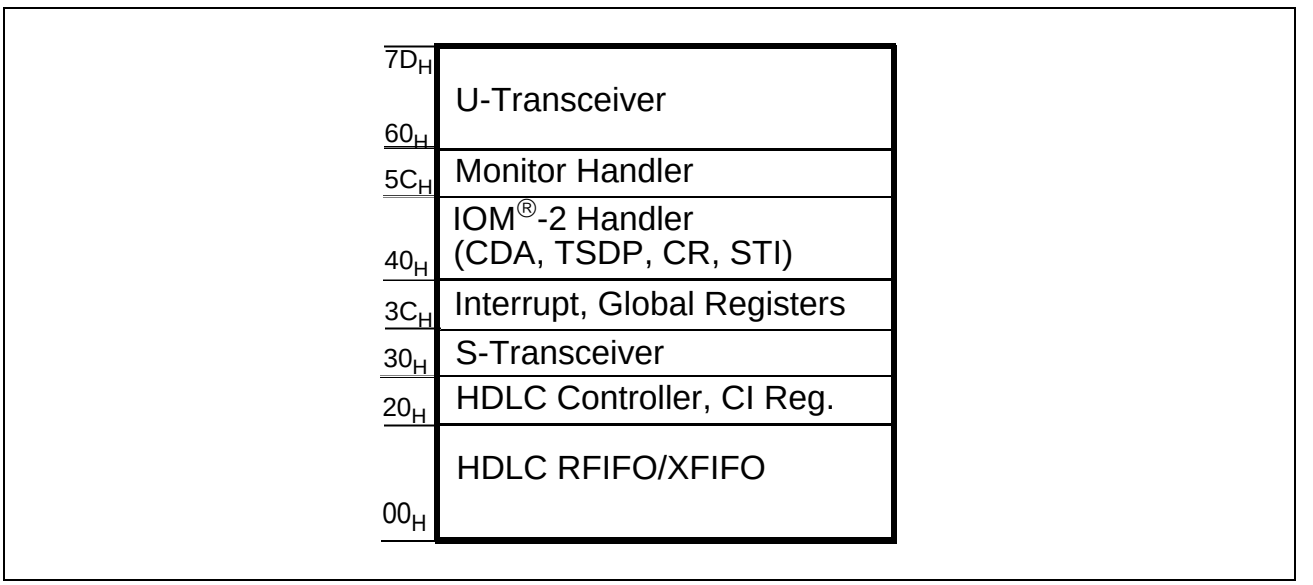


Figure 81 Address Space

4.2 Interrupts

Special events in the Q-SMINT®IX are indicated by means of a single interrupt output, which requests the host to read status information from the Q-SMINT®IX or transfer data from/to the Q-SMINT®IX.

Since only one $\overline{\text{INT}}$ request output is provided, the cause of an interrupt must be determined by the host reading the interrupt status registers of the Q-SMINT®IX.

The structure of the interrupt status registers is shown in **Figure 82**.

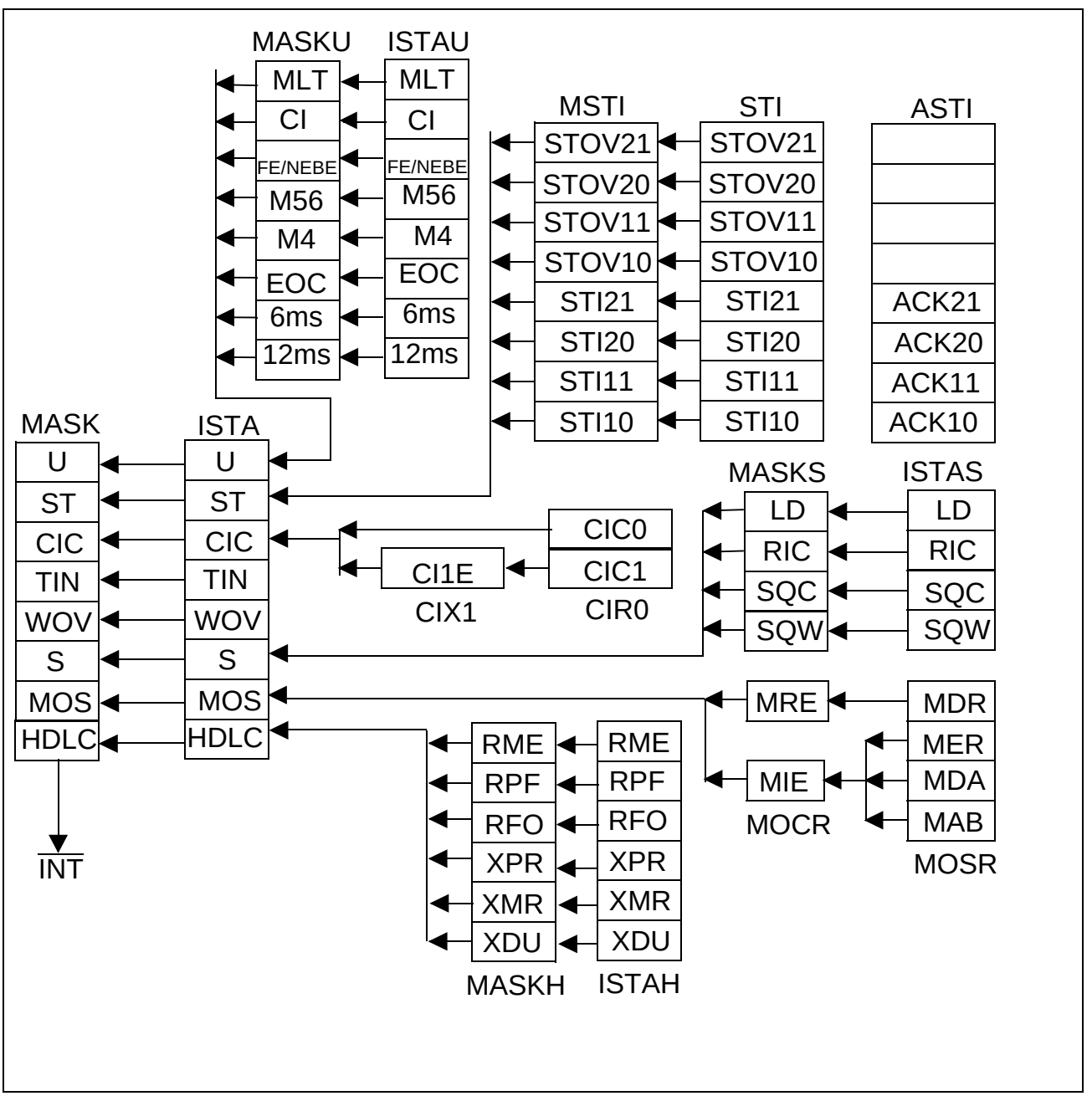


Figure 82 Q-SMINT®IX Interrupt Status Registers

Register Description

After the Q-SMINT®IX has requested an interrupt by setting its $\overline{\text{INT}}$ pin to low, the host must read first the Q-SMINT®IX interrupt status register (ISTA) in the associated interrupt service routine. The $\overline{\text{INT}}$ pin of the Q-SMINT®IX remains active until all interrupt sources are cleared. Therefore, it is possible that the INT pin is still active when the interrupt service routine is finished.

Each interrupt indication of the interrupt status registers can selectively be masked by setting the respective bit in the MASK register.

For some interrupt controllers or hosts it might be necessary to generate a new edge on the interrupt line to recognize pending interrupts. This can be done by masking all interrupts at the end of the interrupt service routine (writing FF_H into the MASK register) and writing back the old mask to the MASK register.

4.3 Register Summary

r(0) = reserved, implemented as zero.

HDLC Control Registers, CI Handler

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
RFIFO	D-Channel Receive FIFO								00_H-$1F_H$	R	
XFIFO	D-Channel Transmit FIFO								00_H-$1F_H$	W	
ISTAH	RME	RPF	RFO	XPR	XMR	XDU	r(0)	r(0)	20_H	R	10_H
MASKH	RME	RPF	RFO	XPR	XMR	XDU	0	0	20_H	W	FC_H
STAR	XDOV	XFW	r(0)	r(0)	RACI	r(0)	XACI	r(0)	21_H	R	40_H
CMDR	RMC	RRES	0	STI	XTF	0	XME	XRES	21_H	W	00_H
MODEH	MDS2	MDS1	MDS0	r(0)	RAC	DIM2	DIM1	DIM0	22_H	R/W	$C0_H$
EXMR	XFBS	RFBS		SRA	XCRC	RCRC	r(0)	ITF	23_H	R/W	00_H
TIMR	CNT			VALUE					24_H	R/W	00_H
SAP1	SAPI1						0	MHA	25_H	W	FC_H
SAP2	SAPI2						0	MLA	26_H	W	FC_H
RBCL	RBC7							RBC0	26_H	R	00_H
RBCH	r(0)	r(0)	r(0)	OV	RBC11			RBC8	27_H	R	00_H
TEI1	TEI1							EA1	27_H	W	FF_H
TEI2	TEI2							EA1	28_H	W	FF_H
RSTA	VFR	RDO	CRC	RAB	SA1	SA0	C/R	TA	28_H	R	$0F_H$
TMH	r(0)	r(0)	r(0)	r(0)	r(0)	r(0)	r(0)	TLP	29_H	R/W	00_H
	reserved								$2A_H$-$2D_H$		

Register Description

CIR0	CODR0		CIC0	CIC1	S/G	BAS	$2E_H$	R	$F3_H$
CIX0	CODX0		TBA2	TBA1	TBA0	BAC	$2E_H$	W	FE_H
CIR1	CODR1				CICW	CI1E	$2F_H$	R	FE_H
CIX1	CODX1				CICW	CI1E	$2F_H$	W	FE_H

S-Transceiver

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
S_ CONF0	DIS_ TR	BUS	EN_ ICV	0	L1SW	0	EXLP	0	30_H	R/W	40_H
	reserved								31_H		
S_ CONF2	DIS_ TX	0	0	0	0	0	0	0	32_H	R/W	80_H
S_STA	RINF		0	ICV	0	FSYN	0	LD	33_H	R	00_H
S_CMD	XINF			DPRIO	1	PD	LP_A	0	34_H	R/W	08_H
SQRR	MSYN	MFEN	0	0	SQR1	SQR2	SQR3	SQR4	35_H	R	00_H
SQXR	0	MFEN	0	0	SQX1	SQX2	SQX3	SQX4	35_H	W	00_H
	reserved								36_H-37_H		
ISTAS	0	x	x	x	LD	RIC	SQC	SQW	38_H	R	00_H
MASKS	1	1	1	1	LD	RIC	SQC	SQW	39_H	R/W	FF_H
S_ MODE	0	0	0	0	DCH_ INH	MODE2-0			$3A_H$	R/W	02_H
	reserved								$3B_H$		

Interrupt, General Configuration

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
ISTA	U	ST	CIC	TIN	WOV	S	MOS	HDLC	$3C_H$	R	00_H
MASK	U	ST	CIC	TIN	WOV	S	MOS	HDLC	$3C_H$	W	FF_H
MODE1	MCLK		CDS	WTC1	WTC2	CFS	RSS2	RSS1	$3D_H$	R/W	04_H
MODE2	LED2	LED1	LEDC	0	0	0	AMOD	PPSDX	$3E_H$	R/W	00_H
ID	0	0	DESIGN						$3F_H$	R	01_H
SRES	0	0	RES_ CI/TIC	0	RES_ HDLC	0	RES_ S	RES_ U	$3F_H$	W	00_H

IOM Handler (Timeslot, Data Port Selection, CDA Data and CDA Control Register)

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
CDA10	Controller Data Access Register								40_H	R/W	FF_H
CDA11	Controller Data Access Register								41_H	R/W	FF_H
CDA20	Controller Data Access Register								42_H	R/W	FF_H
CDA21	Controller Data Access Register								43_H	R/W	FF_H
CDA_ TSDP10	DPS	0	0	0	TSS				44_H	R/W	00_H
CDA_ TSDP11	DPS	0	0	0	TSS				45_H	R/W	01_H
CDA_ TSDP20	DPS	0	0	0	TSS				46_H	R/W	80_H
CDA_ TSDP21	DPS	0	0	0	TSS				47_H	R/W	81_H
	reserved								48_H-$4B_H$		
S_ TSDP_ B1	DPS	0	0	0	TSS				$4C_H$	R/W	84_H
S_ TSDP_ B2	DPS	0	0	0	TSS				$4D_H$	R/W	85_H
CDA1_ CR	0	0	EN_ TBM	EN_I1	EN_I0	EN_O1	EN_O0	SWAP	$4E_H$	R/W	00_H
CDA2_ CR	0	0	EN_ TBM	EN_I1	EN_I0	EN_O1	EN_O0	SWAP	$4F_H$	R/W	00_H

IOM Handler (Control Registers, Synchronous Transfer Interrupt Control)

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
	reserved								50_H		
S_CR	1	CI_CS	EN_D	EN_B2R	EN_B1R	EN_B2X	EN_B1X	D_CS	51_H	R/W	FF_H
HCI_CR	DPS_CI1	EN_CI1	EN_D	EN_B2H	EN_B1H	DPS_H	HCS		52_H	R/W	04_H
MON_CR	DPS	EN_MON	0	0	0	0	MCS		53_H	R/W	40_H
SDS1_CR	ENS_TSS	ENS_TSS+1	ENS_TSS+3	0	TSS				54_H	R/W	00_H
SDS2_CR	ENS_TSS	ENS_TSS+1	ENS_TSS+3	0	TSS				55_H	R/W	00_H
IOM_CR	SPU	0	0	TIC_DIS	EN_BCL	0	DIS_OD	DIS_IOM	56_H	R/W	08_H
MCDA	MCDA21		MCDA20		MCDA11		MCDA10		57_H	R	FF_H
STI	STOV21	STOV20	STOV11	STOV10	STI21	STI20	STI11	STI10	58_H	R	00_H
ASTI	0	0	0	0	ACK21	ACK20	ACK11	ACK10	58_H	W	00_H
MSTI	STOV21	STOV20	STOV11	STOV10	STI21	STI20	STI11	STI10	59_H	R/W	FF_H
	reserved								$5A_H$-$5B_H$		

MONITOR Handler

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
MOR	MONITOR Receive Data								$5C_H$	R	FF_H
MOX	MONITOR Transmit Data								$5C_H$	W	FF_H
MOSR	MDR	MER	MDA	MAB	0	0	0	0	$5D_H$	R	00_H
MOCR	MRE	MRC	MIE	MXC	0	0	0	0	$5E_H$	R/W	00_H
MSTA	0	0	0	0	0	MAC	0	TOUT	$5F_H$	R	00_H
MCONF	0	0	0	0	0	0	0	TOUT	$5F_H$	W	00_H

Register Summary U-Transceiver

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
OPMODE	0	UCI	FEBE	MLT	0	CI_ SEL	0	0	60_H	R*/W	14_H
MFILT	M56 FILTER		M4 FILTER			EOC FILTER			61_H	R*/W	14_H
	reserved								62_H		
EOCR	0	0	0	0	a1	a2	a3	d/m	63_H	R	$0F_H$
	i1	i2	i3	i4	i5	i6	i7	i8	64_H		FF_H
EOCW	0	0	0	0	a1	a2	a3	d/m	65_H	W	01_H
	i1	i2	i3	i4	i5	i6	i7	i8	66_H		00_H
M4RMASK	M4 Read Mask Bits								67_H	R*/W	00_H
M4WMASK	M4 Write Mask Bits								68_H	R*/W	$A8_H$
M4R	verified M4 bit data of last received superframe								69_H	R	BE_H
M4W	M4 bit data to be send with next superframe								$6A_H$	R*/W	BE_H
M56R	0	MS2	MS1	NEBE	M61	M52	M51	FEBE	$6B_H$	R	$1F_H$
M56W	1	1	1	1	M61	M52	M51	FEBE	$6C_H$	W	FF_H
UCIR	0	0	0	0	C/I code output				$6D_H$	R	00_H
UCIW	0	0	0	0	C/I code input				$6E_H$	W	01_H
TEST	0	0	0	0	CCRC	+-1 Tones	0	40 KHz	$6F_H$	R*/W	00_H
LOOP	0	DLB	TRANS	U/IOM	1	LBBD	LB2	LB1	70_H	R*/W	08_H
FEBE	FEBE Counter Value								71_H	R	00_H
NEBE	NEBE Counter Value								72_H	R	00_H
	reserved								73_H-79_H		

ISTAU	MLT	CI	FEBE/ NEBE	M56	M4	EOC	6ms	12ms	$7A_H$	R	00_H
MASKU	MLT	CI	FEBE/ NEBE	M56	M4	EOC	6ms	12ms	$7B_H$	R*/W	FF_H
	reserved								$7C_H$		
FW_ VERSION	FW Version Number								$7D_H$	R	$6x_H$
	reserved								$7E_H$- $7F_H$		

*) read back function for test use

Note: Registers, which are denoted as ‘reserved‘, may not be accessed by the µC, neither for read nor for write operations.

4.4 Reset of U-Transceiver Functions During Deactivation or with C/I-Code RESET

The following U-transceiver registers are reset during deactivation or with software reset:

Table 39 Reset of U-Transceiver Functions During Deactivation or with C/I-Code RESET

Register	Reset to	Affected Bits
EOCR	$0FFF_H$	all bits
EOCW	0100_H	all bits
M4R	BE_H	all bits
M4W	BE_H	all bits
M56R	$1F_H$	all bits are reset besides MS2 and MS1
M56W	FF_H	all bits
TEST		only bit CCRC is reset
LOOP		only the bits LBBD, LB2 and LB1 are reset

4.5 U-Transceiver Mode Register Evaluation Timing

The point of time when mode settings are detected and executed differs with the mode register type. Two different behaviors can be classified:

- evaluation and execution after SW-reset (C/I= RES) or upon transition out of state 'Deactivated'
  Note: Write access to these registers/bits is allowed only, while the state machine is in state Reset or Deactivated.
- immediate evaluation and execution

Below the mode registers are listed and grouped according to the different evaluation times as stated above.

Table 40 U-Transceiver Mode Register Evaluation Timing

Register	Affected Bits
Registers Evaluated After SW-Reset or Upon Transition Out of State Deactivated	
OPMODE	bit UCI, MLT
MFILT	complete register
Immediate Evaluation and Execution	
OPMODE	bit FEBE, CI_SEL
M4RMASK	complete register
M4WMASK	complete register
TEST	complete register
LOOP	complete register
MASKU	complete register

4.6 Detailed HDLC Control and C/I Registers

4.6.1 RFIFO - Receive FIFO

RFIFO read Address: 00-1F$_H$

7							0
Receive data							

The RFIFO contains up to 32 bytes of received data.

After an ISTAH.RPF interrupt, a complete data block is available. The block size can be 4, 8, 16, 32 bytes depending on the EXMR.RFBS setting.

After an ISTAH.RME interrupt, the number of received bytes can be obtained by reading the RBCL register.

A read access to any address within the range 00$_H$-1F$_H$ gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each read access. This allows for the use of efficient “move string” type commands by the microcontroller.

4.6.2 XFIFO - Transmit FIFO

XFIFO write Address: 00-1F$_H$

7							0
Transmit data							

Depending on EXMR.XFBS up to 16 or 32 bytes of transmit data can be written to the XFIFO following an ISTAH.XPR interrupt.

A write access to any address within the range 00-1F$_H$ gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each write access. This allows the use of efficient “move string” type commands by the microcontroller.

4.6.3 ISTAH - Interrupt Status Register HDLC

ISTAH read Address: 20_H

Value after reset: 10_H

Note: The reset value cannot be read right after reset as all interrupts are masked, i.e. the XPR interrupt remains internally stored and can only be read as soon as the corresponding mask bit is set to “0”.

7	6	5	4	3	2	1	0
RME	RPF	RFO	XPR	XMR	XDU	r(0)	r(0)

RME Receive Message End

0 = inactive

1 = One complete frame of length less than or equal to the defined block size (EXMR.RFBS) or the last part of a frame of length greater than the defined block size has been received. The contents are available in the RFIFO. The message length and additional information may be obtained from RBCH and RBCL and the RSTA register.

RPF Receive Full

0 = inactive

1 = A data block of a frame longer than the defined block size (EXMR.RFBS) has been received and is available in the RFIFO. The frame is not yet complete.

RFO Receive Frame Overflow

0 = inactive

1 = The received data of a frame could not be stored, because the RFIFO is occupied. The whole message is lost.
This interrupt can be used for statistical purposes and indicates that the microcontroller does not respond quickly enough to a RPF or RME interrupt (ISTAH).

XPR Transmit Pool Ready

0 = inactive

1 = A data block of up to the defined block size (EXMR.XFBS) can be written to the XFIFO.
A XPR interrupt will be generated in the following cases:
- after a XTF or XME command as soon as the 16 / 32 bytes in the XFIFO are available and the frame is not yet complete.
- after a XTF together with a XME command is issued, when the whole frame has been transmitted.
- after reset
- after XRES

XMR Transmit Message Repeat

0 = inactive

1 = The transmission of the last frame has to be repeated because a collision on the S bus has been detected after the 16^{th}/32^{nd} data byte of a transmit frame.

If a XMR interrupt occurs the transmit FIFO is locked until the XMR interrupt is read by the host (interrupt cannot be read if masked in MASKH).

XDU Transmit Data Underrun

0 = inactive

1 = The current transmission of a frame is aborted by transmitting seven ‘1’s because the XFIFO holds no further data. This interrupt occurs whenever the microcontroller has failed to respond to a XPR interrupt (ISTAH register) quick enough, after having initiated a transmission and the message to be transmitted is not yet complete.

If a XMR interrupt occurs the transmit FIFO is locked until the XDU interrupt is read by the host (interrupt cannot be read if masked in MASKH).

4.6.4 MASKH - Mask Register HDLC

MASKH write Address: 20_H

Value after reset: FC_H

7	6	5	4	3	2	1	0
RME	RPF	RFO	XPR	XMR	XDU	0	0

Each interrupt source in the ISTAH register can be selectively masked by setting the corresponding bit in MASKH to ‘1’. Masked interrupt status bits are not indicated when ISTAH is read. Instead, they remain internally stored and pending, until the mask bit is reset to ‘0’.

Bit 0..7 Mask Bits

0 = interrupt active

1 = interrupt masked

4.6.5 STAR - Status Register

STAR read Address: 21_H

Value after reset: 40_H

7	6	5	4	3	2	1	0
XDOV	XFW	r(0)	r(0)	RACI	r(0)	XACI	0

XDOV Transmit Data Overflow

0 = No transmit data overflow

1 = More than the selected block size of 16 or 32 bytes have been written into the XFIFO, i.e. data has been overwritten.

XFW Transmit FIFO Write Enable

0 = Data can not be written in the XFIFO

1 = Data can be written in the XFIFO. This bit may be polled instead of (or in addition to) using the XPR interrupt.

RACI Receiver Active Indication

0 = The HDLC receiver is not active

1 = The HDLC receiver is active when RACI = '1'. This bit may be polled. The RACI bit is set active after a begin flag has been received and is reset after receiving an abort sequence.

XACI Transmitter Active Indication

0 = The HDLC-transmitter is not active

1 = The HDLC-transmitter is active when XACI = '1'. This bit may be polled. The XACI-bit is active when a XTF-command is issued and the frame has not been completely transmitted.

4.6.6 CMDR - Command Register

CMDR write Address: 21_H

Value after reset: 00_H

7	6	5	4	3	2	1	0
RMC	RRES	0	STI	XTF	0	XME	XRES

RMC Receive Message Complete

0 = inactive

1 = Reaction to RPF (Receive Pool Full) or RME (Receive Message End) interrupt. By setting this bit, the microcontroller confirms that it has fetched the data, and indicates that the corresponding space in the RFIFO may be released.

RRES Receiver Reset

0 = inactive

1 = HDLC receiver is reset, the RFIFO is cleared of any data.

STI Start Timer

0 = inactive

1 = The Q-SMINT®IX hardware timer is started (see TIMR register).

XTF Transmit Transparent Frame

0 = inactive

1 = After having written up to 16 or 32 bytes (EXMR.XFBS) in the XFIFO, the microcontroller initiates the transmission of a transparent frame by setting this bit to ‘1’. The opening flag is automatically added to the message by the Q-SMINT®IX except in the extended transparent mode.

XME Transmit Message End

0 = inactive

1 = By setting this bit to ‘1’ the microcontroller indicates that the data block written last in the XFIFO completes the corresponding frame. The Q-SMINT®IX completes the transmission by appending the CRC (if XCRC = 0) and the closing flag sequence to the data except in the extended transparent mode.

XRES Transmitter Reset

0 = inactive

1 = HDLC transmitter is reset and the XFIFO is cleared of any data. This command can be used by the microcontroller to abort a frame currently in transmission.

All of these bits must not be set twice within one BCL clock cycle.

Note: After a XPR interrupt further data has to be written to the XFIFO and the appropriate Transmit Command (XTF) has to be written to the CMDR register again to continue transmission, when the current frame is not yet complete (see also XPR in ISTAH).
During frame transmission, the 0-bit insertion according to the HDLC bit-stuffing mechanism is done automatically except in extended transparent mode.

4.6.7 MODEH - Mode Register HDLC Controller

MODEH read/write Address: 22_H

Value after reset: $C0_H$

7							0
MDS2	MDS1	MDS0	r(0)	RAC	DIM2	DIM1	DIM0

MDS2-0 Mode Select
Determines the message transfer mode of the HDLC controller, as follows :

MDS2-0	Mode	Address Comparison		Remark
		1.Byte	2.Byte	
0 0 0	Reserved	–	–	–
0 0 1	Reserved	–	–	–
0 1 0	Non-Auto mode/8	TEI1,TEI2	–	One-byte address compare.
0 1 1	Non-Auto mode/16	SAP1,SAP2, SAPG	TEI1,TEI2, TEIG	Two-byte address compare.
1 0 0	Extended transparent mode	–	–	–
1 1 0	Transparent mode 0	–	–	No address compare. All frames accepted.
1 1 1	Transparent mode 1	SAP1,SAP2, SAPG	–	High-byte address compare.
1 0 1	Transparent mode 2	–	TEI1,TEI2, TEIG	Low-byte address compare.

Note: SAP1, SAP2: two programmable address values for the first received address byte (in the case of an address field longer than 1 byte);
SAPG = fixed value FC / FE_H.
TEI1, TEI2: two programmable address values for the second (or the only, in the case of a one-byte address) received address byte; TEIG = fixed value FF_H.

Two different methods of the high byte and/or low byte address comparison can be selected by setting SAP1.MHA and/or SAP2.MLA (see also description of these bits in **Chapter 4.6.10** or **Chapter 4.6.11** respectively).

RAC Receiver Active

0 = The HDLC data is not evaluated in the receiver

1 = The HDLC receiver is activated

DIM2-0 Digital Interface Modes
These bits define the characteristics of the IOM Data Ports (DU, DD). The DIM0 bit enables/disables the stop/go bit (S/G) evaluation. The DIM1 bit enables/disables the TIC bus access. The effect of the individual DIM bits is as follows:

0-0 = Stop/go bit evaluation is disabled

0-1 = Stop/go bit evaluation is enabled

00- = TIC bus access is enabled

01- = TIC bus access is disabled

1xx = Reserved

4.6.8 EXMR - Extended Mode Register

EXMR read/write Address: 23_H

Value after reset: 00_H

7						0
XFBS	RFBS	SRA	XCRC	RCRC	r(0)	ITF

XFBS Transmit FIFO Block Size

0 = Block size for the transmit FIFO data is 32 byte

1 = Block size for the transmit FIFO data is 16 byte

Note: A change of XFBS will take effect after a transmitter command (CMDR.XME, CMDR.XRES, CMDR.XTF) has been written.

RFBS Receive FIFO Block Size

00 = 32 byte

01 = 16 byte

10 = 8 byte

11 = 4 byte

Note: A change of RFBS will take effect after a receiver command (CMDR.RMC, CMDR.RRES) has been written.

SRA Store Receive Address

0 = Receive Address is not stored in the RFIFO

1 = Receive Address is stored in the RFIFO

XCRC Transmit CRC

0 = CRC is transmitted

1 = CRC is not transmitted

RCRC Receive CRC

0 = CRC is not stored in the RFIFO

1 = CRC is stored in the RFIFO

ITF Interframe Time Fill

Selects the inter-frame time fill signal which is transmitted between HDLC-frames.

0 = idle (continuous ‘1’)

1 = flags (sequence of patterns: ‘0111 1110’)

Note: ITF must be set to ‘0’ for power down mode.
In applications with D-channel access handling (collision resolution), the only possible inter-frame time fill is idle (continuous ‘1’). Otherwise the D-channel on the S/T-bus cannot be accessed.

4.6.9 TIMR - Timer Register

TIMR read/write Address: 24_H

Value after reset: 00_H

7	5	4	0
CNT		VALUE	

CNT CNT together with VALUE determines the time period T after which a TIN interrupt (ISTA) will be generated in the normal case:

CNT=0...6: T = CNT x 2.048 sec + T1 with T1 = (VALUE+1) x 0.064 sec

CNT=7: T = T1 = (VALUE+1) x 0.064 sec (generated periodically)

The timer can be started by setting the STI-bit in CMDR and will be stopped when a TIN interrupt is generated or the TIMR register is written.

Note: If CNT is set to 7, a TIN interrupt is indefinitely generated after every expiration of T = T1.

VALUE Determines the time period T1
T1 = (VALUE + 1) × 0.064 sec

4.6.10 SAP1 - SAPI1 Register

SAP1 write Address: 25_H

Value after reset: FC_H

7		0
SAPI1	0	MHA

SAPI1 SAPI1 value

Value of the programmable high address byte. In ISDN LADP protocol (D-channel) this is the Service Access Point Identifier (SAPI) and for B-channel applications it is the RAH value.

MHA Mask High Address

0 = The high address of an incoming frame is compared with SAP1, SAP2 and SAPG.

1 = The high address of an incoming frame is compared with SAP1 and SAPG.
SAP1 can be masked with SAP2. Bit positions of SAP1 are not compared if they are set to ‘1’ in SAP2.

4.6.11 SAP2 - SAPI2 Register

SAP2 write Address: 26_H

Value after reset: FC_H

7		0
SAPI2	0	MLA

SAPI2 SAPI2 value

Value of the programmable high address byte. In ISDN LADP protocol (D-channel) this is the Service Access Point Identifier (SAPI) and for B-channel applications it is the RAL value.

MLA Mask Low Address

0 = The TEI address of an incoming frame is compared with TEI1, TEI2 and TEIG.

1 = The TEI address of an incoming frame is compared with TEI1 and TEIG.
TEI1 can be masked with TEI2. Bit positions of TEI1 are not compared if they are set to ‘1’ in TEI2.

4.6.12 RBCL - Receive Frame Byte Count Low

RBCL read Address: 26_H

Value after reset: 00_H

7							0
RBC7							RBC0

RBC7-0 Receive Byte Count

Eight least significant bits of the total number of bytes in a received message (see RBCH register).

4.6.13 RBCH - Receive Frame Byte Count High for D-Channel

RBCH read Address: 27_H

Value after reset: 00_H.

7					0
r(0)	r(0)	r(0)	OV	RBC11	RBC8

OV Overflow

0 = Message shorter than $(2^{12} – 1) = 4095$ bytes.

1 = Message longer than $(2^{12} – 1) = 4095$ bytes.

RBC8-11 Receive Byte Count

Four most significant bits of the total number of bytes in a received message (see RBCL register).

Note: Normally RBCH and RBCL should be read by the microcontroller after a RME-interrupt, in order to determine the number of bytes to be read from the RFIFO, and the total message length. The contents of the registers are valid only after a RME or RPF interrupt, and remain so until the frame is acknowledged via the RMC bit or RRES.

4.6.14 TEI1 - TEI1 Register

TEI1 write Address: 27_H

Value after reset: FF_H

7							0
TEI1							EA1

TEI1 Terminal Endpoint Identifier

In all message transfer modes except for transparent modes 0, 1 and extended transparent mode, TEI1 is used by the Q-SMINT®IX for address recognition. In the case of a two-byte address field, it contains the value of the first programmable Terminal Endpoint Identifier according to the ISDN LAPD-protocol.

EA1 Address Field Extension Bit

This bit is set to ‘1’ according to HDLC/LAPD.

4.6.15 TEI2 - TEI2 Register

TEI2 write Address: 28_H

Value after reset: FF_H

7							0
TEI2							EA2

TEI2 Terminal Endpoint Identifier

In all message transfer modes except in transparent modes 0, 1 and extended transparent mode, TEI2 is used by the Q-SMINT®IX for address recognition. In the case of a two-byte address field, it contains the value of the second programmable Terminal Endpoint Identifier according of the ISDN LAPD-protocol.

EA2 Address Field Extension Bit

This bit is to be set to ‘1’ according to HDLC/LAPD.

4.6.16 RSTA - Receive Status Register

RSTA read Address: 28_H

Value after reset: $0F_H$

7							0
VFR	RDO	CRC	RAB	SA1	SA0	C/R	TA

VFR Valid Frame

Determines whether a valid frame has been received.
A frame is invalid when there is not a multiple of 8 bits between flag and frame end (flag, abort).

0 = The frame is invalid

1 = The frame is valid

RDO Receive Data Overflow

0 = No receive data overflow

1 = At least one byte of the frame has been lost, because it could not be stored in RFIFO. As opposed the ISTAH.RFO a RDO indicates that the beginning of a frame has been received but not all bytes could be stored as the RFIFO was temporarily full.

CRC CRC Check

0 = The CRC is incorrect

1 = The CRC is correct

RAB Receive Message Aborted

0 = The receive message was not aborted

1 = The receive message was aborted by the remote station, i.e. a sequence of seven 1’s was detected before a closing flag.

SA1-0 SAPI Address Identification

TA TEI Address Identification

These bits are only relevant in modes with address comparison.
The result of the address comparison is given by SA1-0 and TA, as follows:

				Address Match with	
MDS2-0	**SA1**	**SA0**	**TA**	**1st Byte**	**2nd Byte**
010 (Non-Auto/8 Mode)	x x	x x	0 1	TEI2 TEI1	- -
011 (Non-Auto/16 Mode)	0 0 0 0 1 1	0 0 1 1 0 0	0 1 0 1 0 1	SAP2 SAP2 SAPG SAPG SAP1 SAP1	TEIG TEI2 TEIG TEI1 or TEI2 TEIG TEI1
111 (Transparent Mode 1)	0 0 1	0 1 0	x x x	SAP2 SAPG SAP1	- - -
101 (Transparent Mode 2)	- -	- -	0 1	- -	TEIG TEI1 or TEI2
	1	1	x	reserved	

Note: If SAP1 and SAP2 contain identical values, the combination SAP1,2-TEIG will only be indicated by SAP1,0 = ’10’ (i.e. the value ’00’ will not occur in this case).

C/R Command/Response

The C/R bit contains the C/R bit of the received frame (Bit1 in the SAPI address).

Note: The contents of RSTA corresponds to the last received HDLC frame; it is duplicated into RFIFO for every frame (last byte of frame).

4.6.17 TMH -Test Mode Register HDLC

TMH read/write Address: 29_H

Value after reset: 00_H

7							0
r(0)	r(0)	r(0)	r(0)	r(0)	r(0)	r(0)	TLP

TLP Test Loop

0 = inactive

1 = The TX path of the HDLC controller is internally connected to its RX path. Data coming from the IOM-2 will not be forwarded to the HDLC controller.
Setting of TLP is only valid if IOM-2 is active.

Note: The bits7-1 have to be set to “0”.

4.6.18 CIR0 - Command/Indication Receive 0

CIR0 read Address: $2E_H$

Value after reset: $F3_H$

7				0
CODR0	CIC0	CIC1	S/G	BAS

CODR0 C/I0 Code Receive

Value of the received Command/Indication code. A C/I-code is loaded in CODR0 only after being the same in two consecutive IOM-frames and the previous code has been read from CIR0.

CIC0 C/I0 Code Change

0 = No change in the received Command/Indication code has been recognized

1 = A change in the received Command/Indication code has been recognized. This bit is set only when a new code is detected in two consecutive IOM-frames. It is reset by a read of CIR0.

CIC1 C/I1 Code Change

0 = No change in the received Command/Indication code has been recognized

1 = A change in the received Command/Indication code in IOM-channel 1 has been recognized. This bit is set when a new code is detected in one IOM-frame. It is reset by a read of CIR0.

S/G Stop/Go Bit Monitoring

Indicates the availability of the upstream D-channel;

0 = Go

1 = Stop

BAS Bus Access Status

Indicates the state of the TIC-bus:

0 = the Q-SMINT®IX itself occupies the D- and C/I-channel

1 = another device occupies the D- and C/I-channel

Note: The CODR0 bits are updated every time a new C/I-code is detected in two consecutive IOM-frames. If several consecutive valid new codes are detected and CIR0 is not read, only the first and the last C/I code are made available in CIR0 at the first and second read of that register.

4.6.19 CIX0 - Command/Indication Transmit 0

CIX0 write Address: $2E_H$

Value after reset: FE_H

7				0
CODX0	TBA2	TBA1	TBA0	BAC

CODX0 C/I0-Code Transmit

Code to be transmitted in the C/I-channel 0. The code is only transmitted if the TIC bus is occupied, otherwise “1s” are transmitted.

TBA2-0 TIC Bus Address

Defines the individual address for the Q-SMINT®IX on the IOM bus.
This address is used to access the C/I- and D-channel on the IOM interface.

Note: If only one device is liable to transmit in the C/I- and D-channels of the IOM it should always be given the address value ‘7’.

BAC Bus Access Control

Only valid if the TIC-bus feature is enabled (MODE:DIM2-0).

0 = inactive

1 = The Q-SMINT®IX will try to access the TIC-bus to occupy the C/I-channel even if no D-channel frame has to be transmitted. It should be reset when the access has been completed to grant a similar access to other devices transmitting in that IOM-channel.

Note: Access is always granted by default to the Q-SMINT®IX with TIC-Bus Address (TBA2-0, CIX0 register) ‘7’, which has the lowest priority in a bus configuration.

4.6.20 CIR1 - Command/Indication Receive 1

CIR1 read Address: $2F_H$

Value after reset: FE_H

7			0
CODR1		CICW	CI1E

CODR1 C/I1-Code Receive

CICW C/I-Channel Width
Contains the read back value from CIX1 register (see below)

0 = 4 bit C/I1 channel width

1 = 6 bit C/I1 channel width

CI1E C/I1-channel Interrupt Enable
Contains the read back value from CIX1 register (see below)

0 = Interrupt generation ISTA.CIC of CIR0.CIC1is masked

1 = Interrupt generation ISTA.CIC of CIR0.CIC1 is enabled

4.6.21 CIX1 - Command/Indication Transmit 1

CIX1 write Address: $2F_H$

Value after reset: FE_H

7			0
CODX1		CICW	CI1E

CODX1 C/I1-Code Transmit

Bits 5-0 of C/I-channel 1

CICW C/I-Channel Width

0 = 4 bit C/I1 channel width

1 = 6 bit C/I1 channel width

The C/I1 handler always reads and writes 6-bit values but if 4-bit is selected, the higher two bits are ignored for interrupt generation. However, in write direction the full CODX1 code is transmitted, i.e. the host must write the higher two bits to “1”.

CI1E C/I1-channel Interrupt Enable

0 = Interrupt generation ISTA.CIC of CIR0.CIC1is masked

1 = Interrupt generation ISTA.CIC of CIR0.CIC1 is enabled

4.7 Detailed S-Transceiver Registers

4.7.1 S_CONF0 - S-Transceiver Configuration Register 0

S_ CONF0 read/write Address: 30_H

Value after reset: 40_H

7							0
DIS_TR	BUS	EN_ ICV	0	L1SW	0	EXLP	0

DIS_TR Disable Transceiver

0 = All S-transceiver functions are enabled.

1 = All S-transceiver functions are disabled and powered down (analog and digital parts).

BUS Point-to-Point / Bus Selection

0 = Adaptive Timing (Point-to-Point, extended passive bus).

1 = Fixed Timing (Short passive bus), directly derived from transmit clock.

EN_ICV Enable Far End Code Violation

0 = normal operation.

1 = ICV enabled. The receipt of at least one illegal code violation within one multi-frame according to ANSI T1.605 is indicated by the C/I indication ‘1011’ (CVR) in two consecutive IOM frames.

L1SW Enable Layer 1 State Machine in Software

0 = Layer 1 state machine of the Q-SMINT®IX is used.

1 = Layer 1 state machine is disabled. The functionality must be realized in software.
The commands are written to register S_CMD and the status read in the S_STA.

EXLP External Loop

In case the analog loopback is activated with C/I = ARL or with the LP_A bit in the S_CMD register the loop is a

0 = internal loop next to the line pins

1 = external loop which has to be closed between SR1/SR2 and SX1/SX2

Note: For the external loop the transmitter must be enabled (S_CONF2:DIS_TX = 0).

4.7.2 S_CONF2 - S-Transmitter Configuration Register 2

S_ CONF2 read/write Address: 32_H

Value after reset: 80_H

7							0
DIS_TX	0	0	0	0	0	0	0

DIS_TX Disable Line Driver

0 = Transmitter is enabled

1 = Transmitter is disabled

4.7.3 S_STA - S-Transceiver Status Register

S_ STA read Address: 33_H

Value after reset: 00_H

7						0
RINF	0	ICV	0	FSYN	0	LD

Important: This register is used only if the Layer 1 state machine of the device is disabled (S_CONF0:L1SW = 1) and implemented in software! With the layer 1 state machine enabled, the signals from this register are automatically evaluated.

RINF Receiver INFO

00 = Received INFO 0 (no signal)

01 = Received any signal except INFO 0 or INFO 3

10 = reserved

11 = Received INFO 3

ICV Illegal Code Violation

0 = No illegal code violation is detected.

1 = Illegal code violation (ANSI T1.605) in data stream is detected.

FSYN Frame Synchronization State

0 = The S/T receiver is not synchronized.

1 = The S/T receiver has synchronized to the framing bit F.

LD Level Detection

0 = No receive signal has been detected on the line.

1 = Any receive signal has been detected on the line.

4.7.4 S_CMD - S-Transceiver Command Register

S_ CMD read/write Address: 34_H

Value after reset: 08_H

7					0
XINF	DPRIO	1	PD	LP_A	0

Important: This register - except bit DPRIO - is writable only if the Layer 1 state machine of the device is disabled (S_CONF0.L1SW = 1) and implemented in software! With the device layer 1 state machine enabled, the signals from this register are automatically generated. DPRIO can also be written in intelligent NT mode.

XINF Transmit INFO

000 = Transmit INFO 0

001 = reserved

010 = Transmit INFO 2

011 = Transmit INFO 4

100 = Send continuous pulses at 192 kbit/s alternating or 96 kHz rectangular, respectively (TM2)

101 = Send single pulses at 4 kbit/s with alternating polarity corresponding to 2 kHz fundamental mode (TM1)

11x = reserved

DPRIO D-Channel Priority

0 = Priority class 1 for D channel access on IOM

1 = Priority class 2 for D channel access on IOM

PD Power Down

0 = The transceiver is set to operational mode

1 = The transceiver is set to power down mode

LP_A Loop Analog

The setting of this bit corresponds to the C/I command ARL.

0 = Analog loop is open

1 = Analog loop is closed internally or externally according to the EXLP bit in the S_CONF0 register

4.7.5 SQRR - S/Q-Channel Receive Register

SQRR read Address: 35_H

Value after reset: 00_H

7							0
MSYN	MFEN	0	0	SQR1	SQR2	SQR3	SQR4

MSYN Multi-frame Synchronization State

0 = The S/T receiver has not synchronized to the received F_A and M bits

1 = The S/T receiver has synchronized to the received F_A and M bits

MFEN Multiframe Enable

Read-back of the MFEN bit of the SQXR register

0 = S/T multiframe is disabled

1 = S/T multiframe is enabled

SQR1-4 Received S/Q Bits

Received Q bits in frames 1, 6, 11 and 16

4.7.6 SQXR- S/Q-Channel Transmit Register

SQXR write Address: 35_H

Value after reset: 00_H

7							0
0	MFEN	0	0	SQX1	SQX2	SQX3	SQX4

MFEN Multiframe Enable

Used to enable or disable the multiframe structure.

0 = S/T multiframe is disabled

1 = S/T multiframe is enabled

SQX1-4 Transmitted S/Q Bits

Transmitted S bits in frames 1, 6, 11 and 16

4.7.7 ISTAS - Interrupt Status Register S-Transceiver

ISTAS read Address: 38_H

Value after reset: 00_H

7							0
x	x	x	x	LD	RIC	SQC	SQW

These bits are set if an interrupt status occurs and an interrupt signal is activated if the corresponding mask bit is set to “0”. If the mask bit is set to “1” no interrupt is generated, however the interrupt status bit is set in ISTAS. RIC, SQC and SQW are cleared by reading the corresponding source register S_STA, SQRR or writing SQXR, respectively.

x Reserved

LD Level Detection

0 = inactive

1 = Any receive signal has been detected on the line. This bit is set to “1” (i.e. an interrupt is generated if not masked) as long as any receive signal is detected on the line.

RIC Receiver INFO Change

0 = inactive

1 = RIC is activated if one of the S_STA bits RINF or ICV has changed.

SQC S/Q-Channel Change

0 = inactive

1 = A change in the received 4-bit Q-channel has been detected. The new code can be read from the SQRx bits of registers SQRR within the next multiframe[1)]. This bit is reset by a read access to the SQRR register.

SQW S/Q-Channel Writable

0 = inactive

1 = The S channel data for the next multiframe is writable.
The register for the S bits to be transmitted has to be written within the next multiframe. This bit is reset by writing register SQXR.
This timing signal is indicated with the start of every multiframe. Data which is written right after SQW-indication will be transmitted with the start of the following multiframe. Data which is written before SQW-indication is transmitted in the multiframe which is indicated by SQW.
SQW and SQC could be generated at the same time.

1) Register SQRR stays valid as long as no code change has been received.

4.7.8 MASKS - Mask S-Transceiver Interrupt

MASKS read/write Address: 39_H

Value after reset: FF_H

7							0
1	1	1	1	LD	RIC	SQC	SQW

Bit 3..0 Mask bits

0 = The transceiver interrupts LD, RIC, SQC and SQW are enabled

1 = The transceiver interrupts LD, RIC, SQC and SQW are masked

4.7.9 S_MODE - S-Transceiver Mode

S_ MODE read/write Address: $3A_H$

Value after reset: 02_H

7					0
0	0	0	0	DCH_INH	MODE

DCH_ INH D-Channel Inhibit

0 = inactive

1 = The S-transceiver blocks the access to the D-channel on S by inverting the E-bits.

MODE Mode Selection

000 = reserved

001 = reserved

010 = NT (without D-channel handler)

011 = LT-S (without D-channel handler)

110 Intelligent NT mode (with NT state machine and with D-channel handler)

111 Intelligent NT mode (with LT-S state machine and with D-channel handler)

100 reserved

101 reserved

4.8 Interrupt and General Configuration Registers

4.8.1 ISTA - Interrupt Status Register

ISTA read Address: $3C_H$

Value after reset: 00_H

7							0
U	ST	CIC	TIN	WOV	S	MOS	HDLC

U U-Transceiver Interrupt

0 = inactive

1 = An interrupt was generated by the U-transceiver. Read the ISTAU register.

ST Synchronous Transfer

0 = inactive

1 = This interrupt enables the microcontroller to lock on to the IOM®-2 timing, for synchronous transfers.

CIC C/I Channel Change

0 = inactive

1 = A change in C/I0 channel or C/I1 channel has been recognized. The actual value can be read from CIR0 or CIR1.

TIN Timer Interrupt

0 = inactive

1 = The internal timer and repeat counter has expired (see TIMR register).

WOV Watchdog Timer Overflow

0 = inactive

1 = Signals the expiration of the watchdog timer, which means that the microcontroller has failed to set the watchdog timer control bits WTC1 and WTC2 (MODE1 register) in the correct manner. A reset out pulse on pin $\overline{\text{RSTO}}$ has been generated by the Q-SMINT®IX.

S S-Transceiver Interrupt

0 = inactive

1 = An interrupt was generated by the S-transceiver. Read the ISTAS register.

MOS MONITOR Status

0 = inactive

1 = A change in the MONITOR Status Register (MOSR) has occurred.

HDLC HDLC Interrupt

0 = inactive

1 = An interrupt originated in the HDLC interrupt sources has been recognized.

Note: A read of the ISTA register clears only the TIN and WOV interrupts. The other interrupts are cleared by reading the corresponding status register.

4.8.2 MASK - Mask Register

MASK write Address: $3C_H$

Value after reset: FF_H

7							0
U	ST	CIC	TIN	WOV	S	MOS	HDLC

Bit 7..0 Mask bits

0 = Interrupt is not masked

1 = Interrupt is masked

Each interrupt source in the ISTA register can be selectively masked by setting the corresponding bit in MASK to ‘1’. Masked interrupt status bits are not indicated when ISTA is read. Instead, they remain internally stored and pending, until the mask bit is reset to ‘0’.

Note: In the event of a C/I channel change, CIC is set in ISTA even if the corresponding mask bit in MASK is active, but no interrupt is generated.

4.8.3 MODE1 - Mode1 Register

MODE1 read/write Address: $3D_H$

Value after reset: 04_H

7						0
MCLK	CDS	WTC1	WTC2	CFS	RSS2	RSS1

MCLK Master Clock Frequency

The Master Clock Frequency bits control the microcontroller clock output depending on MODE1.CDS = ’0’ or ’1’ (Table **Table 2.1.3**).

	MODE1.CDS = ’0’	MODE1.CDS = ’1’
00 =	3.84 MHz	7.68 MHz
01 =	0.96 MHz	1.92 MHz
10 =	7.68 MHz	15.36 MHz
11 =	disabled	disabled

CDS Clock Divider Selection

0 = The 15.36 MHz oscillator clock divided by two is input to the MCLK prescaler

1 = The 15.36 MHz oscillator clock is input to the MCLK prescaler.

WTC1, 2 Watchdog Timer Control 1, 2

After the watchdog timer mode has been selected (RSS = ‘11’) the watchdog timer is started. During every time period of 128 ms the microcontroller has to program the WTC1 and WTC2 bit in the following sequence (**Chapter 2.2**):

10 first step

01 second step

to reset and restart the watchdog timer.
If not, the timer expires and a WOV-interrupt (ISTA Register) together with a reset out pulse on pin $\overline{\text{RSTO}}$ is generated.
The watchdog timer runs only when the internal IOM®-2 clocks are active, i.e. the watchdog timer is dead when bit CFS = 1 and the U and S-transceivers are in state power down.

CFS Configuration Select

0 = The IOM®-2 interface clock and frame signals are always active, “Deactivated State” of the U-transceiver and the S-transceiver included.

1 = The IOM®-2 interface clocks and frame signals are inactive in the “Deactivated State” of the U-transceiver and the S-transceiver.

RSS2, RSS1 Reset Source Selection 2,1

The Q-SMINT®IX reset sources can be selected according to the table below.

	C/I Code Change	Watchdog Timer	POR/UVD and $\overline{\text{RST}}$
00 =	--	--	x
01 =		$\overline{\text{RSTO}}$ disabled (high impedance)	
10 =	x	--	x
11 =	--	x	x

4.8.4 MODE2 - Mode2 Register

MODE2 read/write Address: $3E_H$

Value after reset: 00_H

7							0
LED2	LED1	LEDC	0	0	0	AMOD	PPSDX

LED2,1 LED Control on pin $\overline{\text{ACT}}$

00 = High

01 = flashing at 8 Hz

10 = flashing at 1 Hz

11 = Low

LEDC LED Control Enable

0 = LED is controlled by the state machines as defined in **Table 4**.

1 = LED is controlled via bits LED2,1.

AMOD Address Mode

Selects between direct and indirect register access of the parallel microcontroller interface.

0 = Indirect address mode is selected. The address line A0 is used to select between address (A0 = ‘0’) and data (A0 = ‘1’) register

1 = Direct address mode is selected. The address is applied to the address bus (A0-A6)

PPSDX Push/Pull Output for SDX

0 = The SDX pin has open drain characteristic

1 = The SDX pin has push/pull characteristic

4.8.5 ID - Identification Register

ID read Address: $3F_H$

Value after reset: 01_H

7							0
0	0	DESIGN					

DESIGN **Design Number**

The design number (DESIGN) allows to identify different hardware designs[1] of the Q-SMINT®IX by software.

000000: Version 1.1

000001: Version 1.2

000001: Version 1.3

1) Distinction of different firmware versions is also possible by reading register $(7D)_H$ in the address space of the U-transceiver (see **Chapter 4.11.19**).

4.8.6 SRES - Software Reset Register

SRES write Address: $3F_H$

Value after reset: 00_H

7							0
0	0	RES_ CI/TIC	0	RES_ HDLC	0	RES_S	RES_U

RES_xx Reset_xx

0 = Deactivates the reset of the functional block xx

1 = Activates the reset of the functional block xx.
The reset state is activated as long as the bit is set to ‘1’

4.9 Detailed IOM®-2 Handler Registers

4.9.1 CDAxy - Controller Data Access Register xy

These registers are used for microcontroller access to the IOM®-2 timeslots as well as for timeslot manipulations. (e.g. loops, shifts, ... see also **“Controller Data Access (CDA)” on Page 31**).

CDAxy read/write Address: $40\text{-}43_H$

7							0
Controller Data Access Register							

Data register CDAxy which can be accessed by the controller.

Register	Value after Reset	Register Address
CDA10	FF_H	40_H
CDA11	FF_H	41_H
CDA20	FF_H	42_H
CDA21	FF_H	43_H

4.9.2 XXX_TSDPxy - Time Slot and Data Port Selection for CHxy

XXX_TSDPxy read/write Address: $44\text{-}4D_H$

7							0
DPS	0	0	0	TSS			

Register	Value after Reset	Register Address
CDA_TSDP10	00_H (= output on B1-DD)	44_H
CDA_TSDP11	01_H (= output on B2-DD)	45_H
CDA_TSDP20	80_H (= output on B1-DU)	46_H
CDA_TSDP21	81_H (= output on B2-DU)	47_H
	reserved	$48\text{-}4B_H$
S_TSDP_B1	84_H (= output on TS4-DU)	$4C_H$
S_TSDP_B2	85_H (= output on TS5-DU)	$4D_H$

This register determines the time slots and the data ports on the IOM®-2 Interface for the data channels xy of the functional units XXX (Controller Data Access (CDA) and S-transceiver (S)).

Note: The U-transceiver is always in IOM-2 channel 0.

DPS Data Port Selection

0 = The data channel xy of the functional unit XXX is output on DD. The data channel xy of the functional unit XXX is input from DU.

1 = The data channel xy of the functional unit XXX is output on DU. The data channel xy of the functional unit XXX is input from DD.

Note: For the CDA (controller data access) data the input is determined by the CDAx_CR.SWAP bit. If SWAP = '0' the input for the CDAxy data is vice versa to the output setting for CDAxy. If the SWAP = '1' the input from CDAx0 is vice versa to the output setting of CDAx1 and the input from CDAx1 is vice versa to the output setting of CDAx0.

TSS Timeslot Selection

Selects one of the 12 timeslots from 0...11 on the IOM®-2 interface for the data channels.

4.9.3 CDAx_CR - Control Register Controller Data Access CH1x

CDAx_CR read/write Address: $4E\text{-}4F_H$

7							0
0	0	EN_TBM	EN_I1	EN_I0	EN_O1	EN_O0	SWAP

Register	Value after Reset	Register Address
CDA1_CR	00_H	$4E_H$
CDA2_CR	00_H	$4F_H$

EN_TBM Enable TIC Bus Monitoring

0 = The TIC bus monitoring is disabled

1 = The TIC bus monitoring with the CDAx0 register is enabled. The TSDPx0 register must be set to 08_H for monitoring from DU, or 88_H for monitoring from DD.

EN_I1, EN_I0 Enable Input CDAx1, CDAx0

0 = The input of the CDAx1, CDAx0 register is disabled

1 = The input of the CDAx1, CDAx0 register is enabled

EN_O1, EN_O0 Enable Output CDAx1, CDAx0

0 = The output of the CDAx1, CDAx0 register is disabled

1 = The output of the CDAx1, CDAx0 register is enabled

SWAP **Swap Inputs**

0 = The time slot and data port for the input of the CDAxy register is defined by its own TSDPxy register. The data port for the CDAxy input is vice versa to the output setting for CDAxy.

1 = The input (time slot and data port) of the CDAx0 is defined by the TSDP register of CDAx1 and the input of CDAx1 is defined by the TSDP register of CDAx0. The data port for the CDAx0 input is vice versa to the output setting for CDAx1. The data port for the CDAx1 input is vice versa to the output setting for CDAx0. The input definition for time slot and data port CDAx0 are thus swapped to CDAx1 and for CDAx1 to CDAx0. The outputs are not affected by the SWAP bit.

4.9.4 S_CR - Control Register S-Transceiver Data

S_CR read/write Address: 51_H

Value after reset: FF_H

7							0
1	CI_CS	EN_D	EN_B2R	EN_B1R	EN_B2X	EN_B1X	D_CS

CI_CS C/I Channel Selection

This bit is used to select the IOM channel to which the S-transceiver C/I-channel is related to.

0 = C/I-channel in IOM-channel 0

1 = C/I-channel in IOM-channel 1

EN_D Enable Transceiver D-Channel Data

0 = The corresponding data path to the transceiver is disabled

1 = The corresponding data path to the transceiver is enabled.

EN_B2R Enable Transceiver B2 Receive Data (transmitter receives from IOM)

0 = The corresponding data path to the transceiver is disabled

1 = The corresponding data path to the transceiver is enabled.

EN_B1R Enable Transceiver B1 Receive Data (transmitter receives from IOM)

0 = The corresponding data path to the transceiver is disabled

1 = The corresponding data path to the transceiver is enabled.

EN_B2X Enable Transceiver B2 Transmit Data (transmitter transmits to IOM)

0 = The corresponding data path to the transceiver is disabled

1 = The corresponding data path to the transceiver is enabled.

EN_B1X Enable Transceiver B1 Transmit Data (transmitter transmits to IOM)

0 = The corresponding data path to the transceiver is disabled

1 = The corresponding data path to the transceiver is enabled.

These bits are used to individually enable/disable the D-channel and the receive/transmit paths for the B-channels for the S-transceiver.

D_CS D Channel Selection

This bit is used to select the IOM channel to which the S-transceiver D-channel is related to.

0 = D-channel in IOM-channel 0

1 = D-channel in IOM-channel 1

4.9.5 HCI_CR - Control Register for HDLC and CI1 Data

HCI_CR read/write Address: 52_H

Value after reset: 04_H

7						0
DPS_CI1	EN_CI1	EN_D	EN_B2H	EN_B1H	DPS_H	HCS

DPS_CI1 Data Port Selection CI1 Handler

0 = The CI1 data is output on DD and input from DU

1 = The CI1 data is output on DU and input from DD

EN_CI1 Enable CI1 Handler

0 = CI1 data access is disabled

1 = CI1 data access is enabled

Note: The timeslot for the C/I1 handler cannot be programmed but is fixed to IOM channel 1.

EN_D Enable D-timeslot for HDLC controller

0 = The HDLC controller does not access timeslot data D

1 = The HDLC controller does access timeslot data D

EN_B2H Enable B2-timeslot for HDLC controller

0 = The HDLC controller does not access timeslot data B2

1 = The HDLC controller does access timeslot data B2

EN_B1H Enable B1-timeslot for HDLC controller

0 = The HDLC controller does not access timeslot data B1 respectively

1 = The HDLC controller does access timeslot data B1

The bits EN_D, EN_B2H and EN_B1H are used to select the timeslot length for the D-channel HDLC controller access as it is capable to access not only the D-channel timeslot. The host can individually enable two 8-bit timeslots B1- and B2-channel, i.e. the first and second octett, (EN_B1H, EN_B2H) and one 2-bit timeslot D-channel (EN_D) on IOM-2. The position is selected via HCS.

DPS_H Data Port Selection HDLC

0 = Transmit on DD, receive on DU

1 = Transmit on DU, receive on DD

HCS HDLC Channel Selection

These two bits determine the IOM®-2 channel of the HDLC controller. The HDLC controller will read and write HDLC data into the selected B1, B2 and D channel timeslots of the selected IOM®-2 channel.

00 = The HDLC data is read and output on IOM-channel 0

01 = The HDLC data is read and output on IOM-channel 1

10 = The HDLC data is read and output on IOM-channel 2[1)]

11 = Not defined

1) If the TIC-bus is enabled, then an HDLC access in IOM-channel 2 is possible only to the B channels.

4.9.6 MON_CR - Control Register Monitor Data

MON_CR read/write Address: 53_H

Value after reset: 40_H

7						0
DPS	EN_MON	0	0	0	0	MCS

DPS Data Port Selection

0 = The Monitor data is output on DD and input from DU

1 = The Monitor data is output on DU and input from DD

EN_MON Enable Output

0 = The Monitor data input and output is disabled

1 = The Monitor data input and output is enabled

MCS MONITOR Channel Selection

00 = The MONITOR data is output on MON0

01 = The MONITOR data is output on MON1

10 = The MONITOR data is output on MON2

11 = Not defined

4.9.7 SDS1_CR - Control Register Serial Data Strobe 1

SDS1_CR read/write Address: 54_H

Value after reset: 00_H

7				0
ENS_ TSS	ENS_ TSS+1	ENS_ TSS+3	0	TSS

This register is used to select position and length of the strobe signal 1. The length can be any combination of two 8-bit timeslot (ENS_TSS, ENS_TSS+1) and one 2-bit timeslot (ENS_TSS+3).

ENS_ TSS Enable Serial Data Strobe of timeslot TSS

0 = The serial data strobe signal SDS1 is inactive during TSS

1 = The serial data strobe signal SDS1 is active during TSS

ENS_ TSS+1 Enable Serial Data Strobe of timeslot TSS+1

0 = The serial data strobe signal SDS1 is inactive during TSS+1

1 = The serial data strobe signal SDS1 is active during TSS+1

ENS_ TSS+3 Enable Serial Data Strobe of timeslot TSS+3 (D-Channel)

0 = The serial data strobe signal SDS1 is inactive during the D-channel (bit7, 6) of TSS+3

1 = The serial data strobe signal SDS1 is active during the D-channel (bit7, 6) of TSS+3

TSS Timeslot Selection

Selects one of 12 timeslots on the IOM®-2 interface (with respect to FSC) during which SDS1 is active high. The data strobe signal allows standard data devices to access a programmable channel.

4.9.8 SDS2_CR - Control Register Serial Data Strobe 2

SDS2_CR read/write Address: 55_H

Value after reset: 00_H

7				0
ENS_ TSS	ENS_ TSS+1	ENS_ TSS+3	0	TSS

This register is used to select position and length of the strobe signal 2. The length can be any combination of two 8-bit timeslot (ENS_TSS, ENS_TSS+1) and one 2-bit timeslot (ENS_TSS+3).

ENS_ TSS Enable Serial Data Strobe of timeslot TSS

0 = The serial data strobe signal SDS2 is inactive during TSS

1 = The serial data strobe signal SDS2 is active during TSS

ENS_ TSS+1 Enable Serial Data Strobe of timeslot TSS+1

0 = The serial data strobe signal SDS2 is inactive during TSS+1

1 = The serial data strobe signal SDS2 is active during TSS+1

ENS_ TSS+3 Enable Serial Data Strobe of timeslot TSS+3 (D-Channel)

0 = The serial data strobe signal SDS2 is inactive during the D-channel (bit7, 6) of TSS+3

1 = The serial data strobe signal SDS2 is active during the D-channel (bit7, 6) of TSS+3

TSS Timeslot Selection

Selects one of 12 timeslots on the IOM®-2 interface (with respect to FSC) during which SDS2 is active high. The data strobe signal allows standard data devices to access a programmable channel.

4.9.9 IOM_CR - Control Register IOM Data

IOM_CR read/write Address: 56_H

Value after reset: 08_H

7							0
SPU	0	0	TIC_DIS	EN_BCL	0	DIS_OD	DIS_IOM

SPU Software Power UP

0 = The DU line is normally used for transmitting data.

1 = Setting this bit to ‘1’ will pull the DU line to low. This will enforce the Q-SMINT®IX and other connected layer 1 devices to deliver IOM-clocking.

TIC_DIS TIC Bus Disable

0 = The last octet of the last IOM time slot (TS 11) is used as TIC bus.

1 = The TIC bus is disabled. The last octet of the last IOM time slot (TS 11) can be used like any other time slot. This means that the timeslots TIC, A/B, S/G and BAC are not available any more.

EN_BCL Enable Bit Clock BCL

0 = The BCL clock is disabled (output is high impedant)

1 = The BCL clock is enabled

DIS_OD Disable Open Drain

0 = IOM outputs are open drain driver

1 = IOM outputs are push pull driver

DIS_IOM Disable IOM

DIS_IOM should be set to ‘1’ if external devices connected to the IOM interface should be “disconnected” e.g. for power saving purposes. However, the Q-SMINT®IX internal operation is independent of the DIS_IOM bit.

0 = The IOM interface is enabled

1 = The IOM interface is disabled (FSC, DCL, clock outputs have high impedance; DU, DD data line inputs are switched off and outputs are high impedant)

4.9.10 MCDA - Monitoring CDA Bits

MCDA read Address: 57_H

Value after reset: FF_H

7							0
MCDA21		MCDA20		MCDA11		MCDA10	
Bit7	Bit6	Bit7	Bit6	Bit7	Bit6	Bit7	Bit6

MCDAxy Monitoring CDAxy Bits

Bit 7 and Bit 6 of the CDAxy registers are mapped into the MCDA register.

This can be used for monitoring the D-channel bits on DU and DD and the “Echo bits” on the TIC bus with the same register.

4.9.11 STI - Synchronous Transfer Interrupt

STI read Address: 58_H

Value after reset: 00_H

7							0
STOV21	STOV20	STOV11	STOV10	STI21	STI20	STI11	STI10

For all interrupts in the STI register the following logical states are applied

0 = Interrupt has not occurred

1 = Interrupt has occurred

STOVxy Synchronous Transfer Overflow Interrupt

Enabled STOV interrupts for a certain STIxy interrupt are generated when the STIxy has not been acknowledged in time via the ACKxy bit in the ASTI register. This must be one (for DPS = ‘0’) or zero (for DPS = ‘1’) BCL clock cycles before the time slot which is selected for the STOV.

STIxy Synchronous Transfer Interrupt

Depending on the DPS bit in the corresponding TSDPxy register the Synchronous Transfer Interrupt STIxy is generated two (for DPS = ‘0’) or one (for DPS = ‘1’) BCL clock cycles after the selected time slot (TSDPxy.TSS).

Note: ST0Vxy and ACKxy are useful for synchronizing microcontroller accesses and receive/transmit operations. One BCL clock is equivalent to two DCL clocks.

4.9.12 ASTI - Acknowledge Synchronous Transfer Interrupt

ASTI write Address: 58_H

Value after reset: 00_H

7							0
0	0	0	0	ACK21	ACK20	ACK11	ACK10

ACKxy Acknowledge Synchronous Transfer Interrupt

After a STIxy interrupt the microcontroller has to acknowledge the interrupt by setting the corresponding ACKxy bit.

0 = No activity is initiated

1 = Sets the acknowledge bit ACKxy for a STIxy interrupt

4.9.13 MSTI - Mask Synchronous Transfer Interrupt

MSTI read/write Address: 59_H

Value after reset: FF_H

7							0
STOV21	STOV20	STOV11	STOV10	STI21	STI20	STI11	STI10

For the MSTI register the following logical states are applied:

0 = Interrupt is not masked

1 = Interrupt is masked

STOVxy Mask Synchronous Transfer Overflow xy

Mask bits for the corresponding STOVxy interrupt bits.

STIxy Synchronous Transfer Interrupt xy

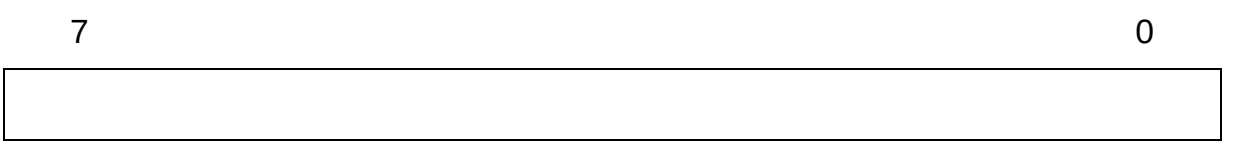
Mask bits for the corresponding STIxy interrupt bits.

4.10 Detailed MONITOR Handler Registers

4.10.1 MOR - MONITOR Receive Channel

MOR read Address: $5C_H$

Value after reset: FF_H

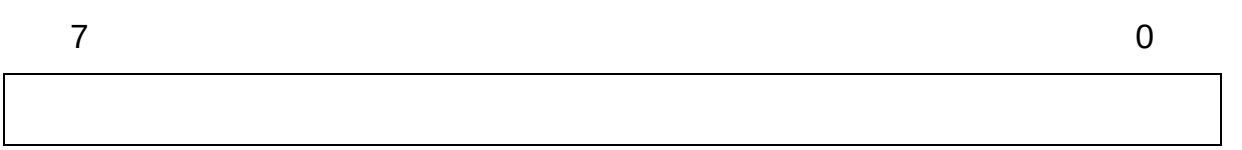


Contains the MONITOR data received in the IOM®-2 MONITOR channel according to the MONITOR channel protocol. The MONITOR channel (0,1,2) can be selected by setting the monitor channel select bit MON_CR.MCS.

4.10.2 MOX - MONITOR Transmit Channel

MOX write Address: $5C_H$

Value after reset: FF_H



Contains the MONITOR data to be transmitted in IOM®-2 MONITOR channel according to the MONITOR channel protocol. The MONITOR channel (0,1,2) can be selected by setting the monitor channel select bit MON_CR.MCS

4.10.3 MOSR - MONITOR Interrupt Status Register

MOSR read Address: $5D_H$

Value after reset: 00_H

7							0
MDR	MER	MDA	MAB	0	0	0	0

MDR MONITOR channel Data Received

0 = inactive

1 = MONITOR channel Data Received

MER MONITOR channel End of Reception

0 = inactive

1 = MONITOR channel End of Reception

MDA MONITOR channel Data Acknowledged

The remote end has acknowledged the MONITOR byte being transmitted.

0 = inactive

1 = MONITOR channel Data Acknowledged

MAB MONITOR channel Data Abort

0 = inactive

1 = MONITOR channel Data Abort

4.10.4 MOCR - MONITOR Control Register

MOCR read/write Address: $5E_H$

Value after reset: 00_H

7							0
MRE	MRC	MIE	MXC	0	0	0	0

MRE MONITOR Receive Interrupt Enable

0 = MONITOR interrupt status MDR generation is masked.

1 = MONITOR interrupt status MDR generation is enabled.

MRC MR Bit Control

Determines the value of the MR bit:

0 = MR is always ‘1’. In addition, the MDR interrupt is blocked, except for the first byte of a packet (if MRE = 1).

1 = MR is internally controlled by the Q-SMINT®IX according to MONITOR channel protocol. In addition, the MDR interrupt is enabled for all received bytes according to the MONITOR channel protocol (if MRE = 1).

MIE MONITOR Interrupt Enable

0 = MONITOR interrupt status MER, MDA, MAB generation is masked

1 = MONITOR interrupt status MER, MDA, MAB generation is enabled

MXC MX Bit Control

Determines the value of the MX bit:

0 = The MX bit is always ‘1’.

1 = The MX bit is internally controlled by the Q-SMINT®IX according to MONITOR channel protocol.

4.10.5 MSTA - MONITOR Status Register

MSTA read Address: $5F_H$

Value after reset: 00_H

7							0
0	0	0	0	0	MAC	0	TOUT

MAC MONITOR Transmit Channel Active

0 = No data transmission in the MONITOR channel

1 = The data transmission in the MONITOR channel is in progress.

TOUT Time-Out

Read-back value of the TOUT bit

0 = The monitor time-out function is disabled

1 = The monitor time-out function is enabled

4.10.6 MCONF - MONITOR Configuration Register

MCONF write Address: $5F_H$

Value after reset: 00_H

7							0
0	0	0	0	0	0	0	TOUT

TOUT Time-Out

0 = The monitor time-out function is disabled

1 = The monitor time-out function is enabled

4.11 Detailed U-Transceiver Registers

4.11.1 OPMODE - Operation Mode Register

The **Op**eration **Mode** register determines the operating mode of the U-transceiver.

OPMODE read*)/**write** Address: 60_H

Reset Value: 14_H

7	6	5	4	3	2	1	0
0	UCI	FEBE	MLT	0	CI_SEL	0	0

UCI Enable/Disable µC Control of C/I Codes

0 = µC control disabled - C/I codes are exchanged via IOM®-2
Read access to register UCIR by the µP is still possible

1 = µC control enabled - C/I codes are exchanged via UCIR and UCIW registers
In this case, the according C/I-channel on IOM®-2 is idle ‘1111‘

FEBE Enable/Disable External Write Access to FEBE Bit in Register M56W

0 = external access to FEBE bit disabled - FEBE bit is controlled by internal FEBE counter

1 = external access to FEBE bit enabled - FEBE bit is controlled by external microprocessor

MLT Enable/Disable Metallic Loop Termination Function
MLT status is reflected in bit MS2 and MS1 in register M56R

0 = MLT disabled

1 = MLT enabled

CI_SEL C/I Code Output Selection
by CI_SEL the user can switch:
– between the standard C/I indications of the NT state machine as implemented in today’s IEC-Q versions or
– newly defined C/I code indications which facilitates control and debugging

0 = Standard NT state machine
compliant to NT state machine of today’s IEC-Q V4.3-V5.3

1 = Simplified NT state machine
output of newly defined C/I code indications for enhanced activation/deactivation control and debugging facilities

4.11.2 MFILT - M Bit Filter Options

The **M Bit Filter** register defines the validation algorithm received Maintenance channel bits (EOC, M4, M56) of the U-interface have to undergo before they are approved and passed on to the µC.

MFILT read*)/**write** Address: 61_H

Reset Value: 14_H

7	6	5	4	3	2	1	0

M56 FILTER	M4 FILTER	EOC FILTER

M56 FILTER controls the validation mode of the spare bits (M51, M52, M61) **on a per bit base** (see **Chapter 2.4.4.3**)**.**

X0 = Apply **same filter** to M5 and M6 bit data as programmed for M4 bit data.

X1 = **On Change**

M4 Filter 3-bit field which controls the validation mode of the M4 bits **on a per bit base** (see **Chapter 2.4.4.1**).

x00 = **On Change**

x01 = **TLL coverage** of M4 bit data

x10 = **CRC coverage** of M4 bit data

x11 = **CRC and TLL coverage** of M4 bit data

0xx = M4 bits **towards state machine** are **covered by TLL.**

1xx = M4 bits **towards state machine** are checked by the same validation algorithm as programmed for the reporting to the system interface (see **Chapter 2.4.4.2**).

EOC FILTER 3-bit field which controls the processing of EOC messages and its verification algorithm (see **Chapter 2.4.3.3**).

100 = EOC **automatic mode**

001 = EOC **transparent mode without any filtering**

010 = EOC **transparent mode with ‘on change’ filtering**

011 = EOC **transparent mode with Triple-Last-Look (TLL) Filtering**

4.11.3 EOCR - EOC Read Register

The **EOC R**ead register contains the last verified EOC message (M1-M3 bits) according to the verification criterion selected in MFILT.EOC FILTER.

EOCR **read** Address: 63_H

Reset Value: $0FFF_H$

15	14	13	12	11	10	9	8

0	0	0	0	a1	a2	a3	d/m
7	6	5	4	3	2	1	0
i1	i2	i3	i4	i5	i6	i7	i8

EOC Embedded Operations Channel (see **Chapter 2.4.3**)

a1 .. a3 address field

d/m data/ message indicator

i1 .. i8 information field,

4.11.4 EOCW - EOC Write Register

Via the **EOC W**rite register, the EOC message (M1-M3 bits) of the next available U superframe can be sent and it will be repeated until a new value is written to EOCW, or the line is deactivated.

Access to the EOCW register is reasonably only if the EOC channel is operated in ‘Transparent mode’, otherwise conflicts with the internal EOC processor may occur.

EOCW **write** Address: 65_H

Reset Value: 0100_H

15	14	13	12	11	10	9	8
0	0	0	0	a1	a2	a3	d/m
7	6	5	4	3	2	1	0
i1	i2	i3	i4	i5	i6	i7	i8

a1 .. a3 address field

d/m data/ message indicator

i1 .. i8 information field (8 codes are reserved by ANSI/ETSI for diagnostic and loopback functions)

4.11.5 M4RMASK - M4 Read Mask Register

Via the **M4 Read Mask** register, the user can selectively control which M4 bit changes are reported via interrupt requests.

M4RMASK read*)/**write** Address: 67_H

Reset Value: 00_H

7	6	5	4	3	2	1	0
M4 Read Mask Bits							

Bit 0..7

0 = M4 bit change indication by interrupt active

1 = M4 bit change indication by interrupt masked

4.11.6 M4WMASK - M4 Write Mask Register

Access to the **M4 Write Mask** register (M4W) is controlled by the **M4WMASK** register. By means of the M4WMASK register the user can control on a per bit base which M4 bits are controlled by the user and which are controlled by the state machine.

M4WMASK read*)/**write** Address: 68_H

Reset Value: $A8_H$

7	6	5	4	3	2	1	0
M4 Write Mask Bits							

Bit 0..7

0 = M4 bit is controlled by state machine/ external pins (PS1,2)

1 = M4 bit is controlled by µC

Bit 6 **Partial Activation Control External/Automatic**,
function corresponds to the MON-8 commands PACE and PACA

0 = SAI bit is controlled and UOA bit is evaluated by state machine

1 = SAI bit is controlled via the µC, UOA=1 is reported to the state machine

4.11.7 M4R - M4 Read

The **R**ead **M4** bit register contains the last received and verified M4 bit data.

M4R **read** Address: 69_H

Reset Value: BE_H

7	6	5	4	3	2	1	0
AIB	UOA	M46	M45	M44	SCO	DEA	ACT

AIB Interruption (according to ANSI)

0 = indicates interruption

1 = inactive

UOA U Activation Only

0 = indicates that only U is activated

1 = inactive

SCO Start-on-Command Only Bit
indicates whether the DLC network will deactivate the loop between calls (defined in Bellcore TR-NWT000397)

0 = Start-on-Command-Only mode active,
in LULT mode the U-transceiver shall initiate the start-up procedure only upon command from the network (‘AR’ primitive)

1 = normal mode,
if the U-transceiver is operated within a DCL configuration as LULT it shall start operation as soon as power is applied

DEA Deactivation Bit

0 = LT informs NT that it will turn off

1 = inactive

ACT Activation Bit

0 = layer 2 not established

1 = signals layer 2 ready for communication

4.11.8 M4W - M4 Write Register

Via the **M4** bit **W**rite register the M4 bits of the next available U-superframe and subsequent ones can be controlled. The value is latched and transmitted until a new value is set.

M4W **write** Address: $6A_H$

Reset Value: BE_H

7	6	5	4	3	2	1	0
NIB	SAI	M46	CSO	NTM	PS2	PS1	ACT

NIB Network Indication Bit

0 = no function (reserved for network use)

1 = no function (reserved for network use)

SAI S Activity Indicator

0 = S-interface is deactivated

1 = S-interface is activated

CSO Cold Start Only

0 = NT is capable to perform warm starts

1 = NT activation with cold start only

NTM NT Test Mode

0 = NT busy in test mode

1 = inactive

PS2 Power Status Secondary Source

0 = secondary power supply failed

1 = secondary power supply ok

PS1 Power Status Primary Source

0 = primary power supply failed

1 = primary power supply ok

ACT Activation Bit

0 = layer 2 not established

1 = signals layer 2 ready for communication

4.11.9 M56R - M56 Read Register

Bits 1 to 3 of the **M5, M6** bit **R**ead register contain the last verified M5, M6 bit information. Bits 5 and 6 reflect the current MLT state (MS2,1). The FEBE/NEBE error indication bits are accommodated at bit positions 0 and 4. They signal that a FEBE and/or NEBE error have/has occurred.

M56R **read** Address: $6B_H$

Reset Value: $1F_H$

7	6	5	4	3	2	1	0
0	MS2	MS1	NEBE	M61	M52	M51	FEBE

MS1,2 MLT Status

00 = Normal Mode

01 = Insertion Loss

10 = Quiet Mode

11 = Reserved

NEBE Near-End Block Error

0 = Near-End Block Error has occurred

1 = no Near-End Block Error has occurred

M61, M52, M51 Received Spare Bits of last U superframe (M51, M52 and M61 have no effect on the Q-SMINT®IX).

FEBE Far-End Block Error

0 = Far-End Block Error has occurred

1 = no Far-End Block Error has occurred

4.11.10 M56W - M56 Write Register

Via the **M56** bit **W**rite register, the M5 and M6 bits of the next available superframe can be set. The value is latched and transmitted as long as a new value is set or the function is disabled. The FEBE bit can only be set and controlled externally if OPMODE.FEBE is set to ‘1’.

M56W **write** Address: $6C_H$

Reset Value: FF_H

7	6	5	4	3	2	1	0
1	1	1	1	M61	M52	M51	FEBE

M61, M52, M51 Transmitted Spare Bits to next U superframe (M51, M52 and M61 have no effect on the Q-SMINT®IX.

FEBE Far-End Block Error

0 = Far-End Block Error has occurred

1 = no Far-End Block Error has occurred

4.11.11 UCIR - C/I Code Read Register

Via the **U**-transceiver **C/I** code **R**ead register a microcontroller can access the C/I code that is output from the state machine.

UCIR **read** Address: $6D_H$

Reset Value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	C/I code output			

4.11.12 UCIW - C/I Code Write Register

The **U**-transceiver **C/I** code **W**rite register allows a microcontroller to control the state of the U-transceiver. To enable this function bit UCI in register OPMODE must be set to ‘1’ before.

UCIW **write** Address: $6E_H$

Reset Value: 01_H

7	6	5	4	3	2	1	0
0	0	0	0	C/I code input			

4.11.13 TEST - Test Register

The **Test** register sets the U-transceiver in the desired test mode.

TEST read*)/**write** Address: $6F_H$

Reset Value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	CCRC	+-1 tones	0	40kHz

CCRC Send Corrupt CRC

0 = inactive

1 = send corrupt (inverted) CRCs

+-1 tones Send +/-1 Pulses Instead of +/-3

0 = issues +/-3 pulses during 40 kHz tone generation or in SSP mode

1 = issues +/-1 pulses

40kHz 40 kHz Test Signal

0 = issues single pulses in state ’Test’

1 = issues a 40 kHz test signal in state ’Test’

4.11.14 LOOP - Loop Back Register

The **Loop** register controls the digital loopbacks of the U-transceiver. The analog loopback (No. 3) is closed by C/I= ‘ARL’.

Note: If the EOC automatic mode is selected (MFILT.EOC Filter = ’100’), then register LOOP is accessed by the internal EOC processor:
EOC-command ’LB1’ (’LB2’) sets LOOP.U/IOM and LOOP.LB1 (LOOP.LB2)
EOC-command ’RTN’ resets LOOP.LB1, LOOP.LB2 and LOOP.LBBD

LOOP read*)/**write** Address: 70_H

Reset Value: 08_H

7	6	5	4	3	2	1	0
0	DLB	TRANS	U/IOM	1	LBBD	LB2	LB1

DLB Close Framer/Deframer Loopback
– the loopback is closed at the analog/digital interface
– prerequisite is that LB1, LB2, LBBD and U/IOM® are set to ‘0’
– only user data is looped and no maintenance data is looped back[1)]

0 = Framer/Deframer loopback open

1 = Framer/Deframer loopback closed

TRANS Transparent/ Non-Transparent Loopback
– in transparent mode user data is both passed on and looped back, whereas in non-transparent mode data is not forwarded but substituted by ’1’s (idle code) and just looped back[2)]
– if LBBD, LB2, LB1 is closed towards the IOM® interface and bit TRANS is set to ’0’ then the state machine has to be put into state ’Transparent’ first (e.g. by C/I = DT) before data is output on the U-interface
– bit TRANS has no effect on DLB and the analog loopback (ARL operates always in transparent mode)

0 = sets transparent loop mode for LBBD, LB2, LB1

1 = sets non-transparent mode for LBBD, LB2, LB1
’1’s are sent on the IOM®-2/PCM interface in the corresponding time-slot

U/IOM Close LBBD, LB2, LB1 Towards U or Towards IOM®
- Switch that selects whether loopback LB1, LB2 or LBBD is closed towards U or towards IOM®-2
- the setting affects all test loops, LBBD, LB2 and LB1
- an individual selection for LBBD, LB2, LB1 is not possible

0 = LB1, LB2, LBBD loops are closed from IOM®-2 to IOM®-2

1 = LB1, LB2, LBBD loops are closed from U to U

LBBD Close Complete Loop (B1, B2, D) Near the System Interface
the direction towards the loop is closed is determined by bit 'U/IOM'

0 = complete loopback open

1 = complete loopback closed

LB2 Close Loop B2 Near the System Interface
the direction towards the loop is closed is determined by bit 'U/IOM'

0 = loopback B2 open

1 = loopback B2 closed

LB1 Close Loop B1 Near the System Interface
the direction towards the loop is closed is determined by bit 'U/IOM'

0 = loopback B1 open

1 = loopback B1 closed

1) If in state Transparent the DLB-loopback is closed from IOM- to IOM, then C/I-code 'DC' instead of 'AI' is issued on the IOM®-2-interface.

2) If in state Transparent the non-transparent LBBD-loopback is closed from U- to U, then C/I-code 'DC' instead of 'AI' is issued on the IOM®-2-interface. However, the correct C/I-code 'AI' can be read from register UCIR.

4.11.15 FEBE - Far End Block Error Counter Register

The **F**ar **E**nd **B**lock **E**rror Counter Register contains the FEBE value. If the register is read out it is automatically reset to '0'.

FEBE **read** Address: 71_H

Reset Value: 00_H

7	6	5	4	3	2	1	0

FEBE Counter Value

4.11.16 NEBE - Near End Block Error Counter Register

The **N**ear **E**nd **B**lock **E**rror Counter Register contains the NEBE value. If the register is read out it is automatically reset to ‘0’.

NEBE **read** Address: 72_H

Reset Value: 00_H

7	6	5	4	3	2	1	0
NEBE Counter Value							

4.11.17 ISTAU - Interrupt Status Register U-Interface

The **I**nterrupt **Sta**tus register **U**-interface generates an interrupt for the unmasked interrupt flags. Refer to **Chapter 2.4.12** for details on masking and clearing of interrupt flags. For the timing of the interrupt flags ISTAU(3:0) refer to **Chapter 2.4.2.4**.

ISTAU **read** Address: $7A_H$

Reset Value: 00_H

7	6	5	4	3	2	1	0
MLT	CI	FEBE/ NEBE	M56	M4	EOC	6ms	12ms

MLT MLT interrupt indication

0 = inactive

1 = MLT interrupt has occurred

CI C/I code indication
the CI interrupt is generated independently on OPMODE.UCI

0 = inactive

1 = CI code change has occurred

FEBE/ NEBE Far End/Near End Block Error indication
register M56R notifies whether a FEBE or NEBE has been detected

0 = inactive

1 = FEBE/NEBE occurred

M56 Validated new M56 bit data received from U-interface

0 = inactive

1 = change of any M5, M6 bit has been detected in receive direction

M4 Validated new M4 bit data received from U-interface

0 = inactive

1 = change of any M4 bit has been detected in receive direction

EOC Validated new EOC data received from U-interface

0 = inactive

1 = new EOC message has been received and acknowledged from U

6 ms 6 ms timer for the transmission of EOC commands on U

0 = inactive

1 = indicates when a EOC command is going to be issued on U

12 ms Superframe marker (each 12 ms) is going to be issued on U in transmit direction
Bellcore test requirement: SR-NWT-002397

0 = inactive

1 = indicates when a SF marker is going to be transmitted on U

4.11.18 MASKU - Mask Register U-Interface

The Interrupt **Mask** register **U**-Interface selectively masks each interrupt source in the ISTAU register by setting the corresponding bit to ‘1’.

MASKU read*)/**write** Address: $7B_H$

Reset Value: FF_H

7	6	5	4	3	2	1	0

MASKU Value

Bit 0..7 Mask bits

0 = interrupt active

1 = interrupt masked

4.11.19 FW_VERSION

FW_VERSION Register contains the Firmware Version number

FW_VERSION **read** Address: $7D_H$

Reset value: $6x_H$

7	6	5	4	3	2	1	0
Firmware Version Number							

Version 1.2 : $6D_H$

Version 1.3 : $6C_H$

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-40 to 85	°C
Storage temperature	T_{STG}	– 65 to 150	°C
Maximum Voltage on V_{DD}	V_{DD}	4.2	V
Maximum Voltage on any pin with respect to ground	V_S	-0.3 to V_{DD} + 3.3 (max. < 5.5)	V

ESD integrity (according EIA/JESD22-A114B (HBM)): 2 kV

Note: Stress above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Line Overload Protection

The Q-SMINT®IX is compliant to ESD tests according to ANSI / EOS / ESD-S 5.1-1993 (CDM), EIA/JESD22-A114B (HBM) and to Latch-up tests according to JEDEC EIA / JESD78. From these tests the following max. input currents are derived (**Table 41**):

Table 41 Maximum Input Currents

Test	Pulse Width	Current	Remarks
ESD	100 ns	1.3 A	3 repetitions
Latch-up	5 ms	+/-200 mA	2 repetitions, respectively
DC	--	10 mA	

5.2 DC Characteristics

V_{DD}/V_{DDA} = 3.3 V +/- 5% ; V_{SS}/V_{SSA} = 0 V; T_A = -40 to 85 °C

Digital Pins	Parameter	Symbol	Limit Values		Unit	Test Condition
			min.	max.		
All	Input low voltage	V_{IL}	-0.3	0.8	V	
	Input high voltage	V_{IH}	2.0	5.25	V	
All except DD/DU $\overline{ACT}$,$\overline{LP2}$I MCLK	Output low voltage	V_{OL1}		0.45	V	I_{OL1} = 3.0 mA
	Output high voltage	V_{OH1}	2.4		V	I_{OH1} = 3.0 mA
DD/DU $\overline{ACT}$,$\overline{LP2}$I MCLK	Output low voltage	V_{OL2}		0.45	V	I_{OL2} = 4.0 mA
	Output high voltage (DD/DU push-pull)	V_{OH2}	2.4		V	I_{OH2} = 4.0 mA
All	Input leakage current	I_{LI}		10	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Output leakage current	I_{LO}		10	µA	0 V ≤ V_{IN} ≤ V_{DD}
Analog Pins						
AIN, BIN	Input leakage current	I_{LI}		70	µA	0 V ≤ V_{IN} ≤ V_{DD}

Table 42 S-Transceiver Characteristics

Pin	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
SX1,2	Absolute value of output pulse amplitude (V_{SX2} - V_{SX1})	V_X	2.03	2.2	2.31	V	R_L = 50 Ω
SX1,2	S-Transmitter output impedance	Z_X	10	34		kΩ	see [1]
			0				see [2][3]
SR1,2	S-Receiver input impedance	Z_R	10 100			kΩ Ω	V_{DD} = 3.3 V V_{DD} = 0 V

[1] Requirement ITU-T I.430, chapter 8.5.1.1a): 'At all times except when transmitting a binary zero, the output impedance , in the frequency range of 2kHz to 1 MHz, shall exceed the impedance indicated by the template in Figure 11. The requirement is applicable with an applied sinusoidal voltage of 100 mV (r.m.s value)'

2) Requirement ITU-T I.430, chapter 8.5.1.1b): 'When transmitting a binary zero, the output impedance shall be > 20 Ω.': Must be met by external circuitry.

3) Requirement ITU-T I.430, chapter 8.5.1.1b), Note: 'The output impedance limit shall apply for a nominal load impedance (resistive) of 50 Ω. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value +/- 10%. The peak amplitude shall be defined as the the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.'

Table 43 U-Transceiver Characteristics

	Limit Values			Unit
	min.	typ.	max.	
Receive Path				
Signal / (noise + total harmonic distortion)[1]	65[2]			dB
DC-level at AD-output	45	50	55	%[3]
Threshold of level detect (measured between AIN and BIN with respect to zero signal)	4	5	16 (PEF 81912)	mV peak
			9 (PEF 81913)	
Input impedance AIN/BIN	80			kΩ
Transmit Path				
Signal / (noise + total harmonic distortion)[4]	70			dB
Common mode DC-level	1.61	1.65	1.69	V
Offset between AOUT and BOUT			35	mV
Absolute peak voltage for a single +3 or -3 pulse measured between AOUT and BOUT[5]	2.42	2.5	2.58	V
Output impedance AOUT/BOUT: Power-up Power-down		 0.8 3	 1.5 6	 Ω Ω

1) Test conditions: 1.4 Vpp differential sine wave as input on AIN/BIN with long range (low, critical range).

2) Versions PEF 8x913 with enhanced performance of the U-interface are tested with tightened limit values

3) The percentage of the "1 "-values in the PDM-signal.

4) Interpretation and test conditions: The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 70 dB below the signal for an evenly distributed but otherwise random sequence of +3, +1, -1, -3.

5) The signal amplitude measured over a period of 1 min. varies less than 1%.

5.3 Capacitances

T_A = 25 °C, 3.3 V ± 5 % V_{SSA} = 0 V, V_{SSD} = 0 V, f_c = 1 MHz, unmeasured pins grounded.

Table 44 Pin Capacitances

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Digital pads: Input Capacitance I/O Capacitance	 C_{IN} $C_{I/O}$		 7 7	 pF pF	
Analog pads: Load Capacitance	 C_L		 3	 pF	 pin AIN, BIN

5.4 Power Consumption

Power Consumption

VDD=3.3 V, VSS=0 V, Inputs at VSS/VDD, no LED connected, 50% bin. zeros, no output loads except SX1,2 (50 Ω[1])

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
Operational U and S enabled, IOM®-2 off		 235 200		 mW mW	 U: ETSI loop 1 (0 m) U: ETSI Loop 2.(typical line)
Power Down		15		mW	

1) 50 Ω (2 x TR) on the S-bus.

5.5 Supply Voltages

VDD_D = + Vdd ± 5%
VDD_A = + Vdd ± 5%

The maximum sinusoidal ripple on VDD is specified in the following figure:

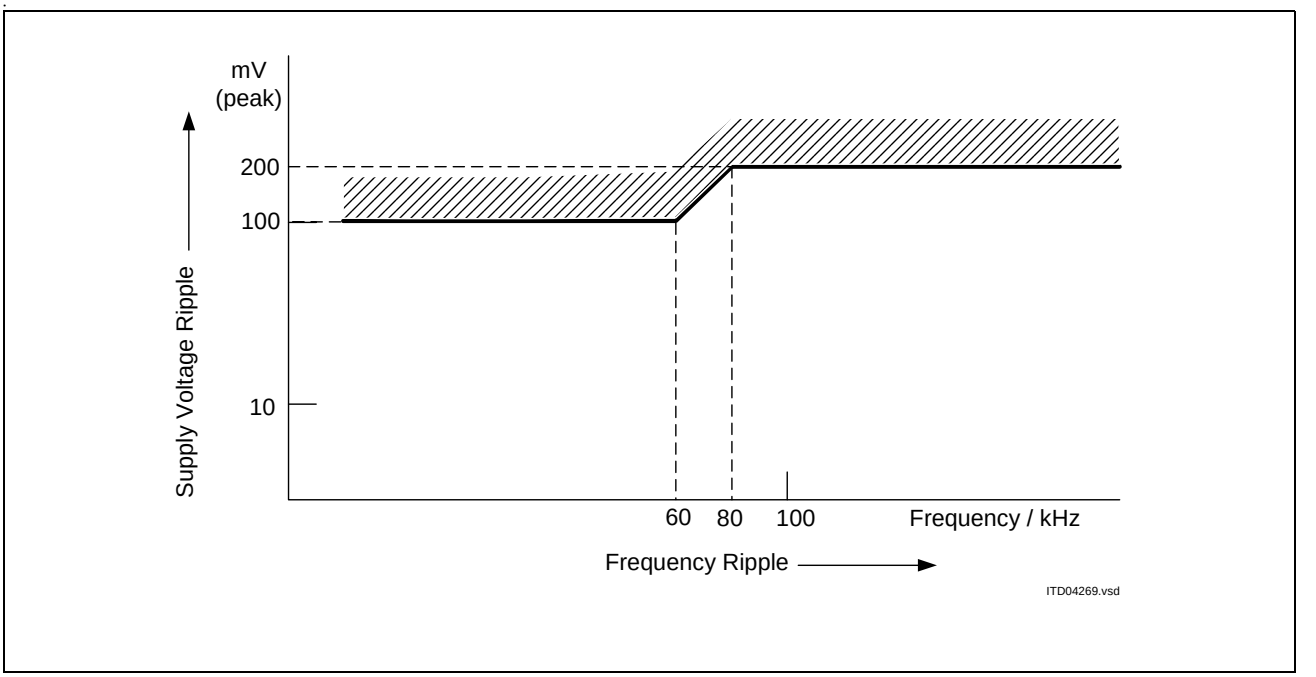


Figure 83 Maximum Sinusoidal Ripple on Supply Voltage

5.6 AC Characteristics

T_A = -40 to 85 °C, V_{DD} = 3.3 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **Figure 84.**

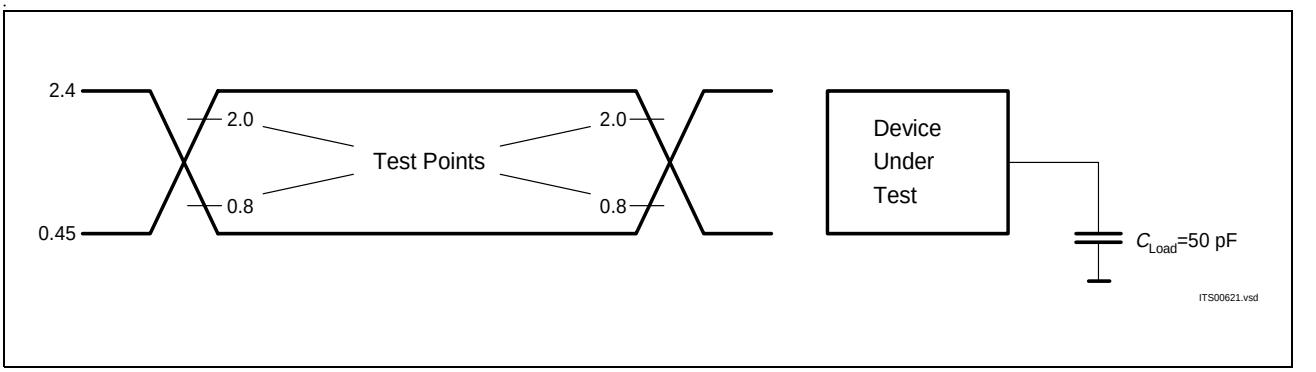


Figure 84 Input/Output Waveform for AC Tests

Parameter All Output Pins	Symbol	Limit values		Unit
		Min	Max	
Fall time			30	ns
Rise time			30	ns

5.6.1 IOM®-2 Interface

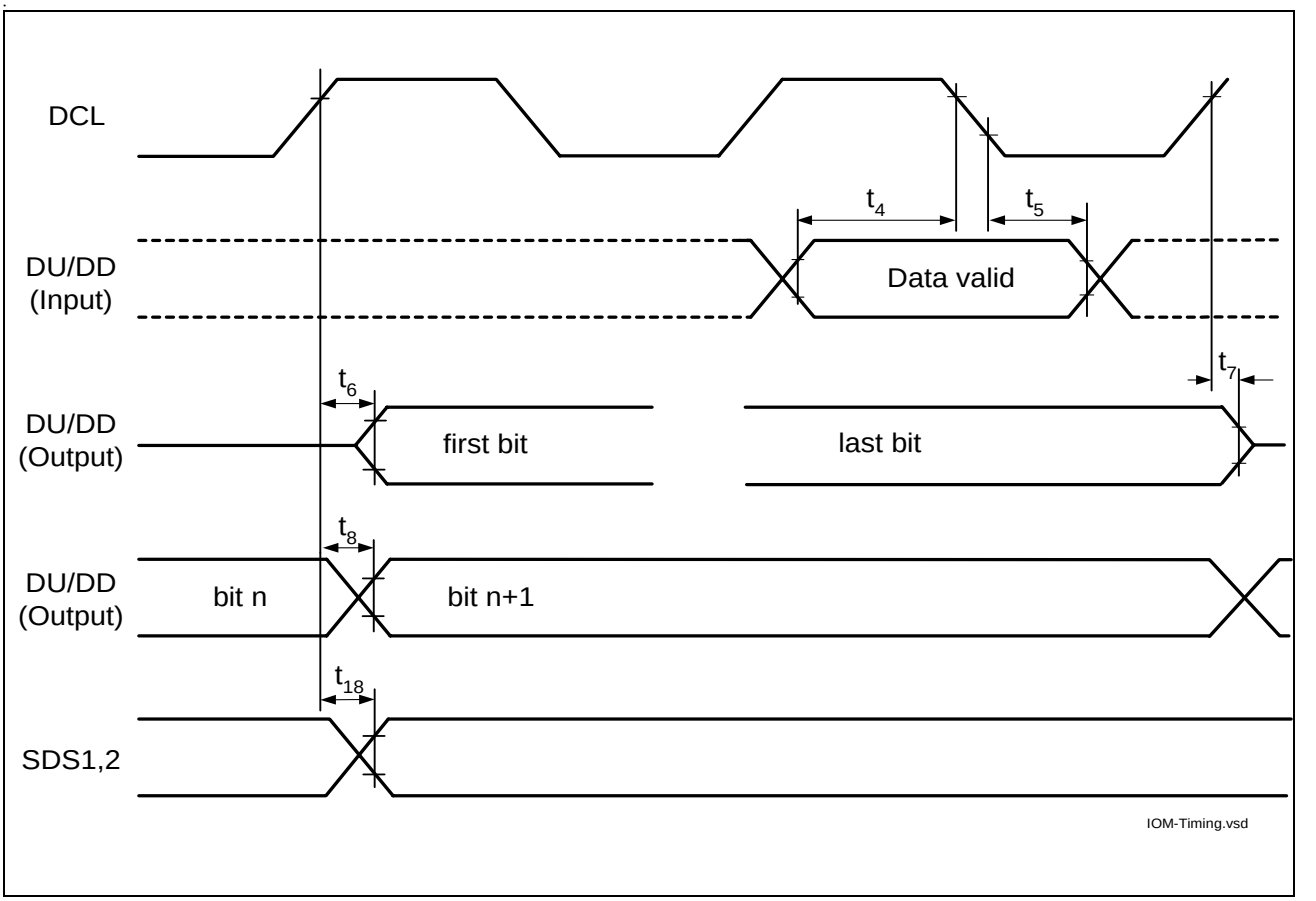


Figure 85 IOM®-2 Interface - Bit Synchronization Timing

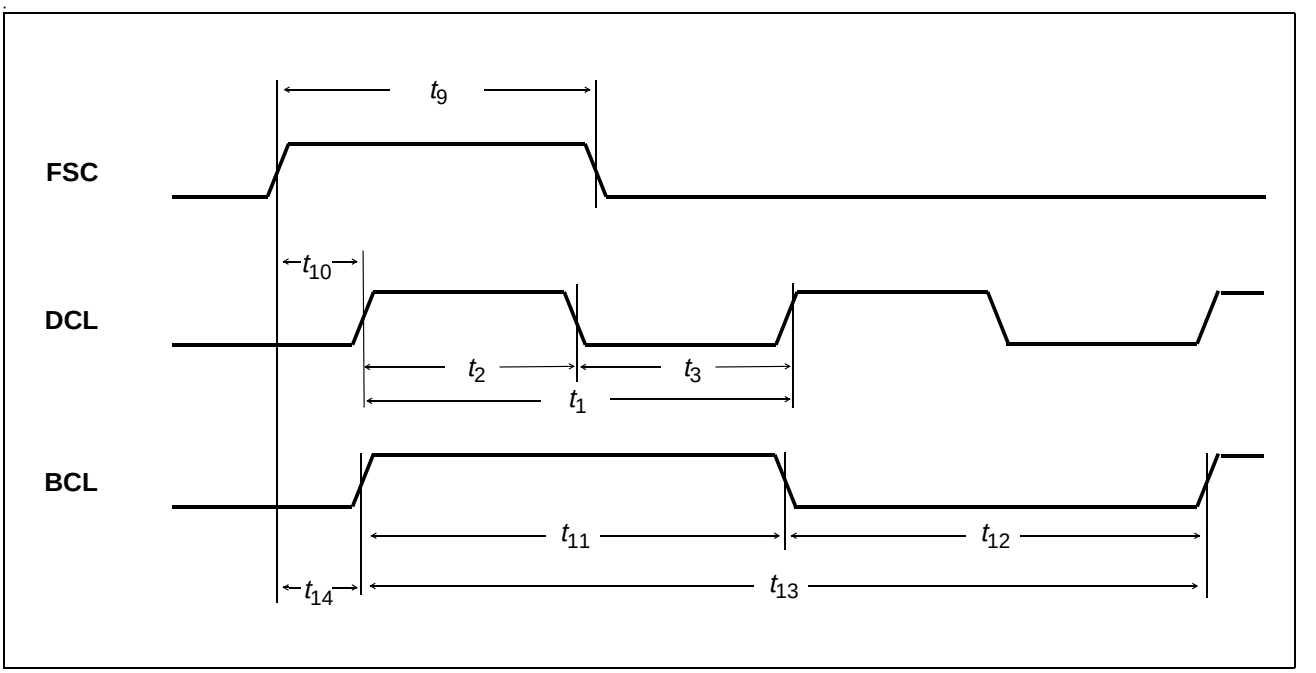


Figure 86 IOM®-2 Interface - Frame Synchronization Timing

Parameter IOM®-2 Interface	Symbol	Limit values			Unit
		Min	Typ	Max	
DCL period	t_1	565	651	735	ns
DCL high	t_2	200	310	420	ns
DCL low	t_3	200	310	420	ns
Input data setup	t_4	20			ns
Input data hold	t_5	20			ns
Output data from high impedance to active (FSC high or other than first timeslot)	t_6			100	ns
Output data from active to high impedance	t_7			100	ns
Output data delay from clock	t_8			80	ns
FSC high	t_9		50% of FSC cycle time		ns
FSC advance to DCL	t_{10}	65	130	195	ns
BCL high	t_{11}	565	651	735	ns
BCL low	t_{12}	565	651	735	ns
BCL period	t_{13}	1130	1302	1470	ns
FSC advance to BCL	t_{14}	65	130	195	ns
DCL, FSC rise/fall	t_{15}			30	ns
Data out fall (C_L = 50 pF, R = 2 kΩ to V_{DD}, open drain)	t_{16}			200	ns
Data out rise/fall (C_L = 50 pF, tristate)	t_{17}			150	ns
Strobe Signal Delay	t_{18}			120	ns

Note: At the start and end of a reset period, a frame jump may occur. This results in a DCL, BCL and FSC high time of min. 130 ns after this specific event.

5.6.2 Serial µP Interface

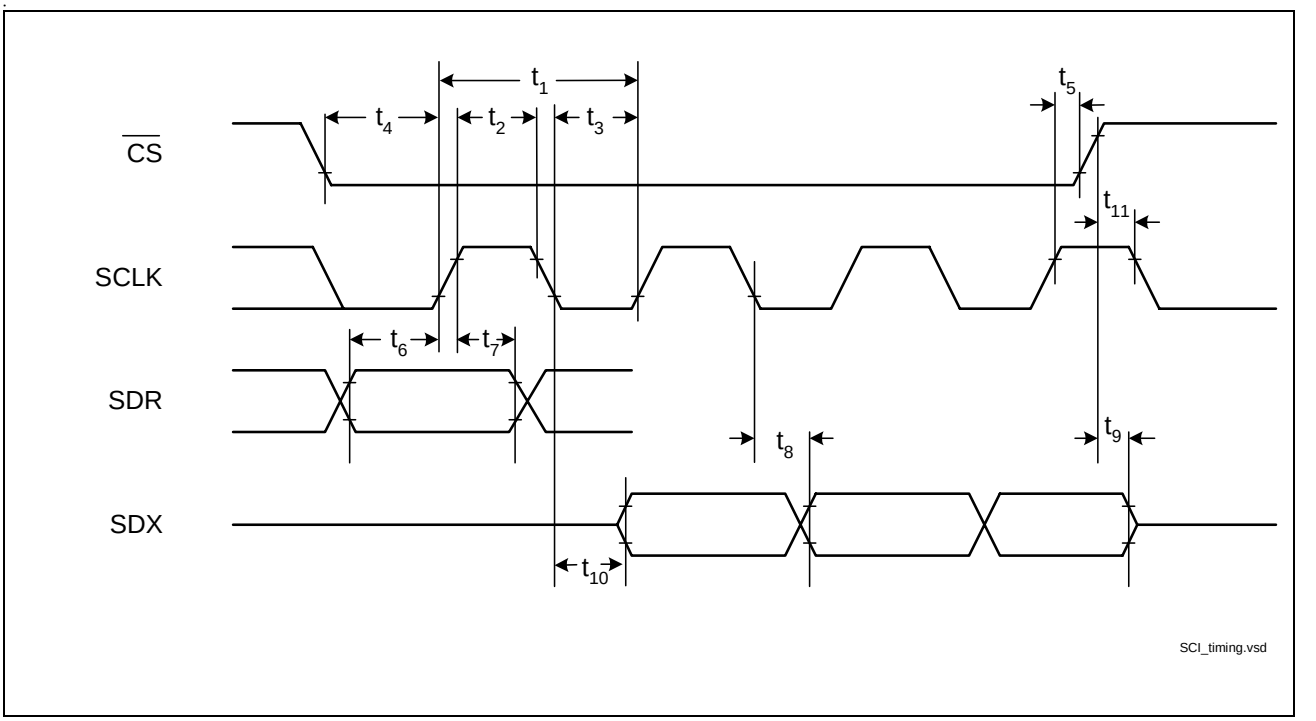


Figure 87 Serial Control Interface

Parameter SCI Interface	Symbol	Limit values		Unit
		Min	Max	
SCLK cycle time	t_1	200		ns
SCLK high time	t_2	80		ns
SCLK low time	t_3	80		ns
$\overline{CS}$ setup time	t_4	20		ns
$\overline{CS}$ hold time	t_5	10		ns
SDR setup time	t_6	15		ns
SDR hold time	t_7	15		ns
SDX data out delay	t_8		60	ns
$\overline{CS}$ high to SDX tristate	t_9		40	ns
SCLK to SDX active	t_{10}		60	ns
$\overline{CS}$ high to SCLK	t_{11}	10		ns

5.6.3 Parallel µP Interface

Siemens/Intel Bus Mode

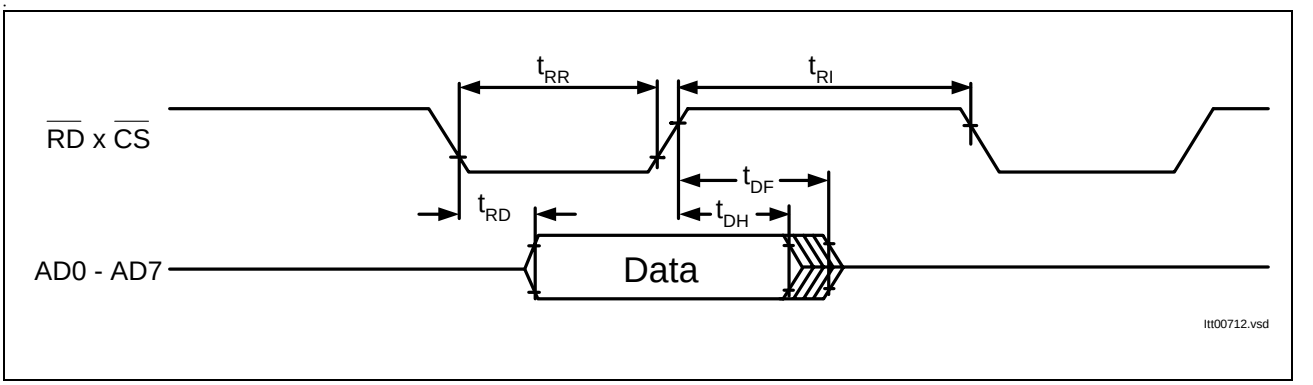


Figure 88 Microprocessor Read Cycle

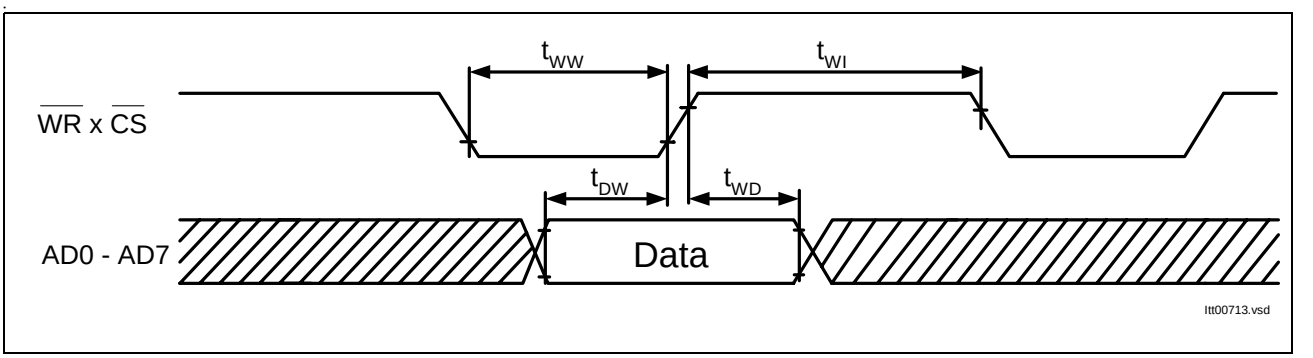


Figure 89 Microprocessor Write Cycle

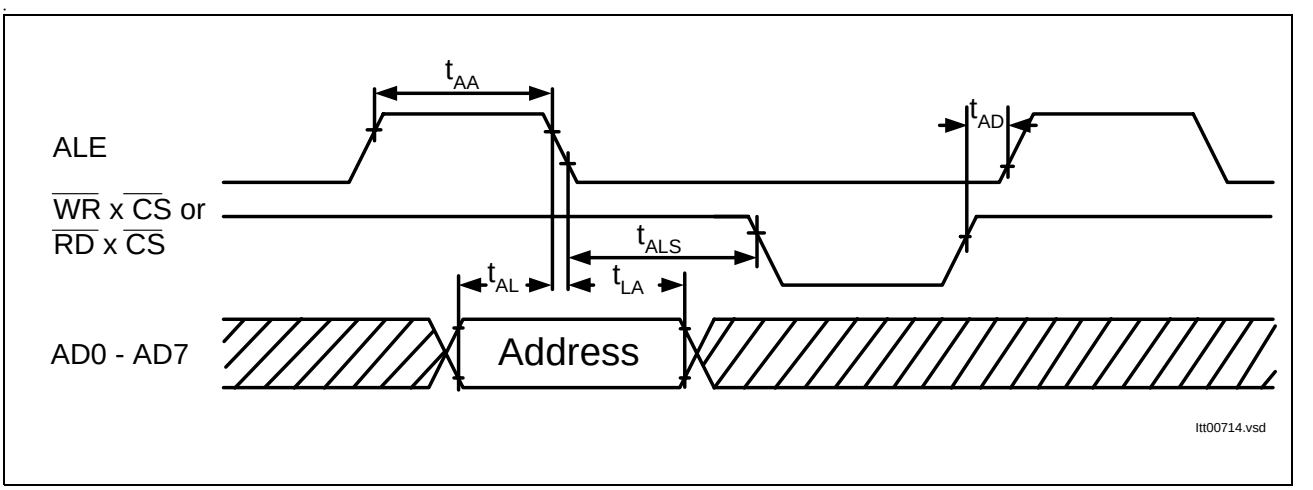


Figure 90 Multiplexed Address Timing

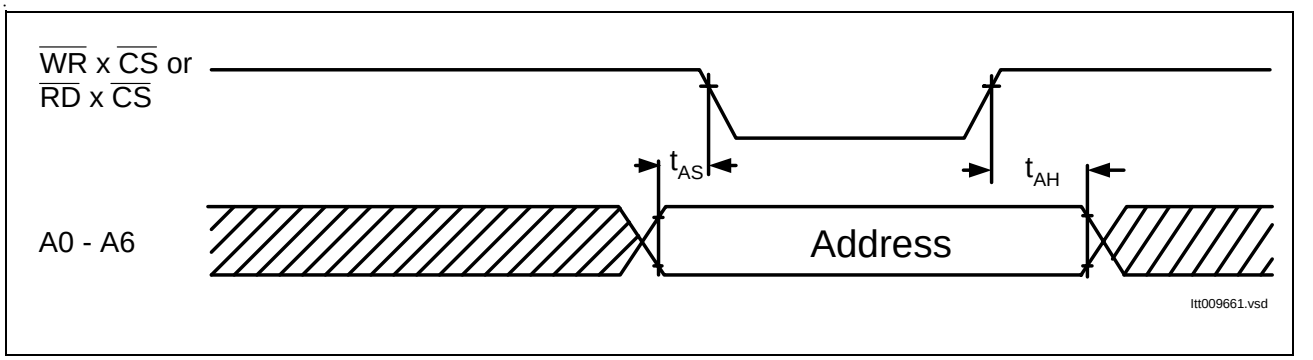


Figure 91 Non-Multiplexed Address Timing

Motorola Bus Mode

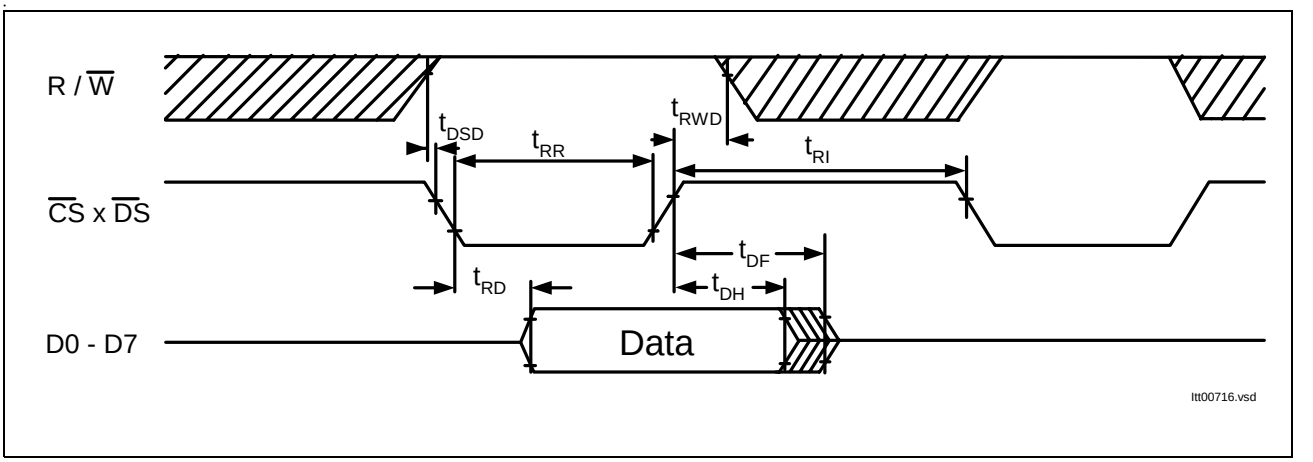


Figure 92 Microprocessor Read Timing

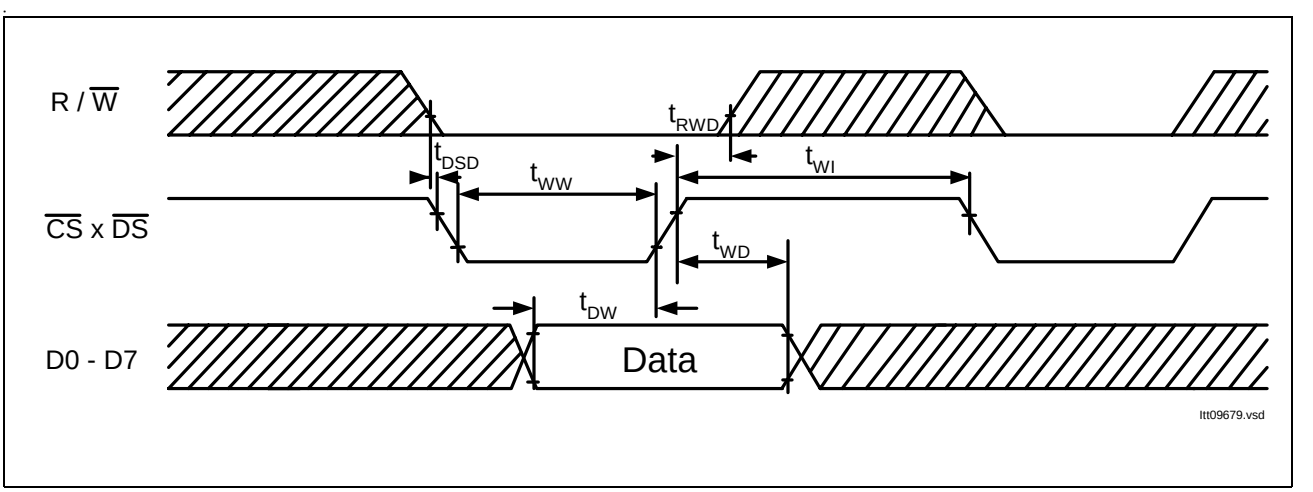


Figure 93 Microprocessor Write Cycle

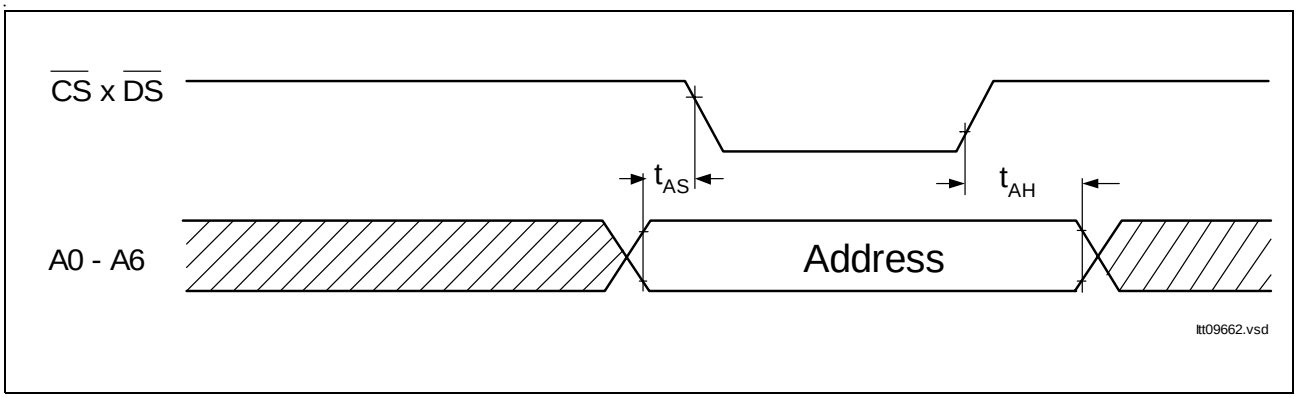


Figure 94 Non-Multiplexed Address Timing

Microprocessor Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	20		ns
Address setup time to ALE	t_{AL}	10		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	10		ns
Address setup time	t_{AS}	10		ns
Address hold time	t_{AH}	10		ns
ALE guard time	t_{AD}	10		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	10		ns
$\overline{RD}$ pulse width	t_{RR}	80		ns
Data output delay from $\overline{RD}$	t_{RD}		80	ns
Data hold from $\overline{RD}$	t_{DH}	0		ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval[1)]	t_{RI}	70		ns
$\overline{W}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{W}$ x $\overline{CS}$	t_{DW}	10		ns
Data hold time $\overline{W}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{W}$ control interval	t_{WI}	70		ns
R/$\overline{W}$ hold from $\overline{CS}$ x $\overline{DS}$ inactive	t_{RWD}	10		ns

1) control interval: t_{RI}' is minimal 70ns for all registers except ISTAU, FEBE and NEBE. However, the time between two consecutive read accesses to one of the registers ISTAU, FEBE or NEBE, respectively, must be longer than 330ns. This does not limit t_{RI} of read sequences, which involve intermediate read access to other registers, as for instance: ISTAU -(t_{RI})- ISTA -(t_{RI})- ISTAH -(t_{RI})- ISTAU.

5.6.4 Reset

Table 45 Reset Input Signal Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Length of active low state	$t_{\overline{RST}}$	4			ms	Power On the 4 ms are assumed to be long enough for the oscillator to run correctly
		2 x DCL clock cycles + 400 ns				After Power On
Delay time for µC access after $\overline{RST}$ rising edge	$t_{\mu C}$	500			ns	

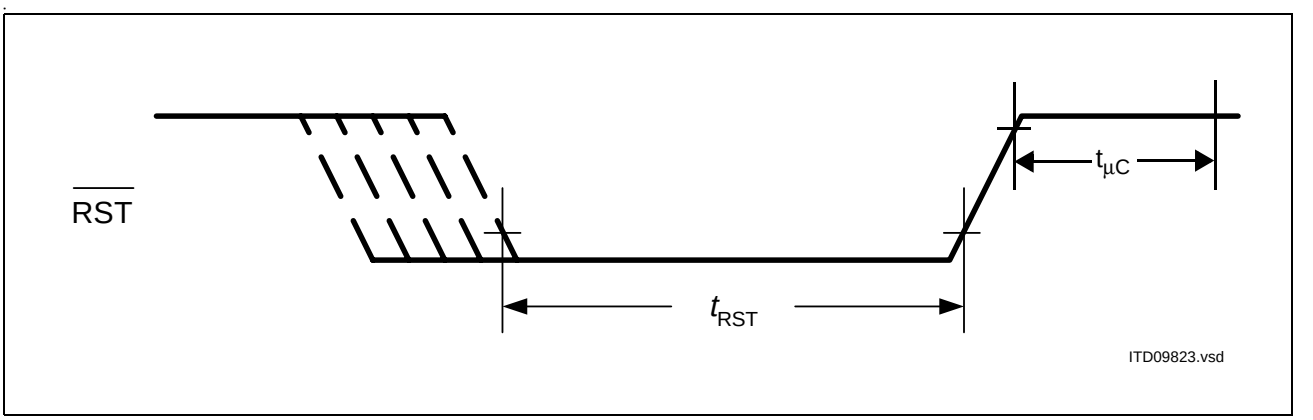


Figure 95 Reset Input Signal

5.6.5 Undervoltage Detection Characteristics

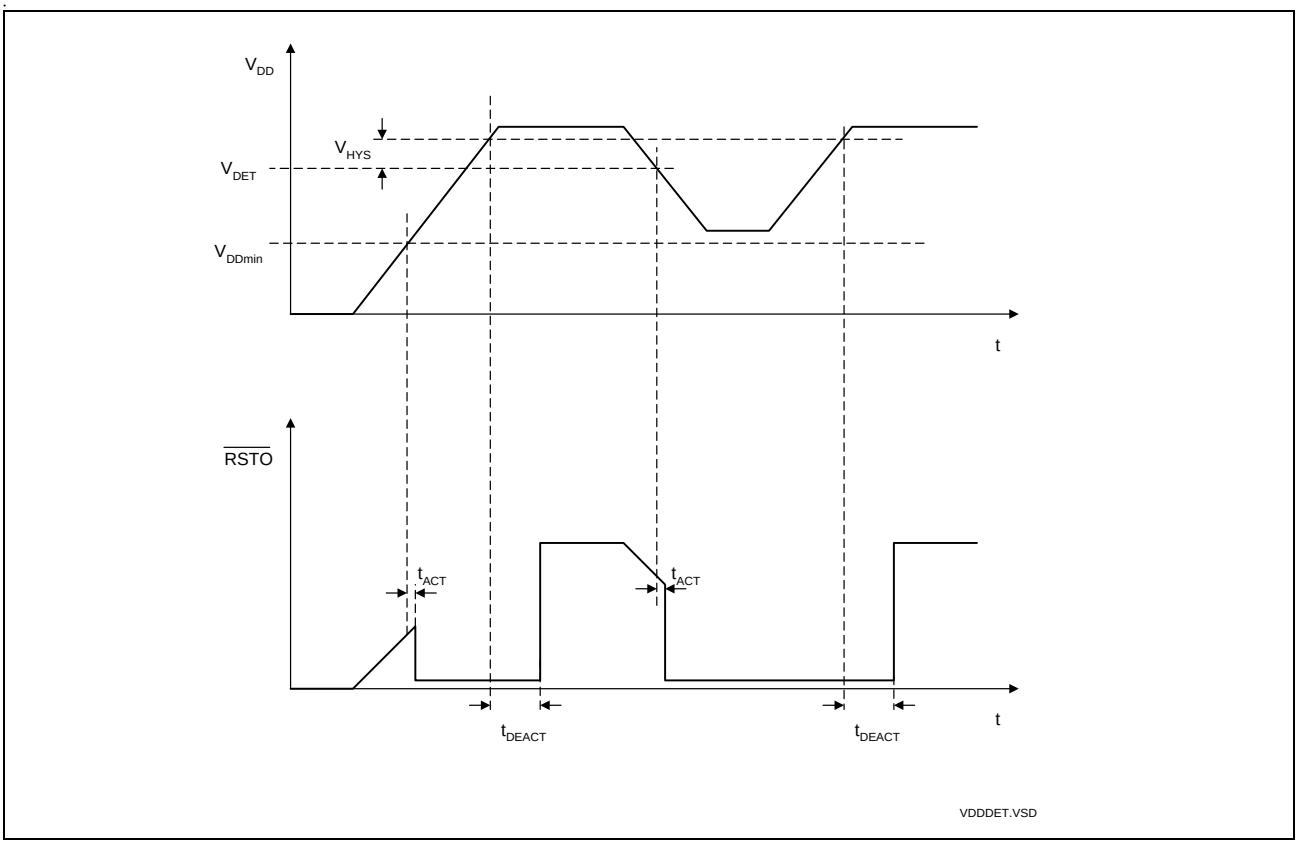


Figure 96 Undervoltage Control Timing

Table 46 Parameters of the UVD/POR Circuit

V_{DD}= 3.3 V ± 5 %; V_{SS}= 0 V; T_A = -40 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Detection Threshold[1]	V_{DET}	2.7	2.8	2.92	V	V_{DD} = 3.3 V ± 5 %
Hysteresis	V_{Hys}	30		90	mV	
Max. rising/falling V_{DD} edge for activation/ deactivation of UVD	dV_{DD}/dt			0.1	V/µs	
Max. rising V_{DD} for power-on[2]				0.1	V/ ms	
Min. operating voltage	V_{DDmin}	1.5			V	

V_{DD}= 3.3 V ± 5 %; V_{SS}= 0 V; T_A = -40 to 85 °C

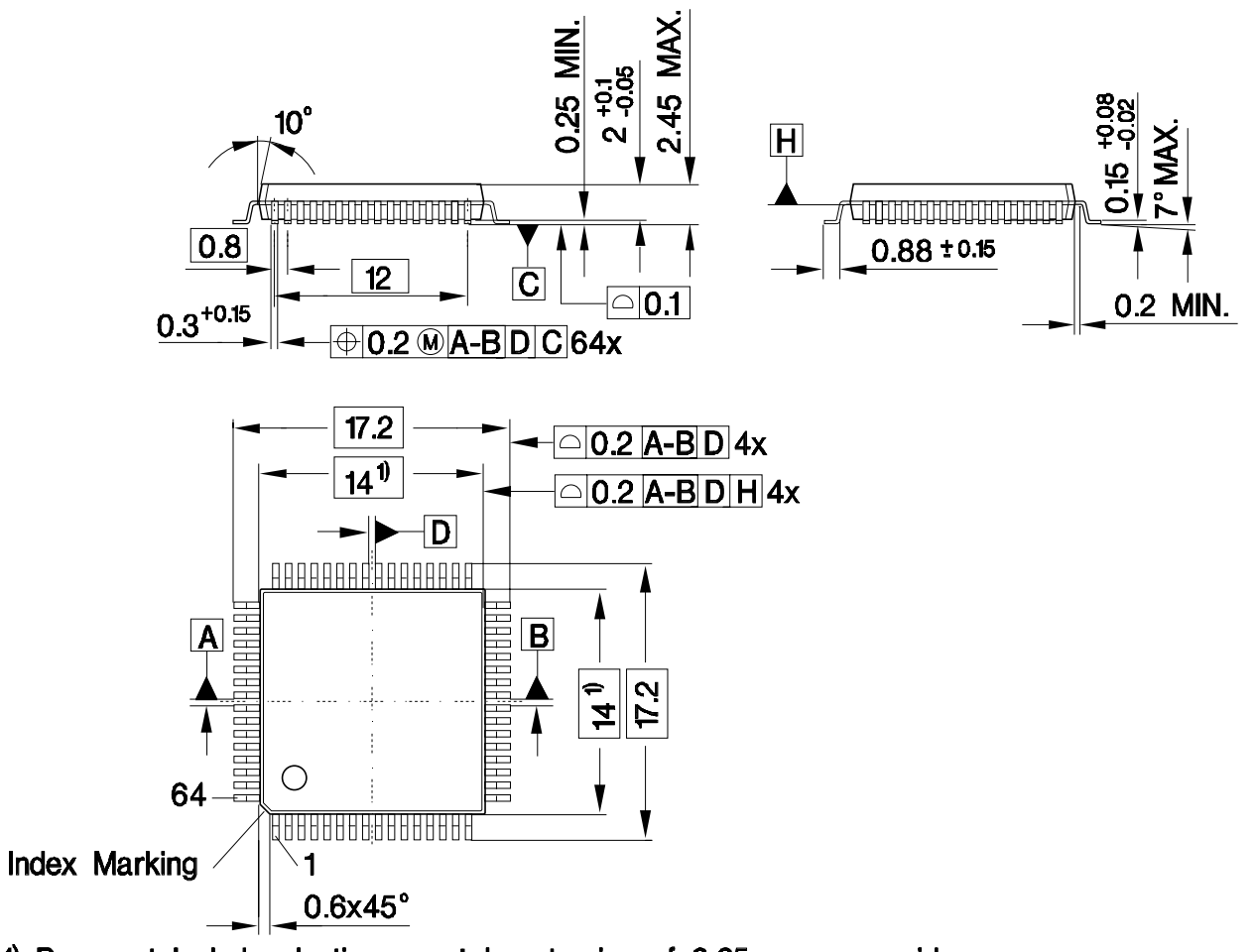
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Delay for activation of $\overline{\text{RSTO}}$	t_{ACT}			10	µs	
Delay for deactivation of $\overline{\text{RSTO}}$	t_{DEACT}		64		ms	

1) The Detection Threshold V_{DET} is far below the specified supply voltage range of analog and digital parts of the Q-SMINT®IX. Therefore, the board designer must take into account that a range of voltages is existing, where neither performance and functionality of the Q-SMINT®IX are guaranteed, nor a reset is generated.

2) If the integrated Power-On Reset of the Q-SMINTIX is selected ($\overline{\text{VDDDET}}$ = '0') and the supply voltage V_{DD} is ramped up from 0V to 3.3V +/- 5%, then the Q-SMINTIX is kept in reset during $V_{DDmin} < V_{DD} < V_{DET} + V_{Hys}$. V_{DD} must be ramped up so slowly that the Q-SMINTIX leaves the reset state after the oscillator circuit has already finished start-up. The start-up time of the oscillator circuit is typically in the range between 3ms and 12ms.

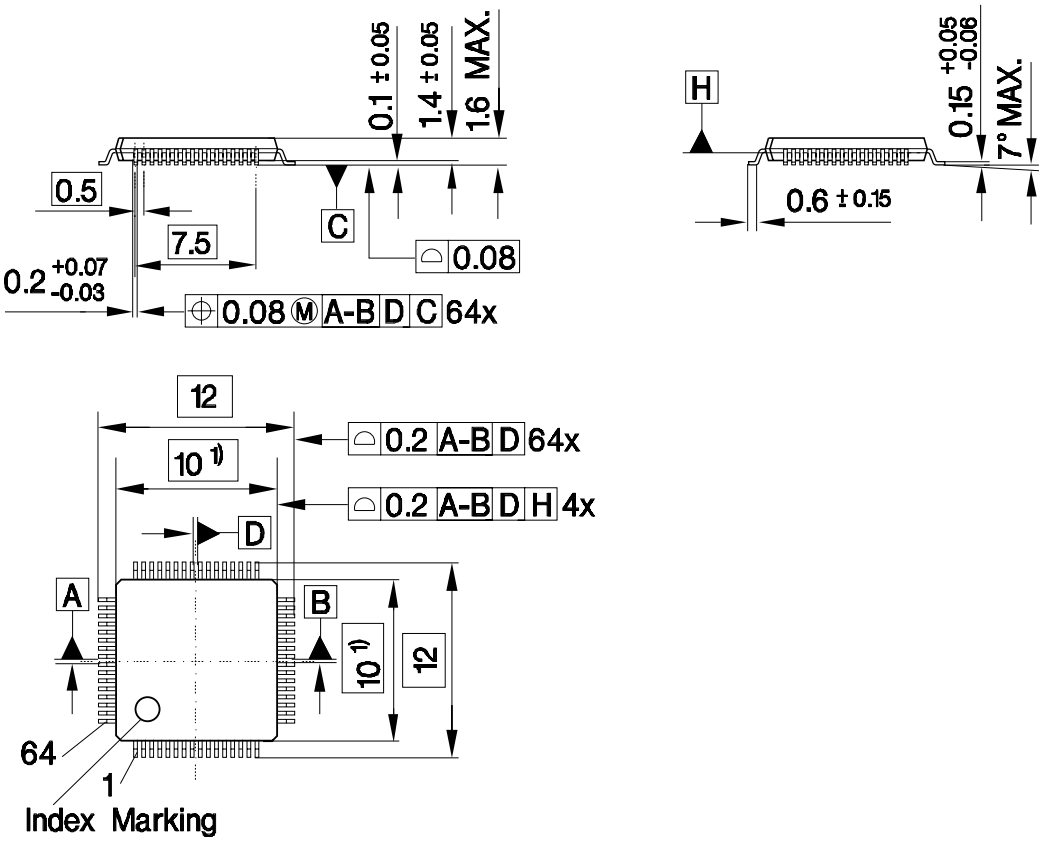
6 Package Outlines

Plastic Package, P-MQFP-64
(Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Plastic Package, P-TQFP-64
(Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

7 Appendix: Differences between Q- and T-SMINT®IX

The Q- and T-SMINT®IX have been designed to be as compatible as possible. However, some differences between them are unavoidable due to the different line codes 2B1Q and 4B3T used for data transmission on the U_{k0} line.

Especially the pin compatibility between Q- and T-SMINT®IX allows for one single PCB design for both series with only some mounting differences. The µC software can distinguish between the Q- and T-series by reading the identification register via the IOM®-2 (MONITOR channel identification command) or the µC interface (register ID.DESIGN), respectively.

The following chapter summarizes the main differences between the Q- and T-SMINT®IX.

7.1 Pinning

Table 47 Pin Definitions and Functions

	Pin T/MQFP-64	Q-SMINT®IX: 2B1Q	T-SMINT®IX: 4B3T
	16	Metallic Termination Input (MTI)	Tie to ‘1‘
	55	Power Status (primary) (PS1)	Tie to ‘1‘
	41	Power Status (secondary) (PS2)	Tie to ‘1‘

7.2 U-Transceiver

7.2.1 U-Interface Conformity

Table 48 Related Documents to the U-Interface

	Q-SMINT®IX: 2B1Q	T-SMINT®IX: 4B3T
ETSI: TS 102 080	conform to annex A compliant to 10 ms interruptions	conform to annex B
ANSI: T1.601-1998 (Revision of ANSI T1.601-1992)	conform MLT input and decode logic	not required
CNET: ST/LAA/ELR/DNP/822	conform	not required
RC7355E	conform	not required
FTZ-Richtlinie 1 TR 220	not required	conform

7.2.2 U-Transceiver State Machines

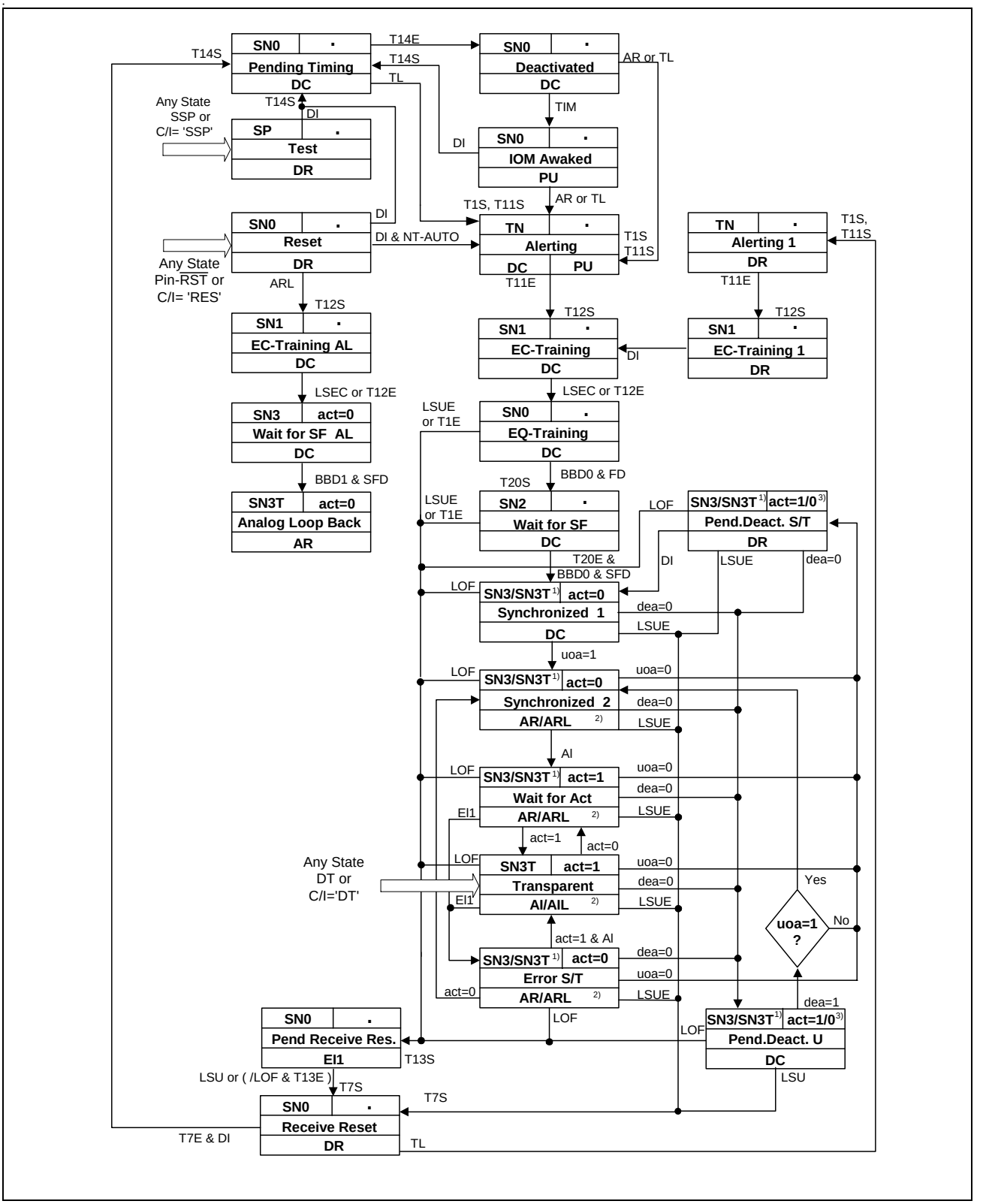


Figure 97 INTC-Q Compatible State Machine Q-SMINT®IX: 2B1Q

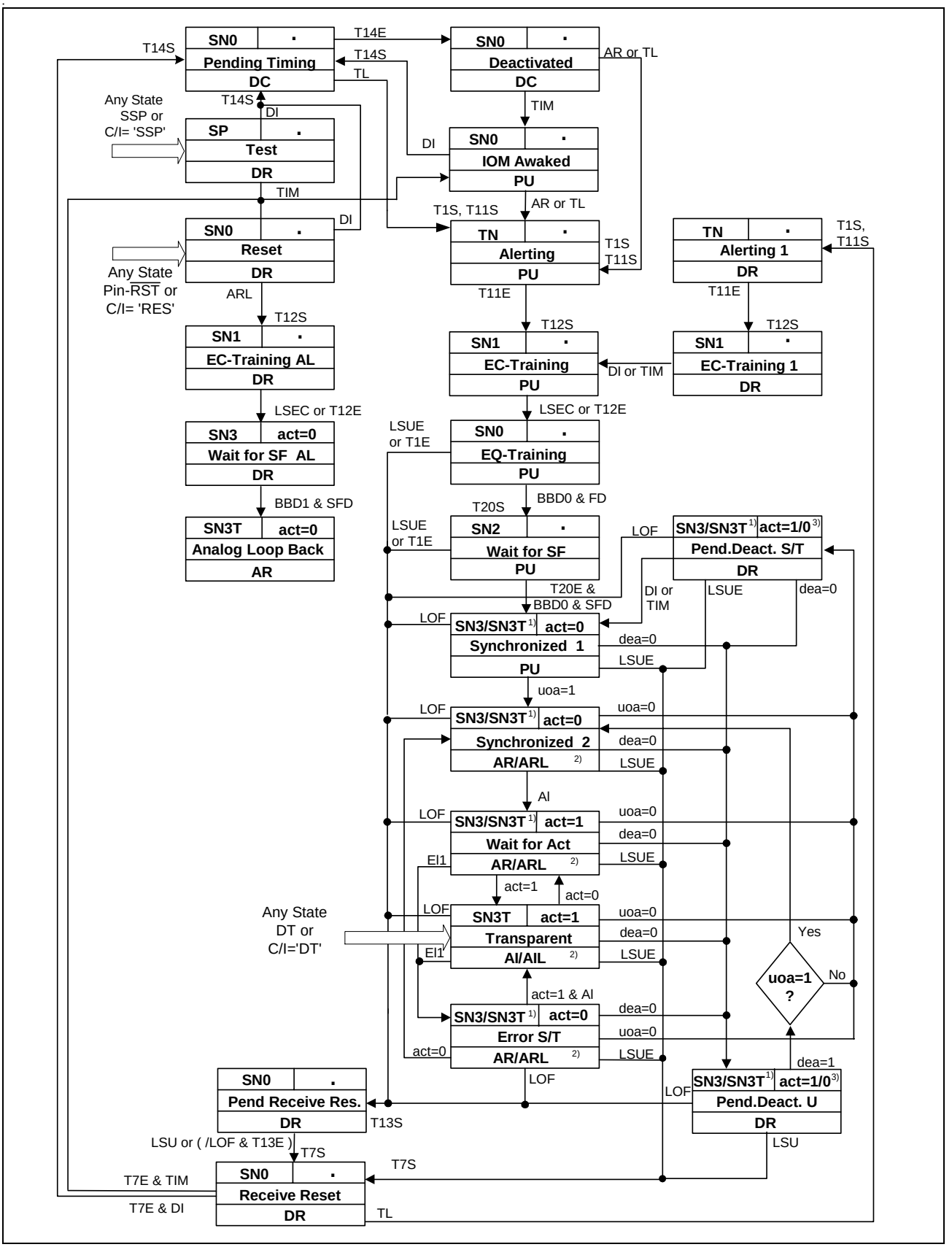


Figure 98 Simplified State Machine Q-SMINT®IX: 2B1Q

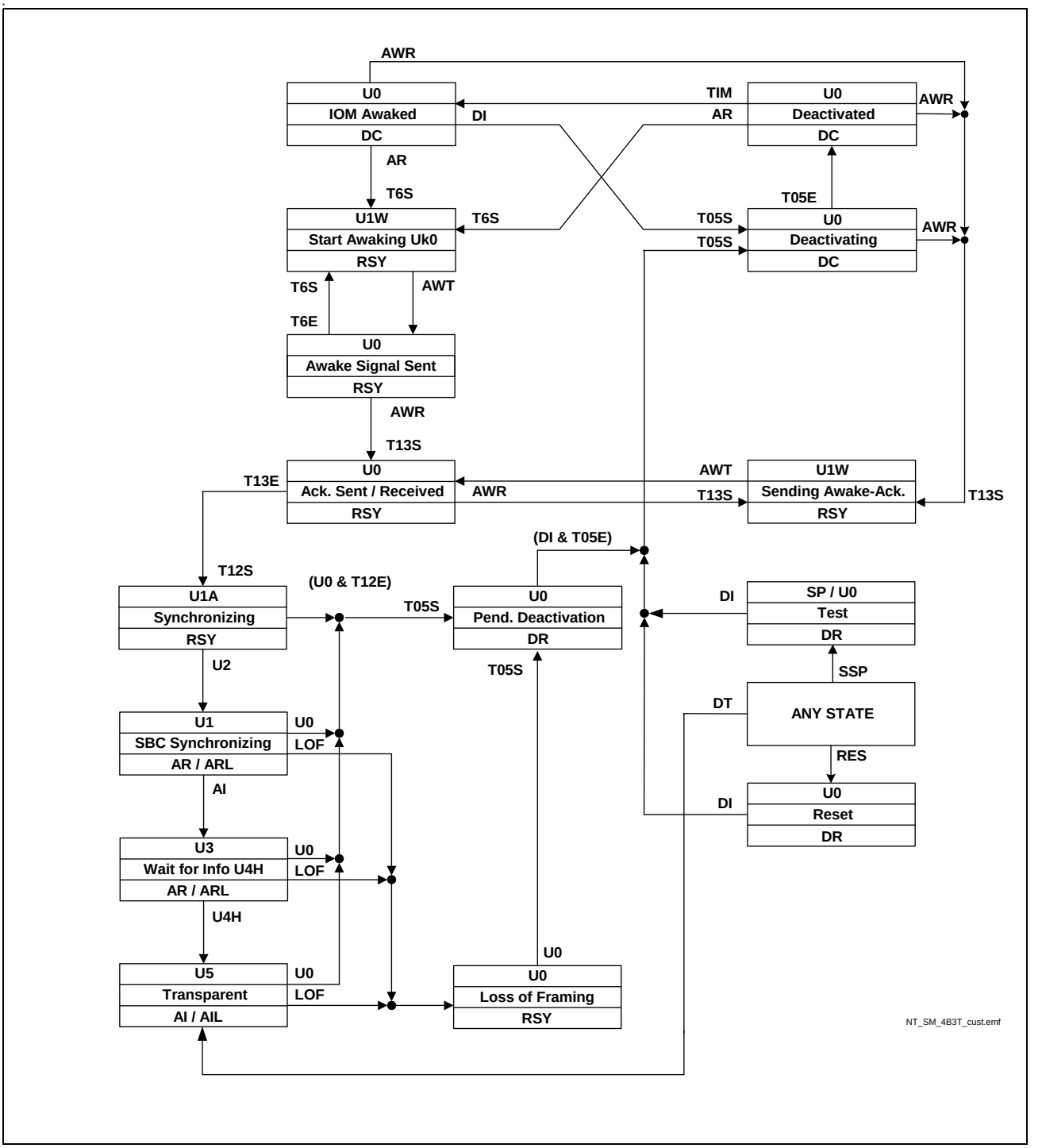


Figure 99 IEC-T/NTC-T Compatible State Machine T-SMINT®IX: 4B3T

Both the Q- and the T-SMINT®IX U-transceiver can be controlled via state machines, which are compatible to those defined for the old NT generation INTC-Q and NTC-T. Additionally, the Q-SMINT®IX possesses a newly defined, so called ‘simplified‘ state machine. This simplified state machine can be used optionally instead of the INTC-Q compatible state machine and eases the U-transceiver control by software. Such a simplified state machine is not available for the T-SMINT®IX.

7.2.3 Command/Indication Codes

Table 49 C/I Codes

Code	Q-SMINT®IX: 2B1Q		T-SMINT®IX: 4B3T	
	IN	**OUT**	**IN**	**OUT**
0000	TIM	DR	TIM	DR
0001	RES	–	–	–
0010	–	–	–	–
0011	–	–	–	–
0100	EI1	EI1	–	RSY
0101	SSP	–	SSP	–
0110	DT	–	DT	–
0111	–	PU	–	–
1000	AR	AR	AR	AR
1001	–	–	–	–
1010	ARL	ARL	–	ARL
1011	–	–	–	–
1100	AI	AI	AI	AI
1101	–	–	RES	–
1110	–	AIL	–	AIL
1111	DI	DC	DI	DC

7.2.4 Interrupt Structure

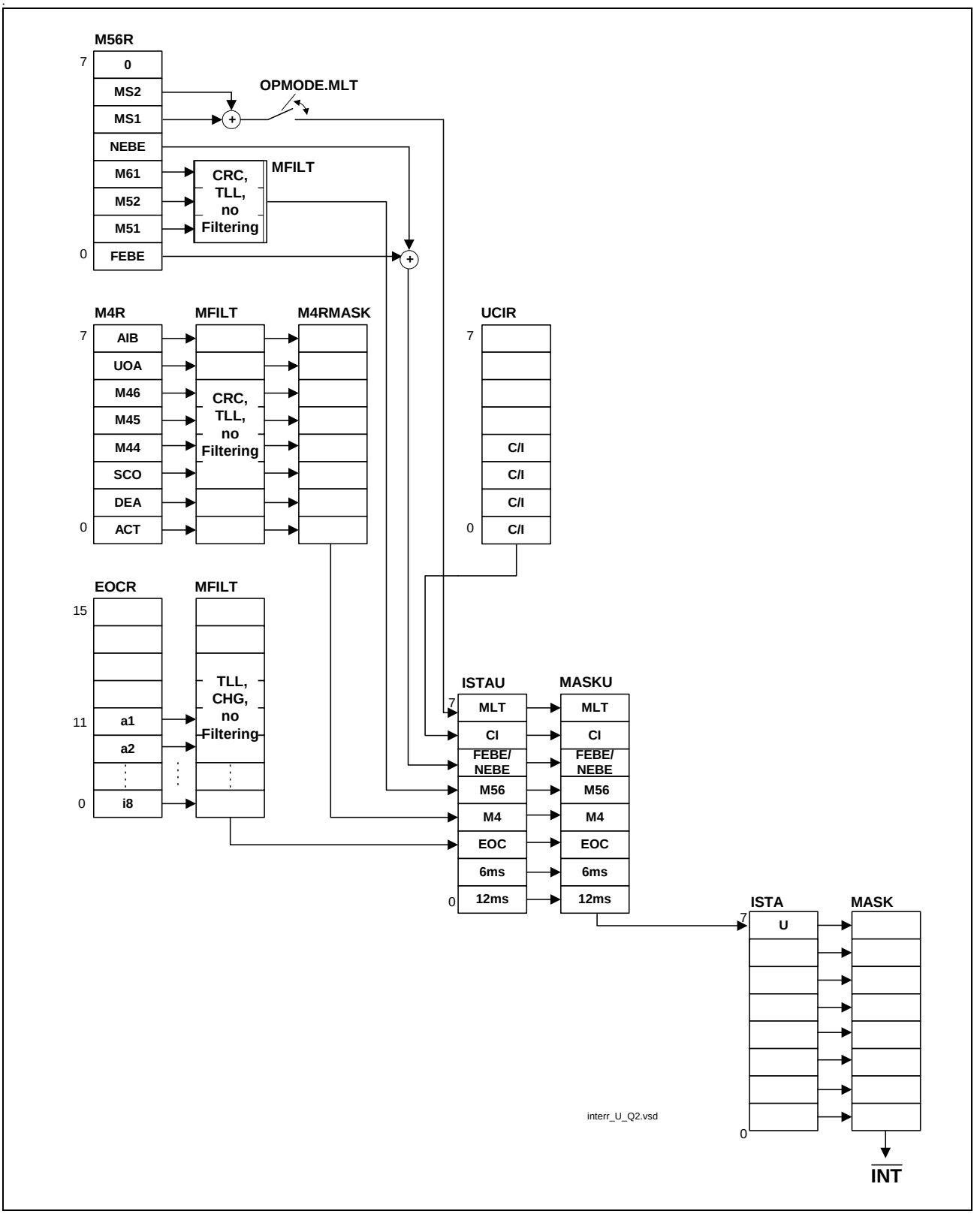


Figure 100 Interrupt Structure U-Transceiver Q-SMINT®IX: 2B1Q

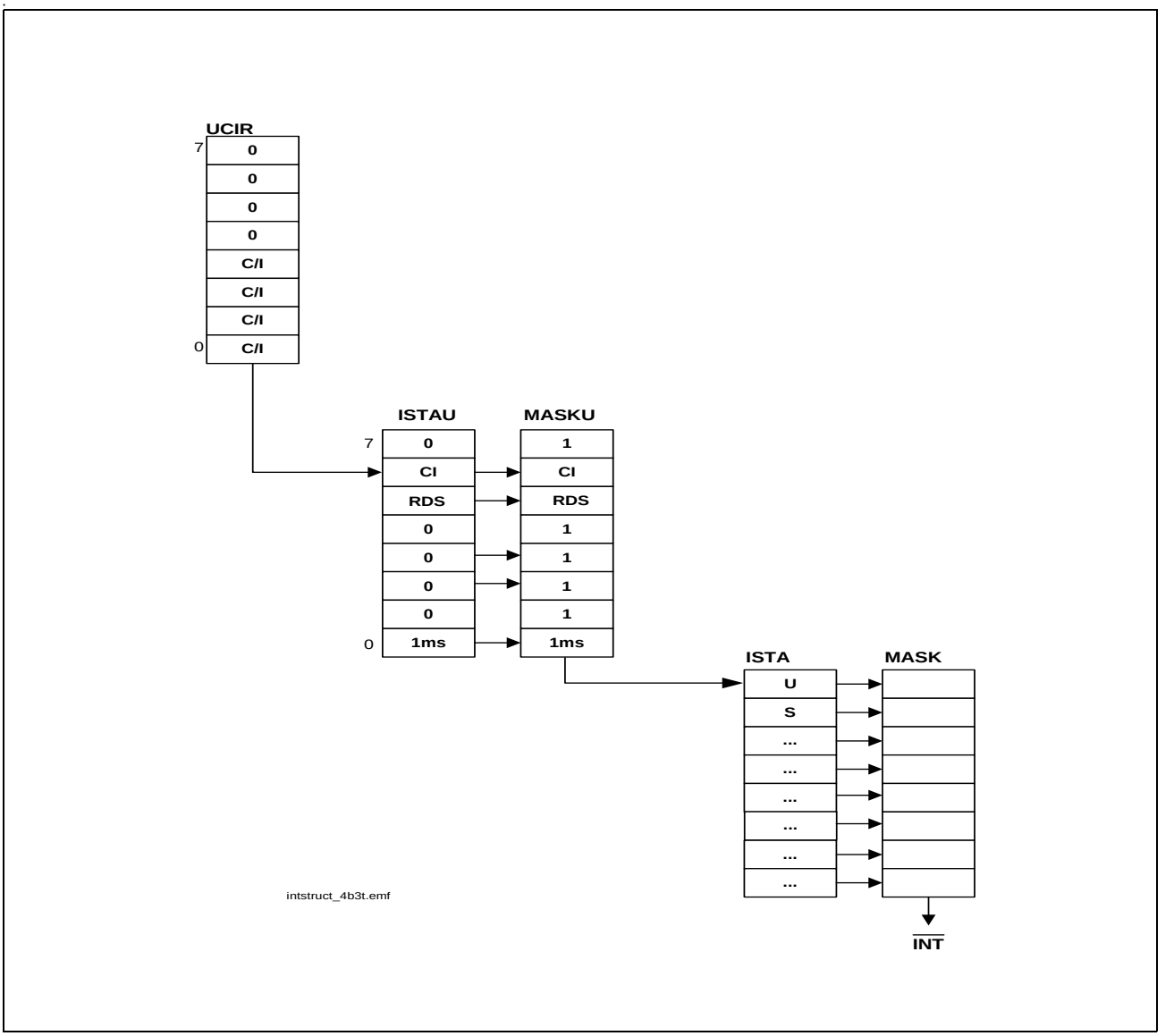


Figure 101 Interrupt Structure U-Transceiver T-SMINT®IX: 4B3T

7.2.5 Register Summary U-Transceiver

U-Interface Registers Q-SMINT®IX: 2B1Q

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
OPMODE	0	UCI	FEBE	MLT	0	CI_ SEL	0	0	60_H	R*/W	14_H
MFILT	M56 FILTER		M4 FILTER			EOC FILTER			61_H	R*/W	14_H
	reserved								62_H		
EOCR	0	0	0	0	a1	a2	a3	d/m	63_H	R	0F
	i1	i2	i3	i4	i5	i6	i7	i8	64_H		FF_H
EOCW	0	0	0	0	a1	a2	a3	d/m	65_H	W	01_H
	i1	i2	i3	i4	i5	i6	i7	i8	66_H		00_H
M4RMASK	M4 Read Mask Bits								67_H	R*/W	00_H
M4WMASK	M4 Write Mask Bits								68_H	R*/W	$A8_H$
M4R	verified M4 bit data of last received superframe								69_H	R	BE_H
M4W	M4 bit data to be send with next superframe								$6A_H$	R*/W	BE_H
M56R	0	MS2	MS1	NEBE	M61	M52	M51	FEBE	$6B_H$	R	$1F_H$
M56W	1	1	1	1	M61	M52	M51	FEBE	$6C_H$	W	FF_H
UCIR	0	0	0	0	C/I code output				$6D_H$	R	00_H
UCIW	0	0	0	0	C/I code input				$6E_H$	W	01_H
TEST	0	0	0	0	CCRC	+-1 Tones	0	40 KHz	$6F_H$	R*/W	00_H
LOOP	0	DLB	TRANS	U/IOM®	1	LBBD	LB2	LB1	70_H	R*/W	08_H
FEBE	FEBE Counter Value								71_H	R	00_H
NEBE	NEBE Counter Value								72_H	R	00_H
	reserved								73_H-79_H		

Appendix: Differences between Q- and T-SMINT,IX

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
ISTAU	MLT	CI	FEBE/ NEBE	M56	M4	EOC	6ms	12ms	$7A_H$	R	00_H
MASKU	MLT	CI	FEBE/ NEBE	M56	M4	EOC	6ms	12ms	$7B_H$	R*/W	FF_H
	reserved								$7C_H$		
FW_ VERSION	FW Version Number								$7D_H$	R	$6x_H$
	reserved								$7E_H$- $7F_H$		

Appendix: Differences between Q- and T-SMINT,IX

U-Interface Registers T-SMINT®IX: 4B3T

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
OPMODE	0	UCI	0	0	0	0	0	0	60_H	R*/W	00_H
	reserved								61_H-$6C_H$		
UCIR	0	0	0	0	C/I code output				$6D_H$	R	00_H
UCIW	0	0	0	0	C/I code input				$6E_H$	W	01_H
	reserved								$6F_H$		
LOOP	0	DLB	TRANS	U/IOM®	1	LBBD	LB2	LB1	70_H	R*/W	08_H
	reserved								71_H		
RDS	Block Error Counter Value								72_H	R	00_H
	reserved								73_H-79_H		
ISTAU	0	CI	RDS	0	0	0	0	1 ms	$7A_H$	R	00_H
MASKU	1	CI	RDS	1	1	1	1	1 ms	$7B_H$	R*/W	FF_H
	reserved								$7C_H$		
FW_ VERSION	FW Version Number								$7D_H$	R	$3x_H$
	reserved								$7E_H$-$7F_H$		

7.3 External Circuitry

The external circuitry of the Q- and T-SMINT®IX is equivalent; however, some external components of the U-transceiver hybrid must be dimensioned different for 2B1Q and 4B3T. All information on the external circuitry is preliminary and may be changed in future documents.

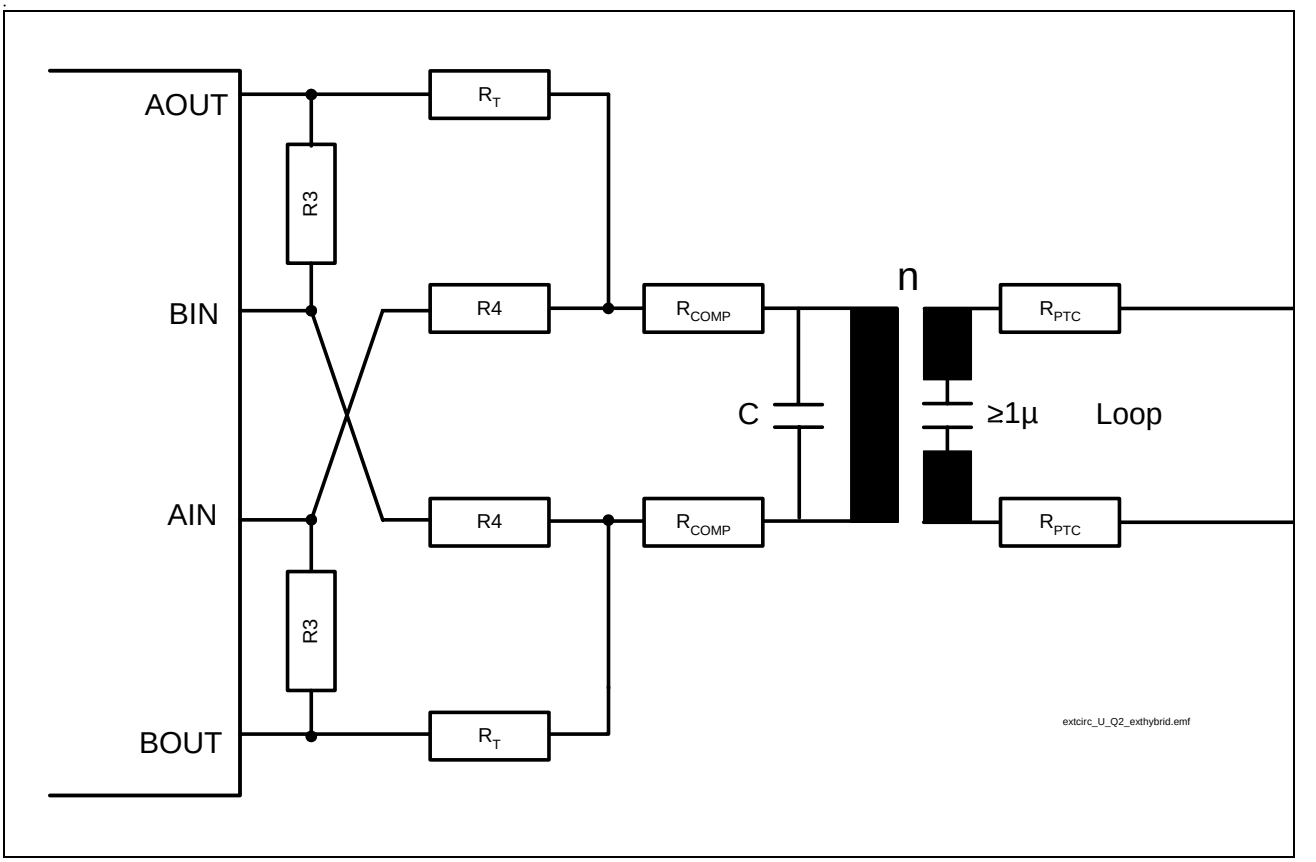


Figure 102 External Circuitry Q- and T-SMINT®IX

Note: the necessary protection circuitry is not displayed in ***Figure 102***

Table 50 Dimensions of External Components

Component	Q-SMINT®IX: 2B1Q	T-SMINT®IX: 4B3T
Transformer: Ratio Main Inductivity	 1:2 14.5 mH	 1:1.6 7.5 mH
Resistance R3	1.3 kΩ	1.75 kΩ
Resistance R4	1.0 kΩ	1.0 kΩ
Resistance R_T	9.5 Ω	25 Ω
Capacitor C	27 nF	15 nF
R_{PTC} and R_{Comp}	$2R_{PTC} + 8R_{Comp} = 40\ \Omega$	$n^2 \times (2R_{COMP} + R_B) + R_L = 20\Omega$

8 Index

R

S

T

U

W

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