ICs for Communications

Smart Integrated Digital Echo Canceller
SIDEC

PEB 20954 Version 1.1

Preliminary Data Sheet Apr.1999

DS 1

PEB 20954 **Revision History:**		**Current Version: Apr.1999, Version 1.1**
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
7	7	power dissipation is 700-900 mW instead of 1200 mW
7,119	7,122	temperature range -40°C - 85°C instead of 0°C - 70°C
-	10	section about SIDEC in VoIP added
58,60	60,62	µP max. timing changed from 20 ns to 25 ns
101	104	Description of bit AACSC.ACSEFFECT corrected
113,114	116,117	Fig. 38 and Fig. 39 interchanged (Now Fig 39 and Fig. 40)
120	123,124	AC Characteristics added
121	124	Capacitances added

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1 Introduction

The **S**mart **I**ntegrated **D**igital **E**cho **C**anceller (SIDEC) suppresses echoes in telecommunication networks which might disturb any kind of terrestrial or wireless communication. It incorporates leading edge CMOS technology as well as SIEMENS' many years' experience in Telecommunication ICs.

In communication links reflections resulting in an electrical echo are due to hybrid splits or imperfect terminations in subscriber loops. Acoustical echoes may occur due to poor isolation of microphone and speaker of some telephone system. These electrical and acoustical echoes disturb the quality of the transmission. To ensure high quality, pure data transmission the ITU-T (International Telecommunications Union, Telecommunication Standardization Sector) suggests in the recommendation G.131 the use of echo cancellers. Echo cancellation is extremely desirable for data links with total round trip transmission times of more than 50 ms.

Smart Integrated Digital Echo Canceller
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PEB 20954

Version 1.1

CMOS

1.1 Key Features

TQFP-144

- 2.048 MHz PCM input and output interfaces with selectable µ- and A-Law coding according to ITU G.711
- Rapid convergence of patented algorithm at the beginning or during a connection even in the presence of background noise at the near end subscriber
- Echo return loss enhancement of > 30 dB (ERLE)
- Detection of double talk for adaptive convergence control
- Independently controlled voiceband echo cancelling according to ITU G.165 and G.168 for
  - 32 channels with end echo path delay of less than 63.75 ms
  - 16 channels with end echo path delay of less than 127.75 ms (usage of two SIDEC in parallel for simultaneous processing of 32 channels is easily possible)
- Smart Non Linear Processor controlled by echoloss, echo path delay and background noise
- Various options for comfort noise injection
- Maskable disabling functions
  - 2100 Hz tone with phase reversal detection
  - 2100 Hz tone without phase reversal detection
  - 2010 Hz continuity check (SS7)
  - via PCM timeslot 16 Bit a, b, c or d according to ITU G.704
  - individual channels maskable via Microprocessor Interface, UCC Interface and Serial Interface
- Integrated Universal Control and Communication Interface (UCCI) for signaling highways with direct hardware control for:
  - disable cancelling
  - configurable disabling functions
  - communication between board controllers

Type	Package
PEB 20954	TQFP-144

- Support of Channel Associated Signaling (CAS) BR transparency (robbed bits) in send path
- Selectable µ- to A-Law or A- to µ-Law Conversion on a global or per channel basis
- Configurable idle channel supervision
- Clear channel capability (64 clear) on a per channel basis
- Special evaluation of bit 8 in T1 Modem calls possible (56 clear)
- Serial 256 kbit/s interface to control the functions disable cancelling, freeze coefficients, clear channel, disable NLP, PCM Law conversion control or combinations of above
- Monitor pins for several internal states
- Switchable global loop from receive output to send input and send output to receive input
- Switchable global attenuation (2.5 dB or 6 dB) at the receive and send output
- Flexible Microprocessor Interface (SIEMENS/Intel or Motorola type, Mux and Demux mode) usable for:
  – configuration of parameters such as thresholds and functions on a global basis
  – Disable cancelling, freeze coefficients, clear channel, disable NLP, PCM Law conversion control (all functions individually for each channel)
  – support of background tests for disabled or idle timeslots (feeding and reading of test levels)
  – possibility to read levels, attenuations, internal states, signal values or all coefficients of a selected timeslot
  – control of the RAM Built In Self Test
- Advanced Integrated Watchdog Timer
- Supervision of the input clocks
- Various clock modes possible for 32.768 MHz and 8.192 MHz
- Boundary Scan according to IEEE 1149.1 Standard
- Power supply: 3.3 V, 5V tolerant inputs
- Typical power dissipation: 700 - 900 mW
- Plastic package TQFP 144
- Temperature range: -40°C - 85°C

1.2 Logic Symbol

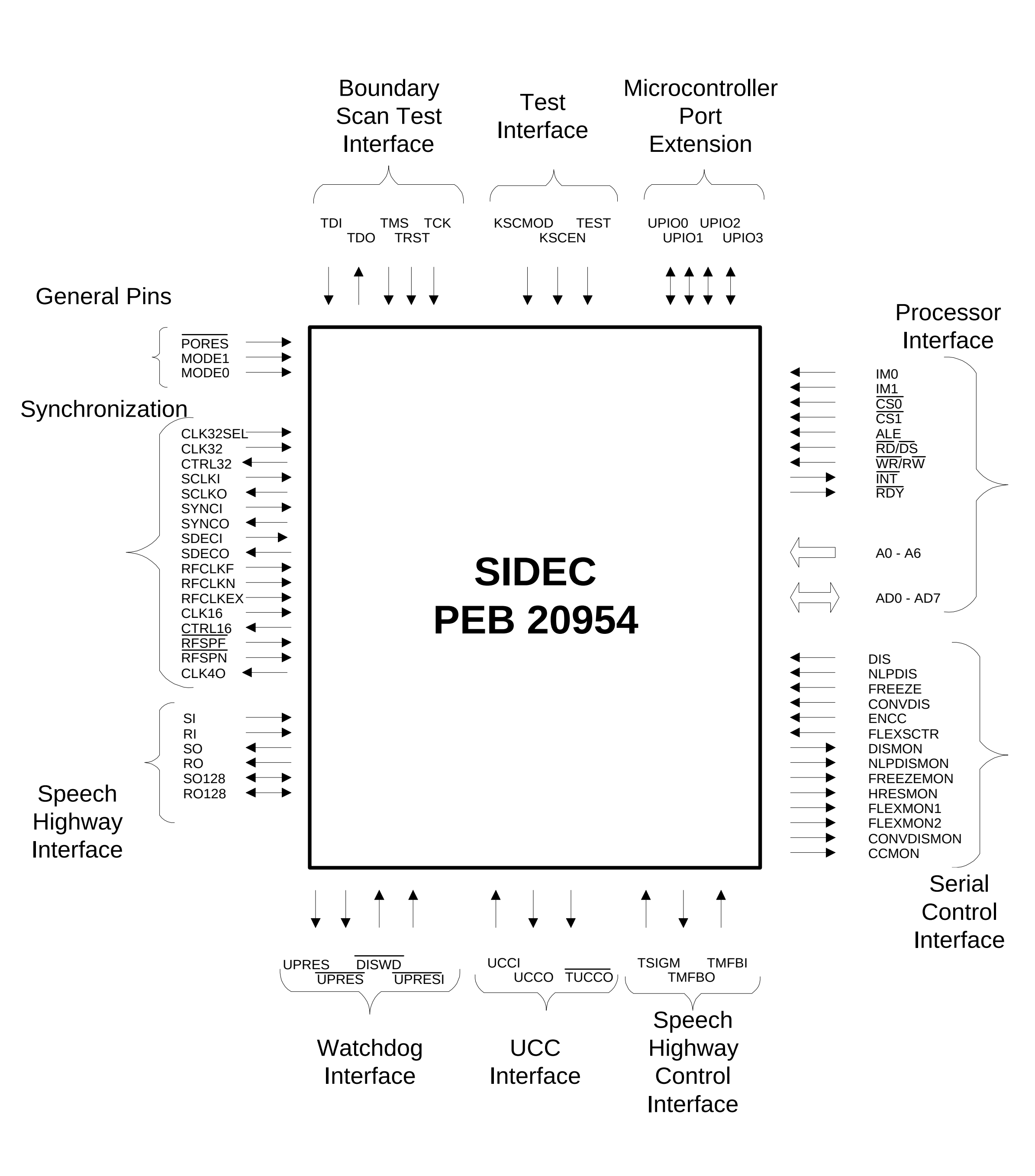

Figure 1 Logic Symbol of the SIDEC

1.3 Typical Applications

The SIDEC can be used for various applications.

Figure 2 to **Figure 5** display typical examples.

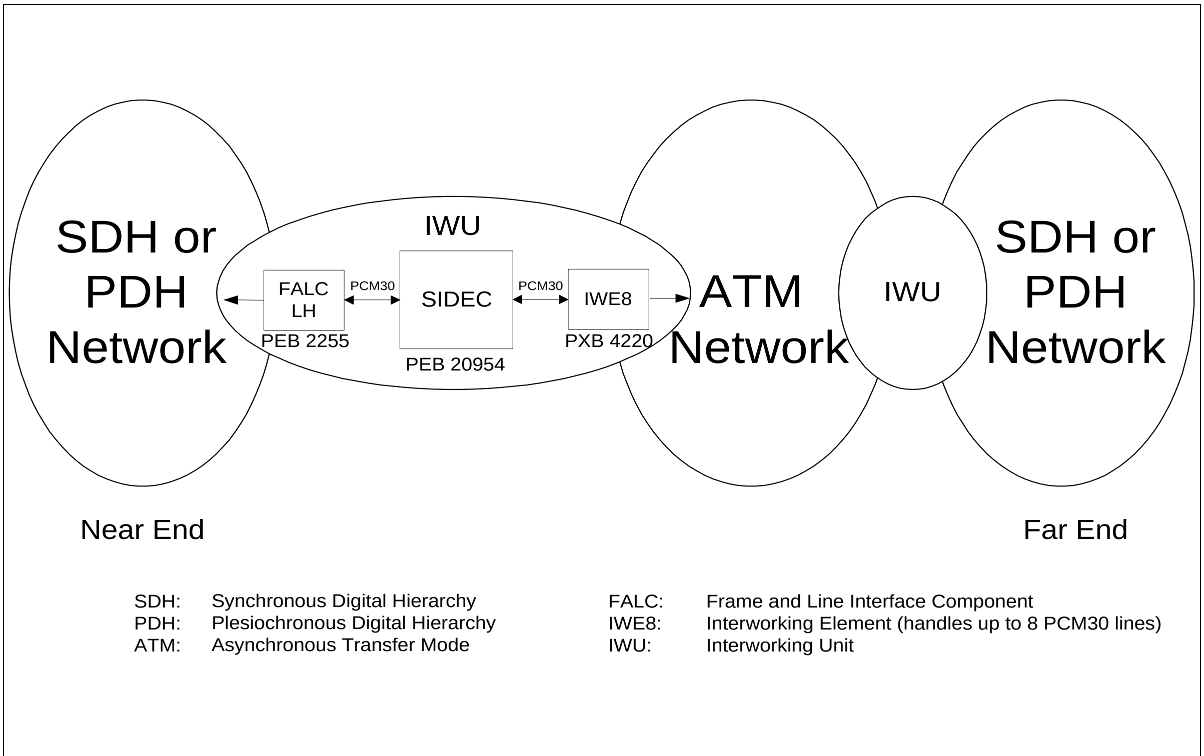

Figure 2 SIDEC in a Circuit Emulation Service Carried over ATM

In this interworking unit there are two SIEMENS products connected to the SIDEC. The FALC PEB 2255 serves as a frame and line interface component whereas the IWE8 PXB 4220 operates as an interworking element.

The delays of networks and the inter working units are usually long. In the application above the SIDEC cancels the echo that is generated by reflection on the near end side and heard by the far end speaker. The SIDEC can cancel end echo paths (SDH or PDH Network on near end side) up to 128 ms. For details see **Figure 11**.

For the set up illustrated in **Figure 2** a application note "Using SIDEC in a Voice over ATM Application" is available.

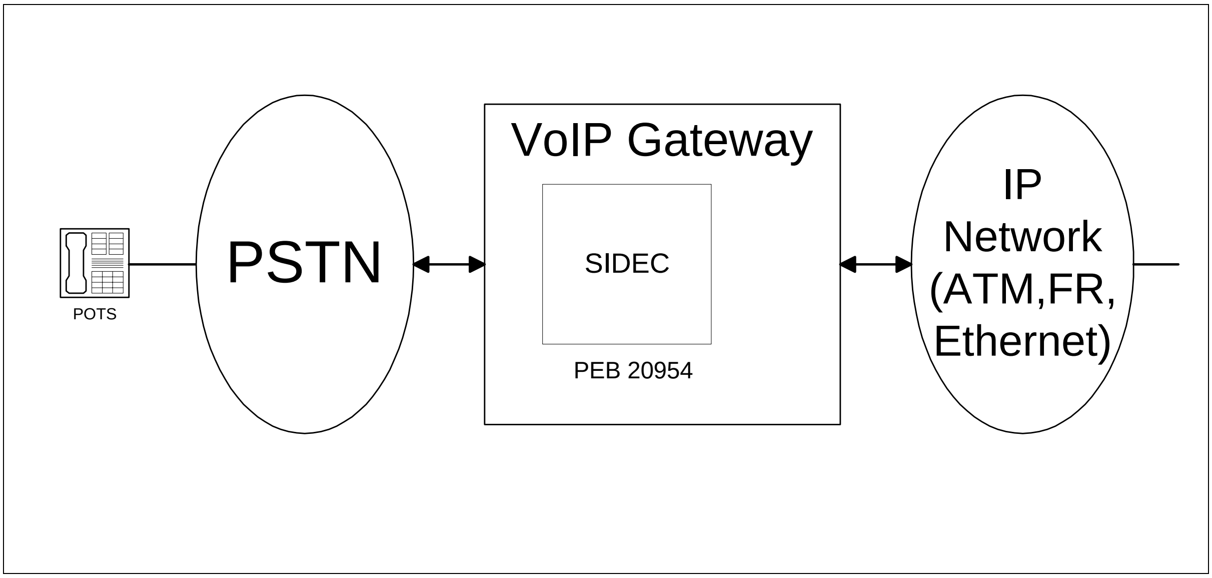

Figure 3 SIDEC in a Voice over IP Gateway

An emerging market in the telecom industry is “Voice Over IP”. Due to the long delay echo cancellation is required. The delay is introduced through packetizing and voice compression. The SIDEC handles different functions in a Voice over IP gateway, such as Voice Detection, Voice Activity Detection, Comfort Noise and A-law u-law conversion regarding G.711.

In a gateway the SIDEC points into the PSTN network as shown in **Figure 3**. The echo itself is generated by the hybrid in the PSTN cloud. Before the voice signal from the POTS gets packetized into ATM, FR or Ethernet cells the echo is being cancelled by the SIDEC.

For a high voice quality in “Voice Over IP” environment echo cancellation is a major requirement.

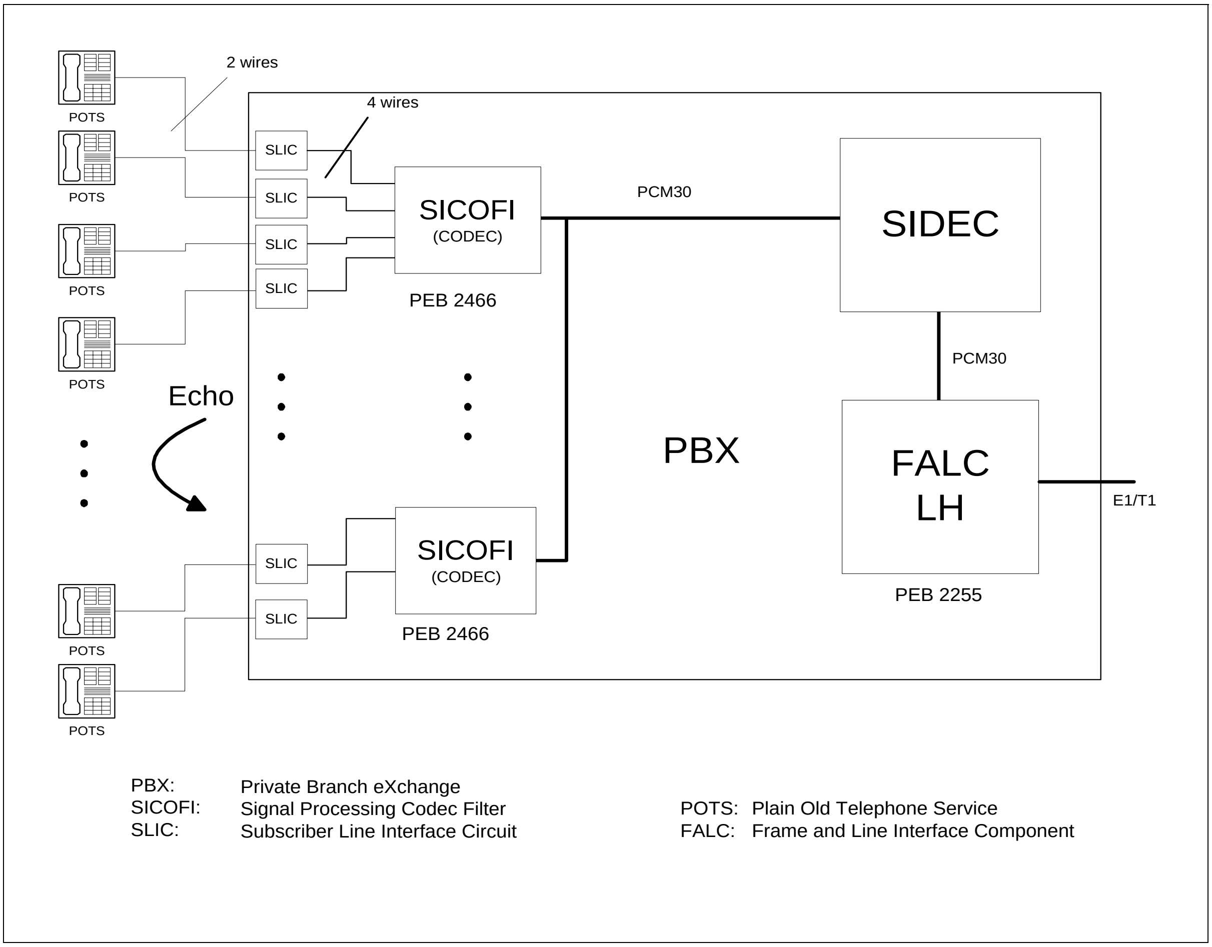

Figure 4 SIDEC in a Private Branch Exchange (PBX)

SIDEC can be used in a PBX or Central Office (CO) to cancel the echo next to the customer side (near end echo). The echo delay is kept short. The delay for this application is usually less than 64ms and the SIDEC can cancel up to 32 channels.

Figure 4 shows a PBX with a T1/E1 interface FALC LH to the CO on the one side. On the other side analog phones are connected.

A possible SIEMENS solution with the SICOFI (includes D/A and A/D conversion) and the SLIC (hybrid) to connect the analog phone is shown above.

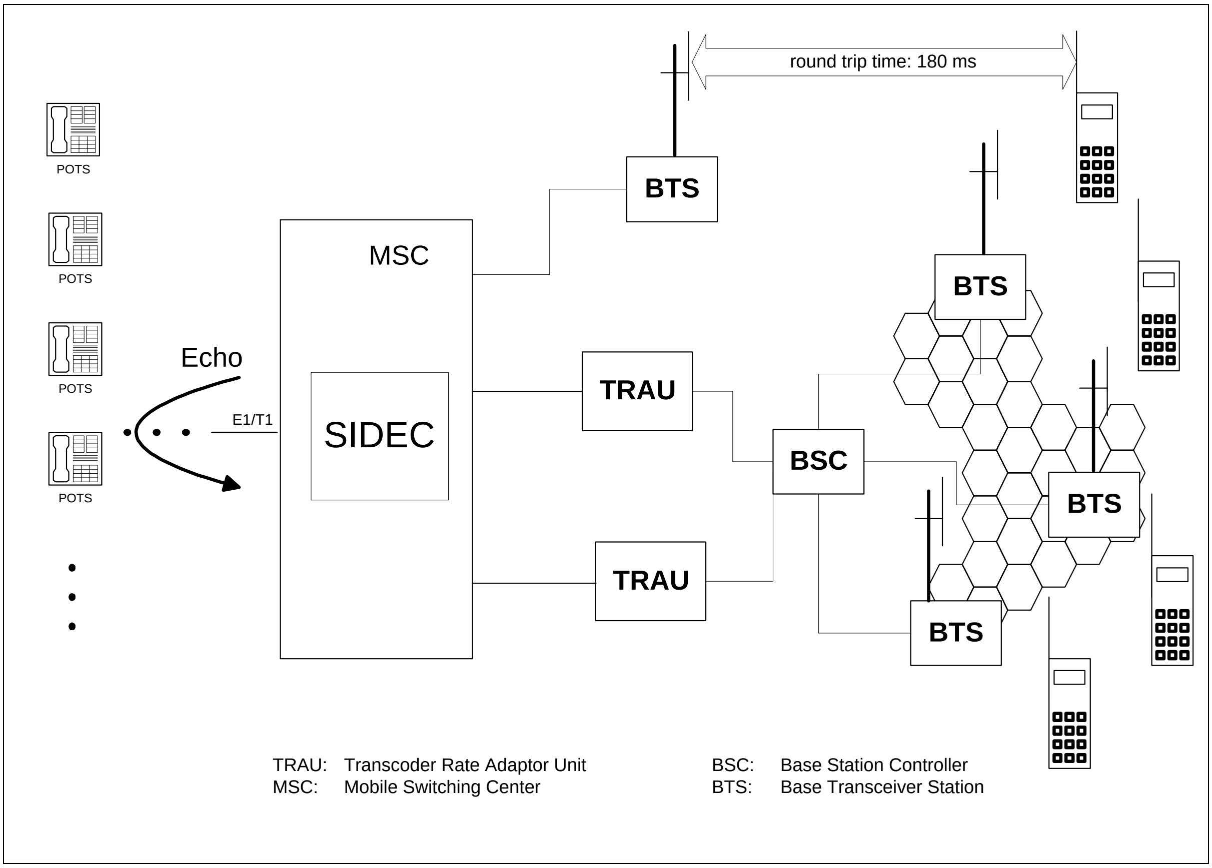

Figure 5 SIDEC in a Wireless System

Due to voice compression and error correction the one way transmission time for wireless voice signals is typically 90 ms. With 180 ms roundtrip time the 50 ms roundtrip time for echo free transmission is exceeded by at least 130 ms. Hence, the speaker on the mobile phone will hear any kind of echo generated in the hybrid next to the POTS or the acoustical echo of the POTS. The SIDEC suppresses those two kinds of echoes if it is incorporated in the MSC. Depending on the individual call the end echo path can differ dramatically. In Europe the end echo path could even go to different countries causing strong dispersion of the echo. Only a high quality echo canceller with long end path delay options guarantees compensation of the strongly varying echoes.

2 Pin Descriptions

2.1 Pin Diagram

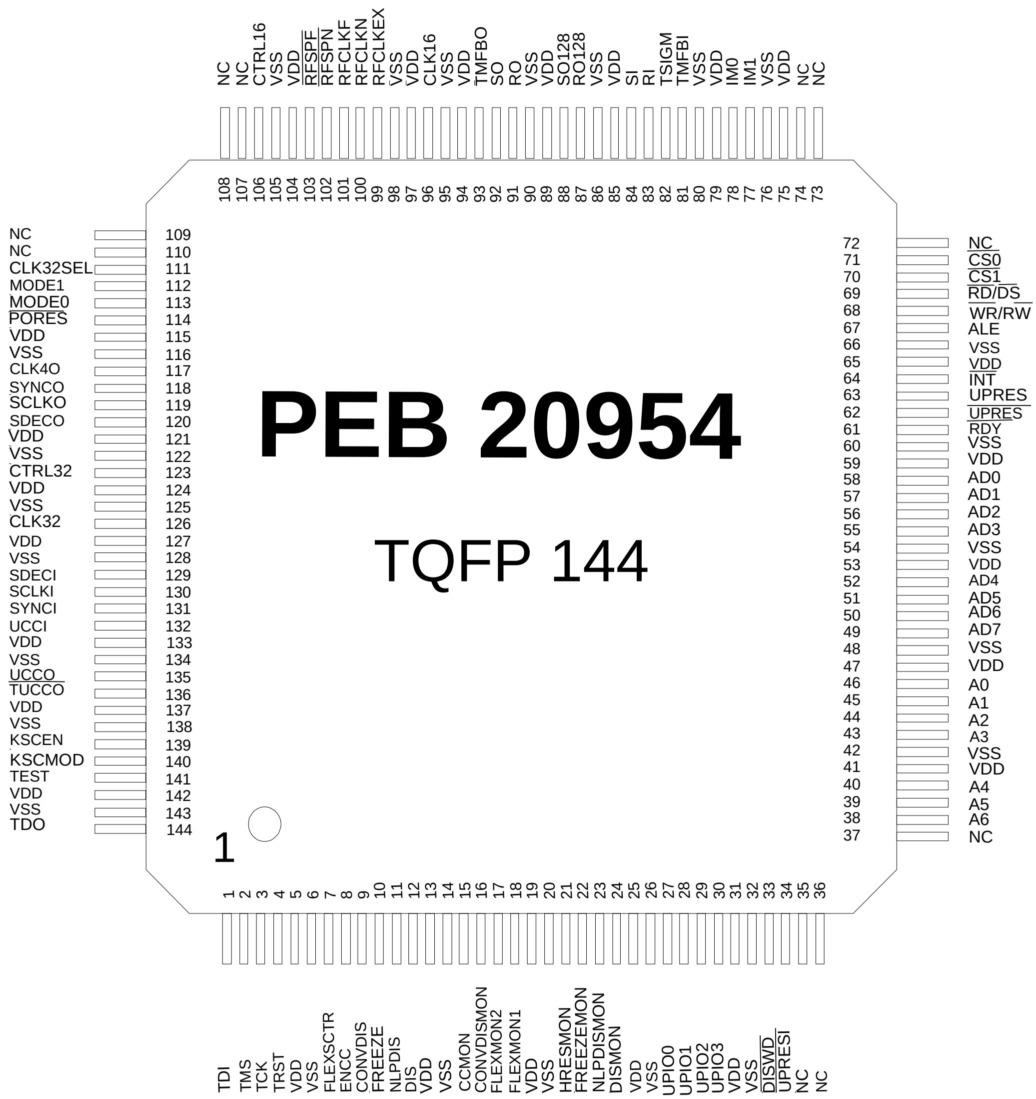

Figure 6 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 General Pins

Pin No.	Symbol	Input (I) Output (O) Pull Up / Pull Down	Function			
114	$\overline{\text{PORES}}$	I, PU	Power On Reset. A low on this pin forces all registers and counters to predefined values			
112 113	MODE1 MODE0	I, PU I, PU	1 1	End delay < 64ms	1 0	For future use
112 113	MODE1 MODE0	I, PU I, PU	0 1	End delay < 128 ms Master Mode	0 0	End delay < 128 ms Slave Mode

Table 2 Synchronization

Pin No.	Symbol	I/O, PU/PD	Function
111	CLK32SEL	I, PU	Selects from which source SCLKO will be derived: '1': SCLKO will be derived from CLK32 by dividing by 4 '0': SCLKO will be derived from CLK16 by dividing by 2
126	CLK32	I, PU	32.768 MHz Operating Clock for the SIDEC
123	CTRL32	O	Control voltage for the 32.768 MHz operating Clock VCO, maskable for reduced power consumption
130	SCLKI	I, PU	System clock input (8.192 MHz) for PCM- and UCCI
119	SCLKO	O	8.192 MHz system clock output, source CLK32 or CLK16 is selectable via pin CLK32SEL, maskable for reduced power consumption
117	CLK4O	O	4.096 MHz system clock output for subsequent circuits, derived from SCLKI, maskable for reduced power consumption

Pin No.	Symbol	I/O, PU/PD	Function
131	SYNCI	I, PU	System Synchronization input pulse. Defines the frame alignment of PCM and UCCI signals in conjunction with the values in registers RIALIGN, SIALIGN, SOALIGN, UCCALIGN, PHALIGN and also the multiframe alignment of the UCCI. Must be integer multiple of 125 µs if UCC Interface is not used. Must be multiple integer of 4 ms if UCC interface is used. Leave open if not used or connect to V_{DD}
118	SYNCO	O	System Synchronization output pulse (see SYNCI), duration configurable one or two SCLKO periods, period 125 µs. If the UCC interface is not used and no SYNCI is applied, SYNCO can take over the part and role of SYNCI.
120	SDECO	O	Synchronization output pulse for other SIDECs if this SIDEC uses its own 32.768 MHz VCO. Can also be used for synchronization of external devices to the serial control input and monitor output signals of the SIDEC.The pulse width is 488 ns with a period of 125 µs.
129	SDECI	I, PU	Synchronization input pulse if the SIDEC uses the 32.768 MHz VCO of another SIDEC. The same SCLKI signal can be applied to SDECI and SCLKI pin if the SCLKI is supplied by a source with correct phase condition to the CLK32 (see **Figure 14**). If the pin is not used leave it open or connect it to V_{DD}.
101	RFCLKF	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6:5]="00"
100	RFCLKN	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6:5]="01"

Pin No.	Symbol	I/O, PU/PD	Function
99	RFCLKEX	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6]='1'
96	CLK16	I, PU	Clock from 16.384 MHz VCXO
106	CTRL16	O	Control voltage for the 16.384 MHz VCXO
103	$\overline{\text{RFSPF}}$	I, PU	Receive Frame Sync Pulse from the far end side (F1). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '0'.
102	$\overline{\text{RFSPN}}$	I, PU	Receive Frame Sync Pulse from the near end side (F2). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '1'.

Table 3 Microprocessor Interface

Pin No.	Symbol	I/O, PU/PD	Function
78	IM0	I, PU	Interface Mode SIEMENS/Intel = low, Motorola = high
77	IM1	I, PU	Interface Mode MUXED = low, DEMUXED = high
71	$\overline{\text{CS0}}$	I, PU	Chip Select. A low signal selects the SIDEC (internally "anded" with $\overline{\text{CS1}}$).
70	$\overline{\text{CS1}}$	I, PU	Chip Select. A low signal selects the SIDEC (internally "anded" with $\overline{\text{CS0}}$).
46-43 40-38	A0..A6	I, PU	Address Bus. Only used in demuxed mode, can be left open in muxed mode.
58-55 52-49	AD0..AD7	I/O, -	Multiplexed Address/Data Bus in multiplexed mode, Data Bus in demultiplexed mode
67	ALE	I, PU	Address Latch Enable in multiplexed mode. Address on AD bus is internally latched with the falling edge of ALE.This signal is also used for the internal clock supervision. In Demuxed mode there must be provided an external independent clock signal (i.e. processor clock) in order to enable proper clock supervision.
69	$\overline{\text{RD}}/\overline{\text{DS}}$	I, PU	SIEMENS/Intel mode. A low indicates a read operation. Motorola mode. Data Strobe, active low to control read/write
68	$\overline{\text{WR}}/\text{R}\overline{\text{W}}$	I, PU	SIEMENS/Intel mode. A low indicates a write operation. Motorola mode. High = read cycle, low = write cycle
64	$\overline{\text{INT}}$	O, (od)	Interrupt request from the SIDEC, active low
61	$\overline{\text{RDY}}$	O, (od)	Ready signal for µC devices that support this feature. For read cycles the signal is asserted after the data on the AD bus is valid. For writing cycles the signal is asserted when a write access is ready to be concluded.

Table 4 Microcontroller Port Extension

Pin No.	Symbol	I/O, PU/PD	Function
27	UPIO0	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
28	UPIO1	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
29	UPIO2	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
30	UPIO3	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO

Table 5 Processor Watchdog Circuit

Pin No.	Symbol	I/O, PU/PD	Function
63	UPRES	O	µP-Reset. High pulse (125 µs) if the µP fails to write predefined values to the registers WDG1 to WDG3 in this sequence within 2 s and $\overline{\text{DISWD}}$='1'. Also active if $\overline{\text{PORES}}$='0' or $\overline{\text{UPRESI}}$='0'
62	$\overline{\text{UPRES}}$	O	Same as UPRES, but low active
33	$\overline{\text{DISWD}}$	I, PU	Disable of µP-Reset on active watchdog condition if set to low
34	$\overline{\text{UPRESI}}$	I, PU	Produces a reset signal at UPRES, $\overline{\text{UPRES}}$ if set to low

Table 6 Speech Highways

Pin No.	Symbol	I/O, PU/PD	Function
84	SI	I, PD	2.048 Mbit/s Send speech highway input. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers SIALIGN and PHALIGN[3:2]
83	RI	I, PD	2.048 Mbit/s Receive speech highway input. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers RIALIGN and PHALIGN[1:0]

Pin No.	Symbol	I/O, PU/PD	Function
92	SO	O	2.048 Mbit/s Send speech highway output. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers SOALIGN and PHALIGN[5:4]
91	RO	O	2.048 Mbit/s Receive speech highway output. This signal will has a fixed delay of one PCM frame (125 µs) with respect to RI
88	SO128	I/O, PU	Auxiliary 2.048 Mbit/s Send speech highway output in 128 ms mode. Input in master mode, output in slave mode. The pins of master and slave SIDEC in 128 ms mode should be connected to enable a 32 channel system. The signal from the slave is multiplexed in the master with the internally generated signal and output (clocked) with the system clock. Tristate and meaningless in 64 ms mode
87	RO128	I/O, PU	Auxiliary 2.048 Mbit/s Receive speech highway output in 128 ms mode. Input in master mode, output in slave mode. The pins of master and slave SIDEC in 128 ms mode should be connected to enable a 32 channel system. The signal from the slave is multiplexed in the master with the internally generated signal and output (clocked) with the system clock. Tristate and meaningless in 64 ms mode

Table 7 UCC Interface

Pin No.	Symbol	I/O, PU/PD	Function
132	UCCI	I, PD	2.048 Mbit/s UCC highway input. Start of timeslot 0, bit 7 and frame number can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers UCCMFR, UCCALIGN and PHALIGN[7:6]
135	UCCO	O	2.048 Mbit/s UCC highway output. Start of timeslot 0, bit 7 and frame number can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers UCCMFR, UCCALIGN and PHALIGN[7:6]
136	$\overline{\text{TUCCO}}$	O	Tristate control signal for external tristate output buffer at the UCCO bus, active low. Remains inactive after a power on reset until the configuration by the µP has been settled. Active only at UCC timeslot 0 for UCC frames that correspond to processed PCM channels

Table 8 Speech Highway Control Signals for Channel Associated Signaling (CAS) in T1 Systems

Pin No.	Symbol	I/O, PU/PD	Function
82	TSIGM	I, PD	Transmit Signaling Marker, indicating robbed bits at SI, corresponding to the delay of SI
81	TMFBI	I, PD	Transmit Multiframe Begin Input corresponding to the delay of SI
93	TMFBO	O	Transmit Multiframe Begin Output corresponding to the delay of SO. The delay of TMFBI to TMFBO is identical to the delay of SI to SO

Table 9 Channelwise Serial Interface

Pin No.	Symbol	I/O, PU/PD	Function
12	DIS	I, PD	Serial 256 kbit/s disable signal to bypass the canceller, NLP and attenuator and to reset the H-Register and Speech Control unit on a per channel basis. High active, maskable, leave open or connect to ground if unused
11	NLPDIS	I, PD	Serial 256 kbit/s signal to disable the NLP on a per channel basis. High active, maskable, leave open or connect to ground if unused
10	FREEZE	I, PD	Serial 256 kbit/s signal to freeze the H-Registers on a per channel basis. High active, maskable, leave open or connect to ground if unused
9	CONVDIS	I, PD	Serial 256 kbit/s signal to disable A/μ-Law conversion on a per channel basis. High active, maskable, leave open or connect to ground if unused
8	ENCC	I, PD	Serial 256 kbit/s signal to enable clear channel transparency on a per channel basis. High active, maskable, leave open or connect to ground if unused, same function as DIS='1' and CONVDIS='1'
7	FLEXSCTR	I, PD	Flexible serial 256 kbit/s control signal on a per channel basis. Configurable by register CONFLEXSCTR. High active, maskable, leave open or connect to ground if unused
24	DISMON	O	Serial 256 kbit/s EC disable (signals bypass channels) monitor output signal ('0': EC on, '1': EC off)
23	NLPDISMON	O	Serial 256 kbit/s NLP disable monitor output signal ('0': NLP on, '1': NLP off)
22	FREEZEMON	O	Serial 256 kbit/s H-Register freeze monitor output signal ('1': freeze, '0': no freeze)
21	HRESMON	O	Serial 256 kbit/s H-Register reset monitor output signal ('1': reset, '0': no reset)

Pin No.	Symbol	I/O, PU/PD	Function
18	FLEXMON1	O	Serial 256 kbit/s monitor output signal (32 channels at 8 kbit/s), monitoring according to settings of the bits CONFLEXMON[7:4], e.g. Idle channel detection, 2010 Hz tone detected, 2100 Hz tone with or without phase reversal detected, double talk detected, no speech detected
17	FLEXMON2	O	Serial 256 kbit/s monitor output signal (32 channels at 8 kbit/s), monitoring according to settings of the bits CONFLEXMON[3:0], e.g. Idle channel detection, 2010 Hz tone detected, 2100 Hz tone with or without phase reversal detected, double talk detected, no speech detected
16	CONVDISMON	O	Serial 256 kbit/s law conversion disable monitor output signal (’1’: conversion disabled, ’0’: conversion enabled)
15	CCMON	O	Serial 256 kbit/s clear channel transparency (64 clear) monitor output signal (’1’: clear channel on, ’0’: clear channel off), same as DISMON=’1’ and CONVDISMON=’1’

Table 10 Test Interface for Boundary Scan according to IEEE 1149.1

Pin No.	Symbol	I/O, PU/PD	Function
1	TDI	I, PU	Test Data Input
144	TDO	O	Test Data Output
2	TMS	I, PU	Test Mode Select
3	TCK	I, PU	Test Clock
4	TRST	I, PU	Boundary Test Reset (active low, should be tied to ’0’ for normal operation)

Table 11 Test Interface

Pin No.	Symbol	I/O, PU/PD	Function
140	KSCMOD	I, PD	SCAN MODE ENABLE pin for enabling of scan test. For normal operation this pin should be left unconnected or connected to V_{SS}.
139	KSCEN	I, PD	SCAN SHIFT ENABLE pin for shift enabling in scan test. For normal operation this pin should be left unconnected or connected to V_{SS}.
141	TEST	I, -	Reserved for special tests (i.e. IDDQ, MBIST, etc.). For normal operation this pin must be connected to V_{SS}. Disables all pull resistances for IDDQ if set to ’1’. Normal operation: ’0’.

3 Functional Description

Figure 7 depicts the Functional Block Diagram of the SIDEC.

3.1 Functional Block Diagram and Description

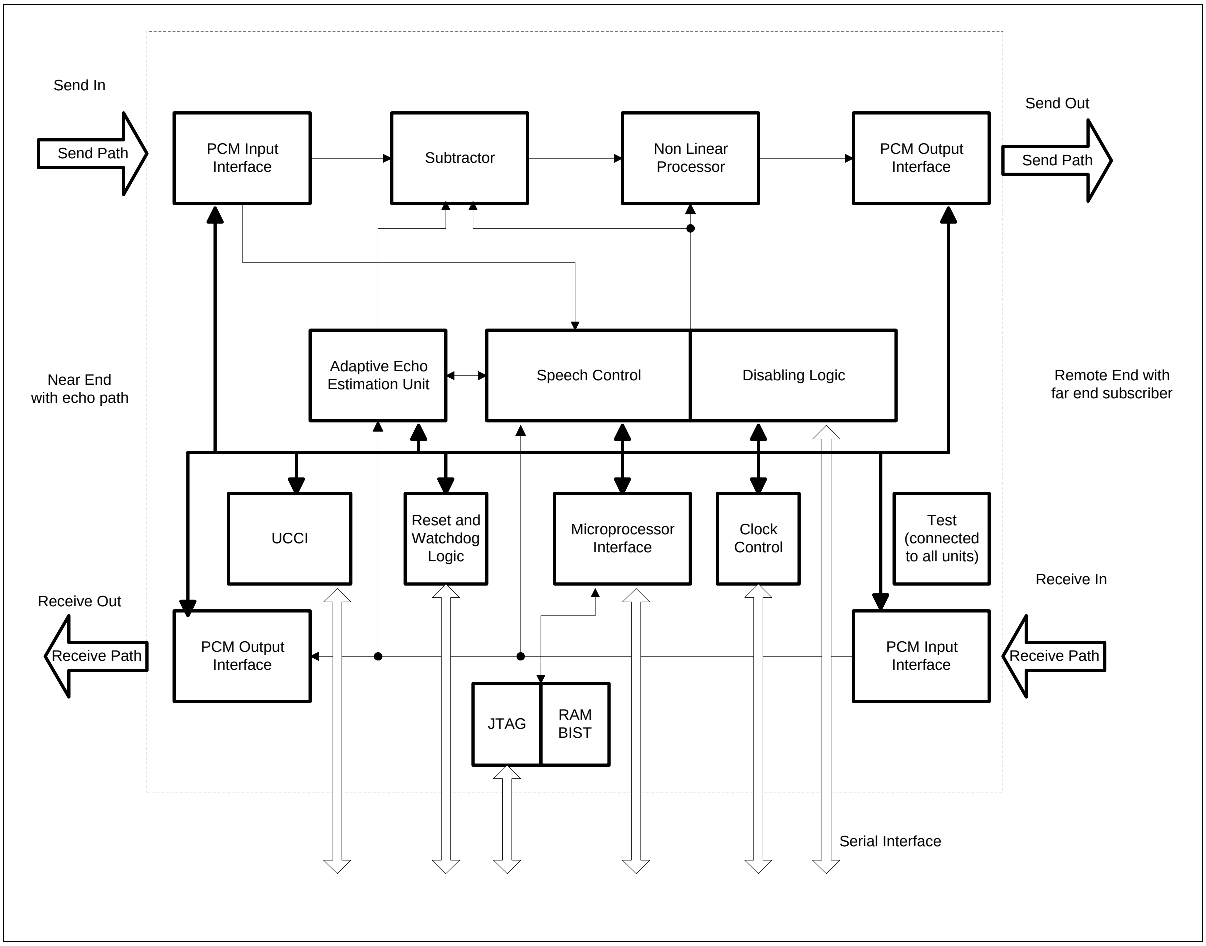

Figure 7 Block Diagram

The following paragraphs describe the functions of the SIDEC block diagramm shown in **Figure 7**.

3.1.1 Speech Control

The Speech Control analyzes the data from the PCM Input Interfaces and external inputs and supervises the functions of the other system components. As soon as the far end subscriber talks, the Adaptive Echo Estimation Unit is activated by the Speech Control. If the double talk condition is detected or a non speech signal with an adequate echo loss enhancement is identified by the Speech Control, the content of the Adaptive Echo Estimation Unit is frozen. Under specific circumstances a reset of the H-Register (described in Section **3.1.3**) of the Adaptive Echo Estimation Unit might be necessary. The H-Register reset signal is also provided by the Speech Control.

3.1.2 Disabling Logic

Upon request of the Speech Control and depending on external inputs the Disabling Logic disables the Non Linear Processor and/or the Subtractor or even the complete Echo Canceller.

If the Speech Control Unit detects, that one of the following conditions is applied to the Echo Canceller, it will disable the device via the Disabling Logic:

– Disabling via 2100 Hz tone without phase reversal
– Disabling via 2100 Hz tone with phase reversal
– Disabling via 2010 Hz continuity check
– Disabling via PCM timeslot 16 Bit a, b, c or d according to ITU G. 704
– Disabling via Idle channel detection.
– Disabling of individual channels via external interfaces (µP, serial and/or UCC interface)

3.1.3 Adaptive Echo Estimation Unit

The Adaptive Echo Estimation Unit contains for each 8 bit signal sampled at 8 kHz memory for 512 / 1024 byte. This is equivalent to 64 / 128 ms end echo path delay. Depending on the end echo path delay of 64 or 128 ms the Adaptive Echo Estimation Unit processes 32 or 16 channels simultaneously, respectively. The corresponding 32 / 16 H-Register for each channel representing the pulse response of the complete echo path are also stored in the Adaptive Echo Estimation Unit. This information simplifies the detection of double speech. A highly sophisticated and patented algorithm guarantees fast and stable convergence even in the presence of near end speech.

The Adaptive Echo Estimation Unit is connected to the Microprocessor Interface in order to configure parameters of the algorithm and to read the content of the H-Register.

3.1.4 PCM Input/Output Interface

Each PCM Input/Output Interface contains a delay element, that is adjustable for max 125 µs delay in 122 ns steps in order to align the corresponding PCM signal to the synchronizing pulse. Unless not bypassed, the delay from Receive In to Receive Out is fixed to one PCM Frame equivalent to 125 µs. The signal Multiframe Begin is delayed accordingly to the send path delay.

Encoder to convert A- or µ-Law PCM signals to linear, and decoder to convert linear PCM signals to A- or µ-Law allow for channelwise Law Conversion (transcoding).

Offset adjustment is implemented at the output of the canceller. The attenuation of 0 dB, 2.5 dB or 6 dB is programmable by a register. The use of this feature requires that the cancelling function for the corresponding timeslot is enabled.

The complete bypassing of individual timeslots and connections from and to the processor interface with the internal canceller is provided for testing of cancelling timeslots.

The least significant bit in the send path can be transmitted transparently to the output if the corresponding external pin TSIGM is activated (CAS bit robbing).

The block PCM Input/Output Interface provides time multiplexing/demultiplexing for 16 or 32 timeslots. (depending on configuration, see section above). In 128 ms echo end path mode the selection of timeslots at the input is assigned as follows:

– Master: Timeslot	0,1,2,3,	8,9,10,11,	16,17,18,19,	24,25,26,27
– Slave: Timeslot	4,5,6,7,	12,13,14,15,	20,21,22,23,	28,29,30,31

The PCM Input/Output Interfaces are connected to the Speech Control Unit, Disabling Logic and the Microprocessor Interface.

3.1.5 Subtractor

The subtractor calculates the difference between the signal from the PCM Send In Interface and the artificial echo provided by the Adaptive Echo Estimation Unit. The subtractor is controlled by the Speech Control.

3.1.6 Non Linear Processor

The Non Linear Processor (NLP) limits the residual echo if only far end talk is present. Three programmable functions are available:

- Block echo and background noise.
- Replace echo and background noise by comfort noise with the level of the determined background noise.
- Clip the level of the echo and the background noise to the level of the background noise. (Experiments show that most people prefer this configuration)

The NLP is controlled by the Disabling Logic and Speech Control.

3.1.7 Microprocessor Interface

The Microprocessor Interface can operate in Intel and Motorola Mode. It provides access to the internal configuration, control states and monitor registers.

3.1.8 Universal Control and Communication Interface

The UCC Interface is a serial hardware interface for SIDEC control and supervision by other boards via a Microprocessor. A special feature of the SIDEC-UCC Interface is, that certain controlling functions like the channelwise disabling or A/μ-Law conversion can be operated directly by the hardware without intervention of the microprocessor. This feature reduces the work load of the processor dramatically.

3.1.9 Watchdog Timer

A Watchdog timer is implemented to reset the on board processor if the software gets stuck in an undefined state as a result of a faulty operation. A reset condition is met if the microprocessor fails to write predefined values to the three watchdog registers in the correct sequence within 2 s. As long as the watchdog is active the SIDEC generates interrupts and/or reset pulses of 125 μs width with a period of 2 s.

3.1.10 Clock Control

The Clock Control supervises and generates all clock signals for proper operation of the ASIC hardware.

3.1.11 JTAG and RAM BIST

The JTAG (Joint Test Application Group) has been implemented according to IEEE 1149.1. A RAM BIST (Random Access Memory Built In Self Test) is also provided.

3.1.12 Test

The Test Unit controls the background test on disabled channels. A built in self test is used for testing internal RAMs. This test can be activated after switching on the supply voltage. The test unit also supervises the Clock Control Unit.

A notebook register allows the check of the μP Interface.

Within the Test Unit the registers for background testing of idling channels are implemented. In this test a pattern is input in the idling channel at Receive in and Send in and evaluated at the Send out port.

During normal operation the Test Unit supervises functions such as read out of levels, internal states and coefficients.

3.2 Description of Functional Features

3.2.1 Channelwise and Global A- and μ-Law Conversion

The SIDEC allows channel individual conversion. **Figure 8** depicts the implementation of the different options for the A- to μ- or μ– to A-Law conversion. Depending on the requirements of the application two settings can be configured: Either global or channel individual law conversion.

Global A- to μ– and μ– to A-Law conversion:

If this modus is chosen by setting CONFLAW.CHIND='0' all 32 PCM channels are converted according to the settings of GALAWFE for the far end and GALAWNE for the near end. A '1' in GALAWFE and GALAWNE indicates that A-Law is used for the corresponding end. A '0' indicates usage of μ-Law. The conversion can be disabled channel individually by setting the CHCTRL0-31.CONVDIS = '1' via software. Law decoding/encoding is then carried out according to GCONVDISLAW. To activate the serial control signal and the UCC interface as disabling source for the PCM law conversion the bits CHCTRL0-31.ENPCTRL must be set to '0'.

Channel individual A- to μ- and μ- to A-Law conversion:

For channel individual conversion the user can configure independently for each channel whether A- to μ-, μ- to A- or no Law conversion is selected via setting IALAWNE for the near end and IALAWFE for the far end with the corresponding value for A- or μ-Law. The conversion can be disabled channel individually by setting the CHCTRL0-31.CONVDIS = '1' via software. Law decoding/encoding is then carried out according to CHCTRL0-31.CONVDISLAW. To activate the serial control signal and the UCC interface as disabling source for the PCM law conversion the bits CHCTRL0-31.ENPCTRL must be set to '0'.

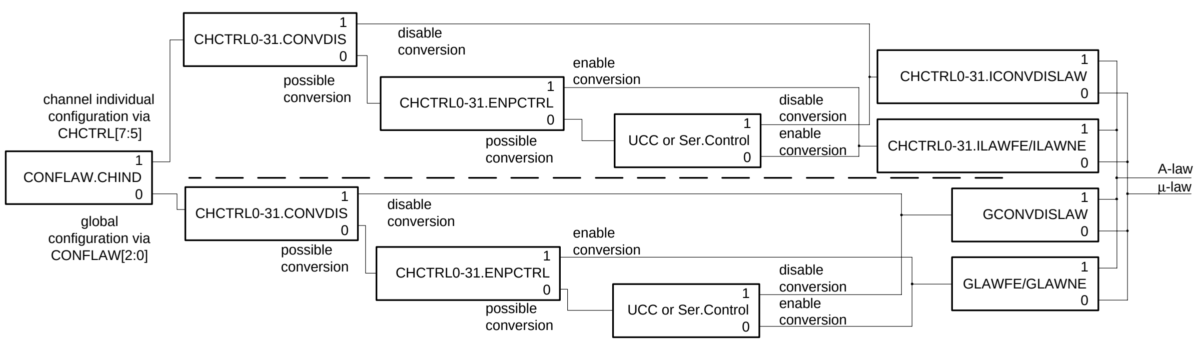

Figure 8 Explanation of Options for A- and μ-Law Conversion

3.2.2 Bypass and Disabling Functions

Figure 9 depicts the bypass and disabling functions of the SIDEC. They can be configured via UCC, Serial and µP Interface.

Setting NLPDIS =’1’ (pin or register setting) leads to bypassing of the Non Linear Processor.

Setting BYPASS = ’1’ (Serial control signal, UCC or 2100 Hz tone via register settings) results in bypassing the Attenuator in the Receive Path as well as in bypassing the Subtractor, the Non Linear Processor and the Attenuator in the Send Path.

Disabling a channel or the complete canceller will result in a BYPASS function, a H-Register reset and a reset of the Speech Control Unit. A bypassed or disabled channel of the SIDEC can still be converted from A/µ- Law or vice versa.

If a Modem call is detected the user can define what action is related to the detection of a Modem call (2100 Hz with phase reversal or without reversal): bypassing, NLP bypassing, H-Register Reset or combination of the functions.

The 64 Clear mode is activated by bypassing and defining the same Law Conversion at near end and far end. In 64 Clear mode the signal is still passed through the frame alignment.

For testing purposes the canceller can be completly bypassed by setting SBYPASS and RBYPASS.

The Receive out signal can be input directly to the Send In port by setting the RSLOOP =’1’. The Send out signal can be input directly to the Receive in port by setting the SRLOOP =’1’. If both loops are configured only RSLOOP will be enabled in the SIDEC.

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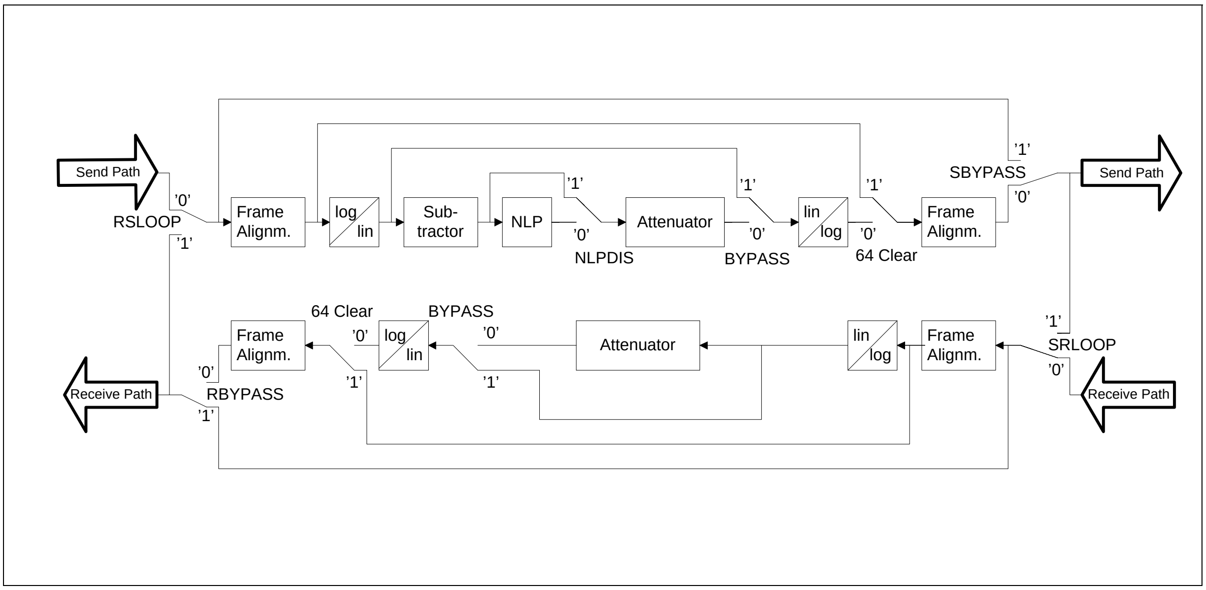

Figure 9 Bypass and Disabling Functions of the SIDEC

3.2.3 UCC Interface

The UCC Interface uses a clock frequency of 2048 kHz. The UCC Signal is structured into frames (period 125 µs) consisting of 32 channels (period 3.9 µs) and a multiframe consisting of 32 frames (period 4 ms). The multiframe is synchronized with the SYNCI Input pulse. The SIDEC reads and writes (tristate controlled) only the channels 0 of the frames. The 32 channels 0 of each multiframe are used to control and supervise the associated PCM channels. UCC Frame 0 corresponds to PCM channel 0, UCC Frame 1 corresponds to PCM channel 1, ... This relation is depicted in **Figure 10**. It is also possible to use one special UCC-Frame for a general purpose. With the registers UCCMFR, UCCALIGN and PHALIGN[7:6] the UCC channel 0 of frame 0 can be shifted to any channel and frame. Hence, up to 32 different devices can be connected in parallel to the UCC Interface.

The output signal UCCO is always in phase with the UCCI input signal.

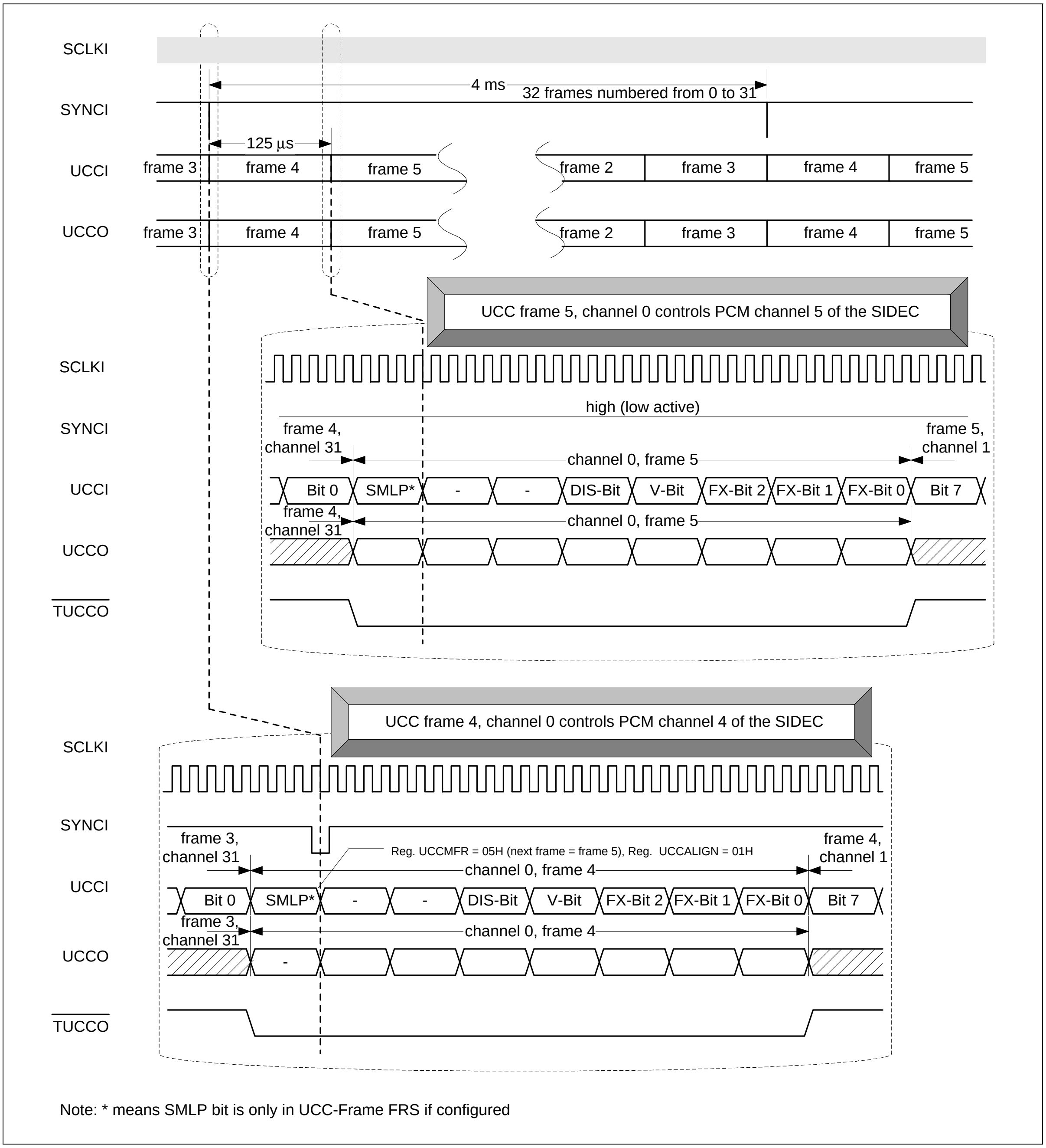

Figure 10 UCC Signal for control of PCM Signal

4 Operational Description

4.1 Pin Connection Diagram for SIDEC

Figure 11 illustrates an example for the pin connection of the SIDEC to an E1/T1 IC and to an interworking element IC.

The SIDEC is used to cancel the echo on the side of the FALC PEB 2254 or FALC-LH PEB 2255 which is the near end in this case. There are two SIEMENS products in this Inter working unit connected to the SIDEC. The FALC serves as a frame and line interface component whereas the IWE8 PEB 4220 operates as an interworking element. For multiframe alignment in the IWE8, FRMFBX must have a correct timing relation to FRDATX. For this purpose the SIDEC adjusts the delay from the TMFBI input to the TMFBO output to the delay of the SI input to the SO output. For the support of the CAS-BR transparency the SIDEC passes the robbed bits that are indicated by the FALC via the TSIGM input directly through to the SO output by overwriting the computed value of the robbed bit with the value of the SI input.

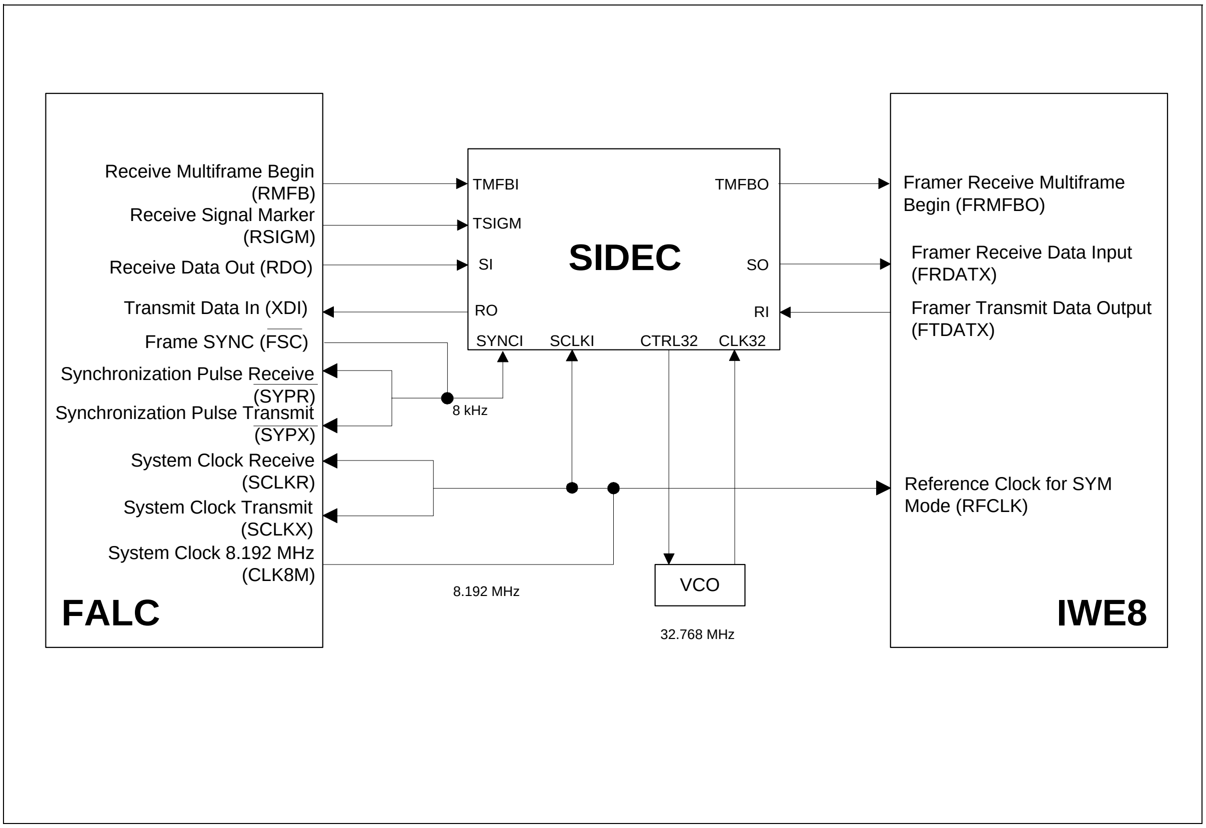

Figure 11 Internet Working Unit: SIDEC between a FALC and IWE8

4.2 Synchronization and Clock Modes

The SIDEC can be connected in different synchronization and clock modes. These modes can be used for several applications.

Basically there are two clock modes, slave and master clock mode (not to be mixed up with 128 ms master and slave mode). The internal clock system in master clock mode is automatically synchronized to the system clock by using an external 32.768 MHz VCO or by generating and deriving the system clock at output pin SCLKO directly from the CLK32 input. SIDEC in master clock mode provides a synchronization pulse at pin SDECO. This pulse can be used by a SIDEC in slave clock mode to synchronize its internal clock system to the system clock without the needs for additional external VCO.

Examples for this mode are the 128 ms delay application and the multiple SIDEC application, see also **Figure 16** and **Figure 17**.

CLK4O is 4.096 MHz system clock output for subsequent circuits, derived from SCLKI.

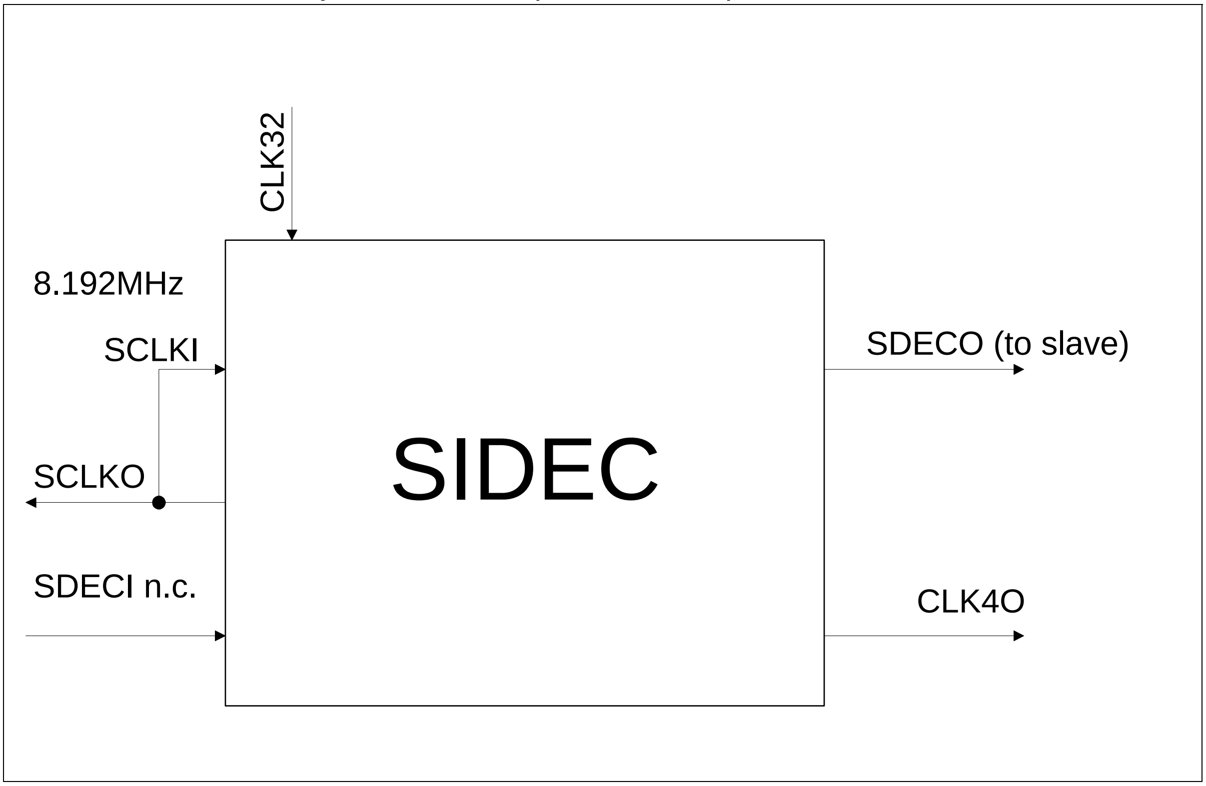

Figure 12 Master Clock Mode with External 32.768 MHz Clock without 8.192 MHz System Clock Input

In **Figure 12** the system clock is reconnected from SCLKO to SCLKI in order to properly process the PCM signals. The system clock at pin SCLKO can also be provided for other devices. The SDECI pin is not connected in the master clock mode. A 32.768 MHz clock has to be provided by an external clock oscillator or other clock source on the system.

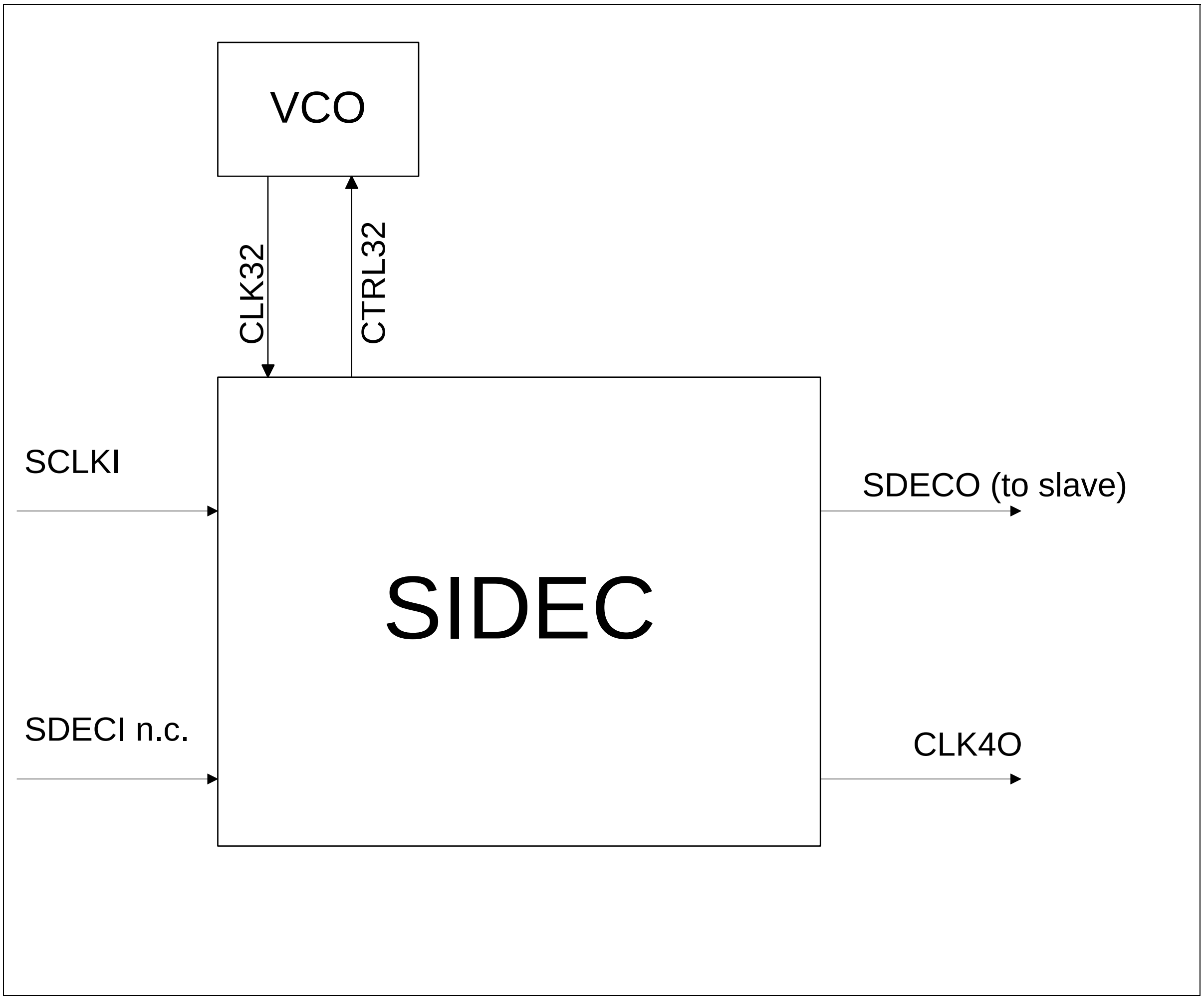

Figure 13 Master Clock Mode with External 8.192 MHz Clock

In the master clock mode with 8.192 MHz clock (**Figure 13**), the 32.768 MHz operating clock is supplied by the VCO. The SIDEC provides a controlling voltage for the VCO in order to synchronize the CLK32 to the system clock SCLKI.

SDECI is not connected and the SDECO can be connected to other SIDECs.

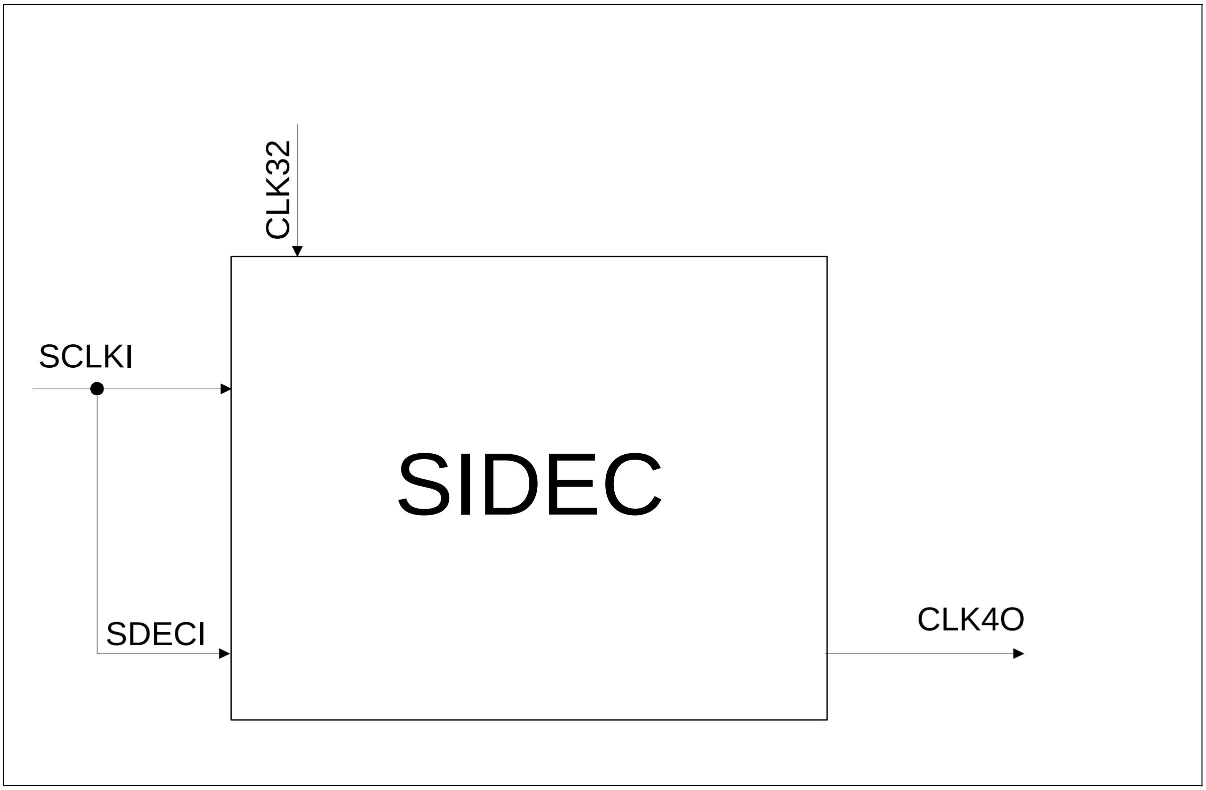

Figure 14 Slave Clock Mode with External 8.192 MHz and 32.768 MHz

In the slave clock mode the 8.192 MHz and the 32.768 MHz clock have to be synchronous and phase aligned (e.g. SCLKI has been derived from CLK32 by some external device). There is no internal synchronization between SCLKI and CLK32. SDECI is needed for correct phase alignment of SCLKI to the internal system clock.

CLK4O is a 4.096 MHz system clock output for subsequent circuits, derived from SCLKI

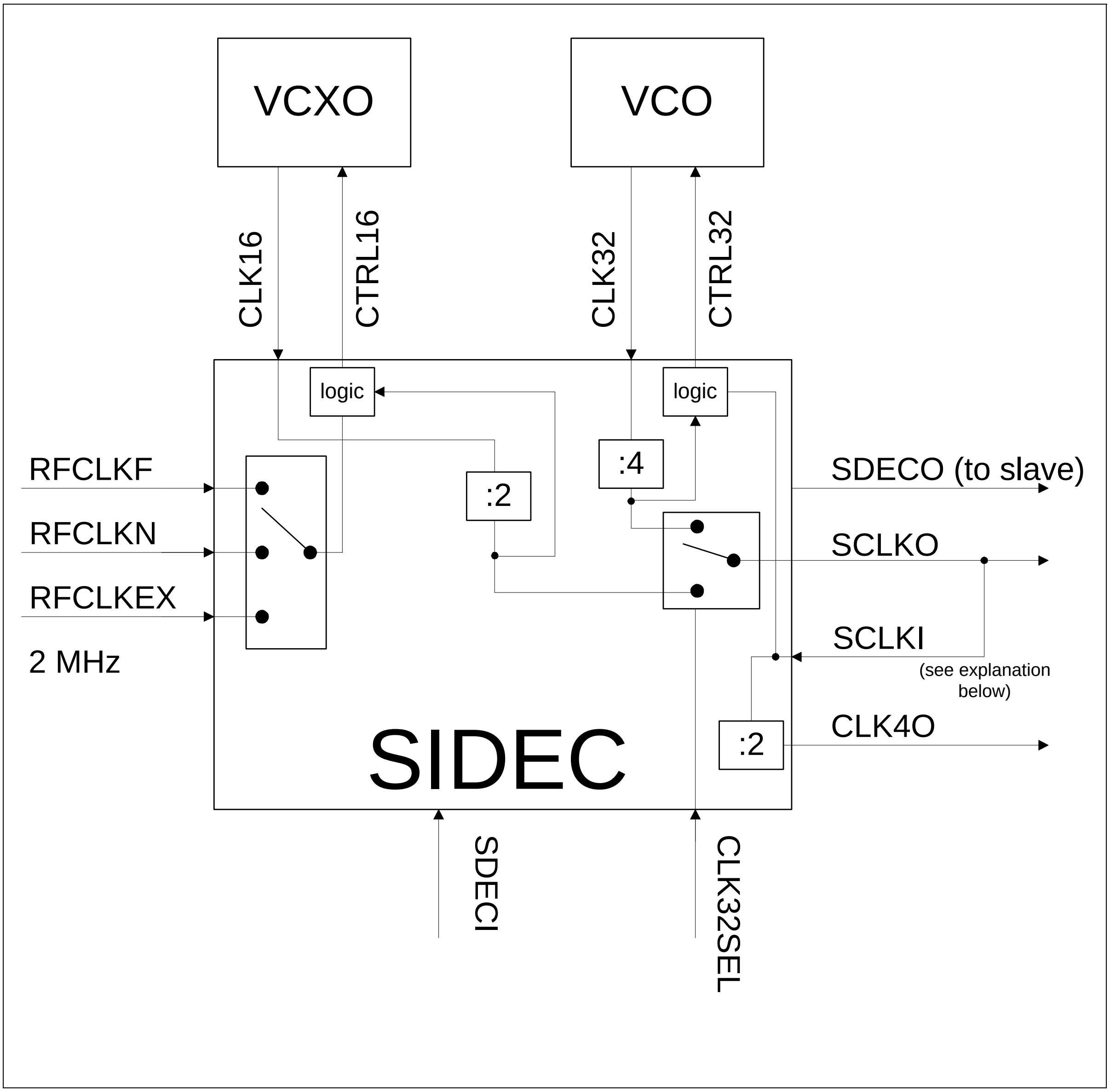

Figure 15 Reference Clock Mode with 2.048 MHz

In this mode a 2.048 MHz system clock is provided at either the RFCLKF, RFCLKN or the RFCLKEX pin. The VCXO and VCO supply the operating clocks for the SIDEC. SDECO can be connected to slave. The feedback from SCLKO to SCLKI in order to generate a control voltage for the 32 MHz VCO makes only sense if SCLKO is derived from CLK16. The SDECI initializes the counter.

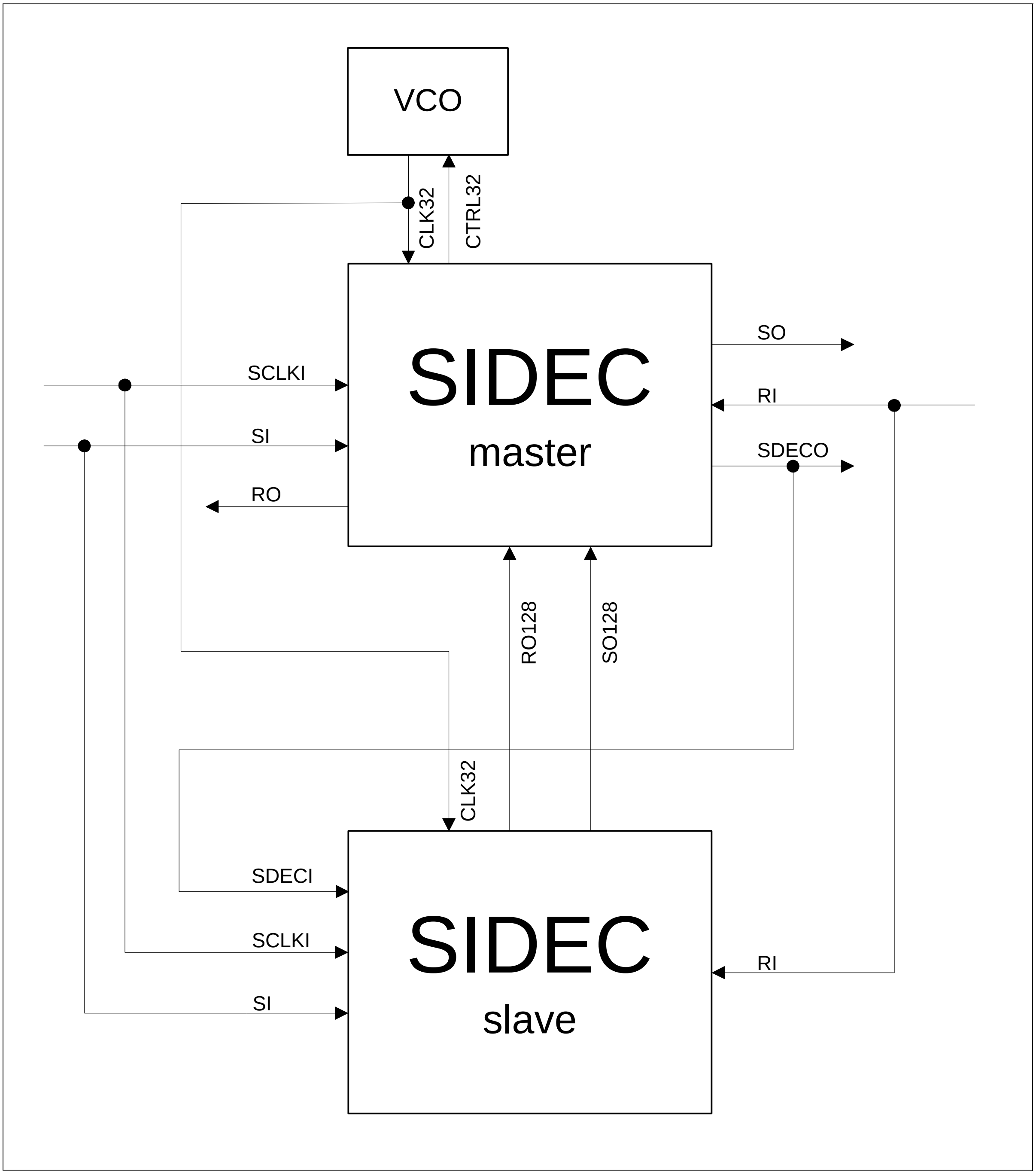

Figure 16 128 ms Delay Mode

The pin connection of a 128 ms master and slave SIDEC is shown in **Figure 16**. The SI and RI is supplied to both SIDECs. The RO and SO is provided by the master. The RO128 and SO128 signals are used to multiplex the 128 ms slave data into the PCM data stream outputs of the master.

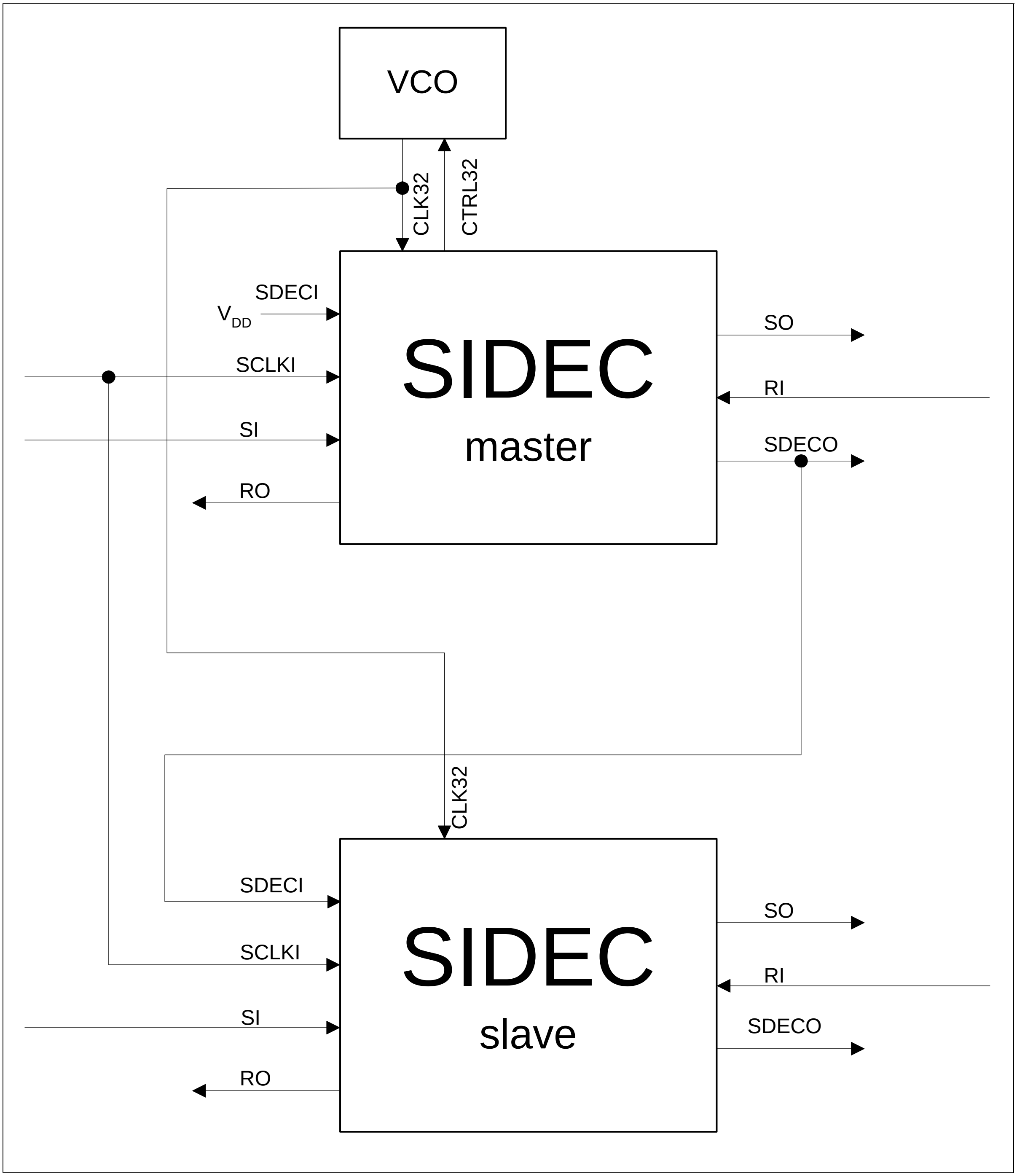

Figure 17 Multiple SIDEC

In multiple SIDEC mode the output SDECO of the clock master SIDEC is used to synchronize clock slave SIDECs to the system clock. In this application multiple E1/T1 lines can be echo cancelled, one E1/T1 line per SIDEC. Leave the SDECI of the master SIDEC open or connect it to ground.

4.3 Timing Patterns

4.3.1 Clock Timing

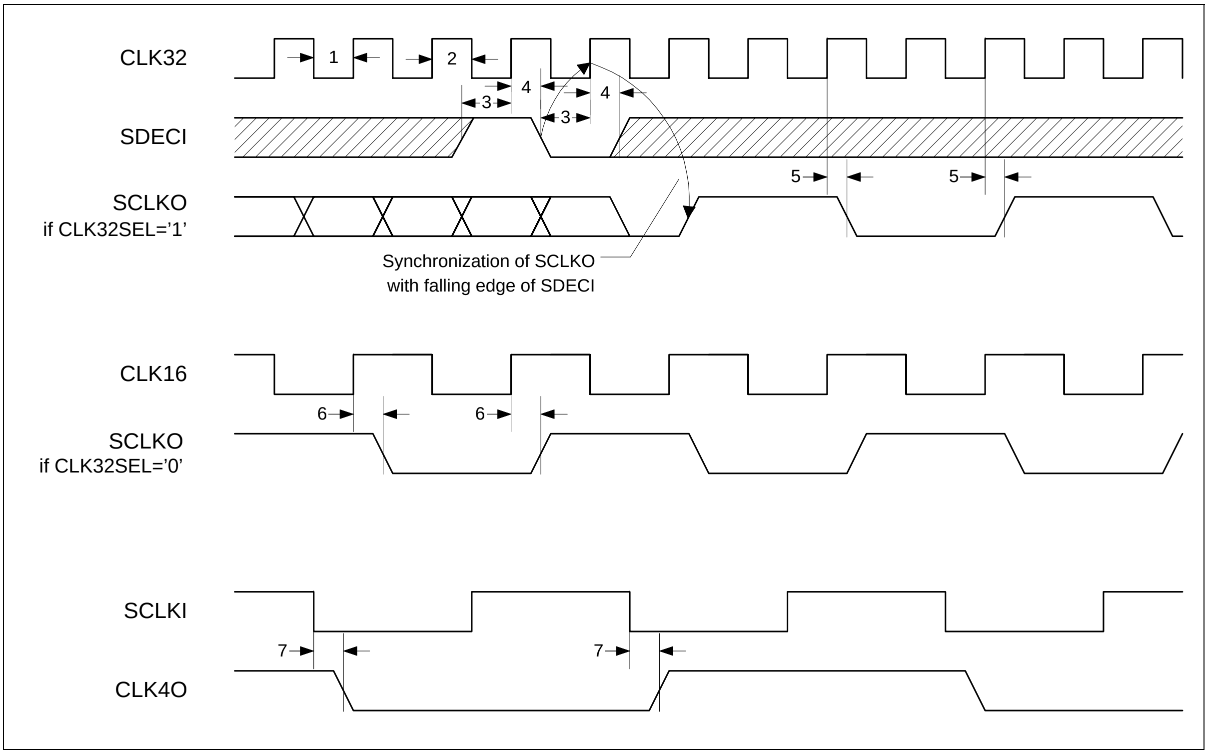

Figure 18 Clock Timing

Table 12 Clock Timing Characteristics (preliminary)

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_clk32_low	CLK32 low time	12		ns
2	t_clk32_high	CLK32 high time	12		ns
3	t_sdeci_setup	SDECI setup time before CLK32 ↑	10		ns
4	t_sdeci_hold	SDECI hold time after CLK 32 ↑	15		ns
5	t_sclko_delay_clk32	SCLKO output delay after CLK32 ↑		30	ns

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
6	t_sclko_delay_clk16	SCLKO output delay after CLK16 ↑	0	30	ns
7	t_clk4o_delay	CLK4O output delay after SCLKI ↓	0	30	ns

Table 13 Periods of Clock Signals

No.	Parameter	min.	nom.	Unit
	CLK32	30	30.52	ns
	CLK16		61.04	ns
	SCLKI		122.07	ns
	CLK4O		244.14	ns

4.3.2 PCM Signal Timing and Frame Alignment

The SIDEC requires the MSB (bit7) first and the LSB (bit0) last as input

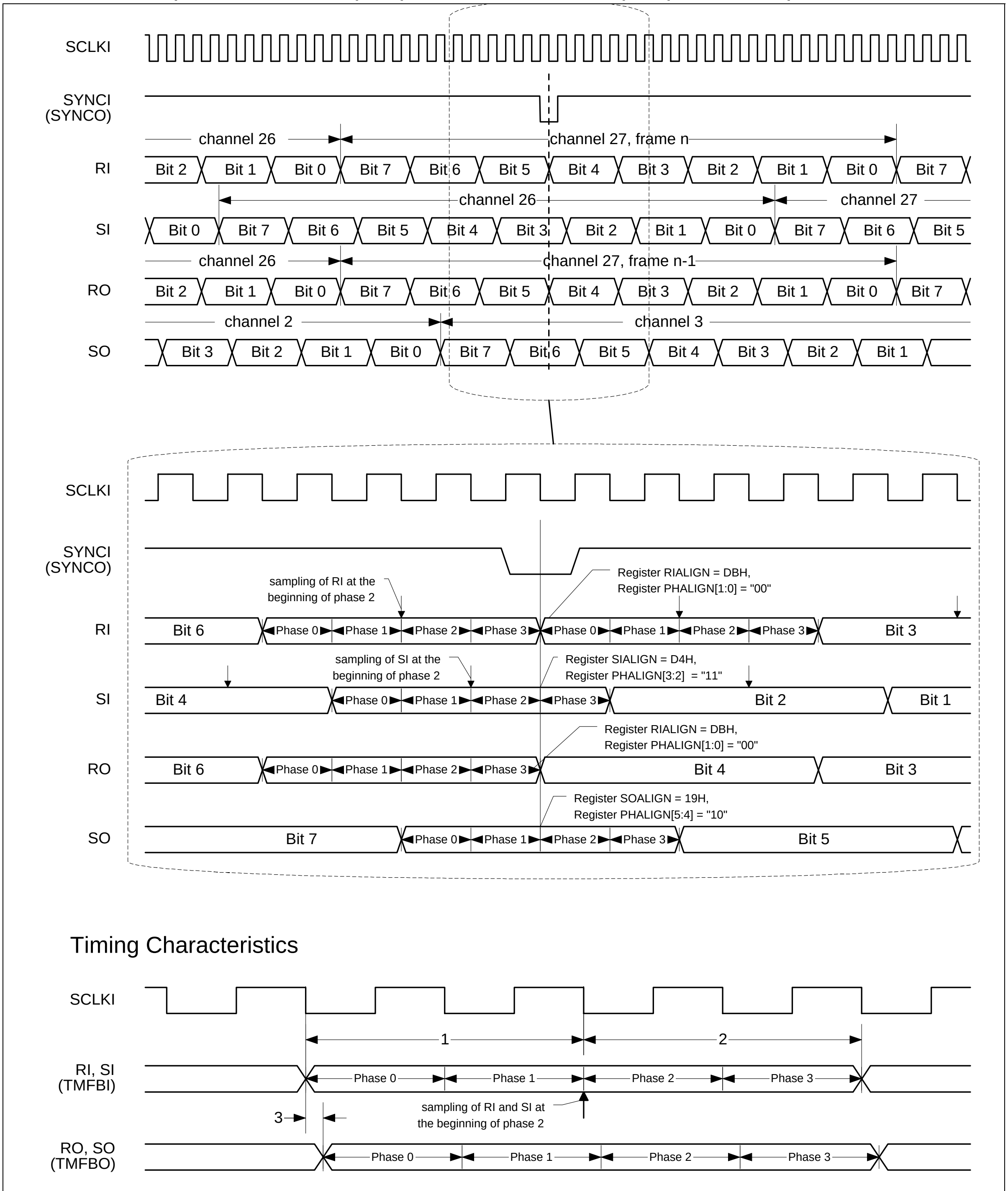

Figure 19 PCM Signal Timing and Frame Alignment

Note: Above values are examples only. PCM frame alignment with respect to the first detection of an active SYNCI (or SYNCO: If no SYNCI is applied, SYNCO takes over the part and role of SYNCI) with the falling edge of SCLKI can be configured by writing to the registers RIALIGN, SIALIGN an SOALIGN. For finer adjustments, the valid bit phase of the PCM signals at the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the register PHALIGN. The configured frame and bit phase alignment always denotes the beginning of the ideal bit phase (no signal delay) at the falling edge of SCLKI.

PCM inputs are always sampled with the falling edge of SCLKI at the beginning of bit phase 2, outputs are clocked with the falling edge of SCLKI at the beginning of bit phase 0. Unless not bypased the PCM output RO has a fixed delay of one PCM frame (125 µs) with respect to RI.

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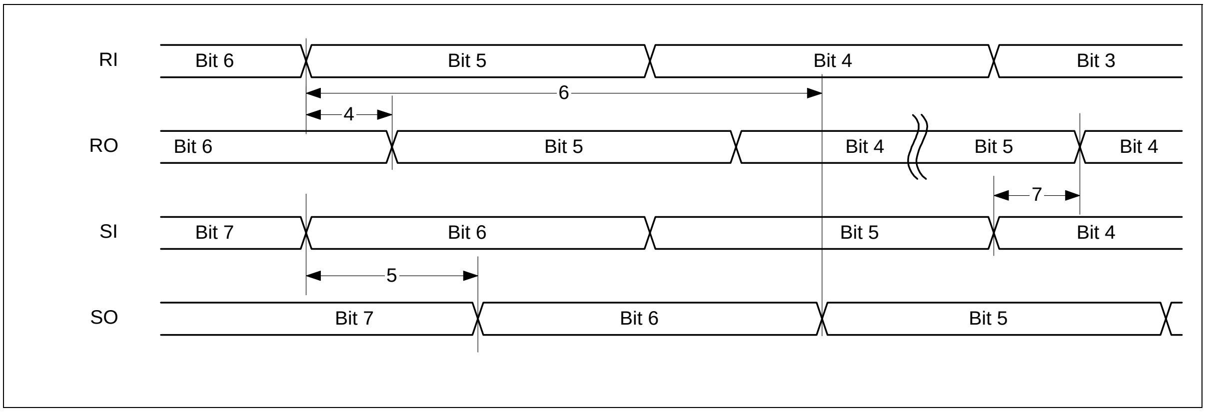

Figure 20 Delay of PCM Signals

Figure 21 illustrates the synchronization of the 2048 kBit/s PCM and UCC signal for a low active SYNCI signal with respect to the internal 8192 kHz SCLKI signal. If SYNCI is sampled with the falling edge of SCLKI (CONFCC.SSCLKEDGE='0') this edge is the synchronization point for PCM and UCC signals. If SYNCI is sampled with the rising edge of SCLKI (CONFCC.SSCLKEDGE='1') the next falling SCLKI edge is the synchronization point for PCM and UCC signals. The SYNCO signal may only be used instead of the SYNCI signal if the UCC Interface is not used

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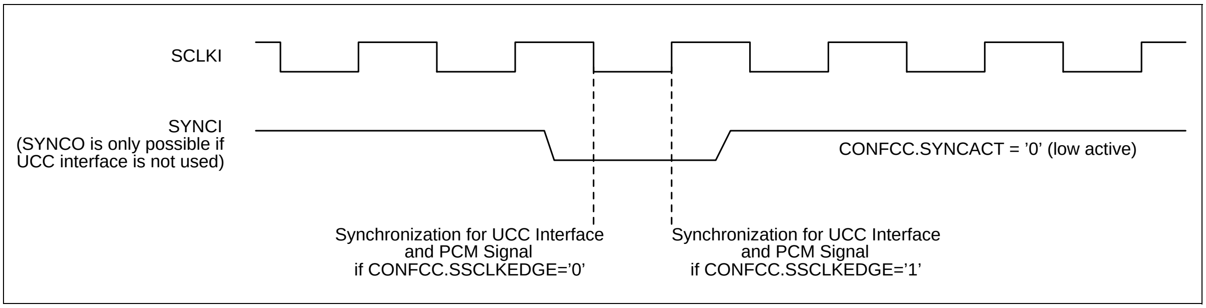

Figure 21 Synchronization of PCM and UCC Signal with respect to SCLKI and SYNCI

Table 14 PCM Signal Timing and Frame Characteristics (preliminary)

No.		Parameter	Limit Values		Unit
			min.	max.	
1	t_pcm_setup	PCM input (RI,SI) input setup time before sampling with SCLKI ↓	15		ns
2	t_pcm_hold	PCM input (RI,SI) input hold time after sampling with SCLKI ↓	15		ns
3	t_pcm_delay	PCM output (RO,SO) delay after SCLKI ↓	0	30	ns
4	t_pcm_ri2ro_delay	delay for bypass RI to RO	0	30	ns
5	t_pcm_si2so_delay	delay for bybass SI to SO	0	30	ns
6	t_pcm_ri2so_delay	delay for bypass RI to SO	0	30	ns
7	t_pcm_si2ro_delay	delay for bypass SI to RO	0	30	ns

4.3.3 Timing of SYNCI and SYNCO

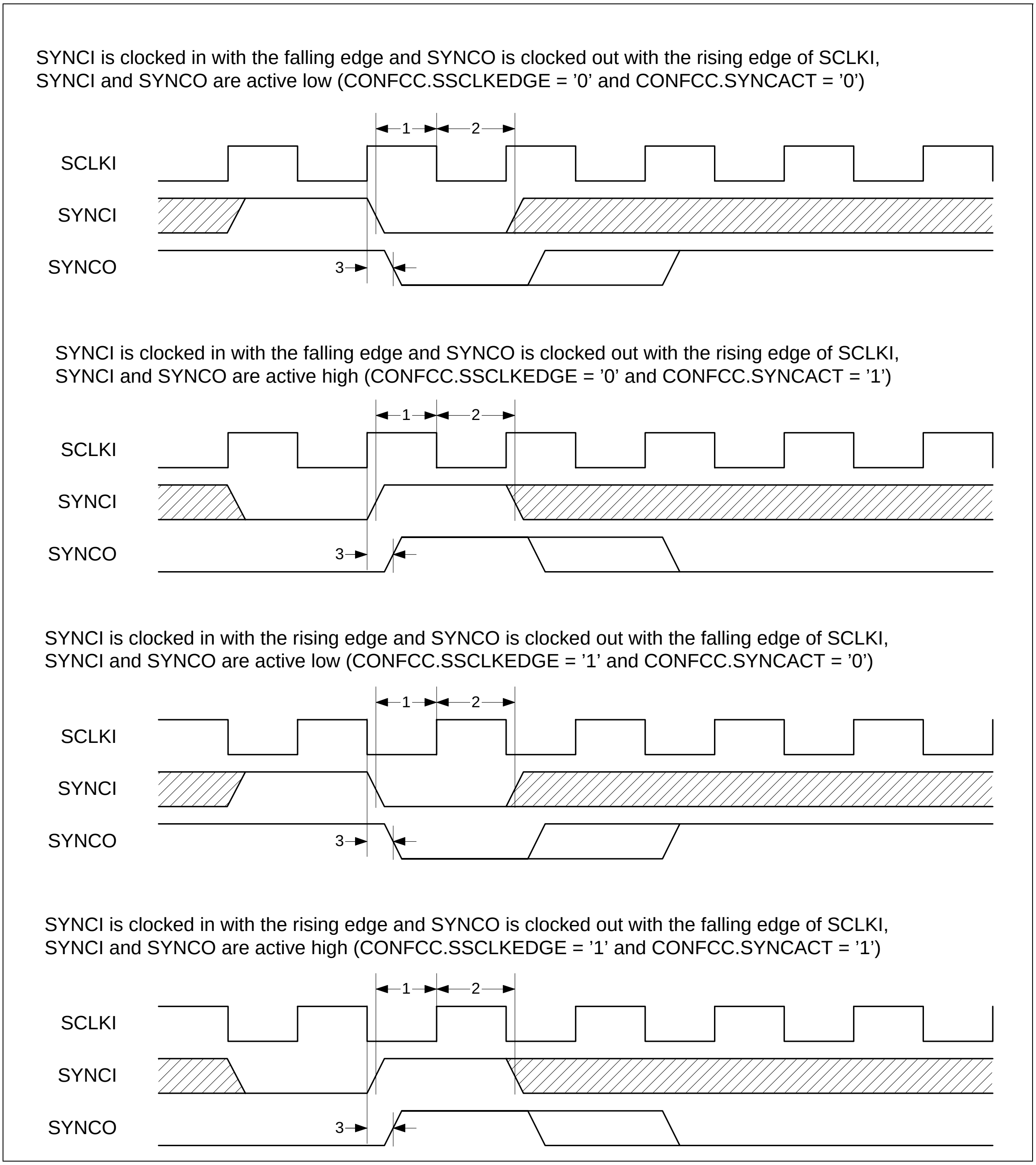

Figure 22 Timing of SYNCI and SYNCO

Figure 22 shows the timing of the synchronization pulses for different configurations.

Note: The duration of SYNCO pulse can be configured by register CONFCC.SYNCODUR to either one or two SCLKI (8.192 MHz) periods.

Table 15 Characteristics of Timing of SYNCI and SYNCO (preliminary)

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_synci_setup	SYNCI setup time before active sampling edge of SCLKI	10		ns
2	t_synci_hold	SYNCI hold time after active sampling edge of SCLKI	10		ns
3	t_synco_delay	SYNCO delay after active output edge of SCLKI	0	30	ns

4.3.4 Clock Timing within External VCO Capture Range

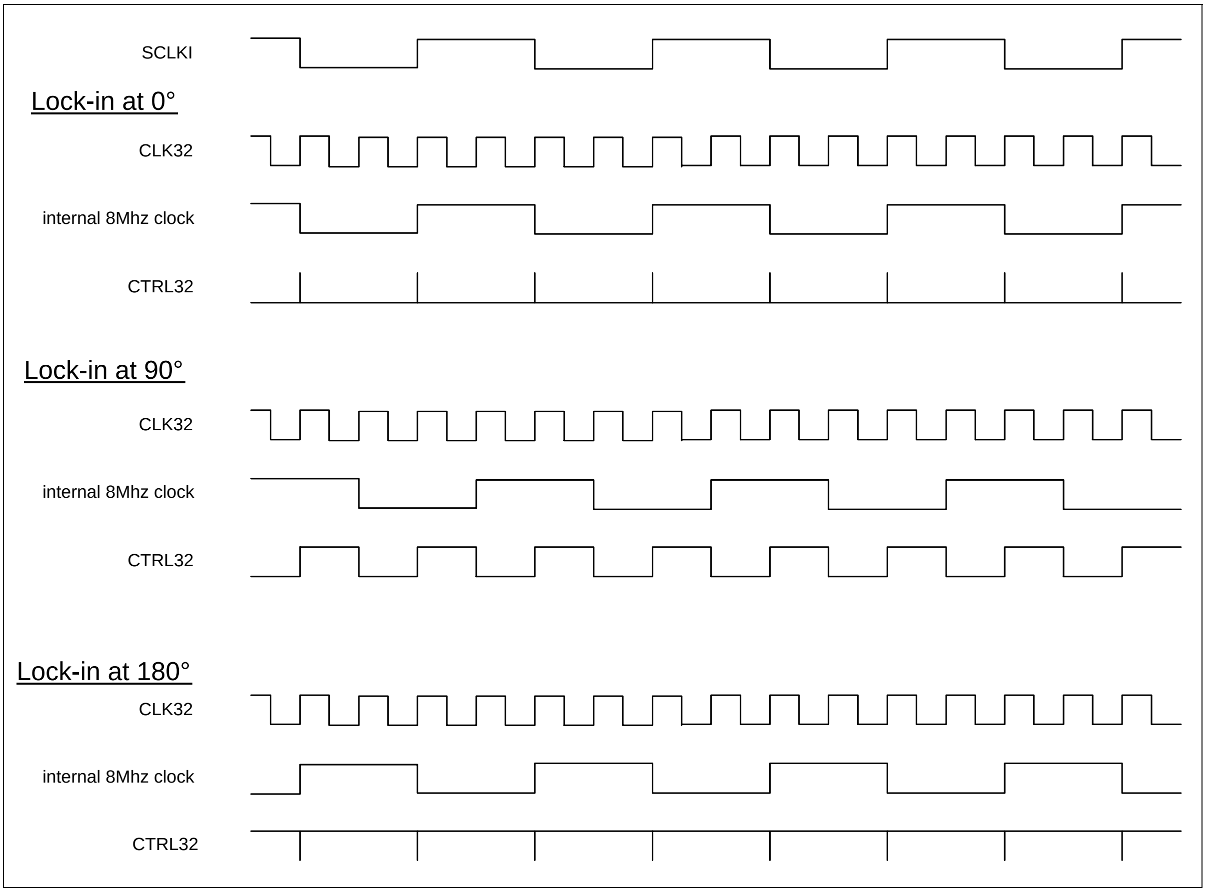

Figure 23 Clock Timing within External VCO Capture Range

In case a 32.768 MHz clock has to be generated and synchronized to the system clock at SCLKI, the signal at pin CTRL32 can be used to control an external VCO. The output at CTRL32 is the signal at SCLKI that is internally 'xored' with an internal 8.192 MHz clock that is derived from the signal pin CLK32 by division by 4. For proper operation of the SIDEC the system clock SCLKI and the internal 8.192 MHz clock must lock in within the capture range from 0° to 180°. CTRL32 can be inverted by bit CONFCC.INVCTRL32 for use of VCOs that increase the frequency with falling voltage.

The internal 8.192 MHz clock can be monitored at pin SCLKO with a delay of three CLK32 periods plus internal signal delay if pin CLK32SEL is set to logic '1'.

4.3.5 Serial Interface (Controlling and Monitoring) Timing

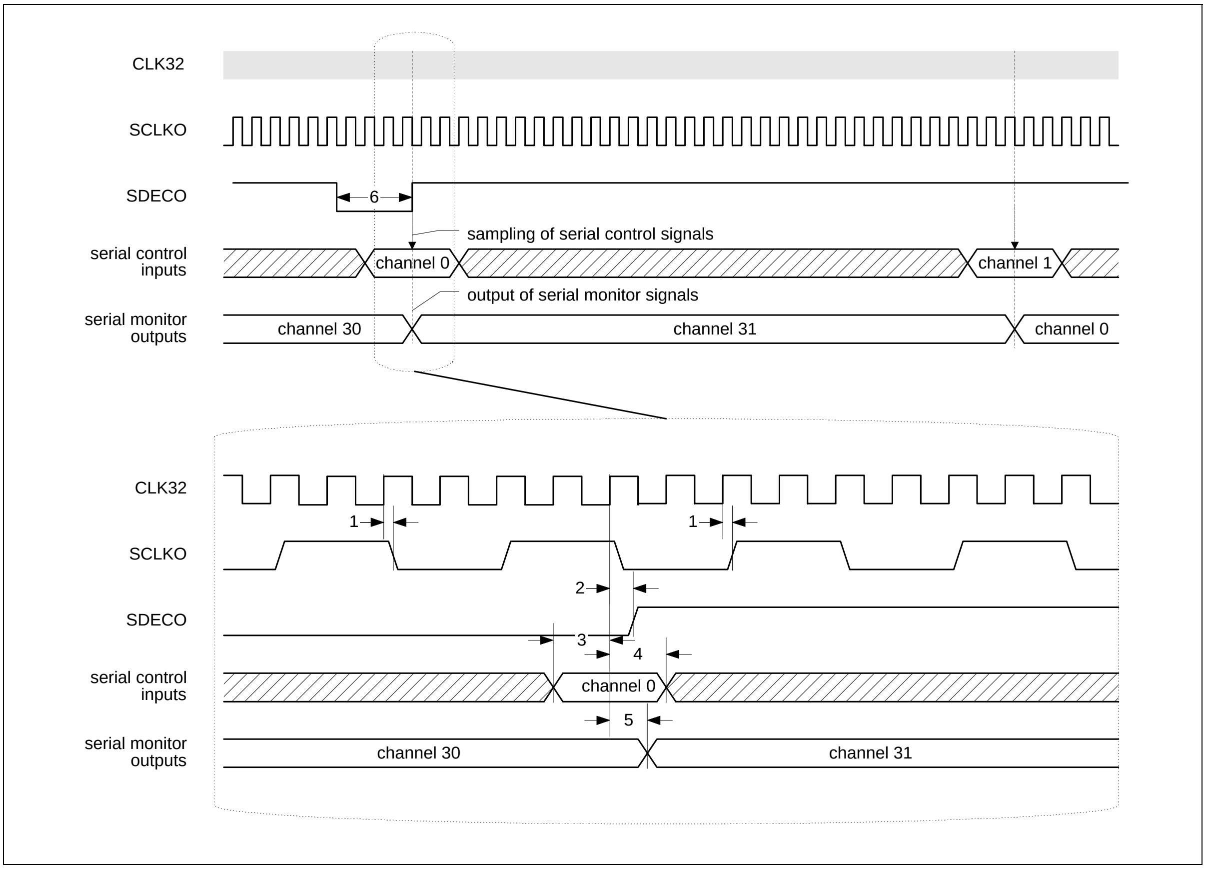

Figure 24 Serial Interface (Controlling and Monitoring) Timing

Table 16 Serial Interface (Controlling and Monitoring) Timing (preliminary)

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_sdeco_delay	SDECO output delay after CLK32 ↑	0	30	ns
2	t_sctr_setup	Serial control signal setup time before sampling with CLK32 ↑	15		ns
3	t_sctr_hold	Serial control signal hold time after sampling with CLK32 ↑	15		ns

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
4	t_smon_delay	Serial monitor signal output delay after CLK32 ↑	0	30	ns
5		SDECO duration	16 * CLK32 period		

4.3.6 UCC Interface Signal Timing and Frame Alignment

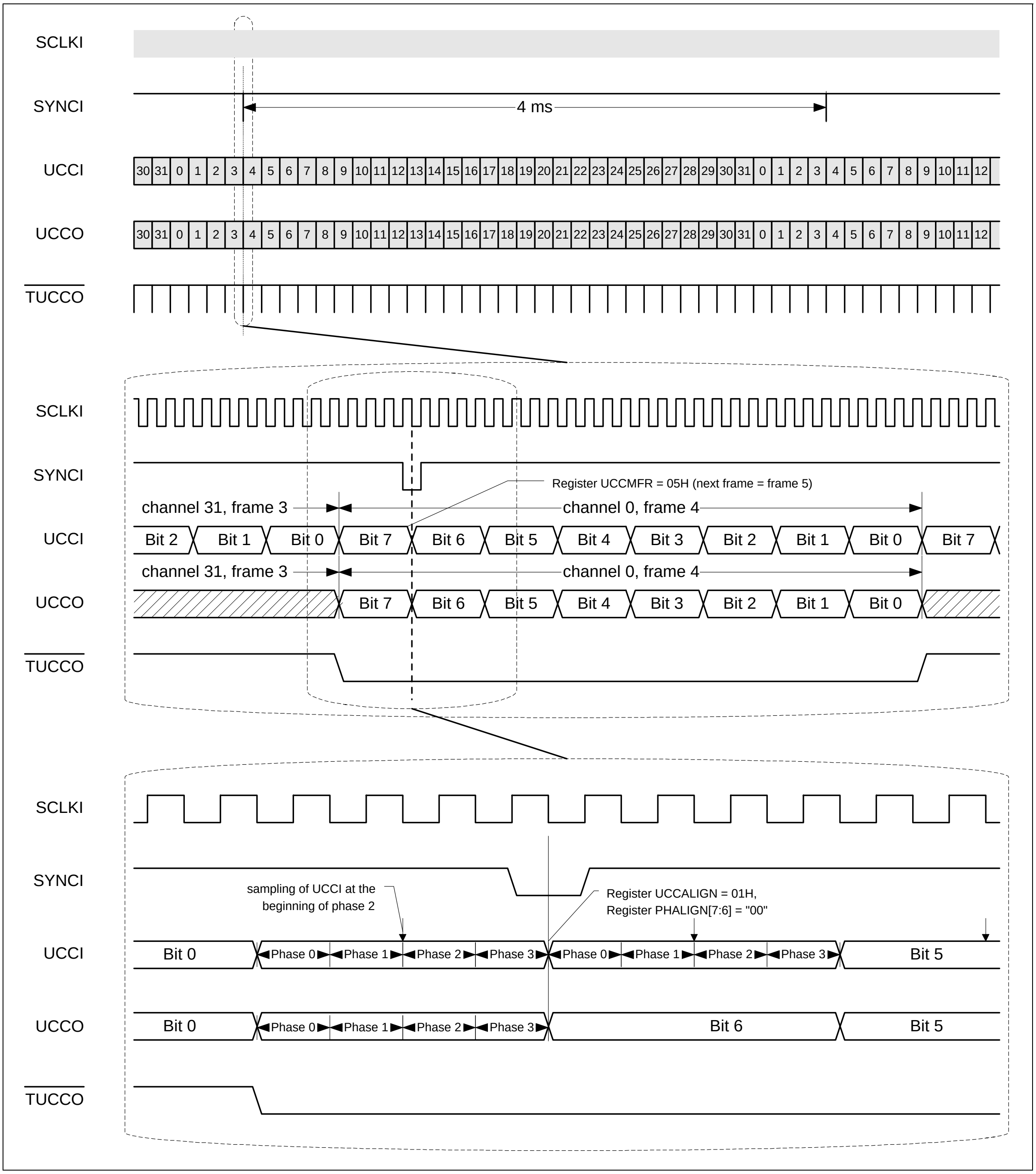

Figure 25 UCC Interface Signal Timing and Frame Alignment

Note: Above values are examples only. For the use of the UCC Interface a SYNCI signal with a period of 4 ms (equivalent to one multiframe) must be applied to the SIDEC. UCC frame and multiframe alignment with respect to the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the registers UCCALIGN and UCCMFR. For finer adjustments, the valid bit phase of the UCC signals at the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the two MSBs of register PHALIGN.

The configured frame and bit phase alignment always denotes the beginning of the ideal bit phase (no signal delay) at the falling edge of SCLKI. If SYNCI is sampled with the falling edge of SCLKI (CONFCC.SSCLKEDGE=’0’) this edge is the synchronization point for PCM and UCC signals. If SYNCI is sampled with the rising edge of SCLKI (CONFCC.SSCLKEDGE=’1’) the next falling SCLKI edge is the synchronization point for PCM and UCC signals. This behavior is identical to the PCM signal behavior and illustrated in **Figure 21** in **Chapter 4.3.2**

UCC inputs are always sampled with the falling edge of SCLKI at the beginning of bit phase 2, UCCO and $\overline{\text{TUCCO}}$ are clocked out with the falling edge of SCLKI at the beginning of bit phase 0. The value of register UCCMFR denotes the frame number of the next complete frame that starts with phase 0, bit 7, channel 0 **after** the first detection of an active SYNCI with the falling edge of SCLKI (see figure below).

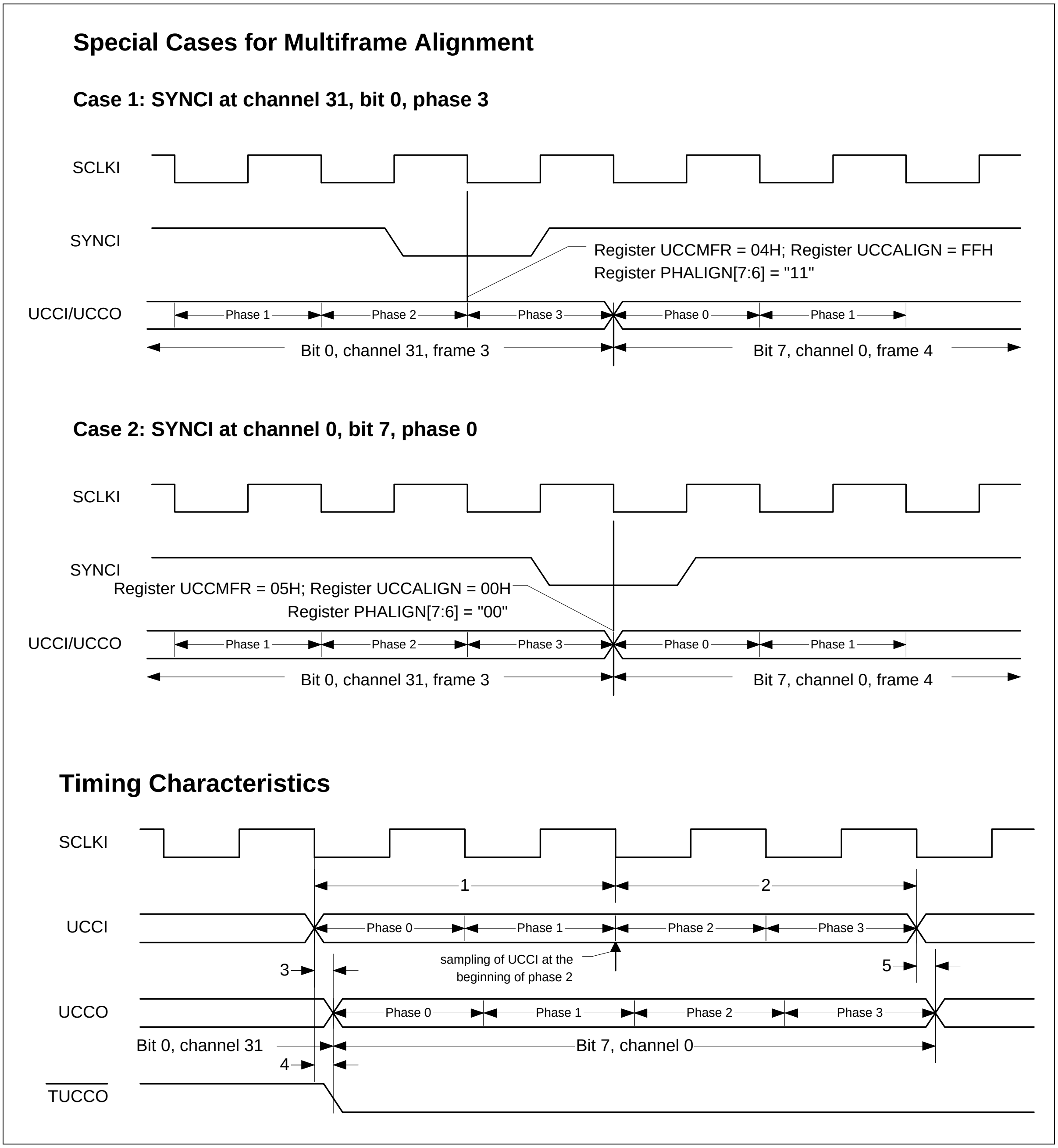

Figure 26 Special Cases for Multiframe Alignment and Timing Characteristics

Table 17 UCC Interface Signal Timing and Frame Alignment (preliminary)

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_ucci_setup	UCCI input setup time before sampling with SCLKI ↓	15		ns
2	t_ucci_hold	UCCI input hold time after sampling with SCLKI ↓	15		ns
3	t_ucco_delay	UCCO output delay after SCLKI ↓	0	30	ns
4	t_tucco_delay	$\overline{\text{TUCCO}}$ output delay after SCLKI ↓	0	30	ns
5	t_ucc_reflect_delay	Propagation delay from UCCI to UCCO for UCC reflect mode	0	30	ns

4.3.7 Speech Highway Control Signals for CAS in T1 Systems

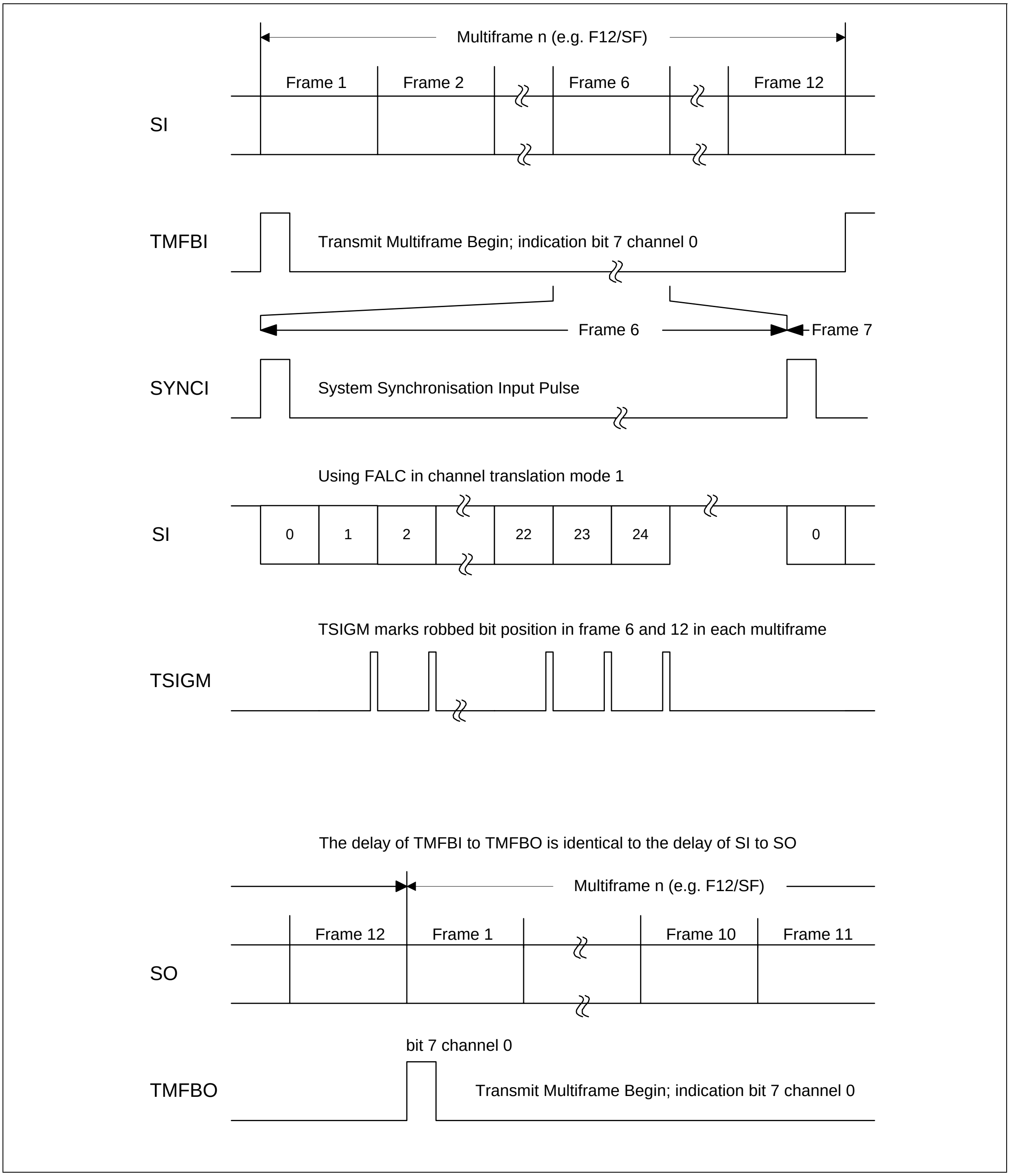

Figure 27 Timing of Supporting signals for CAS-BR Applications

4.3.8 Microprocessor Interface

The SIDEC Microprocessor Interface supports both, SIEMENS/Intel and Motorola mode. In each mode the address can be provided either through the multiplexed address/data or a parallel address bus. In multiplexed mode the address is always sampled with the falling edge of the address latch enable signal on the lower 7 bits of the multiplexed address/data bus. hence, adresses from 00H to 7FH are possible.

Read and write access in Intel mode is controlled by the assigned read and write signals. In Motorola mode it is provided by the data strobe and read/write signal.

The chip select signal is internally simply ’ored’ with the read and write signal in Intel mode and with the data strobe signal in Motorola mode, thus enabling register access through chip select controlled Microprocessor cycles.

For fast processors there is also a ready/acknowledgment signal provided in order to eliminate the need for processor configured wait state insertion.

To write a value in a write protected register the value 95H needs to be written in the register Write Protection.

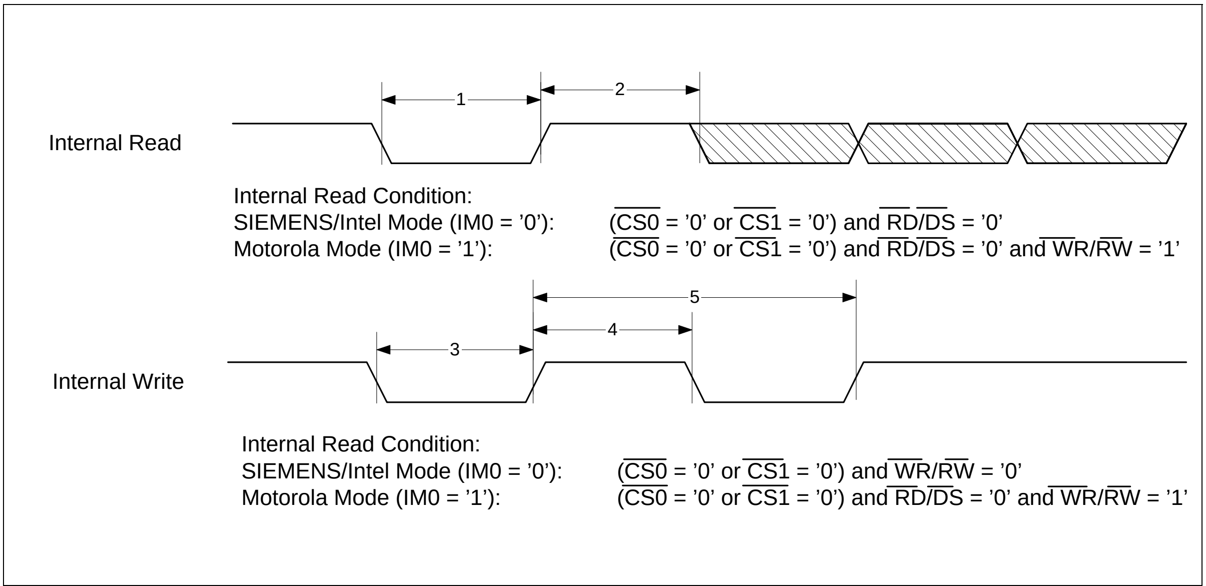

Figure 28 Internal Read Signal and Internal Write Signal

Table 18 Timing of (preliminary) Internal Read Signal and Internal Write Signal

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Active time	40		ns
2	Inactive time	40		ns
3	Active time	40		ns
4	Inactive time	40		ns
5	Interval between two active rising write edges	120		ns

The written value of a register wil be valid for read back 120 ns after rising edge of the WR/RW signal.

4.3.8.1 Intel Mode (IM0='0')

a) Multiplexed Mode (IM1='0')

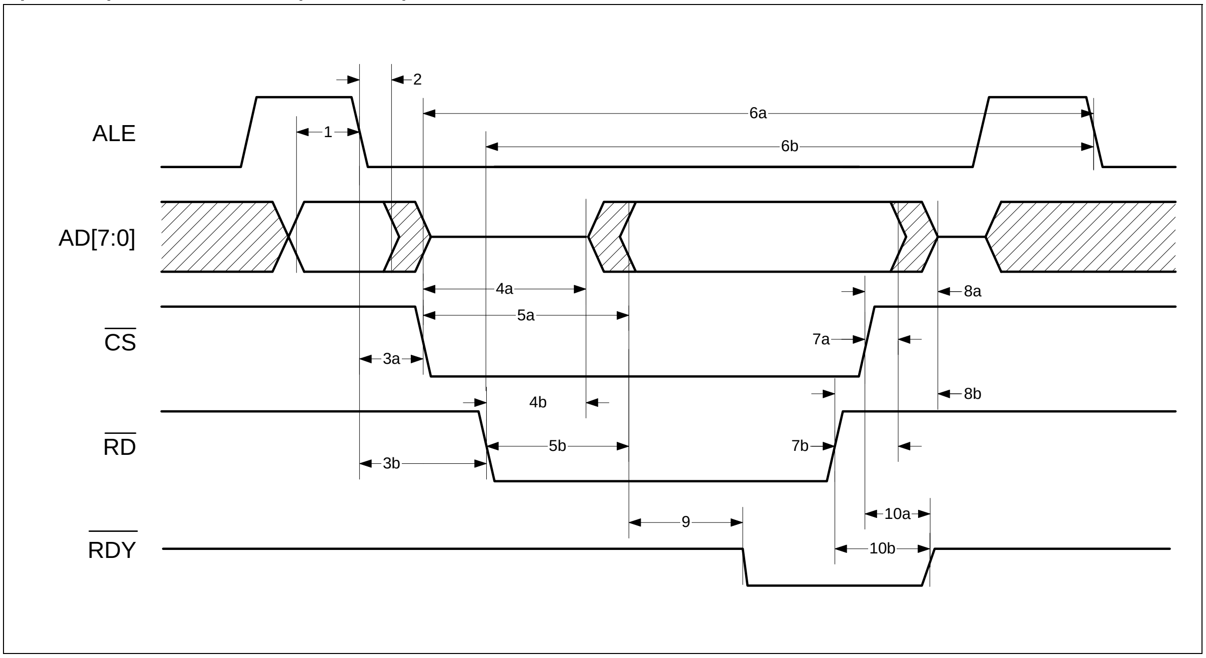

Figure 29 Read Timing in Multiplexed Intel Mode (IM0='0', IM1='0')

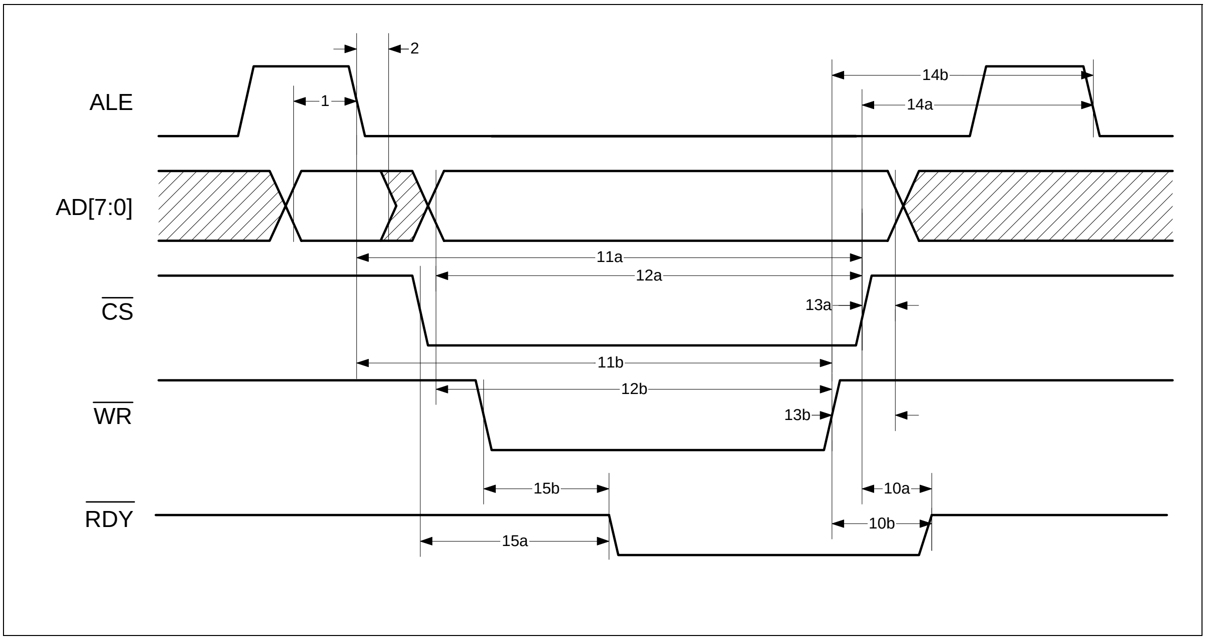

Figure 30 Write Timing in Multiplexed Intel Mode (IM0='0', IM1='0')

b) Demultiplexed Mode (IM1='1')

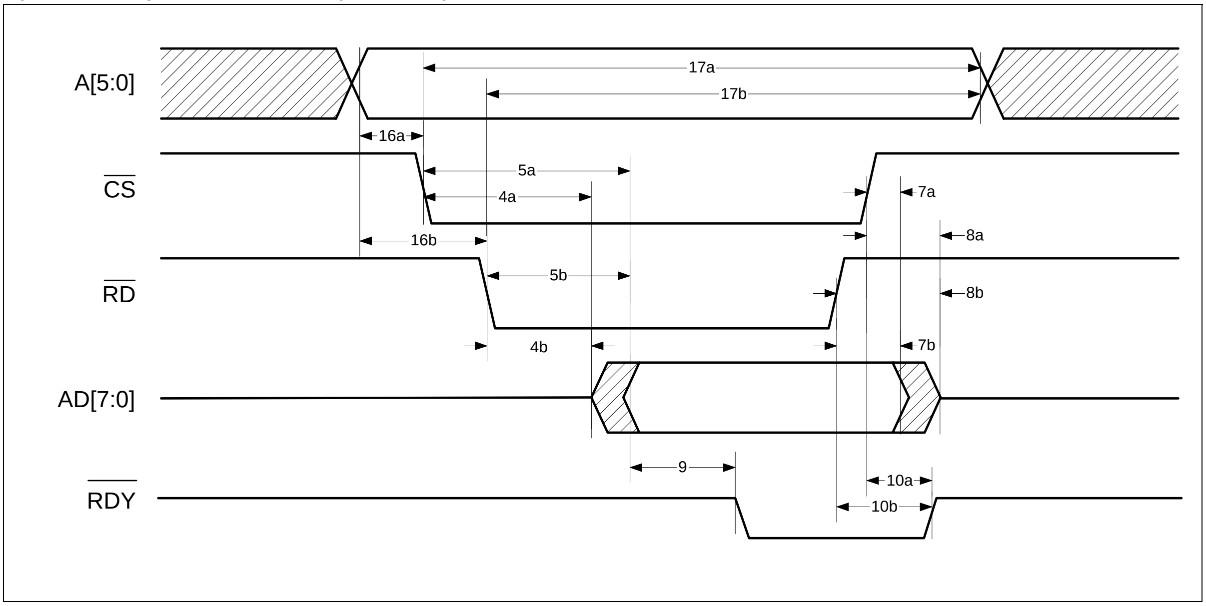

Figure 31 Read Timing in Demultiplexed Intel Mode (IM0='0', IM1='1')

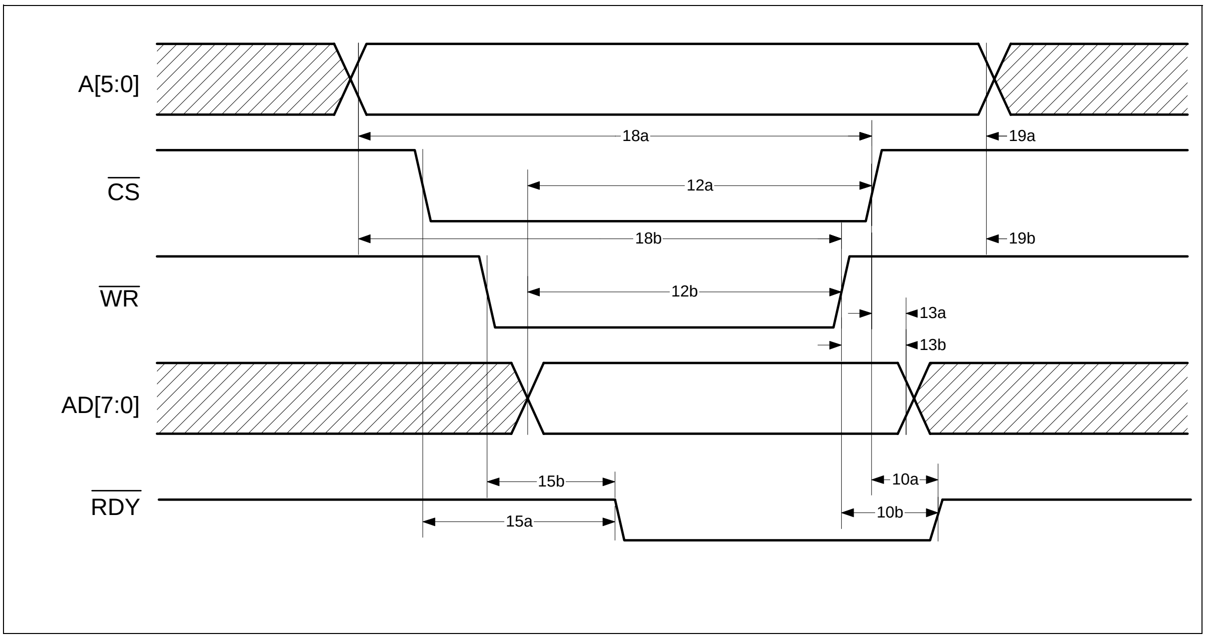

Figure 32 Write Timing in Demultiplexed Intel Mode (IM0='0', IM1='1')

4.3.8.2 Motorola Mode (IM0='1')

a) Multiplexed Mode (IM1='0')

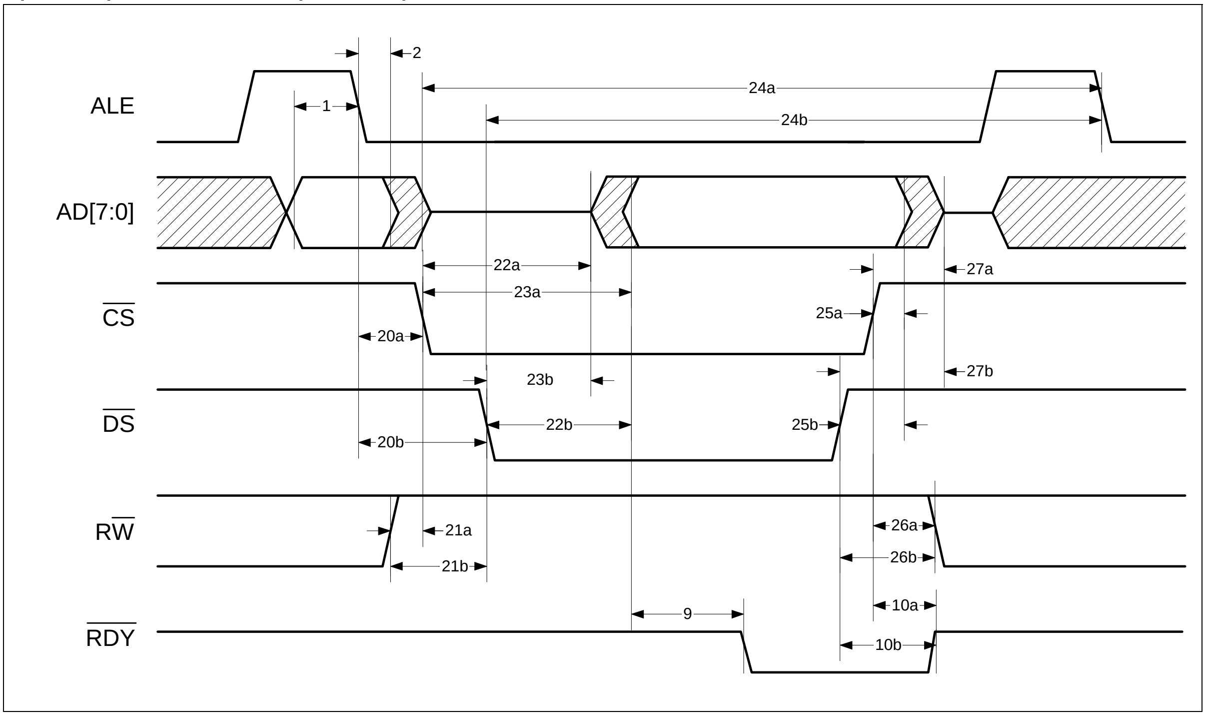

Figure 33 Read Timing in Multiplexed Motorola Mode (IM0='1', IM1='0')

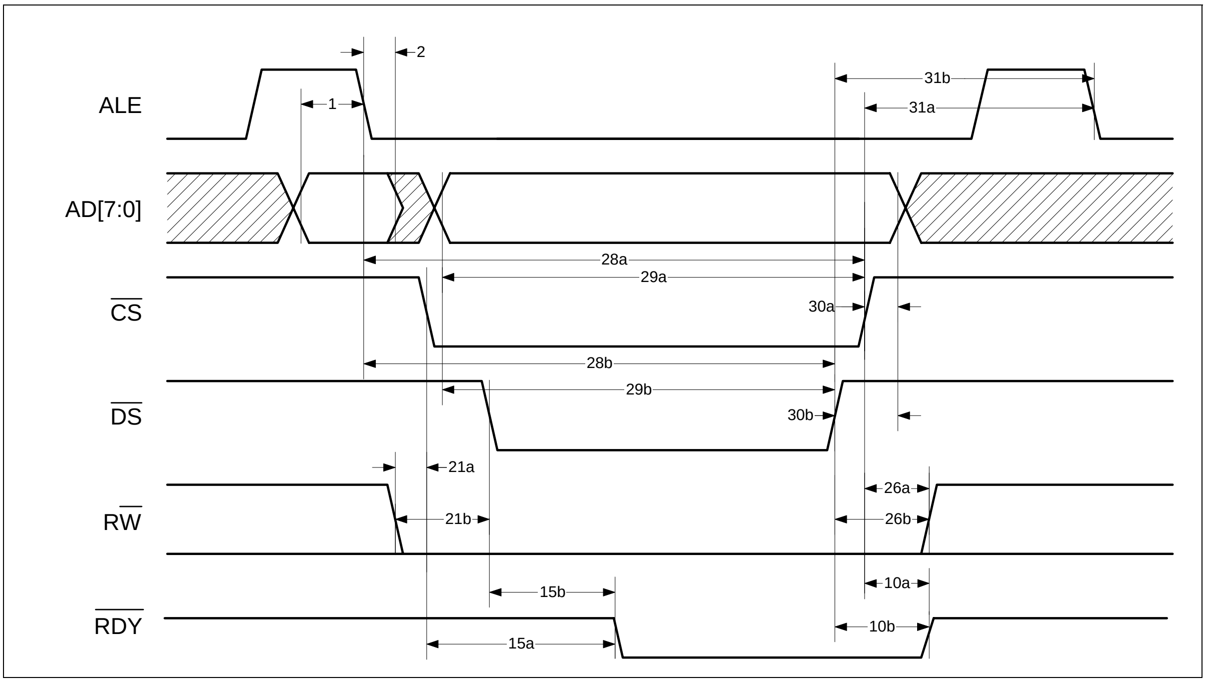

Figure 34 Write Timing in Multiplexed Motorola Mode (IM0='1', IM1='0')

b) Demultiplexed Mode (IM1='1')

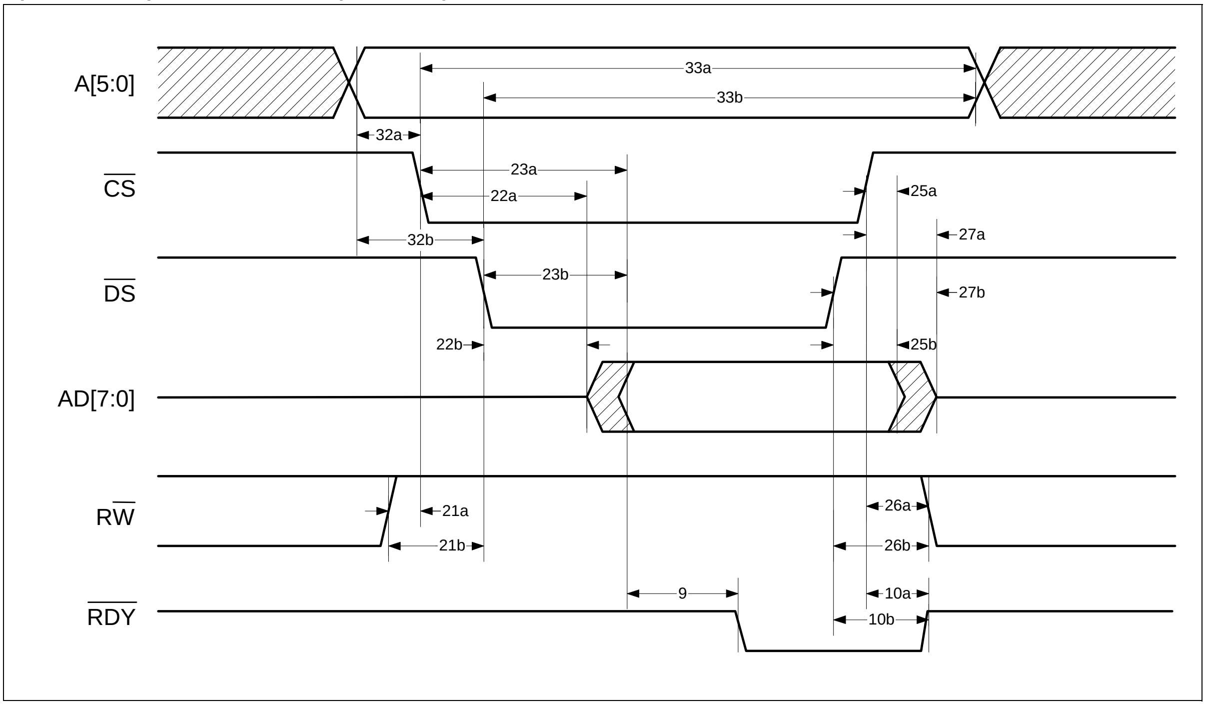

Figure 35 Read Timing in Demultiplexed Motorola Mode (IM0='1', IM1='1')

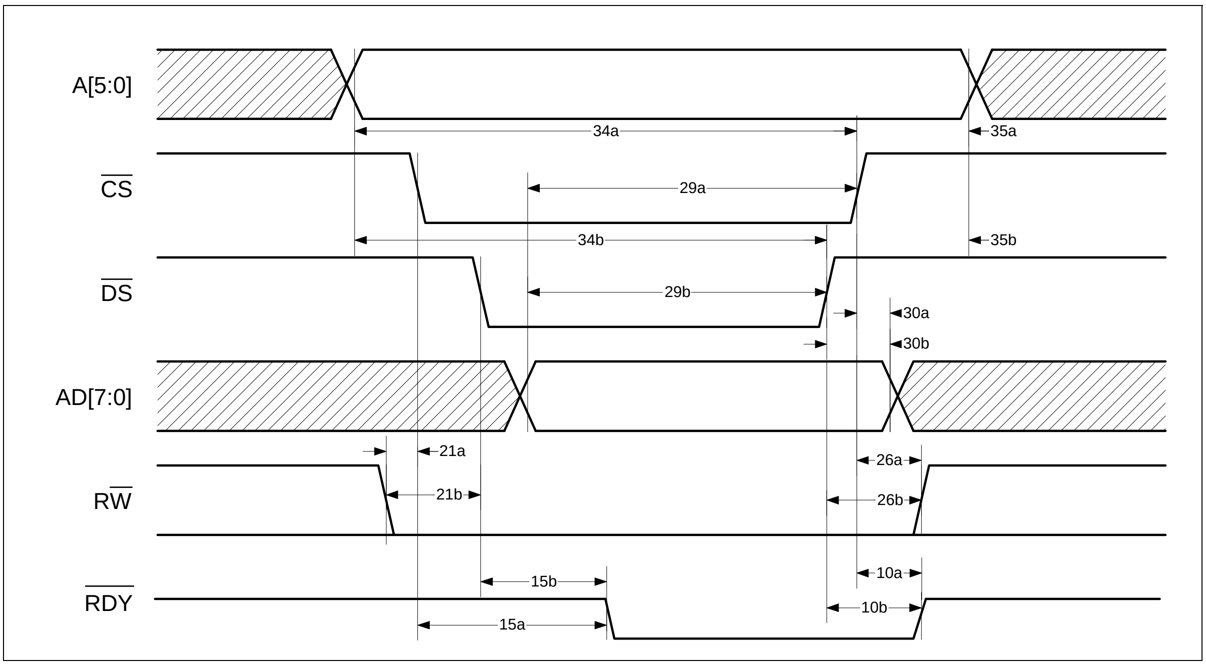

Figure 36 Write Timing in Demultiplexed Motorola Mode (IM0='1', IM1='1')

Table 19 Microprocessor Interface Timing for Figure 29 to Figure 36 (preliminary)

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Address setup before ALE falling edge	15		ns
2	Address hold after ALE falling edge	10		ns
3a	ALE falling edge before CS active if RD asserted	0		ns
3b	ALE falling edge before RD active if CS asserted	0		ns
4a	AD output after CS active if RD asserted	30	90	ns
4b	AD output after RD active if CS asserted	30	90	ns
5a	Read data valid after CS active if RD asserted	30	90	ns
5b	Read data valid after RD active if CS asserted	30	90	ns
6a	ALE rising edge after CS active if RD asserted	100		ns
6b	ALE rising edge after CS active if RD asserted	100		ns
7a	Read data hold after CS inactive if RD asserted	0		ns
7b	Read data hold after RD inactive if CS asserted	0		ns
8a	AD tristate after CS inactive if RD asserted	0	25	ns
8b	AD tristate after RD inactive if CS asserted	0	25	ns
9	RDY asserted after read data valid	15	50	ns
10a	RDY tristate after CS inactive if RD, WR or DS asserted	0	20	ns
10b	RDY tristate after RD, WR or DS inactive if CS asserted	0	20	ns
11a	ALE falling edge before CS rising edge if WR asserted	25		ns

No.	Parameter	Limit Values		Unit
		min.	max.	
11b	ALE falling edge before WR rising edge if CS asserted	25		ns
12a	Write data setup before CS rising edge if WR asserted	25		ns
12b	Write data setup before WR rising edge if CS asserted	25		ns
13a	Write data hold after CS rising edge if WR asserted	20		ns
13b	Write data hold after WR rising edge if CS asserted	20		ns
14a	CS rising edge before ALE falling edge if WR asserted	20		ns
14b	WR rising edge before ALE falling edge if CS asserted	20		ns
15a	RDY asserted after CS active if WR asserted or DS asserted and RW=’0’	30	90	ns
15b	RDY asserted, if CS asserted, after WR active or DS active and RW=’0’	30	90	ns
16a	Address valid before CS active if RD asserted	0		ns
16b	Address valid before RD active if CS asserted	0		ns
17a	Address hold after CS active if RD asserted	100		ns
17b	Address hold after RD active if CS asserted	100		ns
18a	Address setup before CS rising edge if WR asserted	25		ns
18b	Address setup before WR rising edge if CS asserted	25		ns
19a	Address hold after CS rising edge if WR asserted	20		ns
19b	Address hold after WR rising edge if CS asserted	20		ns
20a	ALE falling edge before CS active if DS asserted and RW = ’1’	0		ns

No.	Parameter	Limit Values		Unit
		min.	max.	
20b	ALE falling edge before DS active if CS asserted and $\overline{RW}$ = '1'	0		ns
21a	$\overline{RW}$ setup before CS active if DS asserted	10		ns
21b	$\overline{RW}$ setup before DS active if CS asserted	10		ns
22a	AD output after CS active if DS asserted and $\overline{RW}$ = '1'	30	90	ns
22b	AD output after DS active if CS asserted and $\overline{RW}$ = '1'	30	90	ns
23a	Read data valid after CS active if DS asserted and $\overline{RW}$ = '1'	30	90	ns
23b	Read data valid after DS active if CS asserted and $\overline{RW}$ = '1'	30	90	ns
24a	ALE rising edge after CS active if DS asserted and $\overline{RW}$='1'	100		ns
24b	ALE rising edge after DS active if CS asserted and $\overline{RW}$='1'	100		ns
25a	Read data hold after CS inactive if DS asserted and $\overline{RW}$ = '1'	0		ns
25b	Read data hold after DS inactive if CS asserted and $\overline{RW}$ = '1'	0		ns
26a	$\overline{RW}$ hold after CS inactive if DS asserted	10		ns
26b	$\overline{RW}$ hold after DS inactive if CS asserted	10		ns
27a	AD tristate after CS inactive if DS asserted and $\overline{RW}$ = '1'	0	25	ns
27b	AD tristate after DS inactive if CS asserted and $\overline{RW}$ = '1'	0	25	ns
28a	ALE falling edge before CS rising edge if DS asserted and $\overline{RW}$ = '0'	25		ns
28b	ALE falling edge before DS rising edge if CS asserted and $\overline{RW}$ = '0'	25		ns
29a	Write data setup before CS rising edge if DS asserted and $\overline{RW}$ = '0'	20		ns
29b	Write data setup before DS rising edge if CS asserted and $\overline{RW}$ = '0'	20		ns

No.	Parameter	Limit Values		Unit
		min.	max.	
30a	Write data hold after CS rising edge if DS asserted and $\overline{RW}$ = ’0’	20		ns
30b	Write data hold after DS rising edge if CS asserted and $\overline{RW}$ = ’0’	20		ns
31a	CS rising edge before ALE falling edge if DS asserted and $\overline{RW}$ = ’0’	20		ns
31b	DS rising edge before ALE falling edge if CS asserted and $\overline{RW}$ = ’0’	20		ns
32a	Address valid before CS active if DS asserted and $\overline{RW}$ = ’1’	0		ns
32b	Address valid before DS active if CS asserted and $\overline{RW}$ = ’1’	0		ns
33a	Address hold after CS active if DS asserted and $\overline{RW}$=’1’	100		ns
33b	Address hold after DS active if CS asserted and $\overline{RW}$=’1’	100		ns
34a	Address setup before CS rising edge if DS asserted and $\overline{RW}$ = ’0’	25		ns
34b	Address setup before DS rising edge if CS asserted and $\overline{RW}$ = ’0’	25		ns
35a	Address hold after CS rising edge if DS asserted and $\overline{RW}$ = ’0’	20		ns
35b	Address hold after DS rising edge if CS asserted and $\overline{RW}$ = ’0’	20		ns

4.3.9 JTAG Timing

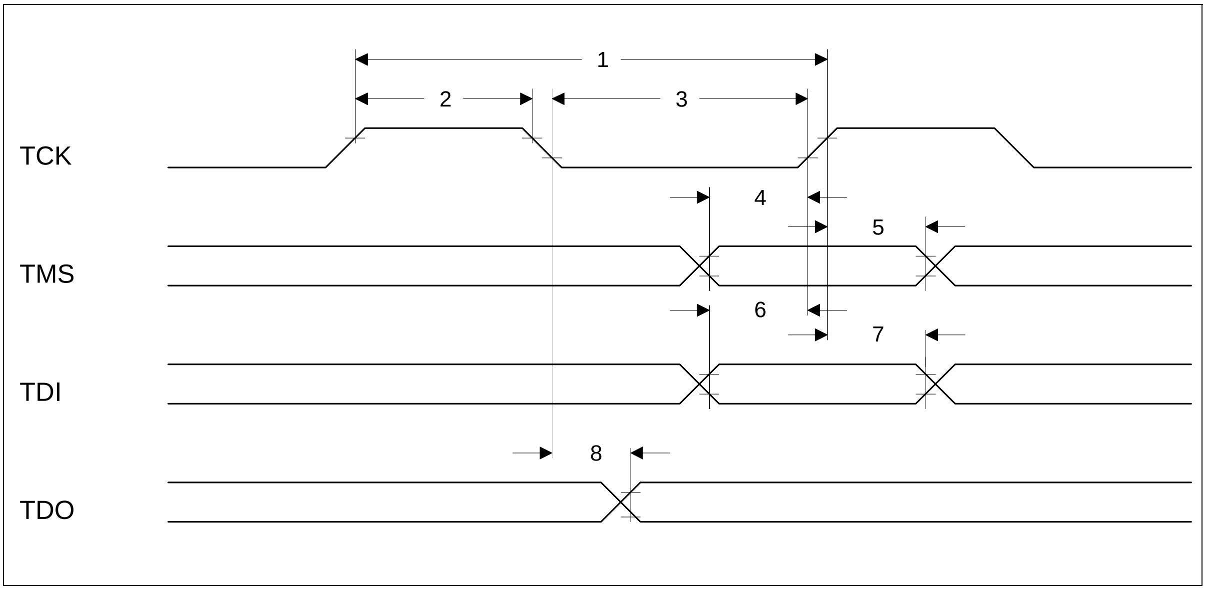

Figure 37 JTAG Boundary Scan Timing

Table 20 JTAG Boundary Scan Timing

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_tck_period	TCK period	250		ns
2	t_tck_high	TCK high time	80		ns
3	t_tck_low	TCK low time	80		ns
4	t_tms_setup	TMS setup time	40		ns
5	t_tms_hold	TMS hold time	40		ns
6	t_tdi_setup	TDI setup time	40		ns
7	t_tdi_hold	TDI hold time	40		ns
8	t_tck_tdo_fall	TDO valid delay		100	ns

5 Register Description

5.1 Register Model

5.2 Detailed Register Description

In the following section the meaning and addresses of the registers of the SIDEC are described, The addresses and reset values are given in Hex-Code indicated by a subsequent capital H. A number '**0**' or '**1**' written in bold type denotes the reset value of the corresponding bit.

To write a value in a write protected register the value 95H needs to be written in the register Write Protection.

5.2.1 Register Map

The following table lists all registers. The table displays the register name, the abbreviation, the reset value, the read/write mode and the page number with the detailed description. The registers are sorted by addresses.

Addr.	Short Name	Full name	R/W	Res. value	page
00H	NOTEBOOK	**Notebook**	R/W	00H	71
01H	WP	**W**rite **P**rotection	W	NOT 95H	73
02H	WDG1	**W**atch**d**o**g 1**	W		73
03H	WDG2	**W**atch**d**o**g 2**	W		74
04H	WDG3	**W**atch**d**o**g 3**	W		74
05H	UPIO	µ**P**-**I**/**O**-Pin extension	R/W	0FH	71
06H	PCMCTRL	**PCM** Bypass and loop **C**on**tr**o**l**	W	00H	74
07H	IRMASK	**I**nter**r**upt **Mask**	W	7FH	73
08H	IRREQ	**I**nter**r**upt-**Req**uest	R		106
09H	CLKSTAT	**Cl**oc**k**-**Stat**us	R		106
0AH	RAMBIST	**RAMBIST**	R/W	00H	71
0BH	CONFCC	**Conf**iguration of **C**lock **C**ontrol unit	W	00H	97
0CH	FSLIPIV	**F**rame **slip** safety **i**nter**v**al	W	28H	97
0DH	RIALIGN	**R**eceive **i**nput frame **align**ment	W	00H	98

Addr.	Short Name	Full name	R/W	Res. value	page
0EH	SIALIGN	**S**end **i**nput frame **align**ment	W	00H	98
0FH	SOALIGN	**S**end **o**utput frame **align**ment	W	00H	98
10H	UCCALIGN	**UCC** frame **align**ment,write protected	W	00H	99
11H	PHALIGN	Bit **Ph**ase **align**ment for RI, SI, SO and UCC	W	00H	99
12H	CONFSCU1	**Conf**iguration of **s**peech **c**ontrol **u**nit **1**	W	69H	89
13H	CONFSCU2	**Conf**iguration of **s**peech **c**ontrol **u**nit **2**	W	97H	90
14H	CONFSCU3	**Conf**iguration of **s**peech **c**ontrol **u**nit **3**	W	A4H	90
15H	CONFSCU4	**Conf**iguration of **s**peech **c**ontrol **u**nit **4**	W	A7H	91
16H	CONFSCU5	**Conf**iguration of **s**peech **c**ontrol **u**nit **5**	W	84H	91
17H	CONFSCU6	**Conf**iguration of **s**peech **c**ontrol **u**nit **6**	W	2AH	92
18H	CONFSCU7	**Conf**iguration of **s**peech **c**ontrol **u**nit **7**	W	8AH	92
19H	CONFSCU8	**Conf**iguration of **s**peech **c**ontrol **u**nit **8**	W	EEH	93
1AH	CONFSCU9	**Conf**iguration of **s**peech **c**ontrol **u**nit **9**	W	44H	93
1BH	CONFSCU10	**Conf**iguration of **s**peech **c**ontrol **u**nit **10**	W	C0H	94
1CH	CONFPSD	**Conf**iguration of 2100 Hz tone **p**hase **s**hift **d**etector	W	43H	95
1DH	CONFSS7	**Conf**iguration of **SS7** continuity check tone detection	W	00H	96
1EH	MONSIL	**Mon**itor **s**end **i**nput **l**evel	R		111
1FH	MONSOL	**Mon**itor **s**end **o**utput **l**eve	R		112
20H	MONRIL	**Mon**itor of **r**eceive **i**nput **l**evel	R		112
21H	MONOFSI	**Mon**itor **of**fset in **s**end path **i**nput	R		113
22H	MONOFSO	**Mon**itor **of**fset in **s**end path **o**utput	R		113
23H	MONAEL	**Mon**itor **a**rtificial **e**cho **l**evel	R		113
24H	MONBNL	**Mon**itor **b**ackground **n**oise **l**evel	R		113
25H	MONERL	**Mon**itor **E**cho **r**eturn **l**oss	R		113
26H	MONCL	**Mon**itor **c**ombined **l**oss without NLP	R		114
27H	MONNLPTHL	**Mon**itor **NLP th**reshold **l**evel	R		114

Addr.	Short Name	Full name	R/W	Res. value	page
28H	MONOCDT	**Mon**itor **o**ver**c**ompensation and **d**ouble **t**alk hang-over time	R		114
29H	MONSI	**Mon**itor **s**end **i**nput **si**gnal (A-/µ-Law encoded)	R		110
2AH	MONSO	**Mon**itor **s**end **o**utput signal (A-/µ-Law encoded	R		111
2BH	MONRI	**Mon**itor of **r**eceive **i**nput signal (A-/µ-Law encoded	R		111
2CH	MONSTAT1	**Mon**itor of internal/external control **stat**es **1**	R		114
2DH	MONSTAT2	**Mon**itor of internal/external control **stat**es **2**	R		115
2EH	MONSTAT3	**Mon**itor of internal/external control **stat**es **3**	R		115
2FH	CTRLTSMON	**Ctrl** of **TS** to be **mon**itored	W	00H	72
30H	CONFPCM	Global **Conf**iguration of **PCM** outputs	W	03H	74
31H	CONFTS16	**Conf**iguration of **TS16** CAS Evaluation for E1 frames	W	12H	82
32H	CONFIDLE	**Conf**iguration of **IDLE** Detection	W	1DH	81
33H	IDLEMASK	**IDLE** detection bit compare **MASK**	W	00H	81
34H	IDLEPATTERN	**Idlepattern**	W	55H	82
35H	ATE	**A**ddress of **Te**st-channel	W	00H	86
36H	SFATSES	**S**uper **f**rame **a**larm and requested **t**ime**s**lot **e**n/disable **s**tatus	R		107
37H	TESTTIMER	µP **Test** and **Timer**	W	00H	86
38H	CTRLTEST	**Contr**o**l** of **test** channel	W	00H	87
39H	TSGSPP	**T**est **s**ignal **g**enerator for **s**end **p**ath **p**attern	W	55H	87
3AH	TSGRPP	**T**est **s**ignal **g**enerator for **r**eceive **p**ath **p**attern	W	55H	88
3BH	HTIM	**H**igh-Byte for **Tim**er	W	00H	89
3CH	LTIM	**L**ow-Byte for **Tim**er	W	00H	89

Addr.	Short Name	Full name	R/W	Res. value	page
3DH	SOTP	**S**end path **o**utput **t**est **p**attern	R		107
3EH	TESTSTAT	Background **test stat**us signals	R		107
3FH	CONFLAW	Global **conf**iguration of PCM encoding **law**	W	00H	75
40H	CHCTRL0	Individual **ch**annel **contr**o**l 0**	W	00H	76
41H	CHCTRL1	Individual **ch**annel **contr**o**l 1**	W	00H	76
42H	CHCTRL2	Individual **ch**annel **contr**o**l 2**	W	00H	76
43H	CHCTRL3	Individual **ch**annel **contr**o**l 3**	W	00H	76
44H	CHCTRL4	Individual **ch**annel **contr**o**l 4**	W	00H	76
45H	CHCTRL5	Individual **ch**annel **contr**o**l 5**	W	00H	76
46H	CHCTRL6	Individual **ch**annel **contr**o**l 6**	W	00H	76
47H	CHCTRL7	Individual **ch**annel **contr**o**l 7**	W	00H	76
48H	CHCTRL8	Individual **ch**annel **contr**o**l 8**	W	00H	76
49H	CHCTRL9	Individual **ch**annel **contr**o**l 9**	W	00H	76
4AH	CHCTRL10	Individual **ch**annel **contr**o**l 10**	W	00H	76
4BH	CHCTRL11	Individual **ch**annel **contr**o**l 11**	W	00H	76
4CH	CHCTRL12	Individual **ch**annel **contr**o**l 12**	W	00H	76
4DH	CHCTRL13	Individual **ch**annel **contr**o**l 13**	W	00H	76
4EH	CHCTRL14	Individual **ch**annel **contr**o**l 14**	W	00H	76
4FH	CHCTRL15	Individual **ch**annel **contr**o**l 15**	W	00H	76
50H	CHCTRL16	Individual **ch**annel **contr**o**l 16**	W	00H	76
51H	CHCTRL17	Individual **ch**annel **contr**o**l 17**	W	00H	76
52H	CHCTRL18	Individual **ch**annel **contr**o**l 18**	W	00H	76
53H	CHCTRL19	Individual **ch**annel **contr**o**l 19**	W	00H	76
54H	CHCTRL20	Individual **ch**annel **contr**o**l 20**	W	00H	76
55H	CHCTRL21	Individual **ch**annel **contr**o**l 21**	W	00H	76
56H	CHCTRL22	Individual **ch**annel **contr**o**l 22**	W	00H	76
57H	CHCTRL23	Individual **ch**annel **contr**o**l 23**	W	00H	76
58H	CHCTRL24	Individual **ch**annel **contr**o**l 24**	W	00H	76
59H	CHCTRL25	Individual **ch**annel **contr**o**l 25**	W	00H	76

Addr.	Short Name	Full name	R/W	Res. value	page
5AH	CHCTRL26	Individual **ch**annel **con**t**r**o**l** **26**	W	00H	76
5BH	CHCTRL27	Individual **ch**annel **con**t**r**o**l** **27**	W	00H	76
5CH	CHCTRL28	Individual **ch**annel **con**t**r**o**l** **28**	W	00H	76
5DH	CHCTRL29	Individual **ch**annel **con**t**r**o**l** **29**	W	00H	76
5EH	CHCTRL30	Individual **ch**annel **con**t**r**o**l** **30**	W	00H	76
5FH	CHCTRL31	Individual **ch**annel **con**t**r**o**l** **31**	W	00H	76
60H	CONFUCC	**Conf**iguration of **UCC** Interface	W	00H	82
61H	UCCMFR	**UCC M**ulti**fr**ame Alignment	W	00H	84
62H	UCCFRS	Selection of the special **UCC** Frame **FRS**	W	00H	84
63H	WRUCC	**W**rite/**R**ead **UCC**I	W	00H	85
64H	DORAM	**D**ata **O**utput **RAM**	W	00H	85
65H	IMASKFRS	**I**nterrupt **Mask** for the special UCC frame **FRS**	W	00H	85
66H	IMASKFRN	**I**nterrupt **Mask** for channel individual UCC frames (**FRN**)	W	00H	86
67H	DIRAM	requested **D**ata **I**nput **RAM** value	R		108
68H	UCCOLD	Changed **UCC** input data **old** value	R		108
69H	UCCNEW	Changed **UCC** input data **new** value	R		108
6AH	UCCSTAT	**UCC stat**us	R		108
6BH	SCMASK	**S**erial **C**ontrol Interface **Mask**	W	3FH	78
6CH	CONFFLEX SCTR	**Conf**iguration of the **flex**ible **s**erial **c**on**tr**ol signal	W	00H	78
6DH	CONFFLEXUCC	**Conf**iguration of the **flex**ible **UCC** control bit (FX-Bit)	W	00H	79
6EH	STATUS	**Status**	R		106
6FH	CONFFLEXMON	**Conf**iguration of **Flex**ible **Mon**itor Signals	W	FEH	79
70H	ASTOC	**A**FI **S**aw-**T**ooth and **O**ffset **C**haracteristic	W	00H	99
71H	AFSTC	**A**FI **F**ilter **S**pring **T**imer **C**onfiguration	W	44H	100

Addr.	Short Name	Full name	R/W	Res. value	page
72H	AEEPD	**A**FI **E**nd **E**cho **P**ath **D**elay	W	0FH	100
73H	AVDDI	**A**FI **V**oice **D**etection, **D**etection **I**ntervals	W	77H	101
74H	AVDHG	**A**FI **V**oice **D**etection, **H**ysteresis and **G**ap	W	74H	102
75H	AVDCI	**A**FI **V**oice **D**etection **C**ount **I**nit	W	85H	103
76H	VDFCTRL	**V**oice **D**etection **F**reeze **C**on**tr**o**l**	W	B4H	95
77H	ATMAT	**A**FI **T**urbo **M**ode **A**ctivation **T**hreshold	W	08H	103
78H	AACSC	**A**FI **A**uxiliary **C**oefficient **S**upervision **C**onfiguration	W	00H	103
79H	ACONF	**A**FI **Conf**iguration	W	10H	104
7AH	AFCMC	**A**FI **F**ilter **C**oefficients **M**onitoring **C**ontrol	W	00H	105
7BH	AFCD1	**A**FI **F**ilter **C**oefficient **D**ata **1**	R		109
7CH	AFCD2	**A**FI **F**ilter **C**oefficient **D**ata **2**	R		109
7DH	AFCD3	**A**FI **F**ilter **C**oefficient **D**ata **3**	R		110

5.2.2 Read-Write-Register

NOTEBOOK[7:0] (Addr.: 00H): **Notebook,** write protected, Reset value = 00H

NOTE BOOK[7]	NOTE BOOK[6]	NOTE BOOK[5]	NOTE BOOK[4]	NOTE BOOK[3]	NOTE BOOK[2]	NOTE BOOK[1]	NOTE BOOK[0]

NOTEBOOK[7:0] Read/Write register for testing of the µP interface, content without effect, write protected

UPIO[7:0] (Addr.: 05H): µ**P-I/O**-Pin extension, Reset value = 0FH

UPIO3	UPIO2	UPIO1	UPIO0	TUPIO3	TUPIO2	TUPIO1	TUPIO0

UPIO3 If TUPIO3='1': Value from Pin UPIO3
If TUPIO3='0': Value that is output at Pin UPIO3

UPIO2 If TUPIO2='1': Value from Pin UPIO2
If TUPIO2='0': Value that is output at Pin UPIO2

UPIO1 If TUPIO1='1': Value from Pin UPIO1
If TUPIO1='0': Value that is output at Pin UPIO1

UPIO0 If TUPIO0='1': Value from Pin UPIO0
If TUPIO0='0': Value that is output at Pin UPIO0

TUPIO3 Tristate control for Pin UPIO3
'**1**': Pin UPIO3 is input
'0': Pin UPIO3 is output

TUPIO2 Tristate control for Pin UPIO2
'**1**': Pin UPIO2 is input
'0': Pin UPIO2 is output

TUPIO1 Tristate control for Pin UPIO1
'**1**': Pin UPIO1 is input
'0': Pin UPIO1 is output

TUPIO0 Tristate control for Pin UPIO0
'**1**': Pin UPIO0 is input
'0': Pin UPIO0 is output

RAMBIST[5:0] (Addr.: 0AH): **RAM BIST,** write protected, Reset value = 00H

-	-	RUN BIST	CUFAIL	AFI3 FAIL	AFI2 FAIL	AFI1 FAIL	AFI0 FAIL

RUNBIST '1': set by µP: activates RAMBIST and signals running RAMBIST
'**0**': set by hardware: signals that RAMBIST is finished (not running),

		the value RESULT is valid, if the RAMBIST was activated before
CUFAIL	’1’:	RAMBIST of central unit failed, i.e. a RAM error was detected
	’**0**’:	RAMBIST of central unit succesful: no error in RAM
AFI3FAIL	’1’:	RAMBIST of adaptive filter unit 3 failed, i.e. a RAM error was detected
	’**0**’:	RAMBIST of adaptive filter unit 3 succesful: no error in RAM
AFI2FAIL	’1’:	RAMBIST of adaptive filter unit 2 failed, i.e. a RAM error was detected
	’**0**’:	RAMBIST of adaptive filter unit 2 succesful: no error in RAM
AFI1FAIL	’1’:	RAMBIST of adaptive filter unit 1 failed, i.e. a RAM error was detected
	’**0**’:	RAMBIST of adaptive filter unit 1 succesful: no error in RAM
AFI0FAIL	’1’:	RAMBIST of adaptive filter unit 0 failed, i.e. a RAM error was detected
	’**0**’:	RAMBIST of adaptive filter unit 0 succesful: no error in RAM

The bits CUFAIL, AFI3FAIL, AFI2FAIL,AFI1FAIL and AFI0FAIL are read only.

5.2.3 Write Register

All Write Registers are Write Only Registers and cannot be read out.

CTRLTSMON[6:0] (Addr.: 2FH): **Control** of **TS** to be **mon**itored, Reset value = 00H

-	SNAP SHOT	MVAL	MCH[4]	MCH[3]	MCH[2]	MCH[1]	MCH[0]

SNAPSHOT	’1’:	Values of the monitor registers are only updated after writing to this register with MVAL set to ’1’. The data remains stored in the monitor registers. An interrupt is generated as soon as the monitor values are valid. STATUS.TSMPOLL is cleared only when a new request is started by access to MVAL.
	’**0**’:	Values of the monitor registers are continuously updated (each time the timeslot MCH[4:0] is detected) if MVAL = ’1’. An interrupt is generated only once and as soon as data becomes available in the monitor registers.
MVAL	’**0**’:	resets the interrupt condition for TSMPOLL in the STATUS register. Stops updating of values if SNAPSHOT = ’0’
	’1’:	starts request for monitoring of the timeslot defined by MCH[4:0].
MCH[4:0]		selects the timeslot (channel) to be monitored

If MVAL = ’1’ the Monitor Read Registers are filled with the values of timeslot MCH[4:0] as soon as this timeslot is processed. The availibility of the monitored values in the Monitor Read Registers is indicated by setting the bit IRREQ.TSM and STATUS.TSM.

WP[7:0] (Addr.: 01H) **W**rite **P**rotection, Reset Value ’protected’= NOT 95H

WP[7]	WP[6]	WP[5]	WP[4]	WP[3]	WP[2]	WP[1]	WP[0]

WP[7:0] Write access to the write protected configuration registers is released by writing the value 95H to this register. The write protection is activated by writing any other value.

IRMASK[6:0] (Addr.: 07H) **I**nterr**upt Mask**, Reset Value = 7FH

-	WDOG MASK	SYNCI MASK	CA MASK	TT MASK	TE MASK	UCC MASK	TSM MASK

If an interrupt source is masked the information is shown in the STATUS register but not in the IRREQ register. Masking and unmasking does not affect the interrupt source. A new interrupt will be generated after masking and unmasking, if interrupt source is active (as indicated in STATUS register).

WDOGMASK ’**1**’: Watchdog condition does not cause an interrupt
’0’: normal operation

SYNCIMASK ’**1**’: Incorrect SYNCI pulse does not cause an interrupt
’0’: normal operation

CAMASK ’**1**’: coefficient available is ignored
’0’: normal operation

TTMASK ’**1**’: test termination is ignored
’0’: normal operation

TEMASK ’**1**’: timer expired is ignored
’0’: normal operation

UCCMASK ’**1**’: UCC interrupt is ignored
’0’: normal operation

TSMMASK ’**1**’: timeslot monitor values available is ignored
’0’: normal operation

WDG1[7:0] (Addr.: 02H) **W**atch**dog 1**

WDG1[7]	WDG1[6]	WDG1[5]	WDG1[4]	WDG1[3]	WDG1[2]	WDG1[1]	WDG1[0]

WDG1[7:0] For watchdog test: Must bewritten with the defined value AAH as the first of the three watchdog registers within 2 seconds

WDG2[7:0] (Addr.: 03H) **Watchdog 2**

WDG2[7]	WDG2[6]	WDG2[5]	WDG2[4]	WDG2[3]	WDG2[2]	WDG2[1]	WDG2[0]

WDG2[7:0] For watchdog test: Must be written with the defined value 99H as the second of the three watchdog registers within 2 seconds

WDG3[7:0] (Addr.: 04H) **Watchdog 3**

WDG3[7]	WDG3[6]	WDG3[5]	WDG3[4]	WDG3[3]	WDG3[2]	WDG3[1]	WDG3[0]

WDG3[7:0] For watchdog test: Must be written with the defined value 1DH as the last of the three watchdog registers within 2 seconds

PCMCTRL[3:0] (Addr.: 06H) **PCM** Bypass and loop **Contr**o**l**, write protected, Reset value = 00H

-	-	-	-	SR LOOP	RS LOOP	R BYPASS	S BYPASS

SRLOOP ’1’: Enables the internal loop from SO signal to RI signal
’**0**’: Normal operation

RSLOOP ’1’: Enables the internal loop from RO signal to SI signal
’**0**’: Normal operation

RBYPASS ’1’: Bypasses the RI input directly to the RO output
’**0**’: Normal operation

SBYPASS ’1’: Bypasses the SI input directly to the SO output
’**0**’: Normal operation

Note: If SRLOOP=’1’ and RSLOOP=’1’ only RSLOOP becomes active.

CONFPCM[7:0] (Addr.: 30H): Global **Conf**iguration of **PCM** outputs, write protected, Reset value = 03H

NLP ITU	NLP MOD	SOATT EN	SOATT MOD	ROATT EN	ROATT MOD	DYN SUB	INVERR SIGN

NLPITU ’1’: NLP comfort noise according to ITU
’**0**’: NLP comfort noise subjective

NLPMOD only if NLPITU = ’1’: ’1’:output signal is band limited noise
’**0**’:output signal is zero, i.e. line is dead

SOATTEN ’1’: Attenuation of send path output enabled and controlled by echo

		canceller en/disable
	’**0**’:	Attenuation of send path output is disabled for all channels
SOATTMOD	’1’:	Attenuation of send path output is 2.5 dB if enabled
	’**0**’:	Attenuation of send path output is 6 dB if enabled
ROATTEN	’1’:	Attenuation of receive path output enabled and controlled by echo canceller en/disable
	’**0**’:	Attenuation of receive path output is disabled for all channels
ROATTMOD	’1’:	Attenuation of receive path output is 2.5 dB if enabled
	’**0**’:	Attenuation of receive path output is 6 dB if enabled
DYNSUB	’**1**’:	The subtractor dynamically attenuates the send output signal if difference is derived from large signal levels
	’0’:	The subtractor operates in linear mode
INVERRSIGN	’**1**’:	Sign of error signal (Echo + Near end speech) is inverted (normal operation)
	’0’:	Sign of error signal (Echo + Near end speech) is not inverted (incorrect operation, for test only)

CONFLAW[3:0] (Addr.: 3FH): Global **conf**iguration of PCM encoding **law**, write protected, Reset value = 00H

-	-	-	-	CHIND	GCONV DISLAW	GALAW NE	GALAW FE

For explanation of A/µ-Law Conversion functions see also **Figure 8**.

CHIND	’1’: Enables individual PCM encoding law settings for each channel by bits 7 to 5 of the individual control registers CHCTRL 0 to 31 ’**0**’: Enables global PCM encoding law configuration for all channels by bits 2 to 0 of this register
GCONVDISLAW	Determines the valid PCM law if the PCM-Law conversion of an individual channel is disabled by any source (µP, UCC or serial control signal) if CHIND = ’0’ ’1’: All PCM channels for which conversion is disabled are A-Law en/decoded* ’**0**’: All PCM channels for which conversion is disabled are µ-Law en/decoded*
GALAWNE	Allows global configuration of near end PCM-Law: ’1’: A-Law PCM encoding at near end side (RO and SI) if CHIND = ’0’ and CONVDIS = ’0’ ’**0**’: µ-Law PCM encoding at near end side (RO and SI) if CHIND = ’0 and CONVDIS = ’0’
GALAWFE	Allows global configuration of far end PCM-Law: ’1’: A-Law PCM encoding at far end side (RI and SO)

if CHIND = ’0’ and CONVDIS = ’0’
’**0**’: µ-Law PCM encoding at far end side (RI and SO)
if CHIND = ’0’ and CONVDIS = ’0’

*Note: In the case of no A-/µ-Law conversion (same law at near and far end side) the PCM encoding law can temporarily be changed by any conversion disabling source (µP, UCC FX-Bit or serial control signal) if GCONVDISLAW is different from GALAWNE/ GALAWFE.

CHCTRL0-31[7:0] (Addr.: 40H-5FH): Individual **ch**annel **con**t**r**o**l**, write protected, Reset value = 00H

ICONV DISLAW	IALAW NE	IALAW FE	CONV DIS	FREEZE	NLPDIS	DIS ABLE	ENP CTRL

The upper three bits ICONVDISLAW, IALAWNE and IALAWFE are only enabled if CONFLAW.CHIND = ’1’. For explanation of law conversion see also **Figure 8**.

ICONVDISLAW — Determines the valid PCM-law of the corresponding channel if the PCM-Law conversion for this channel is disabled (CONVDIS = ’1’) and channel individual settings are enabled (Bit CONFLAW.CHIND = ’1’)
’1’: The corresponding PCM channel is A-Law en/decoded if conversion is disabled*
’**0**’: The corresponding PCM channel is µ-Law en/decoded if conversion is disabled*

IALAWNE — '1': The corresponding PCM channel is A-Law PCM en/decoded at the near end side (RO and SI) if CONFLAW.CHIND = '1' and CONVDIS = '0'
'**0**': The corresponding PCM channel is µ-Law PCM en/decoded at the near end side (RO and SI) if CONFLAW.CHIND = '1' and CONVDIS = '0'

IALAWFE — '1': The corresponding PCM channel is A-Law PCM en/decoded at the far end side (RI and SO) if CONFLAW.CHIND = '1' and CONVDIS = '0'
'**0**': The corresponding PCM channel is µ-Law PCM en/decoded at the far end side (RI and SO) if CONFLAW.CHIND = '1' and CONVDIS = '0'

CONVDIS — '1': Disables the PCM Law conversion (GALAWNE, GALAWFE, IALAWNE, IALAWFE) for the corresponding channel. The valid encoding Law for this channel is determined by the values of the Bits ICONVDISLAW of this register if channel individual settings are configured (CHIND = '1') or the settings of the global register CONFLAW.GCONVDISLAW, if global configuration is configured

		(CHIND = ’0’).
	’**0**’:	Possible PCM Law conversion is enabled if Bit ENPCTRL = ’1’, Law conversion on/off depends on other hardware sources (serial control signals, UCC) if ENPCTRL = ’0’.
FREEZE	’1’:	The H-register of the corresponding channel are frozen
	’**0**’:	The freezing of the H-Register for the corresponding channel depends on the internal control of the speech control unit only if ENPCTRL = ’1’, Freezing of H-Registers for the corresponding channel also depends on other hardware sources (serial control signals) if ENPCTRL = ’0’.
NLPDIS	’1’:	The NLP of the corresponding channel is bypassed
	’**0**’:	The bypass of the NLP for the corresponding channel depends on the internal control of the speech control unit only if ENPCTRL = ’1’, The bypassing of the NLP for the corresponding channel also depends on other hardware sources (serial control signals) if ENPCTRL = ’0’.
DISABLE	’1’:	The entire echo canceling path (subtractor, NLP, attenuator in send and receive path) of the corresponding channel is bypassed and the H-Register and Speech Control Unit are reset.
	’**0**’:	The disabling (bypass) of the entire canceler for the corresponding channel depends on the internal control of the speech control unit only if ENPCTRL = ’1’, The disabling (bypass) of the entire canceler for the corresponding channel also depends on other hardware sources if ENPCTRL = ’0’.
ENPCTRL	’1’:	Only the settings of the bits CONVDIS, FREEZE, NLPDIS, DISABLE are valid for the corresponding channel. All other hardware control sources (serial control signals, UCC, TS16, IDLE detection) for the corresponding channel are disabled.
	’**0**’:	The settings of the bits CONVDIS, FREEZE, NLPDIS, DISABLE for the corresponding channel are ’ored’ with other hardware control sources (serial control signals, UCC, TS16, IDLE detection).

*Note: In the case of no A-/µ-Law conversion (same Law at near and far end side) the PCM encoding law can temporarily be changed by any conversion disabling source (µP, UCC FX-Bit or serial control signal) if ICONVDISLAW is different from IALAWNE/IALAWFE

SCMASK[5:0] (Addr.: 6BH): **S**erial **C**ontrol Interface **Mask**, write protected,
Reset value = 3FH

-	-	DIS MASK	NLPDIS MASK	FREEZE MASK	CONV DIS MASK	ENCC MASK	FLEX SCTR MASK

This register is for masking of external pins of the Serial Interface. The effect of this register depends also on the value of CHCTRL0..31.ENPCTRL.

DISMASK ’**1**’: serial control signal at pin DIS disabled
’0’: serial control signal at pin DIS enabled

NLPDISMASK ’**1**’: serial control signal at pin NLPDIS disabled
’0’: serial control signal at pin NLPDIS enabled

FREEZEMASK ’**1**’: serial control signal at pin FREEZE disabled
’0’: serial control signal at pin FREEZE enabled

CONVDISMASK ’**1**’: serial control signal at pin CONVDIS disabled
’0’: serial control signal at pin CONVDIS enabled

ENCCMASK ’**1**’: serial control signal at pin ENCC disabled
’0’: serial control signal at pin ENCC enabled

FLEXSCTRMASK ’**1**’: serial control signal at pin FLEXSCTR disabled
’0’: serial control signal at pin FLEXSCTR enabled

CONFFLEXSCTR[5:0] (Addr.: 6CH): **Conf**iguration of the **flex**ible **s**erial **c**on**tr**ol signal, write protected, Reset value = 00H

-	-	FS BYPASS	FS NLPDIS	FS FREEZE	FS SCU RESET	FS HRESET	FS CONV DIS

This register determines the function of pin FLEXSCTR if bit SCMASK.FLEXSCTRMASK = ’0’

FSBYPASS ’1’: serial control signal at pin FLEXSCTR leads to bypassing of the PCM signal of the entire cancelling path (canceller ,NLP, attenuator and bypassing of the attenuator in the receive path)
’**0**’: No bypass of the entire compensator by FLEXSCTR

FSNLPDIS ’1’: serial control signal at pin FLEXSCTR disables the NLP and attenuator
’**0**’: No disabling of the NLP and attenuator by FLEXSCTR

FSFREEZE ’1’: serial control signal at pin FLEXSCTR freezes the H-Register
’**0**’: No freeze of the H-Register by FLEXSCTR

FSSCURESET ’1’: serial control signal at pin FLEXSCTR resets the attenuation meters in the speech control unit

	'**0**':	No reset of the attenuation meters unit by FLEXSCTR
FSHRESET	'1':	serial control signal at pin FLEXSCTR resets the H-Register
	'**0**':	No reset of the H-Register by FLEXSCTR
FSCONVDIS	'1':	serial control signal at pin FLEXSCTR disables the PCM-Law conversion (in receive and send path)
	'**0**':	No disable of the PCM-Law conversion by FLEXSCTR

CONFFLEXUCC[5:0] (Addr.: 6DH): **Conf**iguration of the **flex**ible **UCC** control bit (FX-Bit), write protected, Reset value = 00H

-	-	FU BYPASS	FU NLPDIS	FU FREEZE	FU SCU RESET	FU HRESET	FU CONV DIS

This register determines the function of the FX-Bit of the UCC signal. The FX bit is defined in register CONUCC.SELFX.

FUBYPASS	'1':	The FX-Bit leads to bypassing of the PCM signal of the entire cancelling path (canceller, NLP, attenuator in receive and send path)
	'**0**':	No bypass of the entire compensator by the FX-Bit
FUNLPDIS	'1':	THE FX-Bit disables the NLP and attenuator
	'**0**':	No disabling of the NLP and attenuator by the FX-Bit
FUFREEZE	'1':	THE FX-Bit freezes the H-Register
	'**0**':	No freeze of the H-Register by the FX-Bit
FUSCURESET	'1':	THE FX-Bit resets the attenuation meters in the speech controling unit
	'**0**':	No reset of the attenuation meters by the FX-Bit
FUHRESET	'1':	THE FX-Bit resets the H-Register
	'**0**':	No reset of the H-Register by the FX-Bit
FUCONVDIS	'1':	THE FX-Bit disables the PCM-Law conversion (in receive and send path)
	'**0**':	No disable of the PCM-Law conversion by the FX-Bit

Note: Clear channel (64 clear) control by the FX-Bit can be enabled by setting this register to "xx1xxxx1"

CONFFLEXMON[7:0] (Addr.: 6FH): **Conf**iguration of **Flex**ible **Mon**itor Signals, Reset value = FEH

CONF FLEX MON1[3]	CONF FLEX MON1[2]	CONF FLEX MON1[1]	CONF FLEX MON1[0]	CONF FLEX MON2[3]	CONF FLEX MON2[2]	CONF FLEX MON2[1]	CONF FLEX MON2[0]

The bits CONFFLEXMON1[3:0] and CONFFLEXMON2[3:0] configure the serial control signals FLEXMON1 and FLEXMON2, respectively.

CONFFLEXMON1[3:0] / CONFFLEXMON2[3:0]

Configuration of the flexible monitor output signal at pin FLEXMON1/ FLEXMON2

"0000":	Idle channel detected is monitored at pin FLEXMON1 / FLEXMON2
"0001":	2010 Hz speech protection: first level reached (bypass of entire canceller) is monitored at pin FLEXMON1 / FLEXMON2
"0010":	2010 Hz speech protection: second level reached (H-Register reset) is monitored at pin FLEXMON1
"0011":	2010 Hz (SS Nr.7) detected but without speech protection is monitored at pin FLEXMON1 / FLEXMON2
"0100":	Convergence stability protection for non-speech signals active is monitored at pin FLEXMON1 / FLEXMON2
"0101":	Fast convergence mode active is monitored at pin FLEXMON1 / FLEXMON2
"0110":	Near end subscriber is louder than the far end subscriber (true double talk) is monitored at pin FLEXMON1 / FLEXMON2
"0111":	Subtractor bypassed because ERL > value of BYPTHL[4:0] is monitored at pin FLEXMON1 / FLEXMON2
"1000":	2100 Hz with phase shift and speech protection detected is monitored at pin FLEXMON1 / FLEXMON2
"1001":	2100 Hz detected with speech protection is monitored at pin FLEXMON1 / FLEXMON2
"1010":	2100 Hz detected but without speech protection is monitored at pin FLEXMON1 / FLEXMON2
"1011":	"No-voice" detected is monitored at pin FLEXMON1 / FLEXMON2
"1100":	RITESTDATA in channel selected by register ATE (2 MHz stream valid only in selected test channel otherwise all zeros) is monitored at pin FLEXMON1 / FLEXMON2
"1101":	SITESTDATA in channel selected by register ATE (2 MHz stream valid only in selected test channel otherwise all zeros) is monitored at pin FLEXMON1 / FLEXMON2
"1110":	Far end speech exceeds level configured in CONFSCU3.MINLEV and background noise is monitored at pin FLEXMON1 /FLEXMON2

"1111": Near end speech exceeds level configured in CONFSCU3.MINLEV and background noise is monitored at pin FLEXMON1 /FLEXMON2

CONFIDLE[5:0] (Addr.: 32H): **Conf**iguration of **IDLE** Detection, write protected, Reset value = 1DH

-	-	ENIDLE	IDPT[2]	IDPT[1]	IDPT[0]	IDLE MODE	SELSI IDLE

For idle detection the Receive In or Send In input pattern is compared either with itself or with a maskable configurable pattern of Register IDLEPATTERN. An idle channel can be indicated in MONSTAT2.MIDLE. An idle channel can also be displayed at pins FLEXMON1 or FLEXMON2.

ENIDLE '1': Enables IDLE Detection for disabling of channels
A channel that is detected to be idling will be disabled (H-Register reset, bypass, Speech Control reset)
'**0**': Disables IDLE detection

IDPT[2:0] Determines the length of the IDLE detection/protection interval
"000": protection time = 64 ms
"001": protection time = 128 ms
"010": protection time = 512 ms
"011": protection time = 1 s
"100": protection time = 4.1 s
"101": protection time = 8.2 s
"110": protection time = 32.8s
"**111**": protection time = 65.5s (according ITU)

IDLEMODE '1': IDLE detection pattern comparison operates on the last received pattern of the actual surveyed channel
'**0**': IDLE detection pattern comparison operates on the pattern in register IDLEPATTERN

SELSIIDLE '**1**': Idle detection operates on send path input
'0': Idle detection operates on receive path input

IDLEMASK[7:0] (Addr.: 33H): **IDLE** detection bit compare **MASK**,write protected, Reset value = 00H

IDLE MASK[7]	IDLE MASK[6]	IDLE MASK[5]	IDLE MASK[4]	IDLE MASK[3]	IDLE MASK[2]	IDLE MASK[1]	IDLE MASK[0]

IDLEMASK [7:0] '1': The corresponding bit is ignored for pattern comparison
'**0**': normal operation (bit comparison enabled)

IDLEPATTERN[7:0] (Addr.: 34H): **Idlepattern**, write protected, Reset value = 55H

IDLE PAT TERN[7]	IDLE PAT TERN[6]	IDLE PAT TERN[5]	IDLE PAT TERN[4]	IDLE PAT TERN[3]	IDLE PAT TERN[2]	IDLE PAT TERN[1]	IDLE PAT TERN[0]

The reset value corresponds to a level minus infinity for A-Law encoding

IDLEPATTERN [7:0] IDLE Pattern for comparison with the receive values if CONFIDLE.IDLEMODE = ’0’

CONFTS16[5:0] (Addr.: 31H) **Conf**iguration of **TS16** CAS Evaluation for E1 frames, write protected, Reset value = 12H

-	-	ENTS16	SELSI TS16	FLINV	FL SEL[1]	FL SEL[0]	FL FREEZE

ENTS16 ’1’: TS16 CAS Evaluation enabled
’**0**’: TS16 CAS Evaluation disabled

SELSITS16 ’**1**’: TS16 CAS Evaluation operates on send path input
’0’: TS16 CAS Evaluation operates on receive path input

FLINV Inversion of selected flag bit, "Active" means an enabled time slot.
A change of this bit means a change of the incoming TS 16 flag bit.
’1’: flag bit is active ’0’
’**0**’: flag bit is active ’1’

FLSEL [1:0] Selection of flag bit (MSB of TS 16 is bit 7):
"00": En/Disable via D-Bit (bit 4 and bit 0 of TS 16 are evaluated)
"**01**": En/Disable via C-Bit (bit 5 and bit 1 of TS 16 are evaluated)
"10": En/Disable via B-Bit (bit 6 and bit 2 of TS 16 are evaluated)
"11": En/Disable via A-Bit (bit 7 and bit 3 of TS 16 are evaluated)

FLFREEZE ’1’: Freeze (no update) of flag bits
’**0**’: normal operation

CONFUCC[6:0] (Addr.: 60H): **Conf**iguration of **UCC** Interface, write protected, Reset value = 00H

-	R LISTEN	EN TUCCO	EN DISHW	SEL FX[1]	SEL FX[0]	EN SMLP HW	RSW CTRL

RLISTEN — This bit is only active in Reflect Mode which can be configured via bit CONFUCC.RSWCTRL or SMLP bit of UCC Interface.
’1’: UCCI input data will be transferred to IRAM and interrupt will be generated
’**0**’: Normal operation: No data is transferred to IRAM, no interrupts are generated except by SMLP bit in UCC special frame if unmasked.

ENTUCCO — ’1’: Control signal for external tristate buffer $\overline{\text{TUCCO}}$ is enabled for processed channels only (all 32 channels in 64 ms mode or 16 channels in 128 ms mode if bit UCCFRS.128FRSEN is set to ’1’). The mode depends on setting of Pins MODE1 and MODE0.
’**0**’: Tri-State-Buffer control signal $\overline{\text{TUCCO}}$ is disabled, i.e. = ’1’

ENDISHW — ’1’: The UCC DIS-Bit (Bit 4) of associated channel (see **Figure 10**) is used for disabling of the associated channel.
’**0**’: disable special handling of the DIS-Bit (Bit 4) for channel individual UCC frames by hardware

SELFX [1:0] — Selects the UCC bit for the flexible control bit (FX-Bit)
"11" : UCC-Bit 2 is selected
"10" : UCC-Bit 1 is selected
"01" : UCC-Bit 0 is selected
"**00**" : No UCC-Bit is selected, i.e. UCC FX-Bit is disabled

ENSMLPHW — Enables special handling of the SMLP bit in the special frame FRS by hardware if the special frame mode is enabled (Bit NOFRS = ’0’)
’1’: The reflection of UCCI to UCCO is activated by the hardware at the beginning of the next channel individual frame after the bit SMLP in FRS (UCC Special Frame) changes from ’0’ to ’1’. The value of the current FRS is the last that is transferred to IRAM, all the following FRS’s will no longer be transferred to the IRAM. Only a change of the SLMPbit in FRS is indicated by an interrupt if not maked by IMASKFRS[7]. Additionally the current status of the channel individual control bits DIS-Bit and FX-Bit is frozen. This reflection is deactivated with the beginning of the next channel individual frame after the FRS, in which the hardware detects a ’1’ to ’0’ change of the SMLP bit. The value of this FRS is transferred to the IRAM.
’**0**’: normal operation, reflection control by bit RSWCTRL

RSWCTRL — Only effective if ENSMLPHW = ’0’, Reflection control by software.
’1’: The reflection of UCCI to UCCO is activated by the software, not by the hardware via SMLP bit evaluation. Only a change of the SLMP in FRS is indicated, and the current status of the channel individual control bits DIS-Bit and FX-Bit is frozen.
The timing for de/activation of the reflection depends solely on

the performance of the software and is unpredictable!
'**0**': normal operation

Note: In 128 ms mode the DIS-Bit and the FX-Bit are only evaluated in the 16 processed channels.

UCCMFR[4:0] (Addr.: 61H): **UCC Multifr**ame Alignment, write protected, Reset value = 00H

-	-	-	UCC MFR[4]	UCC MFR[3]	UCC MFR[2]	UCC MFR[1]	UCC MFR[0]

UCCMFR[4:0] Denotes the UCC frame number for the next complete UCC frame (beginning with bit 7, phase 0, channel 0) after the first detection of an active SYNCI impulse with the falling edge of SCLKI (UCC frame alignment is configured by register UCCALIGN). For explanation see also **Figure 25** and **Figure 26**.

UCCFRS[6:0] (Addr.: 62H): Selection of the special **UCC** Frame **FRS**, write protected, Reset value = 00H

-	NOFRS	128FRS EN	UCC FRS[4]	UCC FRS[3]	UCC FRS[2]	UCC FRS[1]	UCC FRS[0]

NOFRS '1': The UCC frame corresponding to the value in UCCFRS[4:0] is not handled as the special UCC frame containing global SIDEC information but as a frame that contains channel individual information (like the other UCC frames)
'**0**': The UCC frame corresponding to the value in UCCFRS[4:0] is handled as the special UCC frame that contains global SIDEC related (not channel individual) information.
Note: If this setting is configured, the PCM channel that corresponds to the value in UCCFRS[4:0] can not individually be controlled directly via UCC and is considered as a PCM channel containing no payload data. The DIS-Bit and the FX-Bit are not evaluated for this channel and set inactive. It is the responsibility of the software to disable the Echo Canceller and Law conversion function via the channel individual control registers CHCTR* in order to enable the transparent (64-clear) mode for this channel.

128FRSEN '1': enables the output of all frames at UCCO and the activation of TUCCO for all frames in 128 ms mode even if the number does not correspond to one of the 16 processed channels.*

	'**0**': disables the output of all frames at UCCO and the activation of TUCCO for all frames in 128 ms mode if the number does not correspond to one of the 16 processed channels.*
UCCFRS[4:0]	Denotes the frame number of the special UCC frame FRS.

*Caution: The activation of the bit 128FRSEN is solely intended for a configuration where only one SIDEC in 128 ms mode is used for one PCM30 interface processing only 16 channels. If two SIDECs in 128 ms master and slave mode are used in parallel for one PCM interface the activation of this bit could result in severe damage of the external driver at the UCCO bus.

WRUCC[5:0] (Addr.: 63H): **W**rite/**R**ead **UCC**I, Reset value = 00H

-	-	WRO RAM	ARAM[4]	ARAM[3]	ARAM[2]	ARAM[1]	ARAM[0]

WRORAM	'1': Write access: the byte stored in register DORAM is written to the UCC output RAM (ORAM) at UCC frame number ARAM [4:0].
	'**0**': read access: the byte stored in the UCC input RAM (IRAM) at UCC frame number ARAM [4:0] is copied to register DIRAM. Data can be read after 8 CLK32 cycles.
ARAM [4:0]	Value corresponds to the ORAM or IRAM address where data is written to or read from

DORAM[7:0] (Addr.: 64H): **D**ata **O**utput **RAM**, Reset value = 00H

DO RAM[7]	DO RAM[6]	DO RAM[5]	DO RAM[5]	DO RAM[3]	DO RAM[2]	DO RAM[1]	DO RAM[0]

DORAM [7:0]	Data to be written to the ORAM at address WRUCC. ARAM [4:0]

IMASKFRS[7:0] (Addr.: 65H): **I**nterrupt **Mask** for the special UCC frame **FRS**, Reset value = 00H

IMASK FRS[7]	IMASK FRS[6]	IMASK FRS[5]	IMASK FRS[4]	IMASK FRS[3]	IMASK FRS[2]	IMASK FRS[1]	IMASK FRS[0]

IMASKFRS[7:0]	Each activated (set to '1') mask bit prevents the generation of an UCC interrupt at a change of the corresponding bit in FRS.

Note: In 128 ms mode the change of an unmasked bit generates an interrupt condition only if the frame number of the special UCC frame corresponds to one of the 16 processed channels or bit UCCFRS.128FRSEN is set to '1'.

IMASKFRN[7:0] (Addr.: 66H): **I**nterrupt **Mask** for channel individual UCC frames (**FRN**), Reset value = 00H

IMASK FRN[7]	IMASK FRN[6]	IMASK FRN[5]	IMASK FRN[4]	IMASK FRN[3]	IMASK FRN[2]	IMASK FRN[1]	IMASK FRN[0]

IMASKFRN[7:0] Each activated (set to ’1’) mask bit prevents the generation of an UCC interrupt at a change of the corresponding bit in any channel individual UCC frame FRN.

Note: In 128 ms mode the change of an unmasked bit in one of the channel individual UCC frames generates an interrupt condition only if the frame number of the changed frame corresponds to one of the 16 processed channels or bit UCCFRS.128FRSEN is set to ’1’.

TESTTIMER[1:0] (Addr.: 37H): µP **Test** and **Timer**, write protected, Reset value = 00H

-	-	-	-	-	-	UPTEST	RUN TIMER

UPTEST enable for the self test:
’1’: self test is executed in the test channel selected by ATE and values of register CTRLTEST are evaluated. This channel is bypassed according to **Figure 9** with "BYPASS".
’**0**’: self test disabled

RUNTIMER ’1’: start timer*
’**0**’: disable/stop timer*

* Note: For using the timer in conjunction with the self-test, the timer should be started at the same time the test is activated.

ATE[4:0] (Addr.: 35H): **A**ddress of **Te**st-channel, write protected, Reset value = 00H

-	-	-	ATE[4]	ATE[3]	ATE[2]	ATE[1]	ATE[0]

ATE [4:0] On the one hand this value corresponds to the channel for which the determination is made if it is en/disabled (result in bit TSEN in register SFATSES). On the other hand, the value corresponds to the channel in which the test is executed.

Note: A test can only be executed in a disabled channel. Therefore, it must be determined whether the channel is en/disabled. Once a test is started it can only be terminated by the software by resetting the bit TESTTIMER.UPTEST. If the channel that is background tested by the software suddenly becomes enabled by external sources before the test is terminated an interrupt is generated that informs the software to abort the test immediately.

CTRLTEST[7:0] (Addr.: 38H): **Contr**o**l** of **test** channel, Reset value = 00H

T FREEZE	T NLPDIS	T ATTDIS	T SINDIS	T EN	T ALAW	T EDEL[1]	T EDEL[0]

TFREEZE — Freeze of speech control unit and H-Register in selected test channel:
'1': speech control unit and H-Register are frozen
'**0**': normal operation

TNLPDIS — NLP disable (bypass) in selected test channel:
'1': NLP disabled
'**0**': normal operation

TATTDIS — Disable of output attenuator in selected test channel:
'1': Attenuator disabled
'**0**': normal operation, according to setting of register CONFPCM

TSINDIS — Disable of "no speech" detection in selected test channel:
'1': "no speech" detection disabled
'**0**': normal operation

TEN — En/Disable of selected test channel:
'1': test channel enabled
'**0**': test channel disabled (H-Register and Attenuation meters reset)

TALAW — PCM encoding Law selection of selected test channel:
'1': test channel A-Law encoded
'**0**': test channel µ-Law encoded

TEDEL [1:0] — end echo delay for test pattern:
"11": 7*125 µs
"10": 6*125 µs
"01": 5*125 µs
"**00**": 4*125 µs

Note: For the internal functionality of the channel that is tested in the background all external control sources have no effect.

TSGSPP[7:0] (Addr.: 39H): **T**est **s**ignal **g**enerator for **s**end **p**ath **p**attern, Reset value = 55H

SG MOD1	SPTP[6]	SPTP[5]	SPTP[4]	SPTP[3]	SPTP[2]	SPTP[1]	SPTP[0]

SGMOD1 operation mode1 for signal generator (see **Table 21**)
SPTP [6:0] Send path test pattern amplitude, log, A-/µ-Law encoded

TSGRPP[7:0] (Addr.: 3AH): **T**est **s**ignal **g**enerator for **r**eceive **p**ath **p**attern,
Reset value = 55H

SG MOD0	RP TP[6]	RP TP[5]	RP TP[4]	RP TP[3]	RP TP[2]	RP TP[1]	RP TP[0]

SGMOD0 operation mode 0 for signal generator (see **Table 21**)
RPTP[6:0] receive path test pattern amplitude, log, A-/µ-Law encoded

The sign of the test sequence is determined by the following table. The amplitude is given by TSGSPP[6:0] and TSGRPP[6;0]. Hence, rectified test signals are generated (see **Figure 38**).

SGMOD1	SGMOD0	Test Signal Sign changes according to:
0	**0**	2105 Hz
0	1	2105 Hz inverted
1	0	2010 Hz
1	1	random sequence

Table 21 Settings of SGMOD1 and SGMOD0 of register TSGSPP and TSGRPP, respectively

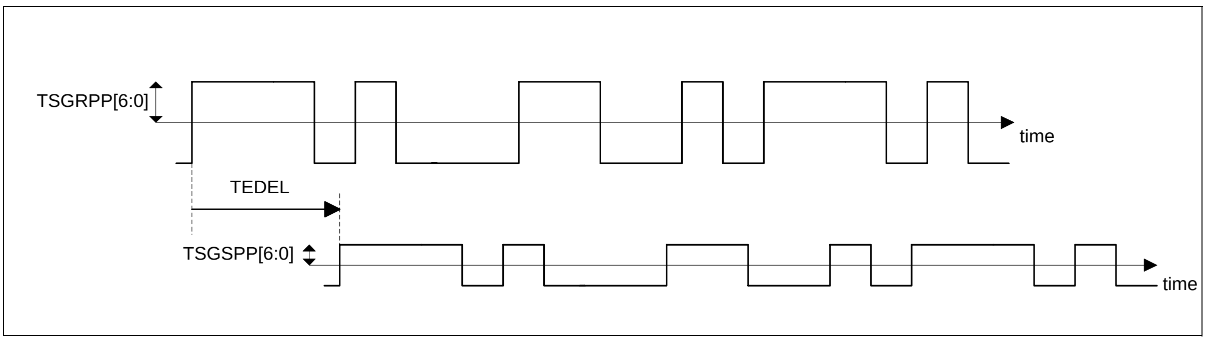

Figure 38 Explanation of Test Pattern Generation (random sign signal)

HTIM[7:0] (Addr.: 3BH): **H**igh-Byte for **Tim**er, Reset value = 00H

TIM[15]	TIM[14]	TIM[13]	TIM[12]	TIM[11]	TIM[10]	TIM[9]	TIM[8]

The timer can be used by the processor, if the processor wants to do different operations inbetween. The timer is counting downward. The timing decrement is 1 ms. The accuracy of the timer is +0 ... 1 ms. The maximum value is 65535 ms.

TIM[15:8] load value for the Timer (high byte)

LTIM[7:0] (Addr. 3CH): **L**ow-Byte for **Tim**er, Reset value = 00H

TIM[7]	TIM[6]	TIM[5]	TIM[4]	TIM[3]	TIM[2]	TIM[1]	TIM[0]

TIM[7:0] load value for the Timer (low byte)

CONFSCU1[7:0] (Addr.: 12H): **Conf**iguration of **s**peech **c**ontrol **u**nit **1**, write protected, Reset value = 69H

BN ADD[3]	BN ADD[2]	BN ADD[1]	BN ADD[0]	ADAPT FAST[1]	ADAPT FAST[0]	ADAPT SLOW[1]	ADAPT SLOW[0]

BNADD [3:0] Safety distance for SO > background noise + BNADD comparison

"0000": +0 dB "0001": 1.5 dB
"0010": 3 dB "0011": 4.5 dB
"0100": 6 dB "0101": 7.5 dB
"**0110**": 9 dB "0111": 10.5 dB
"1000": 12 dB "1001": 13.5 dB
"1010": 15 dB "1011": 16.5 dB
"1100": 18 dB "1101": 21 dB
"1110": 22.5 dB "1111": 24 dB

Attenuation Measurement

ADAPTFAST[1:0] Fast count period for attenuation meters for total echo attenuation and transhybrid loss
"00": 2 ms "01": 1 ms "**10**": 500 µs "11": 250 µs

ADAPTSLOW[1:0] Slow count period for attenuation meters for total echo attenuation and transhybrid loss
"00": 64 ms "**01**": 32 ms "10": 16 ms "11": 8 ms

CONFSCU2[7:0] (Addr.: 13H): **Conf**iguration of **s**peech **c**ontrol **u**nit **2**, write protected, Reset value = 97H

BYP THL[4]	BYP THL[3]	BYP THL[2]	BYP THL[1]	BYP THL[0]	RE ADD[1]	RE ADD[0]	DHHLEC

BYPTHL[4:0] Transhybrid loss as of which the canceling unit is bypassed
"00000": 0 dB
"00001": 3 dB
"00010": 6 dB
"00011": 9 dB
"00100": 12 dB
...
"**10010**": 54 dB
...
"11111": 93 dB (theoretical value only, attenuation will never be reached)

READD[1:0] Safety distance for SO > residual echo + READD comparison
"00": +0 dB "01": +3 dB "10": +6 dB "**11**": +9 dB

DHHLEC ’**1**’:Enables detection of a change in end echo path in the case of high hybrid loss
’0’: disabled

CONFSCU3[7:0] (Addr.: 14H): **Conf**iguration of **s**peech **c**ontrol **u**nit **3**, write protected, Reset value = A4H

MIN LEV[4]	MIN LEV[3]	MIN LEV[2]	MIN LEV[1]	MIN LEV[0]	DT TIME[1]	DT TIME[0]	ITUDT

H-Register Control:

MINLEV[4:0] Minimum level of SI and RI for controlling of the coefficients (H-Register)
"00000": minus infinite, no residual echo limitation
"00001": -67.5 dBm0
"00010": -66.0 dBm0
"00011": -64.5 dBm0
"00100": -63 dBm0
...
"**10100**": -39.0 dBm0
...
"11111": -22.5 dBm0

Double Talk:

DTTIME[1:0] Double talk hangover time
"00": 32 ms "01": 64 ms "**10**": 128 ms "11": 256 ms

ITUDT '**0**': double talk detection operates up to 0 dB transhybrid loss
'1': double talk detection according ITU: transhybrid loss greater or equal 6 dB

CONFSCU4[7:0] (Addr.: 15H): **Conf**iguration of **s**peech **c**ontrol **u**nit **4**, write protected, Reset value = A7H

OC INC[1]	OC INC[0]	OC DEC[1]	OC DEC[1]	SI ADD[1]	SI ADD[0]	OC AMRES	OC HRES

Overcompensation:

OCINC[1:0] Increment period for overcompensation evaluation
"00": 32 ms "01": 16 ms "**10**": 8 ms "11": 4 ms

OCDEC[1:0] Decrement period for overcompensation evaluation
"00": 16 ms "01": 8 ms "**10**": 4 ms "11": 2 ms

SIADD[1:0] Safety distance for SO > SI + SIADD comparison
"00": +0 dB "**01**": +3 dB "10": +6 dB "11": +9 dB

OCAMRES '0': no reset of attenuation meters in case of overcompensation
'**1**': reset of attenuation meters only in case of overcompensation

OCHRES '0':no reset via overcompensation detection
'**1**': reset via overcompensation detection (H-Register reset only)

CONFSCU5[7:0] (Addr.: 16H): **Conf**iguration of **s**peech **c**ontrol **u**nit **5**, write protected, Reset value = 84H

NLP RANGE [4]	NLP RANGE [3]	NLP RANGE [2]	NLP RANGE [1]	NLP RANGE [0]	SWMIN ATT[2]	SWMIN ATT[1]	SWMIN ATT[0]

Non Linear Processor (NLP) activation

NLPRANGE[4:0] Operating range for the NLP
"00000": minus infinite: no residual echo limitation
"00001": -66 dBm0
"00010" -63 dBm0
"00011": -60 dBm0
"00100": -57 dBm0
...
"**10000**": -21 dBm0
...
"11000": +3 dBm0

SWMINATT[2:0]	Minimum attenuation for switchover to final residual echo level "000": 0 dB "001": 3 dB "010": 6 dB "011": 9 dB "**100**": 12 dB "101": 15dB "110": 18dB "111": 21dB

CONFSCU6[7:0] (Addr.: 17H): **Conf**iguration of **s**peech **c**ontrol **u**nit **6**, write protected, Reset value = 2AH

REL ADD[2]	REL ADD[1]	REL ADD[0]	RI MIN[2]	RI MIN[1]	RI MIN[0]	OF CNT[1]	OF CNT[0]

RELADD[2:0]	Safety increment for the residual echo limiter threshold "000": 0 dB "**001**": 3 dB "010": 6 dB "011": 9 dB "100": 12 dB "101": 15 dB "110": 18 dB "111": 21 dB
RIMIN[2:0]	Reduction of receive path level for determination of the temporary NLP threshold "000": 0 dB "001": 3 dB "**010**": 6 dB "011": 9 dB "100": 12 dB "101": 15 dB "110": 18 dB "111": 21 dB
Offset:	
OFCNT[1:0]	Count period for offset measurements "00": disabled "01": 64 ms **"10"**: 16 ms "11": 1 ms

CONFSCU7[7:0] (Addr.: 18H): **Conf**iguration of **s**peech **c**ontrol **u**nit **7**, write protected, Reset value = 8AH

NOISE INC[3]	NOISE INC[2]	NOISE INC[1]	NOISE INC[0]	BN INC[1]	BN INC[0]	BN DEC[1]	BN DEC[0]

NLP comfort noise:	
NOISEINC[3:0]	Increase of the noise level for maximum level evaluation "0000": -6 dB "0001": -4.5 dB "0010": -3 dB "0011": -1.5 dB "0100": +0 dB "0101": +1.5 dB "0110": +3 dB "0111": +4.5 dB "**1000**": +6 dB "1001": +7.5 dB "1010": +9 dB "1011": +10.5 dB "1100": +12 dB "1101": +13.5 dB "1110": +15 dB "1111": +16.5 dB
BNINC[1:0]	Incrementing period for background noise evaluation counter "00": 64 ms "01": 32 ms "**10**": 16 ms "11": 8 ms
BNDEC[1:0]	Decrementing period for background noise evaluation counter

"00": 16 ms "01": 8 ms "**10**": 4 ms "11": 2 ms

CONFSCU8[7:0] (Addr.: 19H), **Conf**iguration of **s**peech **c**ontrol **u**nit **8**, write protected, Reset value = EEH

BNMAX SL[3]	BNMAX SL[2]	BNMAX SL[1]	BNMAX SL[0]	BNMAX RL[3]	BNMAX RL[2]	BNMAX RL[1]	BNMAX RL[0]

BNMAXSL[3:0] Maximum send path level for background noise measurement
"0000": minus infinite
"0001": -66 dBm0
"0010": -63 dBm0
"0011": -60 dBm0
"0100": -57 dBm0
...
"**1110**": -27 dBm0
"1111": -24 dBm0 (not possible)

BNMAXRL[3:0] Maximum receive path level for background noise measurement
"0000": minus infinite
"0001": -66 dBm0
"0010": -63 dBm0
"0011": -60 dBm0
"0100": -57 dBm0
...
"**1110**": -27 dBm0
"1111": -24 dBm0 (not possible)

CONFSCU9[7:0] (Addr.: 1AH), **Conf**iguration of **s**peech **c**ontrol **u**nit **9**, write protected, Reset value = 44H

DISBY	PSBY	DISNLP DIS	PSNLP DIS	DIS HRES	PS HRES	PSLM RES	DIS RES

Bypass of Non Linear Processor (NLP), Subtractor and Attenuator (Receive and Send path):

DISBY '**0**': no bypass via 2100 Hz Disabler without phase shift
'1': bypass via 2100 Hz Disabler even without phase shift

PSBY '0': no bypass via 2100 Hz Disabler even with phase shift
'**1**': bypass via 2100 Hz Disabler with phase shift

Disable/Bypass of NLP:

DISNLPDIS '**0**': no disable via 2100 Hz Disabler without phase shift
'1': disable via 2100 Hz Disabler even without phase shift

PSNLPDIS ’**0**’: no disable via 2100 Hz Disabler even with phase shift
’1’: disable via 2100 Hz Disabler with phase shift

Coefficient (H-Register) reset:

DISHRES ’**0**’: no reset via 2100 Hz Disabler without phase shift
’1’: reset via 2100 Hz Disabler even without phase shift

PSHRES ’0’: no reset via 2100 Hz Disabler even with phase shift
’**1**’: reset via 2100 Hz Disabler with phase shift

Reset of attenuation meters in SCU:

PSLMRES ’**0**’: no reset of via 2100 Hz Disabler even with phase shift
’1’: reset via 2100 Hz Disabler with phase shift

DISRES ’**0**’: no reset via 2100 Hz disable tone without phase shift
’1’: reset via 2100 Hz disable tone even without phase shift

CONFSCU10[7:0] (Addr.: 1BH): **Conf**iguration of **s**peech **c**ontrol **u**nit **10**, write protected, Reset value = C0H

DIS LOCK[4]	DIS LOCK[3]	DIS LOCK[2]	DIS LOCK[1]	DIS LOCK[0]	DIS 56EN	ITU DIS	SP PROT

Additional Controls:

DISLOCK[4:0] Self-locking level after response of the 2100 Hz tone disabler.
The tone disabler is inactive if the level is below the following value.

"00000":	minus infinite
"00001":	-67.5dBm0
"00010":	-66.0dBm0
"00011":	-64.5dBm0
"00100":	-63 dBm0
...	
"**11000**":	-33.0 dBm0
...	
"11111":	-22.5 dBm0

DIS56EN ’**0**’: no special evaluation of bit 8 (LSB) in T1 frames for modem calls
’1’: special evaluation of bit 8 (LSB) in T1 frames for modem calls: If all bit 8 (LSB) are ’1’ the first seven bit will bypass the echo canceller.

ITUDIS ’**0**’: drop out time for tone disabler up to > 400 ms (necessary for some modems). Interruption up to 400 ms of modem tone does not cause enabling of canceller.
’1’: drop out time for tone disabler < 400 ms according ITU

SPPROT Speech protection for 2100 Hz tone detection:

'**0**': normal speech protection
'1': Increased Speech protection

VDFCTRL[7:0] (Addr.: 76H): **V**oice **D**etection **F**reeze **Con**t**r**o**l**,
write protected, Reset value = B4H

VDF RELEN	VDF REL[2]	VDF REL[1]	VDF REL[0]	VD FSOL[3]	VD FSOL[2]	VD FSOL[1]	VD FSOL[0]

VDFRELEN '0': No freeze of H-Register on no voice detection when combined loss (ERL+ERLE) > VDFREL
'**1**':Freeze of H-Register on no voice detection when combined loss (ERL+ERLE) > VDFREL

VDFREL[2:0]: Threshold for total echo loss (ERL+ERLE) at which H-Register are frozen on a no voice signal detection if VDFRELEN = '1'
"000": 27 dB "001": 28.5 dB
"010": 30 dB "**011**": 31.5 dB
"100": 33 dB "101": 34.5 dB
"110": 36 dB "111": 37.5 dB

VDFSOL[3:0] Threshold for residual echo level at Send Out below which the H-Register are frozen on a 'no voice' signal.
"0000":minus infinite: no freezing for periodic signals
"0001":-66 dBm0
"0010":-63 dBm0
"0011":-60 dBm0
"**0100**":-57 dBm0
...
"1101":-30 dBm0
"1110":-27 dBm0
"1111":-24 dBm0

CONFPSD[7:0] (Addr.: 1CH): **Conf**iguration of 2100 Hz tone **p**hase **s**hift **d**etector,
write protected, Reset value = 43H

DT30DIS	DEP[1]	DEP[0]	DBP MIN[1]	DBP MIN[0]	DBP MAX[2]	DBP MAX[1]	DBP MAX[0]

DT30DIS '**0**': disable evaluation if phase shift detection of >30 ms is identified
'1': enable phase shift detection >30 ms

DEP[1:0] Evaluation time:
If no phase shift is detected in the time interval below the evaluation is terminated.

	"00": 749 ms	"01": 833 ms
	"**10**": 916 ms	"11": 999 ms
DBPMIN[1:0]	Minimum interruption time that results in response:	
	"**00**": 1.125 ms	"01": 2.250 ms
	"10": 3.375 ms	"11": 4.500 ms
DBPMAX[2:0]	Maximum interruption time that results in response:	
	"000": 27 ms	"001": 28 ms
	"010": 29 ms	"**011**": 30 ms
	"100": 32 ms	"101": 33 ms
	"110": 34 ms	"111": 35 ms

DBPMIN[1:0] and DBPMAX[2:0] determine the evaluation window.

CONFSS7[7:0] (Addr.: 1DH): **Conf**iguration of **SS7** continuity check tone detection, write protected, Reset value = 00H

DIS NR7[3]	DIS NR7[2]	DIS NR7[1]	DIS NR7[0]	BY NR7[3]	BY NR7[2]	BY NR7[1]	BY NR7[0]

If CONFSS7[7:0] = 00H the 2010 Hz tone detection is disabled.

DISNR7[3:0]	protection time for reset of H-register after SS7 continuity check tone detection. For this time the 2010 Hz signal must be applied to the SIDEC to reset the H-Register.	
	"**0000**": no reset	"0001": 8ms
	"0010": 16ms	"0011": 24ms
	"0100": 32ms	"0101": 40ms
	"0110": 48ms	"0111": 56ms
	"1000": 64ms	"1001": 72ms
	"1010": 80ms	"1011": 88ms
	"1100": 96ms	"1101": 104ms
	"1110": 112ms	"1111": 120ms
BYNR7[3:0]	protection for bypass of the canceller after SS7 continuity check tone detection. For this time the 2010 Hz signal must be applied to the SIDEC to bypass the Echo Canceller.	
	"**0000**": no bypass	"0001": 8ms
	"0010": 16ms	"0011": 24ms
	"0100": 32ms	"0101": 40ms
	"0110": 48ms	"0111": 56ms
	"1000": 64ms	"1001": 72ms
	"1010": 80ms	"1011": 88ms
	"1100": 96ms	"1101": 104ms
	"1110": 112ms	"1111": 120ms

CONFCC[6:0] (Addr.: 0BH) **Config**uration of **C**lock **C**ontrol unit, write protected,
Reset value = 00H

-	INV CTRL32	SYNC ACT	SYNCO DUR	SSCLK EDGE	DIS CTRL32	DIS SCLKO	DIS CLK4O

INVCTRL32	’1’:	Inverts the control voltage signal for the 32MHz VCO at pin CTRL32 (see **Figure 23**)
	’**0**’:	no inversion of the control voltage signal for the 32MHz VCO at pin CTRL32 (see **Figure 23**)
SYNCACT	’1’:	SYNCI/SYNCO is active high (active edge is the rising edge)
	’**0**’:	SYNCI/SYNCO is active low (active edge is the falling edge)
SYNCODUR	’1’:	SYNCO duration is 2 SCLK periods
	’**0**’:	SYNCO duration is 1 SCLK period
SSCLKEDGE	’1’:	SYNCI is sampled with the rising edge of SCLKI, SYNCO is output with the falling edge of SCLKI (see **Figure 21**).
	’**0**’:	SYNCI is sampled with the falling edge of SCLKI, SYNCO is output with the rising edge of SCLKI (see **Figure 21**).
DISCTRL32	’1’:	disables (constantly set to ’1’) the output of the control voltage signal for the 32MHz VCO at pin CTRL32
	’**0**’:	enables the output of the control voltage signal for the 32MHz VCO at pin CTRL32
DISSCLKO	’1’:	disables (constantly set to ’1’) the output of the system clock at pin SCLKO
	’**0**’:	enables the output of the system clock at pin SCLKO
DISCLK4O	’1’:	disables (constantly set to ’1’) the output of the clock at pin CLK4O
	’**0**’:	enables the output of the clock at pin CLK4O

FSLIPIV[6:0] (Addr.: 0CH) **F**rame **slip** safety **i**nter**v**al, write protected,
Reset value = 28H

-	RF CLKEX	RFN	FSLIP IV[4]	FSLIP IV[3]	FSLIP IV[2]	FSLIP IV[1]	FSLIP IV[0]

RFCLKEX	’1’:	Selects RFCLKEX as reference clock for the 16MHz PLL
	’**0**’:	Selects RFCLKN or RFCLKF (depending on bit RFN)as reference clock for the 16MHz PLL
RFN	’**1**’:	Selects RFCLKN as reference clock for the 16MHz PLL if bit RFCLKEX = ’0’, and $\overline{\text{RFSPN}}$ as external data buffer sync pulse
	’0’:	Selects RFLCKF as reference clock for the 16MHz PLL if bit RFCLKEX = ’0’, and $\overline{\text{RFSPF}}$ as external data buffer sync pulse

FSLIPIV[4:0] Determines the safety interval around the SYNCO pulse, which represents the minimum allowed distance between SYNCO and RFSPN or RFSPF in 2 µs steps. If the distance between RFSPN/F and SYNCO becomes smaller than FSLIPIV[4:0] * 2 µs, SYNCO will jump to the optimal distance of 62.5 µs with respect to RFSPN/F (frame slip). The default value is "**01000**".

RIALIGN[7:0] (Addr.: 0DH): **R**eceive **i**nput frame **align**ment, write protected, Reset value = 00H.

RI ALIGN[7]	RI ALIGN[6]	RI ALIGN[5]	RI ALIGN[4]	RI ALIGN[3]	RI ALIGN[2]	RI ALIGN[1]	RI ALIGN[0]

RIALIGN[7:0] Determines the valid frame bit of the receive input PCM frame (starting with bit 7 channel 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. (00H = bit 7, channel 0; FFH = bit 0, channel 31). For explanation see **Figure 19**.

SIALIGN[7:0] (Addr.: 0EH): **S**end **i**nput frame **align**ment, write protected, Reset value = 00H.

SI ALIGN[7]	SI ALIGN[6]	SI ALIGN[5]	SI ALIGN[4]	SI ALIGN[3]	SI ALIGN[2]	SI ALIGN[1]	SI ALIGN[0]

SIALIGN[7:0] Determines the valid frame bit of the send input PCM frame (starting with bit 7 channel 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. (00H = bit 7, channel 0; FFH = bit 0, channel 31). For explanation see **Figure 19**.

SOALIGN[7:0] (Addr.: 0FH): **S**end **o**utput frame **align**ment, write protected, Reset value = 00H.

SO ALIGN[7]	SO ALIGN[6]	SO ALIGN[5]	SO ALIGN[4]	SO ALIGN[3]	SO ALIGN[2]	SO ALIGN[1]	SO ALIGN[0]

SOALIGN[7:0] Determines the valid frame bit of the send output PCM frame (starting with bit 7 channel 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. (00H = bit 7, channel 0; FFH = bit 0, channel 31). For explanation see **Figure 19**.

UCCALIGN[7:0] (Addr.: 10H): **UCC** frame **align**ment,write protected, Reset value = 00H

UCC ALIGN[7]	UCC ALIGN[6]	UCC ALIGN[5]	UCC ALIGN[4]	UCC ALIGN[3]	UCC ALIGN[2]	UCC ALIGN[1]	UCC ALIGN[0]

UCCALIGN[7:0] Determines the valid frame bit of the UCC frame (starting with bit 7 channel 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. (00H = bit 7, channel 0; FFH = bit 0, channel 31). For explanation see **Figure 25**.

PHALIGN[7:0] (Addr. 11H): Bit **Ph**ase **align**ment for RI, SI, SO and UCC, write protected, Reset value = 00H,

UCCPH ALIGN[1]	UCCPH ALIGN[0]	SOPH ALIGN[1]	SOPH ALIGN[0]	SIPH ALIGN[1]	SIPH ALIGN[0]	RIPH ALIGN[1]	RIPH ALIGN[0]

UCCPHALIGN[1:0] Determines the valid bit phase of the UCC frame bit (starting with phase 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. ("00" = bit phase 0, "11" = bit phase 3) For explanation see **Figure 25**.

SOPHALIGN[1:0] Determines the valid bit phase of the send output frame bit (starting with phase 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. ("00" = bit phase 0, "11" = bit phase 3) For explanation see **Figure 19**.

SIPHALIGN[1:0] Determines the valid bit phase of the send input frame bit (starting with phase 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. ("00" = bit phase 0, "11" = bit phase 3) For explanation see **Figure 19**.

RIPHALIGN[1:0] Determines the valid bit phase of the receive input frame bit (starting with phase 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. ("00" = bit phase 0, "11" = bit phase 3) For explanation see **Figure 19**.

ASTOC[7:0] (Addr.:70H): **A**FI **S**aw-**T**ooth and **O**ffset **C**haracteristic, write protected, Reset value = 00H

ST RISE[2]	ST RISE[1]	ST RISE[0]	ST FALL[2]	ST FALL[1]	ST FALL[0]	AMPL[1]	AMPL[0]

Low frequency components are superimposed to the Receive In AFI input signal to increase stability. Under normalconditions this superimposition is not necessary.

STRISE[2:0] Saw-tooth rising clock frequency

STFALL[2:0] Saw-tooth falling clock frequency
The clock for the increasing a decreasing saw tooth offset voltage is:

"**000**": 4 kHz	"001": 2 kHz
"010": 1 kHz	"011": 500 Hz
"100": 250 Hz	"101": 125 Hz
"110": 62.5 Hz	"111": 31.25 Hz

If STRISE[2:0] and STFALL[2:0] are set to "000", the clock will be switched off.

AMPL[1:0] Saw-tooth and offset amplitude:
The maximum values of the saw tooth characteristic or offset (clock is switched off) are:

"**00**": 15	"01": 31
"10": 63	"11": 127

These values will be added to the linearized receive path signals. The max. linearized value in A/µLaw Code is 8064/8031

AFSTC[6:4,2:0] (Addr.:71H): **A**FI **F**ilter **S**pring **T**imer **C**onfiguration, write protected, Reset value = 44H**,**

-	AC SPT[2]	AC SPT[1]	AC SPT[0]	-	C SPT[2]	C SPT[1]	C SPT[0]

Additional damping of the Coefficients. This feature is disabled as soon as the coefficients are frozen.

ACSPT[2:0] Aux. coefficients spring timer

CSPT[2:0] Coefficients spring timer
The period for ACSPT[2:0] and CSPT[2:0] is:

"000": 250 µs	"001": 500 µs
"010": 1 ms	"011": 2 ms
"**100**": 4ms	"101": 8 ms
"110": 16 ms	"111": 32 ms

AEEPD[3:0] (Addr.: 72H): **A**FI **E**nd **E**cho **P**ath **D**elay, write protected, Reset value = 0FH

-	-	-	-	DELAY [3]	DELAY [2]	DELAY [1]	DELAY [0]

DELAY[3:0] End echo path delay:
Depending on the presumed delay in the end echo path, this register is set to DELAY := <echo_delay> / 8 ms -1. Thus, the AFI handles end echo path delays in the range 8 ms to 128 ms. For end echo

delays > 64 ms, a tandem configuration of two SIDEC ASICs has to be used in which a single SIDEC chip processes only every other four channels:

Master:	0,1,2,3,	8,9,10,11,	16,17,18,19,	24,25,26,27
Slave:	4,5,6,7,	12,13,14,15,	20,21,22,23,	28,29,30,31

If the 128 ms mode is not selected (pins MODE0 and MODE1), any DELAYs > 64 ms in register AEEPD are interpreted as 64 ms.

"0000": 8 ms	"0001": 16 ms
"0010": 24 ms	"0011": 32 ms
"0100": 40 ms	"0101": 48 ms
"0110": 56 ms	"0111": 64 ms
"1000": 72 ms	"1001": 80 ms
"1010": 88 ms	"1011": 96 ms
"1100": 104 ms	"1101": 112 ms
"1110": 120 ms	"**1111**": 128 ms

AVDDI[7:0] (Addr.: 73H): **A**FI **V**oice **D**etection, **D**etection **I**ntervals, write protected, Reset value = 77H

VDMAX INTER VAL[3]	VDMAX INTER VAL[2]	VDMAX INTER VAL[1]	VDMAX INTER VAL[0]	VD INTER VAL[3]	VD INTER VAL[2]	VD INTER VAL[1]	VD INTER VAL[0]

VDMAXINTERVAL[3:0]

Time interval for detecting maximum value for "no-voice" detection: VDMAXINTERVAL defines the time range over which the maximum of the received values for "no-voice"-detection is determined.

"0000": 8 ms	"0001": 16 ms
"0010": 24 ms	"0011": 32 ms
"0100": 40 ms	"0101": 48 ms
"0110": 56 ms	"**0111**": 64 ms
"1000": 72 ms	"1001": 80 ms
"1010": 88 ms	"1011": 96 ms
"1100": 104 ms	"1101": 112 ms
"1110": 120 ms	"1111": 128 ms

VDINTERVAL[3:0]

Time interval for voice detection:
VDINTERVAL defines the time range over which received values are checked for "no-voice"-detection. The coding is the same as for AEEPD.DELAY.

"0000": 8 ms	"0001": 16 ms
"0010": 24 ms	"0011": 32 ms

"0100": 40 ms	"0101": 48 ms
"0110": 56 ms	"**0111**": 64 ms
"1000": 72 ms	"1001": 80 ms
"1010": 88 ms	"1011": 96 ms
"1100": 104 ms	"1101": 112 ms
"1110": 120 ms	"1111": 128 ms

AVDHG[7:0] (Addr.: 74H): **A**FI **V**oice **D**etection, **H**ysteresis and **G**ap, write protected, Reset value = 74H

VDSO DELAY [3]	VDSO DELAY [2]	VDSO DELAY [1]	VDSO DELAY [0]	VD DIFF[3]	VD DIFF[2]	VD DIFF[1]	VD DIFF[0]

VDSODELAY[3:0] Delay for switching off "no-voice" after last detection

"0000"**:** 8 ms	"0001": 16 ms
"0010": 24 ms	"0011": 32 ms
"0100": 40 ms	"0101": 48 ms
"0110": 56 ms	"**0111**": 64 ms
"1000": 72 ms	"1001": 80 ms
"1010": 88 ms	"1011": 96 ms
"1100": 104 ms	"1101": 112 ms
"1110": 120 ms	"1111": 128 ms

VDDIFF[3:0] VDDIFF defines the criterion for deciding whether a received value contributes to the "no-voice"-counting or not. A value does contribute if its amplitude differs by less than VDDIFF from the maximum in the interval AVDDI.VDMAXINTERVAL.
VDSODELAY defines the "hang-over" time of "no-voice" after it has been detected for the last time. This delay time is only evaluated if hysteresis is enabled for "no-voice" detection in ACONF.VDHYST.
Difference between max. and current value for voice detection:

"0000"**:** 0 dB	"0001": 3 dB
"0010": 6 dB	"0011": 9 dB
"**0100**": 12 dB	"0101": 15 dB
"0110": 18 dB	"0111": 21 dB
"1000": 24 dB	"1001": 27 dB
"1010": 30 dB	"1011": 33 dB
"1100": 36 dB	"1101": 39 dB
"1110": 42 dB	"1111": 45 dB

AVDCI[7:0] (Addr.: 75H): **A**FI **V**oice **D**etection **C**ount **I**nit, write protected, Reset value = 85H

VDCI [7]	VDCI [6]	VDCI [5]	VDCI [4]	VDCI [3]	VDCI [2]	VDCI [1]	VDCI [0]

VDCI[7:0] Voice Detection Counter Init value:
A counter is used to count the number of values within the VDINTERVAL which fulfill the "no-voice"-criterion. "no-voice" is detected, if the counter ends up with a value that is greater or equal to 512 (64 ms mode) or 1024 (128 ms mode), respectively. The init -value for this counter is determined by VDCI in the following way:
64 ms Mode: <init-value> = VDCI[7..0] * 2
128 ms Mode: <init-value> = VDCI[7..0] * 4
The reset value of 85H requires that 48% of the values must fulfill the "no-voice" criterion in case the default VDINTERVAL (64 ms) is set)

ATMAT[3:0] (Addr.: 77H): **A**FI **T**urbo **M**ode **A**ctivation **T**hreshold, write protected, Reset value = 08H

-	-	-	-	TURBO TH[3]	TURBO TH[2]	TURBO TH[1]	TURBO TH[0]

TURBOTH[3:0] Turbo Threshold:
This register specifies the threshold for activating the AFI turbo mode (turbo-on indicates that the AFI is adapting to a new end echo path). Turbo mode is activated if the absolute value of one or more auxiliary coefficents is greater than 351 + 4 * TURBOTH.
The default threshold is 383.

AACSC[7:0] (Addr.: 78H): **A**FI **A**uxiliary **C**oefficient **S**upervision **C**onfiguration, write protected, Reset value = 00H**,**

ACS EFFECT	ACSC TH[4]	ACSC TH[3]	ACSC TH[2]	ACSC TH[1]	ACSC TH[0]	ACS TH[1]	ACS TH[0]

To improve handling of periodic signals, two thresholds are used to determine when - probably due to a periodic signal - most of the auxiliary coefficients are becoming quite large. In that case, coefficient update should be slowed down. The slow down mode condition is described by ACSCTH[4:0] and ACSTH[1:0]. The effect of the slow down mode can be configured via the bit ACSEFFECT.

ACSEFFECT	ACSEFFECT specifies the effect of slow-down mode. If set to '1', coefficient update is limited to increasing/decreasing by at most 1. If set to '0', coefficient increment/decrement takes place in the normal way of operation, but turbo mode is disabled. Per default (after reset) it is not active. '**0**': normal operation '1': Disable turbo mode, Coeff. update limited to +/- 1
ACSCTH[4:0]	Aux. Coeff. Supervision Count Threshold: ACSCTH specifies the threshold for activating the slow-down mode of operation. Slow-down mode is active if at least 8 * ACSCTH auxiliary coefficients are "large". The default value ACSCTH[4:0]="**00000**" switches off supervision.
ACSTH[1:0]	Aux. Coeff. Supervision Threshold: ACSTH specifies the threshold above which the absolute value of an auxiliary coefficient is considered "large". It refers to TURBOTH in register ATMAT: "**00**": ATMAT.TURBOTH - 32 "01": ATMAT.TURBOTH - 16 "10": ATMAT.TURBOTH - 8 "11": ATMAT.TURBOTH

ACONF[6:0] (Addr.: 79H): **A**FI **Conf**iguration, write protected, Reset value = 10H

-	EMAF	VD HYST	VD IHA	VD AT[3]	VD AT[2]	VD AT[1]	VD AT[0]

EMAF	Echo, Minimum Attenuation Factor for end echo path '**0**': Attenuation 0 dB (no attenuation) '1': Attenuation 6 dB
VDHYST	Voice Detection, Hysteresis On/Off: VDHYST selects whether a hysteresis is used for switching off "no-voice". '**0**': means that "no-voice" is active only if the set of received values currently in the detection set (AVDDI.VDINTERVAL) fulfill the "no-voice" criterion. '1': means that "no-voice" - once activated - remains active for the time specified in AVDHG.VDSODELAY.
VDIHA	Voice Detection, Ignore High Amplitude: '**1**': received values with an amplitude above 126 (logarithmic) are ignored for "no-voice" detection. '0': all values are taken into account, no values are ignored
VDAT[3:0]	Specifies a lower limit on the amplitude of received

values that are considered for "no-voice"-detection. It is configured in the range from -42 dBm0 (VDAT[3:0] = "0001") to 0 dBm0 (VDAT[3:0] = "1111") in steps of 3 dBm0. With VDAT set to the default value "0000", no lower limit on the amplitude is in effect for "no-voice"-detection.

"**0000**": - infinity	"0001": -42 dBm
"0010": -39 dBm	"0011": -36 dBm
"0100": -33 dBm	"0101": -30 dBm
"0110": -27 dBm	"0111": -24 dBm
"1000": -21 dBm	"1001": -18 dBm
"1010": -15 dBm	"1011": -12 dBm
"1100": -9 dBm	"1101": -6 dBm
"1110": -3 dBm	"1111": 0 dBm

AFCMC[7,4:0] (Addr.: 7AH): **A**FI **F**ilter **C**oefficients **M**onitoring **C**ontrol,
Reset value = 00H

MON ON	-	-	CH SEL[4]	CH SEL[3]	CH SEL[2]	CH SEL[1]	CH SEL[0]

To successively read out all coefficients of a channel's filter, the processor writes the channel number and a set MONON bit to this register. The coefficients and aux. coefficients of the channel are delivered in ascending order via the registers AFCD1 thru AFCD3. The SIDEC interrupt request "Monitored coefficient available" indicates availability of the next coefficient. A running readout procedure stops immediately if the processor writes the AFCMC register again.

MONON — Monitoring on/off:
If MON_ON is cleared, coefficient readout is completely reset immediately. If '1' is written to an already set MONON bit, MONON is first cleared to reset the readout procedure and then set to start readout for the new channel. If coefficient readout is not stopped explicitely by the processor, readout ends after delivery of the channel's last coefficient which resets the MONON bit.

CHSEL[4:0] — Channel selection:
In 128 ms mode the ASIC does not respond to requests for data channels it does not process (e.g. in master mode the chip responds only to requests for channels 0 to 3, 8 to 11, 16 to 19 and 24 to 27.

5.2.4 Read Register

CLKSTAT[5:0] (Addr.: 09H): **Cl**oc**k**-**Stat**us

-	-	RF CLKEX	RF CLKN	RF CLKF	SCLKI	CLK16	CLK32

RFCLKEX ’1’: no valid 2 MHz clock available at pin RFCLKEX
RFCLKN ’1’: no valid 2 MHz clock available at pin RFCLKN
RFCLKF ’1’: no valid 2 MHz clock available at pin RFCLKF
SCLKI ’1’: no valid 8 MHz clock available at pin SCLKI
CLK16 ’1’: no valid 16MHz clock available at pin CLK16
CLK32 ’1’: no valid 32 MHz clock available at pin CLK32

IRREQ[6:0] (Addr.: 08H): **I**nter**r**upt-**Req**uest

-	WDOG	SYNCI	CA	TT	TE	UCC	TSM

WDOG ’1’: Watchdog interrupt
SYNCI ’1’: SYNCI interrupt (no valid SYNCI detected)
CA ’1’: H-register coefficient available for readout interrupt
TT ’1’: Test termination because of enabled test timeslot interrupt
TE ’1’: Timer expired interrupt
UCC ’1’: UCC interrupt
TSM ’1’: Timeslot monitor interrupt, reset when accessing CTRLTSMON.MVAL

Note: Each bit of this register will generate an interrupt at pin INT if activated (internally set to ’1’). The bits and the pin INT are cleared after read. Setting of these bits by activated source can be inhibited by masking in register IRMASK.

STATUS[6:0] (Addr.: 6EH): **Status**

-	WDOG POLL	SYNCI POLL	CA POLL	TT POLL	TE POLL	UCC POLL	TSM POLL

Bits are reset when the interrupt source is no longer valid
WDOGPOLL ’1’: Watchdog status
SYNCIPOLL ’1’: SYNCI status (no valid SYNCI detected)
CAPOLL ’1’: H-register coefficient available for readout status
TTPOLL ’1’: Test termination because of enabled test timeslot status
TEPOLL ’1’: Timer expired status

UCCPOLL	'1':	UCC status
TSMPOLL	'1':	Timeslot monitor status

SFATSES[2:0] (Addr.: 36H): **S**uper **f**rame **al**arm and requested **t**ime**s**lot **e**n/disable **s**tatus

-	-	-	-	-	TSEN VALID	TSEN	SFA

TSENVALID	'1':	TSEN value for the requested TS in register ATE is valid
	'0':	TSEN value not valid since channel defined in register ATE is not detected yet
TSEN	'1':	requested TS in register ATE is enabled, no test recommended
	'0':	requested TS in register ATE is disabled, test permissible
SFA	'1':	alarm, because not synchronized to PCM30 superframe
	'0':	no alarm, because either synchronization to PCM superframe or TS16 CAS evaluation is deactivated (Bit CONFTS16.ENTS16 = '0')

SOTP[6:0] (Addr.: 3DH): **S**end path **o**utput **t**est **p**attern

-	SOTP[6]	SOTP[5]	SOTP[4]	SOTP[3]	SOTP[2]	SOTP[1]	SOTP[0]

SOTP[6:0]	Result of background test of timeslot defined in register ATE, amplitude A-/µ-Law encoded

TESTSTAT[7:0] (Addr.: 3EH): Background **test stat**us signals

DISPS	DIS	NLP	FREEZE	HRESET	ERL	FCM	NO SPEECH

This register contains results of background test of timeslot defined in register ATE

DISPS	'1':	2100 Hz tone with phase shift detected
	'0':	no 2100 Hz tone with phase shift detected
DIS	'1':	2100 Hz tone detected
	'0':	no 2100 Hz tone detected
NLP	'1':	NLP active
	'0':	NLP disabled (bypassed)
FREEZE	'1':	H-Register frozen
	'0':	H-Register not frozen
HRESET	'1':	H-Register reset

	'0': H-Register not reset
ERL	'1': echo return loss > value of BYPTHL[4:0]
	'0': echo return loss not > value of BYPTHL[4:0]
FCM	'1': fast convergence mode
	'0': normal convergence mode
NOSPEECH	'1': no speech detected
	'0': speech detected

DIRAM[7:0] (Addr.: 67H): requested **D**ata **I**nput **RAM** value

DIRAM [7]	DIRAM [6]	DIRAM [5]	DIRAM [4]	DIRAM [3]	DIRAM [2]	DIRAM [1]	DIRAM [0]

DIRAM[7:0] Requested UCC input data for UCC frame defined in WRUCC.ARAM[4:0]

UCCOLD[7:0] (Addr.: 68H): Changed **UCC** input data **old** value

UCC OLD[7]	UCC OLD[6]	UCC OLD[5]	UCC OLD[4]	UCC OLD[3]	UCC OLD[2]	UCC OLD[1]	UCC OLD[0]

UCCOLD[7:0] Data prior to the modification of the modified UCC frame that caused the UCC interrupt. The corresponding frame number of the modified frame value is stored in UCCSTAT.AFR[4:0].

UCCNEW[7:0] (Addr.: 69H): Changed **UCC** input data **new** value

UCC NEW[7]	UCC NEW[6]	UCC NEW[5]	UCC NEW[4]	UCC NEW[3]	UCC NEW[2]	UCC NEW[1]	UCC NEW[0]

UCCNEW[7:0] Modified data of the changed UCC frame that caused the UCC interrupt. The corresponding frame number of the modified frame value is stored in UCCSTAT.AFR[4:0].

UCCSTAT[6:0] (Addr.: 6AH): **UCC stat**us

	INVALID	NO SYNC	AFR[4]	AFR[3]	AFR[2]	AFR[1]	AFR[0]

INVALID '1': possible data loss, because old interrupt has not yet been processed

	’0’:	modified data valid
NOSYNC	’1’:	UCC unit is not synchronized to SYNCI pulse, i.e. the SYNCI pulse period is not an integer multiple of 32 UCC frames (4ms).
	’0’:	UCC unit is synchronized to SYNCI pulse, i.e. a SYNC pulse with a period of an integer multiple of 32 UCC frames (4ms) was detected
AFR[4:0]		value corresponds to the UCC frame that was modified

Note: Read access to this register is identified as acknowledge for the UCC interrupt and should be read after UCCOLD and UCCNEW. This access resets the bit STATUS.UCCPOLL and enables a new UCC interrupt.

AFCD1[7:0] (Addr.: 7BH): **A**FI **F**ilter **C**oefficient **D**ata **1**

COEF [13]	COEF [12]	COEF [11]	COEF [10]	COEF [9]	COEF [8]	COEF [7]	COEF [6]

Read access to this register is identified as acknowledgment for the coefficient availibility (CA) interrupt. If an additional access to register AFCD2 and (or) AFCD3 is necessary, register AFCD1 should be read after AFCD2 and (or) AFCD3. This access resets the bit STATUS.CAPOLL and enables a new CA interrupt. The conversion from the 14 bit register value to the linear value is depicted in **Table 22**.

COEF[13:6] MSB of monitored filter coefficient

AFCD2[7:0] (Addr.: 7CH): **A**FI **F**ilter **C**oefficient **D**ata **2**

ISLAST	-	COEF [5]	COEF [4]	COEF [3]	COEF [2]	COEF [1]	COEF [0]

ISLAST	’1’: COEF is last coefficient for channel readout
COEF[5:0]	LSB of monitored coefficient. The conversion from the 14 bit register value to the linear value is depicted in **Table 22**.

AFI Coefficient Register Value														Linear Value																	
13	12	11	10	9	8	7	6	5	4	3	2	1	0	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	0	0	0	A	B	C	D	E	F	G	H	I	J	S	0	0	0	0	0	0	0	A	B	C	D	E	F	G	H	I	J
S	0	0	1	A	B	C	D	E	F	G	H	I	J	S	0	0	0	0	0	0	1	A	B	C	D	E	F	G	H	I	J
S	0	1	0	A	B	C	D	E	F	G	H	I	J	S	0	0	0	0	0	1	A	B	C	D	E	F	G	H	I	J	0
S	0	1	1	A	B	C	D	E	F	G	H	I	J	S	0	0	0	0	1	A	B	C	D	E	F	G	H	I	J	0	0
S	1	0	0	A	B	C	D	E	F	G	H	I	J	S	0	0	0	1	A	B	C	D	E	F	G	H	I	J	0	0	0
S	1	0	1	A	B	C	D	E	F	G	H	I	J	S	0	0	1	A	B	C	D	E	F	G	H	I	J	0	0	0	0
S	1	1	0	A	B	C	D	E	F	G	H	I	J	S	0	1	A	B	C	D	E	F	G	H	I	J	0	0	0	0	0
S	1	1	1	A	B	C	D	E	F	G	H	I	J	S	1	A	B	C	D	E	F	G	H	I	J	0	0	0	0	0	0

Table 22 Conversion of AFI Coefficients from Register Value to Sign (S) and Absolute Linear Value

AFCD3[7:0] (Addr.: 7DH): **AFI Filter Coefficient Data 3**

AUX COEF [9]	AUX COEF [8]	AUX COEF [7]	AUX COEF [6]	AUX COEF [5]	AUX COEF [4]	AUX COEF [3]	AUX COEF [2]

AUXCOEF[9:2] Most significant bits of the auxiliary coefficient monitored

The following read registers contain channel individual values. The channel number defined in register CTRLTSMON.MCH[4:0]

Since MVAL is the interrupt source indicating an update of the monitor registers it must be reset after the monitor registers are read out in order to avoid an unwanted interrupt.

MONSI[7:0] (Addr.: 29H): **Mon**itor **s**end **i**nput **si**gnal (A-/µ-Law encoded)

MON SI[7]	MON SI[6]	MON SI[5]	MON SI[4]	MON SI[3]	MON SI[2]	MON SI[1]	MON SI[0]

The content of this register is PCM encoded.

MONSO[7:0] (Addr.: 2AH): **Mon**itor **s**end **o**utput signal (A-/µ-Law encoded)

MON SO[7]	MON SO[6]	MON SO[5]	MON SO[4]	MON SO[3]	MON SO[2]	MON SO[1]	MON SO[0]

The content of this register is PCM encoded.

MONRI[7:0] (Addr.: 2BH): **Mon**itor of **r**eceive **i**nput signal (A-/µ-Law encoded)

MON RI[7]	MON RI[6]	MON RI[5]	MON RI[4]	MON RI[3]	MON RI[2]	MON RI[1]	MON RI[0]

The content of this register is PCM encoded

MONSIL[7:0] (Addr.: 1EH): **Mon**itor **s**end **i**nput **l**evel

MON SIL[7]	MON SIL[6]	MON SIL[5]	MON SIL[4]	MON SIL[3]	MON SLI[2]	MON SIL[1]	MON SIL[0]

The content of this register is encoded logarithmically. The maximum value of 191 corresponds to 3 dBm0. A decrease of 16 is equivalent to a decrease of 6 dB. The following table displays the relation between the register value and the dBm0 value.

Register Value	**Level [dBm0]**	**Register Value**	**Level [dBm0]**
191	+3	88	-36
184	0	80	-39
176	-3	72	-42
168	-6	64	-45
160	-9	56	-48
152	-12	48	-51
144	-15	40	-54
136	-18	32	-57
128	-21	24	-60
120	-24	16	-63
112	-27	8	-66
104	-30	1	-69
96	-33	0	- infinity

Table 23 Conversion of Monitor Register Values to dBm0 Values

MONSOL[7:0] (Addr.: 1FH): **Mon**itor **s**end **o**utput **l**evel

MON SOL[7]	MON SOL[6]	MON SOL[5]	MON SOL[4]	MON SOL[3]	MON SOL[2]	MON SOL[1]	MON SOL[0]

The content of this register is encoded logarithmically. For conversion to dBm0 see **Table 23** .

MONRIL[7:0] (Addr.: 20H): **Mon**itor of **r**eceive **i**nput **l**evel

MON RIL[7]	MON RIL[6]	MON RIL[5]	MON RIL[4]	MON RIL[3]	MON RIL[2]	MON RIL[1]	MON RIL[0]

The content of this register is encoded logarithmically. For conversion to dBm0 see **Table 23** .

MONOFSI[5:0] (Addr.: 21H): **Mon**itor **of**fset in **s**end path **i**nput

-	-	MON OFSI[5]	MON OFSI[4]	MON OFSI[3]	MON OFSI[2]	MON OFSI[1]	MON OFSI[0]

The content of this register is a linear value in "1 complement" notation.

MONOFSO[5:0] (Addr.: 22H): **Mon**itor **of**fset in **s**end path **o**utput

-	-	MON OFSO[5]	MON OFSO[4]	MON OFSO[3]	MON OFSO[2]	MON OFSO[1]	MON OFSO[0]

The content of this register is a linear value in "1 complement" notation.

MONAEL[7:0] (Addr.: 23H): **Mon**itor **a**rtificial **e**cho **l**evel

MON AEL[7]	MON AEL[6]	MON AEL[5]	MON AEL[4]	MON AEL[3]	MON AEL[2]	MON AEL[1]	MON AEL[0]

The content of this register is encoded logarithmically. For conversion to dBm0 see **Table 23** .

MONBNL[6:0] (Addr. 24H): **Mon**itor **b**ackground **n**oise **l**evel

-	MON BNL[6]	MON BNL[5]	MON BNL[4]	MON BNL[3]	MON BNL[2]	MON BNL[1]	MON BNL[0]

The content of this register is encoded logarithmically. For conversion to dBm0 see **Table 23** .

MONERL[7:0] (Addr.: 25H): **Mon**itor **E**cho **r**eturn **l**oss

MON ERL[7]	MON ERL[6]	MON ERL[5]	MON ERL[4]	MON ERL[3]	MON ERL[2]	MON ERL[1]	MON ERL[0]

The content of this register is encoded logarithmically. For conversion to dBm0 see **Table 23** .

MONCL[7:0] (Addr.: 26H): **Mon**itor **c**ombined **l**oss without NLP

MON CL[7]	MON CL[6]	MON CL[5]	MON CL[4]	MON CL[3]	MON CL[2]	MON CL[1]	MON CL[0]

The content of this register is encoded logarithmically. For conversion to dBm0 see **Table 23** .

MONNLPTHL[7:0] (Addr.: 27H): **Mon**itor **NLP thr**eshold **l**evel

MON NLP THL[7]	MON NLP THL[6]	MON NLP THL[5]	MON NLP THL[4]	MON NLP THL[3]	MON NLP THL[2]	MON NLP THL[1]	MON NLP THL[0]

The content of this register is encoded logarithmically. For conversion to dBm0 see **Table 23** .

MONOCDT[7:0] (Addr.: 28H): **Mon**itor **o**ver**c**ompensation and **d**ouble **t**alk hang-over time

MON OCE[3]	MON OCE[2]	MON OCE[1]	MON OCE[0]	MON DTHOT [3]	MON DTHOT [2]	MON DTHOT [1]	MON DTHOT [0]

MONOCE[3:0] Overcompensation evaluation
MONDTHOT[3:0] Double talk hang-over time

MONSTAT1[7:0] (Addr.: 2CH): **Mon**itor of internal/external control **stat**es **1**

MNS	M DIS NOSP	M DIS	M DISPS	M HRES	M FREEZE	M NLP	M ECBP

MNS ’1’: "no-voice" detected
MDISNOSP ’1’: 2100Hz detected but without speech protection
MDIS ’1’: 2100Hz detected with speech protection
MDISPS ’1’: 2100Hz with phase shift and speech protection detected
MHRES ’1’: H-Register reset
MFREEZE ’1’: H-Register frozen
MNLP ’1’: NLP active

MECBP ’1’: Entire echo cancellation path bypassed

MONSTAT2[7:0] (Addr.: 2DH): **Mon**itor of internal/external control **stat**es **2**

M ERLBP	M DT	M FCM	M CSPR	M NR7 NOSP	M NR7 DIS	M NR7 BY	M IDLE

The contents of individual bits of this register can also be output at pin FLEXMON1 or FLEXMON2 if configured in register CONFLEXMON.

MERLBP	’1’:	Subtractor bypassed because ERL > value of BYPTHL[4:0]
MDT	’1’:	near end subscriber is louder than the far end subscriber (true double talk)
MFCM	’1’:	Fast convergence mode active
MCSPR	’1’:	Convergence stability protection for non-speech signals active
MNR7NOSP	’1’:	2010Hz (SS Nr.7) detected but without speech protection
MNR7DIS	’1’:	2010Hz speech protection: second level reached (H-Register reset)
MNR7BY	’1’:	2010Hz speech protection: first level reached (bypass of entire canceller)
MIDLE	’1’:	Idle channel detected

MONSTAT3[7:0] (Addr.: 2EH): **Mon**itor of internal/external control **stat**es **3**

M TS16	M UCCD	M UCCFX	M SCDIS	MSC NLPDIS	MSC FREEZE	MSC CONV DIS	MFLEX SCTR

MTS16	’1’:	channel disabled by TS16 CAS evaluation
MUCCD	’1’:	disable by UCC-DIS-Bit active
MUCCFX	’1’:	UCC-FX bit active
MSCDIS	’1’:	serial control signal DIS active
MSCNLPDIS	’1’:	serial control signal NLPDIS active
MSCFREEZE	’1’:	serial control signal FREEZE active
MSCCONVDIS	’1’:	serial control signal CONVDIS active
MFLEXSCTR	’1’:	serial control signal FLEXSCTR active

6 SIDEC Performance

This section describes the preliminary performance of the SIDEC. The measurements are based on the preliminary emulation results. The test, signals and methods are described in ITU G.168. For the measurements a regular analog hybrid with 6 dB echo return loss is used. No significant difference for high dispersion hybrids is expected, since the SIDEC evaluates not only a "echo window" but the complete echo path delay time.

6.1 Test No.1 - Steady state residual and returned echo level test

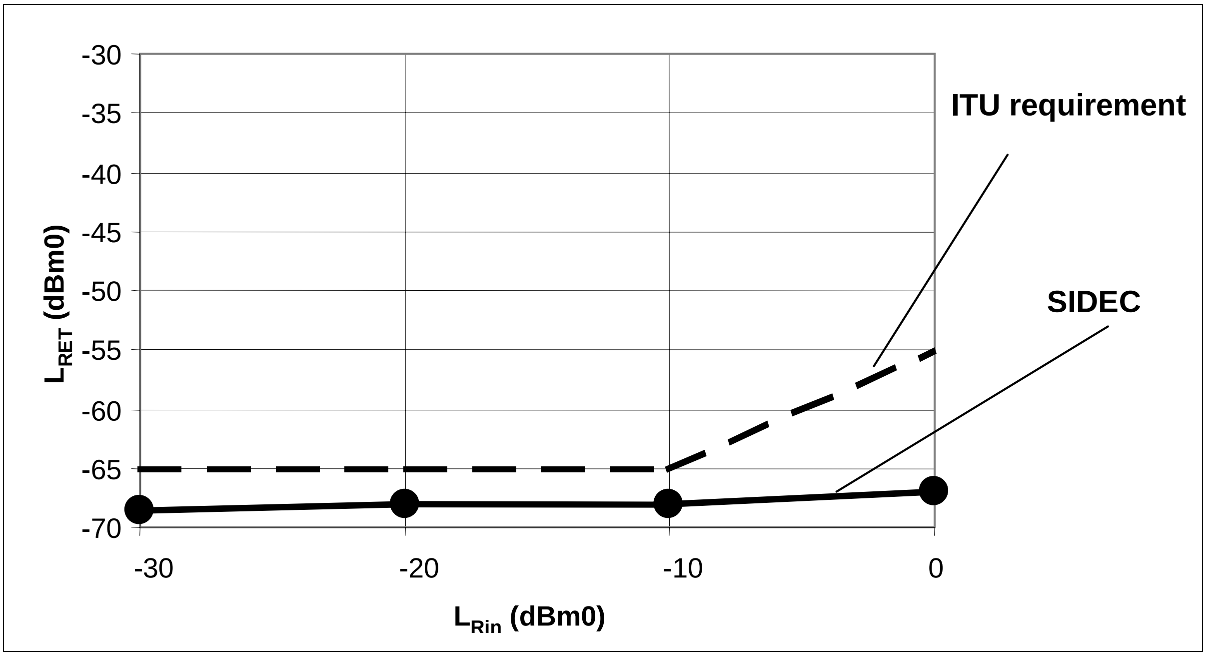

Figure 39 SIDEC steady state behavior with NLP enabled

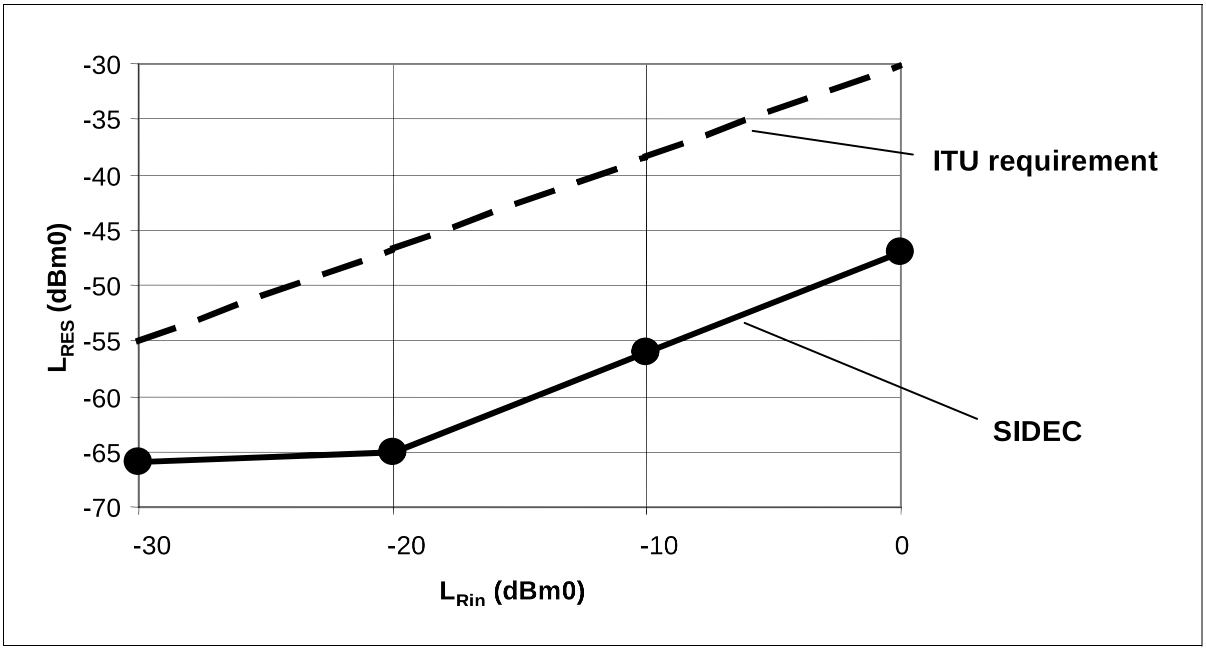

Figure 40 SIDEC steady state behavior with NLP disabled

6.2 Test No. 2 - Convergence and steady state residual and returned echo level test

6.2.1 Test 2A: Convergence test with NLP enabled

Receive Level R_{in}	Time until A_{COM}=			
	16 dB (CONV)		Boundary value of **Figure 39**	
	Requirement ITU G.168	measured value	Requirement ITU G.168	measured value
0 dBm0	< 1 s	200 ms	< 1 s	670 ms
-10 dBm0	< 1 s	150 ms	< 1 s	520 ms
-20 dBm0	< 1 s	150 ms	< 1 s	410 ms
-30 dBm0	< 1 s	150 ms	< 1 s	450 ms

6.2.2 Test 2B: Convergence test with NLP disabled

Receive Level R_{in}	Time until A_{COM}=			
	16 dB (CONV)		Boundary value of **Figure 40**	
	Requirement ITU G.168	measured value	Requirement ITU G.168	measured value
0 dBm0	< 1 s	200 ms	< 10 s	520 ms
-10 dBm0	< 1 s	200 ms	< 10 s	600 ms
-20 dBm0	< 1 s	400 ms	< 10 s	1300 ms
-30 dBm0	< 1 s	400 ms	< 10 s	1200 ms

6.2.3 Test 2C: Convergence test in the presence of background noise

For this test the NLP is enabled and the convergence time is t_d = 1 s.

Receive Level R_{in}	Transmit Noise Level	Residual output level L_{RES}	
		Requirement ITU G.168	measured value
0 dBm0	-30 dBm0	-30 dBm0	-67 dBm0
-10 dBm0	-30 dBm0	-30 dBm0	-66 dBm0
-20 dBm0	-35 dBm0	-35 dBm0	-66 dBm0
-25 dBm0	-40 dBm0	-40 dBm0	-64 dBm0

6.3 Test No. 3 - Performance under conditions of double talk

6.3.1 Test 3A: Double talk test with low near end levels

For this test the NLP is disabled and the convergence time is t_d = 5 s.

Receive Level R_{in}	Transmit Noise Level	Residual output level L_{RES}	
		Requirement ITU G.168	measured value
0 dBm0	-15 dBm0	< -15 dBm0	-31 dBm0
-10 dBm0	-25 dBm0	< -25 dBm0	-43 dBm0
-20 dBm0	-35 dBm0	< -35 dBm0	-56 dBm0
-25 dBm0	-40 dBm0	< -40 dBm0	-56 dBm0

6.3.2 Test 3B: Double talk test with high near end levels

For this test the NLP is disabled and the testtime is > 5 s.

Receive Level R_{in}	Transmit Noise Level	Residual output level L_{RES}	
		Requirement ITU G.168	measured value
0 dBm0	0 dBm0	< -30 dBm0	-51 dBm0
-10 dBm0	-10 dBm0	< -38 dBm0	-55 dBm0
-20 dBm0	-20 dBm0	< -47 dBm0	-62 dBm0
-25 dBm0	-30 dBm0	< -55 dBm0	-66 dBm0

6.3.3 Test 3C: Double talk under simulated conversion

This test is under study and most values are not defined

6.4 Test No. 4 - Leak rate test

During this test the H-Register is frozen.Therefore, no divergence occurs.

6.5 Infinite return loss convergence test

The previous echo return loss is 6 dB at an analog hybrid. The NLP is disabled and the measurement is made 500 ms after interrupting the end echo path.

Receive	Residual output level L_{RES}	
Level R_{in}	Requirement ITU G.168	measured value
0 dBm0	< TBD dBm0	-76 dBm0
-10 dBm0	< TBD dBm0	-76 dBm0
-20 dBm0	< TBD dBm0	-67 dBm0
-25 dBm0	< TBD dBm0	-67 dBm0

6.6 Non divergence on narrow band signals

This test is under study and the most values are not defined.

6.7 Stability Test

Receive	Residual output level L_{RES}	
Level R_{in}	Requirement ITU G.168	measured value
+3 dBm0	< -27.5 dBm0	-28 dBm0
0 dBm0	< -30 dBm0	-31 dBm0
-10 dBm0	< -38 dBm0	-41 dBm0
-20 dBm0	< -47 dBm0	-51 dBm0
-30 dBm0	< -55 dBm0	- 61 dBm0

6.8 Test No. 8 - Non convergence of the canceller on specific ITU-T No. 5, 6 and 7 in band signaling and continuity check tones

The SIDEC incorporate a 2010 Hz tone detector to allow a continuity check in System 6 and 7. In many applications a disabling control via the switch is possible. In this case this function has to be switched off (reset value, Register CONFSS7 = 00H).

Operating level / Non operating level:	> -31dBm0 / < -34dBm0
Operating frequency:	1968Hz...2032Hz
Operating time for disabling	12ms + guard time adjusted in BYNR7[3:0]
Operating time for H-Register-Reset	12ms + guard time adjusted in D!SNR7[3:0]
None operating frequency:	0...1945 and 2055Hz...4000Hz
Release time:	10ms

6.9 Test No. 9 - Comfort noise test

The SIDEC is fitted with a circuit which is in compliance with this requirement, but most subscribers prefer the solution which limit the send in signal (noise from the near end + echo) to the noise level which was measured before (Reset value).

6.10 Test No. 10 - Canceller operation on the calling/caller station side

These tests are checked and are "OK"

Features of the 2100Hz tone disabler:

Operating frequency	2065 Hz - 2140 Hz
Not operating frequency	< 2000 Hz, > 2180 Hz
Holding Band	390 Hz - 3000 Hz
Operating level / Not operating level	> -31 dBm0 / < -34 dBm0
Operate time / Not operating time	> 260 ms / < 200 ms
Hold time / Release time	> 210 ms / < 270 ms
Guard band noise level to inhibit the operating	> signal level
Maximum noise level for operation	< signal level - 5 dB
False operation due to speech/data signals	< 10/100h

Features of the phase reversal enhancement:

Operating frequency	2010Hz +/- 21Hz
Operating phase / Not operating phase	> +/-155° / < +/- 110°

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter		Symbol	Limit Values	Unit
Ambient temperature under bias	PEB PEF	T_A T_A	0 to 70 – 40 to 85	°C °C
Storage temperature		T_{stg}	– 65 to 125	°C
IC supply voltage		V_{DD}	0 to 3.6	V
Voltage on any functional pin (**not** V_{DD} and **not** V_{SS}) with respect to ground		V_S	-0.4 to 5.5	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF		$V_{ESD,HBM}$	2000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

***Note:** Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{DD}	3.0	3.6	V	
Ground	V_{SS}	0	0	V	

Note: In the operating range, the functions given in the circuit description are fulfilled.

7.3 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	– 0.4	0.8	V	1)
Input high voltage	V_{IH}	2.0	5.5	V	
Output low voltage	V_{OL}		0.45	V	I_{OL} = 4 mA 2) I_{OL} = 2.5 mA 3)
Output high voltage	V_{OH}	2.4		V	I_{OH} = – 1.0 mA
Avg. power supply current	I_{CC} (AV)		300	mA	V_{DD} = 3.3 V, T_A = 25 °C:
Input leakage current	I_{IL}		5	µA	V_{DD} = 3.3 V, GND = 0 V; all other pins are floating; V_{IN} = 0 V,
Output leakage current	I_{OZ}		5	µA	V_{DD} = 3.3 V, GND = 0 V; V_{OUT} = 0 V,

1) Permanent exposure to negative input voltages may result in minor degradation of lifetime

2) Apply to the following O or I/O pins:
UUPIO0, UPIO1, UPIO2, UPIO3, AD[0:6], $\overline{RDY}$, UPRES, $\overline{UPRES}$, $\overline{INT}$, RO, SO, TMFBO, CLK4O, SYNCO, SCLKO, SDECO, UCCO, $\overline{TUCCO}$

3) Apply to all the I/O and O pins that do not appear in the list in note **2)**)

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

7.4 AC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{il}		0.45	V	1)
Input high voltage	V_{ih}	2.4		V	

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Output low voltage	V_{ol}		0.8	V	I_{ol} = 4 mA [2)] I_{ol} = 2.5 mA [3)]
Output high voltage	V_{oh}	2.0		V	I_{ol} = – 1.0 mA

1) Permanent exposure to negative input voltages may result in minor degradation of lifetime

2) Apply to the following O or I/O pins:
UPIO0, UPIO1, UPIO2, UPIO3, AD[0:6], $\overline{\text{RDY}}$, UPRES, $\overline{\text{UPRES}}$, $\overline{\text{INT}}$, RO, SO, TMFBO, CLK4O, SYNCO, SCLKO, SDECO, UCCO, $\overline{\text{TUCCO}}$

3) Apply to all the I/O and O pins that do not appear in the list in note **2)**)

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage

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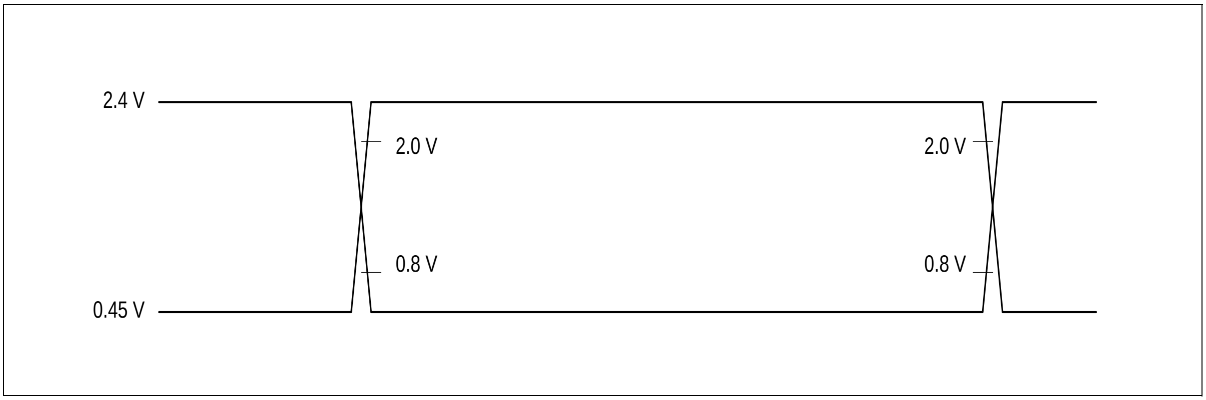


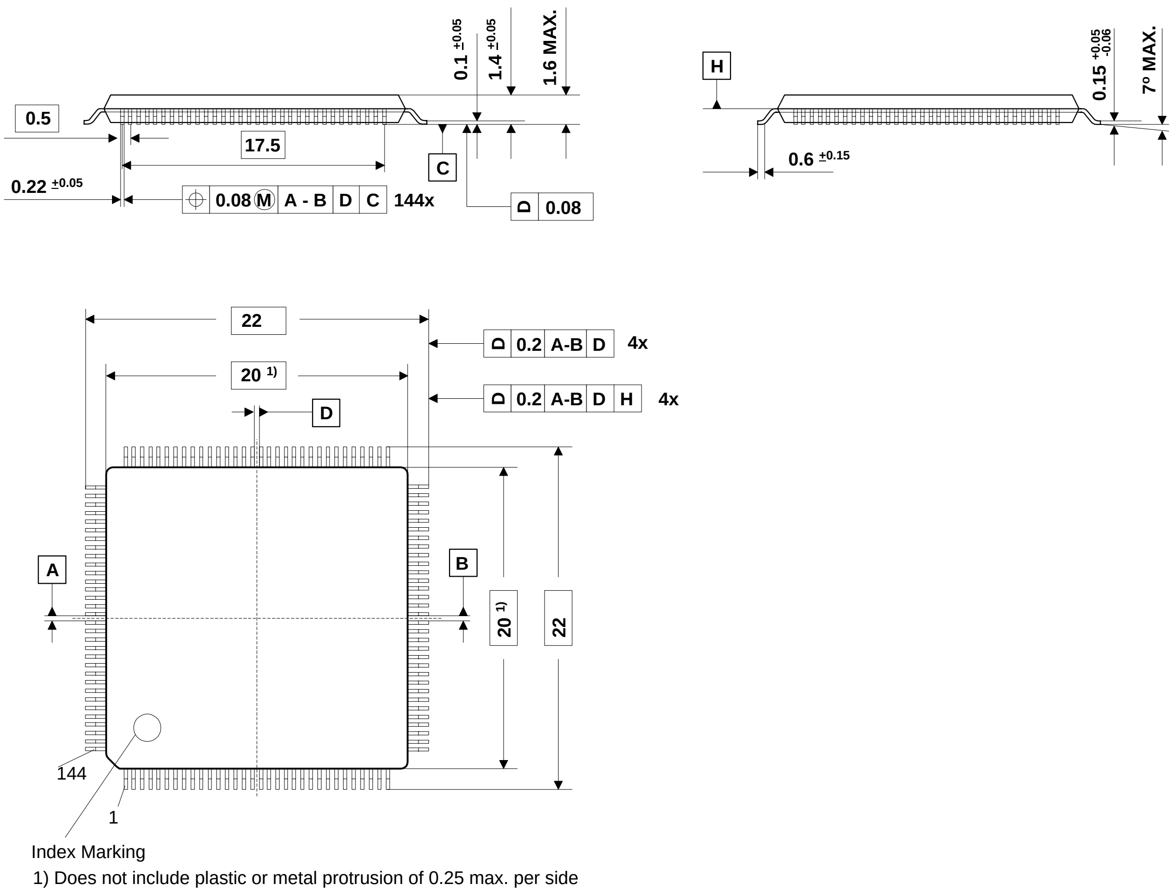
Figure 41 Input/Output Waveforms for AC-Tests

7.5 Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Clock input capacitance	C_{XIN}		10	pF	f_C = 1 MHz The pins, which are not under test, are connected to GND
Clock output capacitance	C_{XOUT}		10	pF	
Input capacitance	C_{IN}		10	pF	
Output capacitance	C_{OUT}		10	pF	

8 Package Outlines

TQFP-144
(144pin Thin Plastic Quad Flatpack



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

9 Glossary

acoustic echo

Acoustic echoes consist of reflected signals caused by acoustic environments, e.g. hands-free phones which are connected with a 2-wire circuit to a hybrid. An echo path is introduced by the acoustic path from earphone to microphone.

combined loss (A_{COM})

The sum of echo return loss, echo return loss enhancement and non-linear processing loss (if present). This loss relates L_{Rin} to L_{RET} by:
$L_{RET} = L_{Rin} - A_{COM}$, where:
$A_{COM} = A_{ECHO} + A_{CANC} + A_{NLP}$

comfort noise

Insertion of pseudo-random noise during the silent interval when the NLP operates or allowance of some of the background or idle channel noise to pass through the NLP in order to prevent the annoyance of intervals of speech with background noise followed by intervals of silence.

composite echo

Composite echoes consist of the electric echoes and acoustic echoes caused by reflected signals at hybrids and acoustic environments, e.g. hands-free telephones.

convergence

The process of developing a model of the echo path which will be used in the echo estimator to produce the estimate of the circuit echo.

convergence time

For a defined echo path, the interval between the instant a defined test signal is applied to the receive-in port of an echo canceller with the estimated echo path impulse response initially set to zero, and the instant the returned echo level at the send-out port reaches a defined level.

echo canceller

A voice-operated device placed in the 4-wire portion of a circuit and used for reducing near-end echo present on the send path by subtracting an estimation of that echo from the near-end echo (see **Figure 42**)

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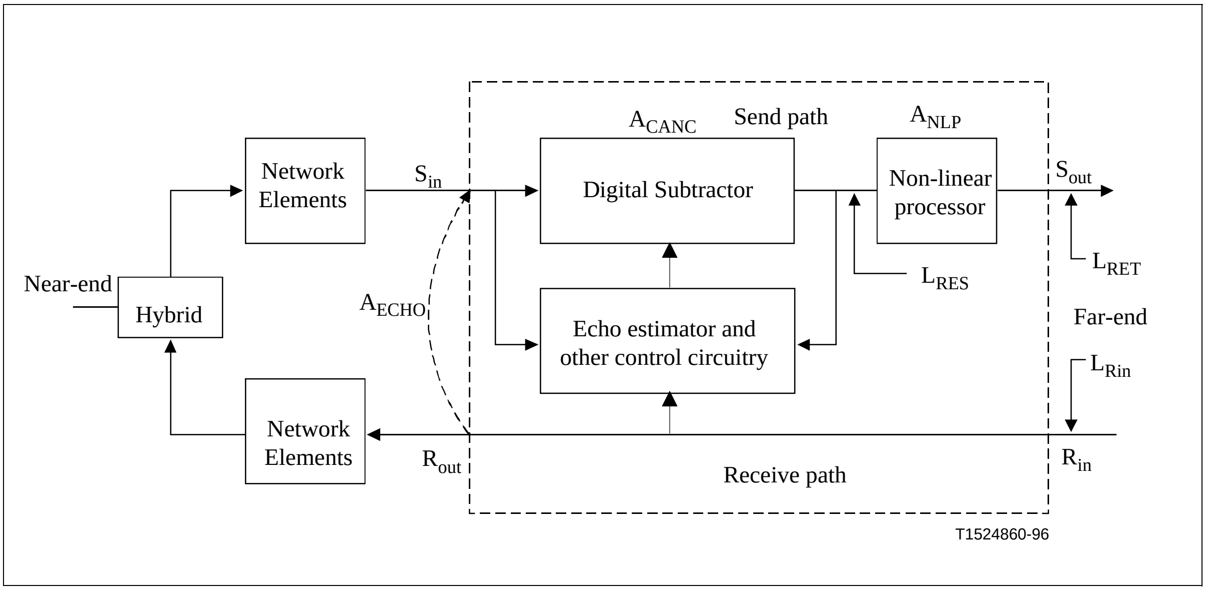

Figure 42 Location of levels and loss of an echo canceller

echo path

The transmission path between R_{out} and S_{in} of an echo canceller. This term is intended to describe the signal path of the echo.

echo path capacity

The maximum echo path delay for which an echo canceller is designed to operate.

echo path delay (t_d)

The delay from the Rout port to the Sin port due to the delays inherent in the echo path transmission facilities including dispersion time due to the network elements. In case of multiple echo paths, all delays and dispersions of any individual echo path are included. The dispersion time, which varies with different networks, is required to accommodate the band-limiting, and hybrid transit effects.

echo return loss (ERL) (A_{ECHO})

The attenuation of a signal from the receive-out port (R_{out}) to the send-in port (S_{in}) of an echo canceller, due to transmission and hybrid loss, i.e. the loss in the (near-end) echo path.

echo return loss enhancement (ERLE) (A_{CANC})

The attenuation of the echo signal as it passes through the send path of an echo canceller. This definition specifically excludes any non-linear processing on the output of the canceller to provide for further attenuation.

electric echo

Electric echoes consist of reflected signals caused by the near-end impedance mismatch, e.g. at a 2-wire/4-wire conversion unit (hybrid).

far end

The side of an echo canceller which does not contain the echo path on which the echo canceller is intended to operate.

H register

The register within the echo canceller which stores the impulse response model of the echo path.

leak time

The interval between the instant a test signal is removed from the receive-in port of a fully-converged echo canceller and the instant the echo path model in the echo canceller changes such that, when a test signal is reapplied to R_{in} with the convergence circuitry inhibited, the returned echo is at a defined level.

This definition refers to echo cancellers employing, for example, leaky integrators in the convergence circuitry.

near-end

The side of an echo canceller which contains the echo path on which the echo canceller is intended to operate. This includes all transmission facilities and equipment (including the hybrid and terminating telephone set) which is included in the echo path.

non-linear processor (NLP)

A device having a defined suppression threshold level and in which:
a)signals having a level detected as being below the threshold are suppressed; and
b)signals having a level detected as being above the threshold are passed although the signal may be distorted.

NOTE 1 – The precise operation of a NLP depends upon the detection and control algorithm used.

NOTE 2 – An example of a NLP is an analogue center clipper in which all signal levels below a defined threshold are forced to some minimum value.

non-linear processing loss (A_{NLP})

Additional attenuation of residual echo level by a NLP placed in the send path of an echo canceller.

pure delay (t_r)

The delay from the R_{out} port to the Sin port due to the delays inherent in the near-end echo path transmission facilities, not including dispersion time due to the network elements. In this case, the transit time directly across the hybrid is assumed to be zero (see **Figure 43**).

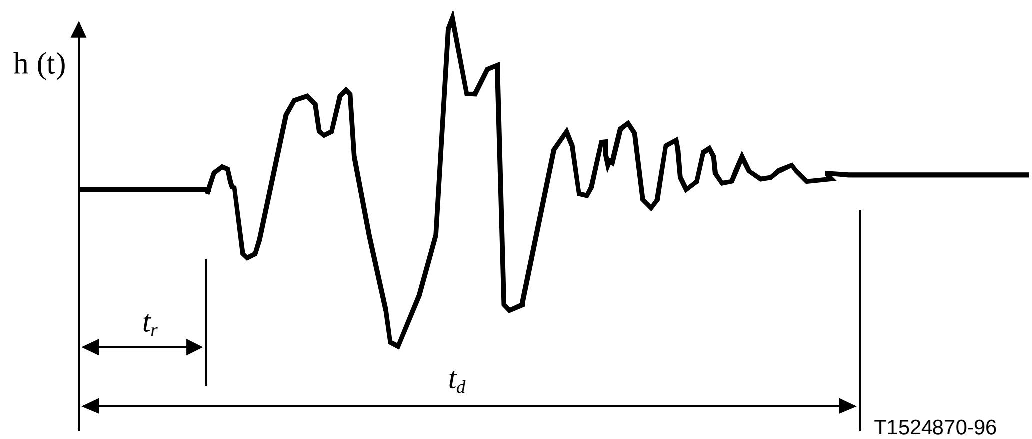

Figure 43 Example of an impulse response of an echo path

residual echo level (L_{RES})

The level of the echo signal which remains at the send-out port of an operating echo canceller after imperfect cancellation of the circuit echo. It is related to the receive-in signal L_{Rin} by:

$L_{RES} = L_{RIN} - A_{ECHO} - A_{CANC}$

Any non-linear processing is not included.

returned echo level (L_{RET})

The level of the signal at the send-out port of an operating echo canceller which will be returned to the talker. The attenuation of a NLP is included, if one is normally present. L_{RET} is related to L_{Rin} by:

$L_{RET} = L_{RIN} - (A_{ECHO} + A_{CANC} + A_{NLP})$
If non-linear processing is not present, note that $L_{RES} = L_{RET}$.

10 Index

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