SIEMENS

ISDN Burst Tranceiver Circuit (IBC) PEB 2095

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2095-C	Q67100-H8398	C-DIP-24
PEB 2095-N	Q67100-H8396	PL-CC-28 (SMD)
PEB 2095-P	Q67100-H8397	P-DIP-24

The PEB 2095 ISDN Burst Transceiver Circuit (IBC) is a half duplex transceiver for the 2-wire transmission line (CCITT U-reference point). Full duplex transmission is achieved using a time compression multiplex (ping-pong) technique. Furthermore, the device links the 2-wire transmission line to the ISDN Oriented Modular (IOM) interface and hence to the powerful Siemens ISDN device family. From the point of view of the OSI communications protocol model, the device manages layer-1 of the interface protocol and can communicate with other layer-1 or layer-2 devices over the IOM interface.

A second device, the PEB 2090 ISDN Echo Cancellation Circuit (IEC), may also be used at the U-reference point. The device chosen depends on the application. The IBC proves more cost-effective for shorter range transmission applications (2 – 3.5 km), especially PBX.

The IBC is available as a 24-pin CMOS device.

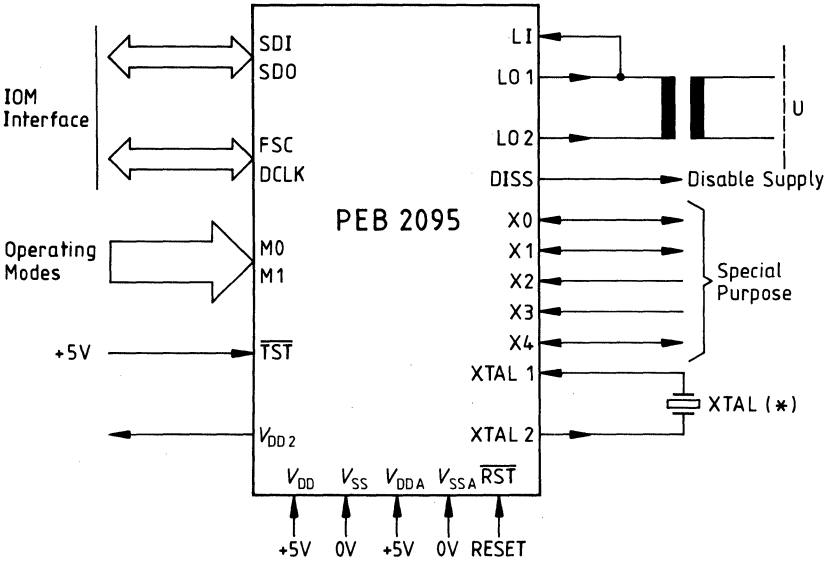
The device operates from a single 5-V power supply.

The maximum power consumption is 80 mW.

Features:

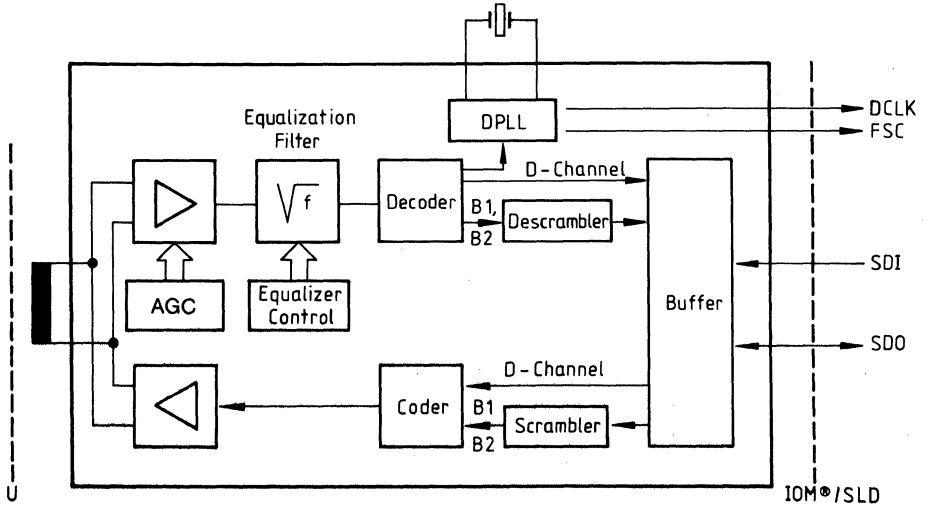
- Half duplex burst mode 2-wire U-interface transceiver
- Mode configurable to function at both ends of the line
- 144 kbit/s user bit rate (2B + D)
- 384-kHz line clock rate
- IOM compatible
- Clock and frame recovery
- Adaptive line equalization and amplification at receiver
- Implementation of activation/deactivation procedures
- Built-in wake-up function for activation from power down state
- Switching of test loops
- Typical length of loop: up to 3.5 km with 0.6 mm diameter wire
- Advanced CMOS technology
- Low power consumption: 6 mW power down
  80 mW power up (maximum)

Logic Symbol



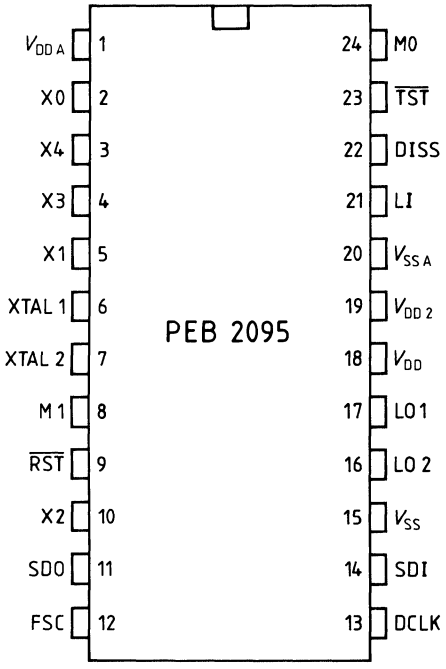
*) An external oscillator can also be used as a clock input to XTAL1.
In this configuration XTAL2 is not connected.

Block Diagram

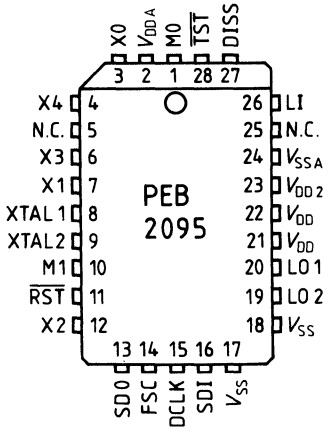


Pin Configurations
(top view)

P-DIP; C-DIP



PL-CC



*) XTAL2 not connected when external oscillator is used

Pin Definitions and Functions

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
16	20	LO1		Line transmitter; output 1
17	19	LO2	O	Line transmitter; output 2 — U interface
21	26	LI	I	Line receiver
11	13	SD0	O	Serial data out
14	16	SDI	I	Serial data in — IOM interface
13	15	DCLK	I/O	Serial data clock
12	14	FSC	I/O	Frame sync.
24	1	M0	I	Operating mode setup pins
8	10	M1	I	
2	3	X0	I/O	Multifunctional pins; mode specific functions
5	7	X1	I/O	
10	12	X2	I	
4	6	X3	I	
3	4	X4	I/O	
6	8	XTAL1	I	External crystal or external oscillator input.
7	9	XTAL2	O	External crystal connection (n.c. when external oscillator is used).
23	28	$\overline{TST}$	I	Device test pin; not for general use; tie high always.
22	27	DISS	O	Disable supply
9	11	$\overline{RST}$	I	Hardware reset pin; active low
18	21, 22	V_{DD}	I	Digital power supply 5 V ± 5%
15	17, 18	V_{SS}	I	Digital ground
1	2	V_{DDA}	I	Analog power supply 5 V ± 5%
20	24	V_{SSA}	I	Analog ground
19	23	V_{DD2}	O	2.5 V output; connected to V_{DD} via 10 nF capacitor connected to V_{SSA} via 10 nF capacitor
	5; 25	N.C.		Not connected internally

System Integration

There are three operating modes:

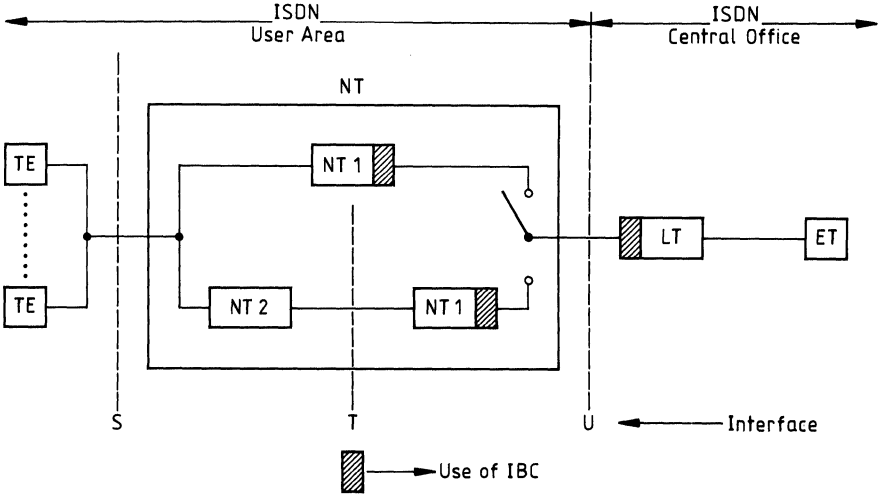
LT: Line Termination i.e. in the Local Exchange/PBX
TE: Terminal Equipment i.e. in the Subscriber Terminal
NT: Network Termination

Two examples of LT mode are illustrated, one connected directly to the terminal, one connected to a network termination. In the latter case, the terminal is connected over the S interface for the network termination. Because of the multiplexing facility on the S-bus to eight terminals may be connected to one network termination and hence to one subscriber line. In the former case (without a network termination) only one terminal per subscriber line is possible. The diagram also indicates that either the IBC or the IEC may be used for 2-wire transmission. Choice is dependent upon the transmission line characteristics, but in general the IBC is the more cost-effective for shorter range transmission applications (especially PBX).

In the LT mode, the IBC managers layer-1 functions and communicates over the IOM interface with the ICC (ISDN Communication Controller) which handles most layer-2 functions. A microprocessor (handling higher layer functions) controls and communicates with the ICC. A similar configuration is required in the TE mode, employing the same division of tasks.

In the NT mode, however, the configuration is much different. In this case the network termination is acting as an NT1 (according to CCITT notation). **Figure 1** illustrates two possible NT configurations.

Figure 1
NT Configuration



In both cases, NT1 refers to a simple layer-1 translation between the U interface and the S/T interface. This is achieved by the simple pairing of the IBC with an IOM compatible S-bus interface circuit (e.g. the SBC PEB 2080).

In this configuration, no ICC or microprocessor is required because layer-2 and higher are passed transparently through NT1. The IOM interface acts as an intermediate interface common to both devices.

On the other hand NT2 in **figure 1** differs from NT1 in that it includes higher level OSI functions. It could, for example, be a PBX. In this case the PBX would be connected directly over the S interface (not U interface) to the subscriber terminal(s).

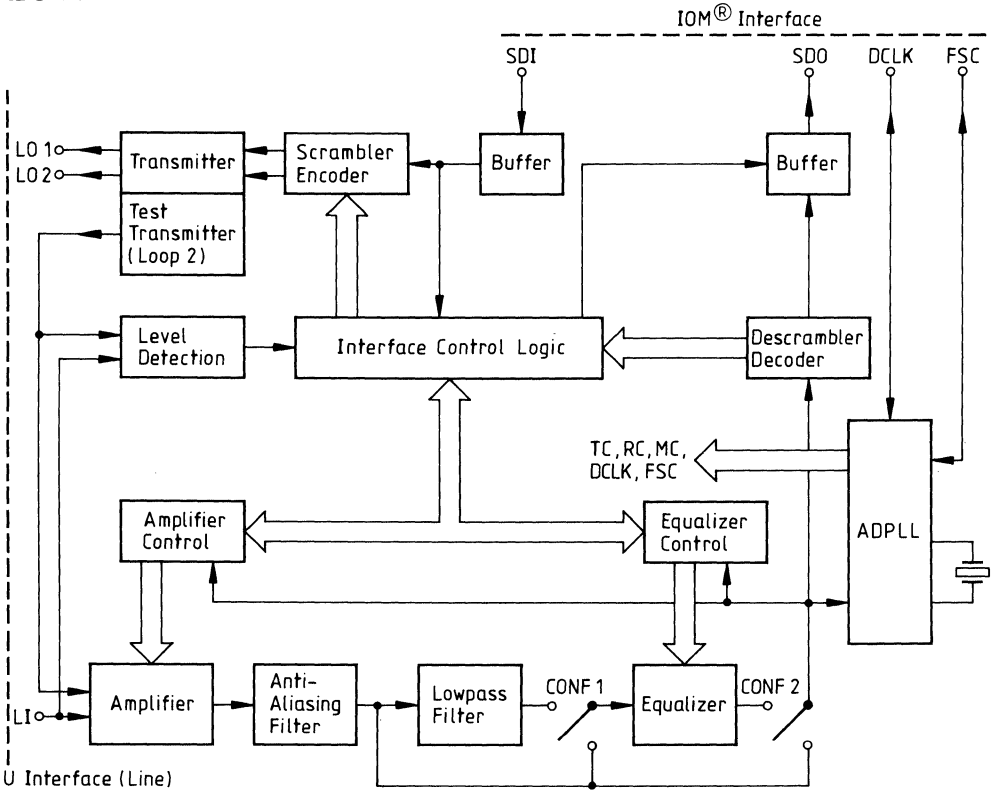
Note: **Figure 1** illustrates the CCITT defintion of the U reference point i.e. between a local exchange and a network termination. The direct connection of terminals to a PBX over a 2-wire loop is not considered by CCITT since it is not in the public network domain. Since the IBC can be used in both the aforementioned configurations, this document, for simplicity, will use the term U reference point for both. Furthermore the term U interface will refer only to the time division multiplexing technique for transmission over a 2-wire loop.

Functional Description

IBC Device Architecture and General Functions

The ISDN Burst Transceiver Circuit (IBC PEB 2095) performs the layer-1 functions of the time-division multiplex implementation of the U interface. This is a half duplex technique (ping-pong) involving transmission by only one device at any one time. Furthermore the IBC acts a link between the U interface to the IOM interface and hence to other layer-1 or layer-2 devices within the system. **Figure 2** depicts the device architecture.

Figure 2
IBC Device Architecture



TC = Transmitter Clock
RC = Receiver Clock
MC = Master Clock

Some of the relationships between the blocks of the device architecture and the IBC functions outlined below can be traced at this stage. This section, however, will deal in more detail with these relationships.

The following are the main functions of the IBC

- Activation/deactivation procedures. Activation may be initialized by either infos from the line or primitives from the IOM interface
- To increase the quality of signal received from the line, the receiver stage contains both an adaptive amplifier and equalizer
- Synchronous timing must be maintained on both sides of the device. All internal clocks are synchronized to the upstream data clock (system clock). All generated downstream clocks are synchronized, in turn, to these internal clocks.
- Testing and diagnostic functions: Testloops may be closed, test signals may be generated.

Furthermore, the IBC must also link 2 different interfaces, the IOM interface and the U interface. To do this transparently, the IBC must compensate for the following main differences between them:

- The U interface is a burst mode interface while the IOM interface is continuous
- The frame structure and data transmission techniques on both interfaces are different
- The B channels are scrambled on the U interface and unscrambled on the IOM interface
- The clock rates are different and are transmitted in a different manner. In the U interface the clock is implicit in the data stream; in the IOM interface 2 separate clocks, DCLK and FSC, must be provided.

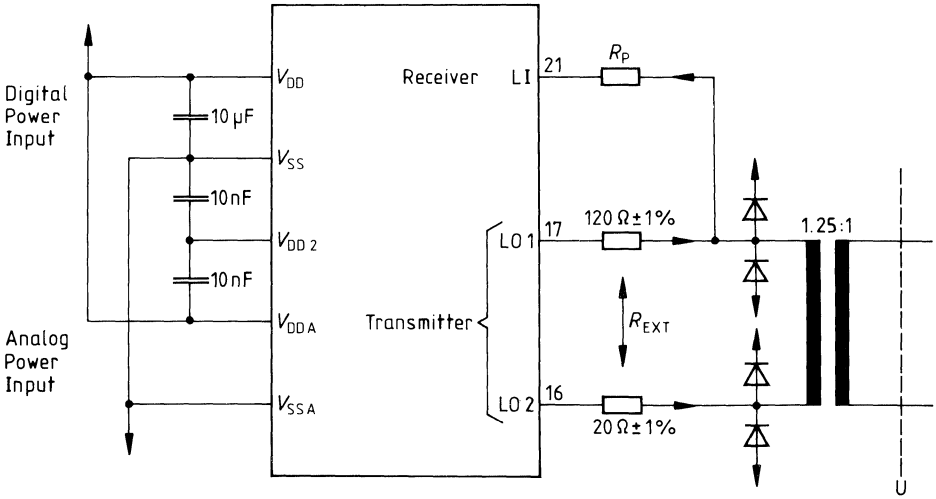
Analog Functions

Figure 3 depicts the analog and power connections to the IBC. Both analog and digital power may be connected to a single power source. The reference voltage V_{DD2} must be linked by two 10 nF capacitors to V_{SS} and V_{DDA}. External to the transmitter and receiver a transformer (ratio 1.25:1) and external resistance (R_{EXT} = 140 Ω ± 1%) are connected as shown. Voltage overload protection is achieved by splitting R_{EXT} into 120 Ω and 20 Ω (for current limitation) and adding clamping diodes. If required a resistor may be added to the signal input line for current limitation.

The transmitter stage is realized as a voltage source with an internal resistance R_i = 15 Ω ±40%. It delivers a pulse of amplitude 2 V ±10% (0-to-peak). Assuming a transformer winding resistance of the order of 1 Ω, the output resistance seen from the U interface will be 100 Ω.

Referring again to **figure 2**, the receiver input stages can be seen. They consist of a variable gain amplifier, to compensate for signal losses on the line (dynamic range 30 dB). This is followed by an anti-aliasing filter and a switched capacitor low pass filter. Finally a switched capacitor equalizer suppresses the out-of-band noise, which has passed the (anti-aliasing) filter stage, while keeping the pulse distortion low (dynamic range 15.36 dB).

Figure 3
IBC Analog Connections



Note V_{DD2} is a 2.5 V Reference Output

Both the amplifier and the equalizer are adaptive. The amplifier has 128 possible settings and the equalizer 8 (in this sense they are digital). The adaptive logic can be stopped by externally setting the amplifier and equalizer over the IOM interface. Once set in this way, the settings remain constant. The monitor channel can also be used to program some other functions.

The level detection block monitors the receive line and informs the interface logic when an incoming signal is present. It also monitors the test transmitter to perform a similar function during test loop implementation.

Digital Functions

The DPLL circuitry works with an external oscillator or crystal of 15.36 MHz ±100 ppm. This is used to synchronize all bit and frame clocks with the incoming system clock (i.e. from upstream). In the LT mode, the system clock is supplied over the IOM interface. Generation of half-bauded AMI pulses for the line is accomplished by deriving a synchronous transmitter clock using the DPLL. At the NT/TE end of the line, the data clock of 384 kHz is implicitly received in the data stream and is extracted by the IBC. From this all synchronous clocks are derived with the aid of the DPLL.

An incorporated finite state machine controls ISDN layer-1 activation/deactivation. This includes wake signal recognition in the "deactivated" state.

Due to the burst nature of U interface communication and the continuous nature of communication on the IOM interface, a buffer memory is required to compensate for timing differences.

The digital control logic also sets the adaptive coefficients on the AGC amplifier and the SC equalization filter.

Scrambler/Descrambler

B channel data on the U interface is scrambled to give a flat continuous power density spectrum and to ensure enough pulses are present on the line for a reliable clock extraction to be performed at the downstream end.

The IBC therefore, contains a scrambler and descramber, in the transmit and receive directions respectively. The basic form of these are illustrated in **figure 4** and **figure 5**.

The form is in accordance with the CCITT V.27 scramber/descrambler and contains supervisory circuitry which ensures no periodic patterns appear on the line.

Figure 4
IBC Scrambler

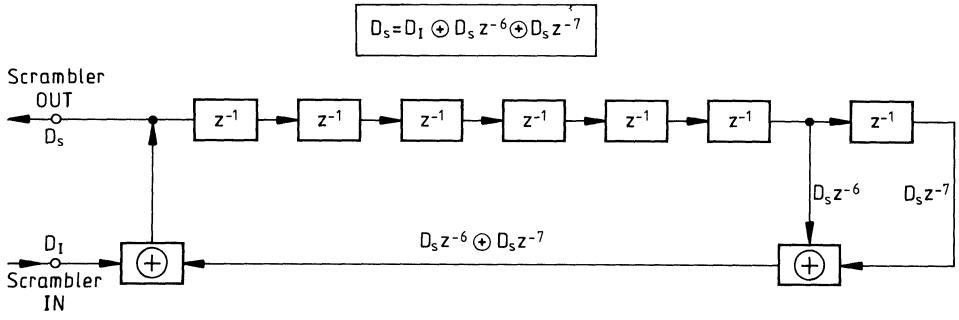
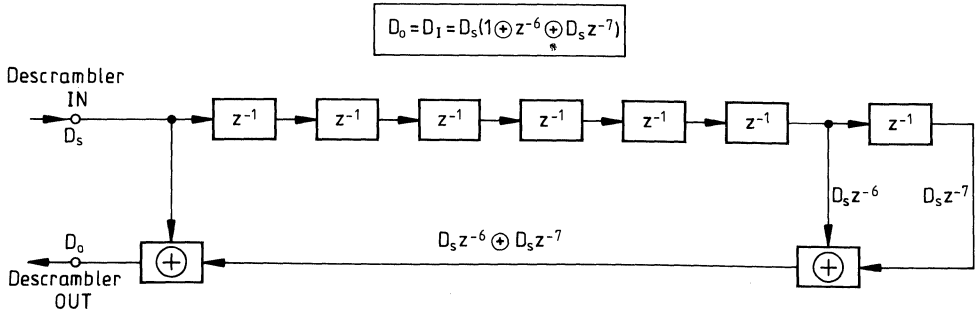


Figure 5
IBC Descrambler



Interfaces

The IBC operates 3 interfaces:

- U interface
- IOM interface
- SLD interface

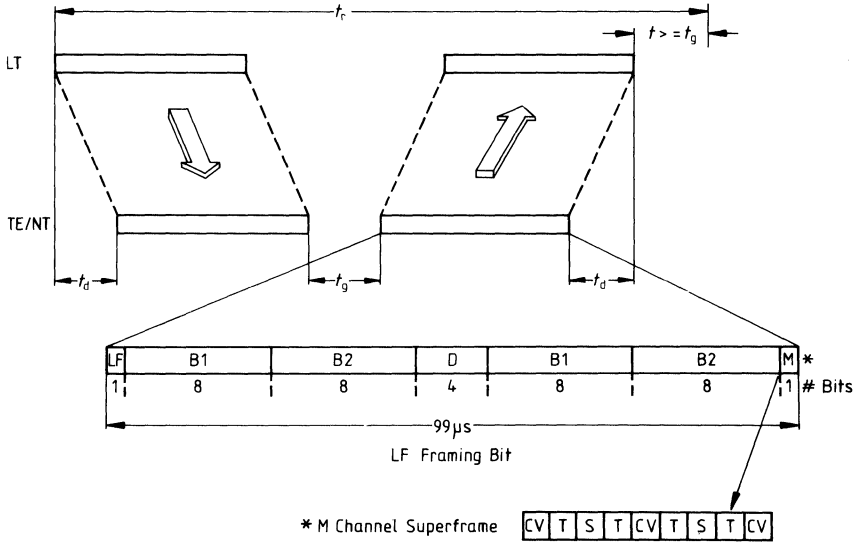
U Interface

Figure 6 demonstrates the general principles of the U interface burst mode communication technique. A frame transmitted by the exchange (LT) is received by the terminal equipment (TE) after a given propagation delay. The terminal equipment waits a minimum guard time (5.2 µs) while the line clears. It then transmits a frame to the exchange. The exchange will begin a transmission every 250 µs (known as the burst repetition period). However, the time between the reception of a frame from the TE and the beginning of transmission of the next frame by the LT must be greater than the minimum guard time. Communication between an LT and an NT follows the exact same procedure.

Within a burst, the data rate is 384 kbit/s and the 38-bit frame structure is as shown in **figure 4**. The framing bit (LF) is always logical "1". The frame also contains the user channels (2B + D). Note that the B channels are scrambled. It can readily be seen that in the 250 µs burst repetition period, 4 D bits, 16 B1 bits and 16 B2 bits are transferred in each direction. This gives an effective full duplex data rate of 16 kbit/s for the D channel and 64 kbit/s for each B channel.

The final bit of the frame is called the M bit. Four successive M bits, from four successive U frames, constitute a superframe **(figure 6)**. Three signals are carried in this superframe. Every fourth M bit is a code violation (CV) and is used for superframe synchronization. This can be regarded as the first bit of the superframe. From this reference, bit 3 of the superframe is the service channel bit (S). The S channel bit is transmitted once in each direction in every fourth burst repetition period. Hence the duplex S channel has a data rate of 1 kbit/s. It conveys test loop control information from the LT to the TE/NT and reports of transmission errors from the TE/NT to the LT. Bit 2 and bit 4 of the superframe are T bits. These constitute the 2 kbit/s T channel which extends the T channel of the IOM frame **(figure 7)** onto the U interface.

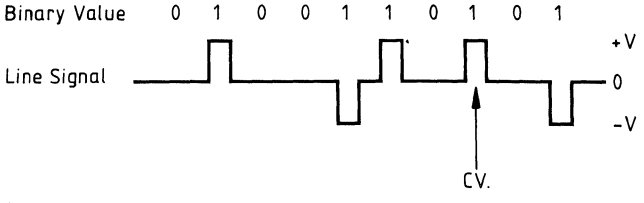
Figure 6
U Interface Transmission/Reception



Timings: t_r = Burst Repetition Period = 250 µs
t_d = Line Delay = 20.8 µs max.
t_g = Guard Time = 5.2 µs min.

The coding technique used on the U interface is half-bauded AMI code (i.e. with a 50% pulse width). **Figure 7** illustrates the code. As can be seen, a logical '0' corresponds to a neutral level, a logical '1' is coded as alternate positive and negative pulses. The figure also illustrated how a code violation may be achieved (CV); either two successive positive (as shown) or negative pulses.

Figure 7
Half-Bauded AMI Code



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.3 to V_{DD} +0.3	V

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse **(figure 8).**

Figure 8

Test Condition for Maximum Input Current

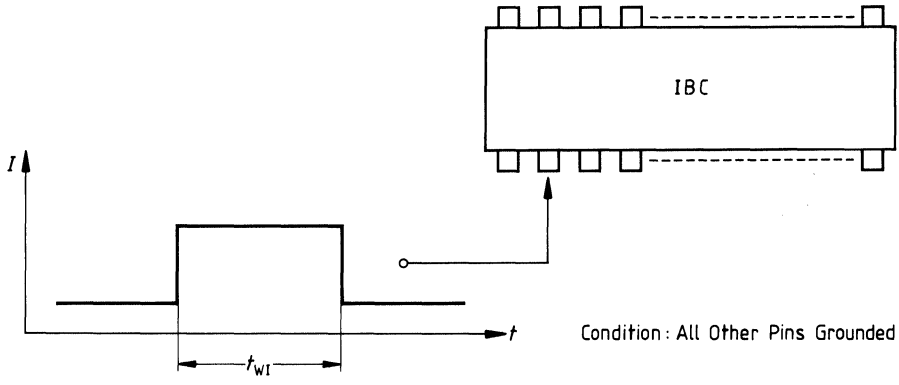


Figure 9

Transmitter Input Current
The destruction limits are given in **figure 9**
$R_1 \geq 250\ \Omega$.

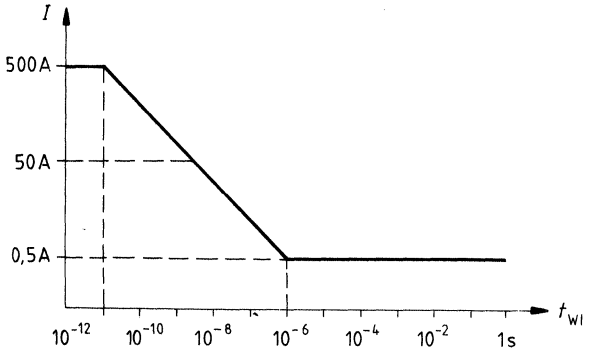
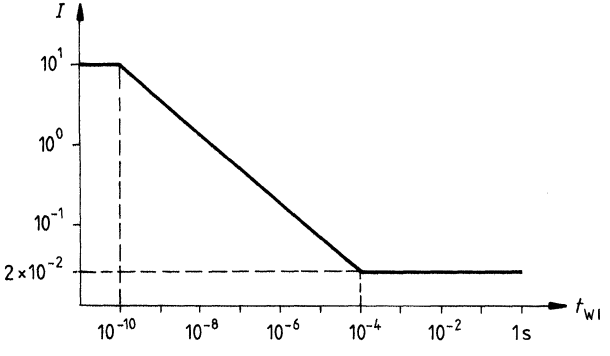


Figure 10

Receiver Input Current
The destruction limits are given in **figure 10**
$R_1 \geq 250\ \Omega$.



DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$; $V_{SSA} = 0\ V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	Remarks
L-input voltage	V_{IL}	V_{SS}-0.4	0.8	V		
H-input voltage	V_{IH}	2.0	V_{DD}+0.4	V		
L-output voltage[1)] L-output voltage[2)]	V_{OL1} V_{OL2}		0.45 0.45	V V	$I_{OL} = 2$ mA $I_{OL} = 7$ mA	All pins except L01,2 LI XTAL1 XTAL2
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD}-0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -200\ \mu A$	
Power supply current operational Power supply current power down	I_{CC} I_{CC}		13 1.3	mA mA	$V_{DD} = 5$ V, inputs at 0 V or V_{DD}, no output loads.	
Input leakage current	I_{LI}		10	µA	$0V < V_{IN} < V_{DD}$ to 0V	
Output leakage current	I_{LO}		10	µA	$0V < V_{OUT} < V_{DD}$ to 0V	
Absolute value of[3)] output pulse amplitude[4)] $(V_{L01} - V_{L02})$[5)]	V_X	4.45 −5.25 0	5.25 −4.45 0	V V V	$I_O \le 16$ mA $I_O \le 16$ mA $I_O = 0$	L01,2
Pulse width	P_W	1.22	1.38	µs		
Transmitter output impedance	R_X	9	21	Ω		
L-input voltage H-input voltage	V_{IL} V_{IH}	V_{DD}-0.5 V_{DD}-0.5	0.5	V V		XTAL1
L-output voltage H-output voltage	V_{OL} V_{OH}	 V_{DD}-0.5	0.5	V V	$I_O \le 100\ \mu A$ $C_L \le 100$ pF	XTAL2

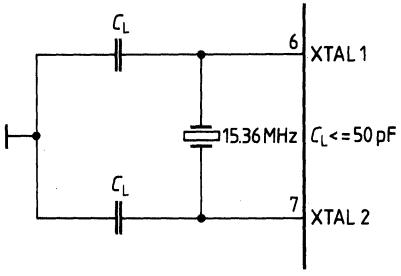
Notes: 1) All outputs except SDO
2) Output SDO only
3) Positive pulse
4) Negative pulse
5) No pulse

Capacitances

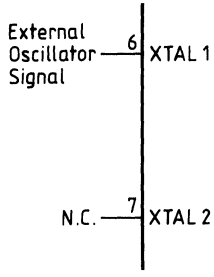
$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$; $V_{SSA} = 0\ V$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input capacitances Output capacitance	C_{IN} C_{IO}		7 7	pF pF	
Output capacitance against V_{SSA}	C_{OUT}		10	pF	L01,2
Load capacitance	C_L		50	pF	XTAL1,2

Figure 11
Recommended Oscillator Circuits



Crystal Oscillator Mode



Driving from External Source

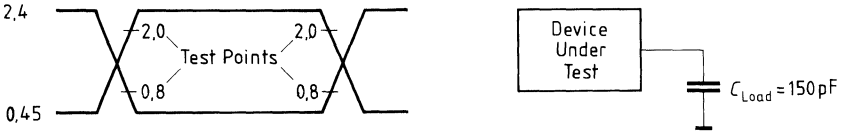
AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

Inputs are driven at 2.4 V for a logic "1" and at 0.4 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".

The AC testing input/output waveforms are shown below.

Figure 12
Input/Output Waveform for AC Tests



Clock Timing

The following timing-descriptions summarizes the clocks produced in the different operating modes and their respective duty cycles. The table also indicates which clocks are derived directly from the crystal and which are synchronized to the line using the on-board DPLL circuitry.

Table 1
Mode Specific Pin Functions

Mode	Name	Description	Pin	I/O	Function
LT	PFOFF	Power Feed OFF	X4	I	Puts the IBC into a powerfeed off state. This state is indicated by C/I code HI.
LT	MPF	Main Power Feed	X3	I	The 8-bit supply current equivalent is read serially through this pin into I (7:0) from the local power supply. The read is synchronous to the B1 channel in the IOM frame (time slot 0 in LT:mux mode). Used for power supply control by the layer-2 device. Tie low when not in use.
TE/NT	$\overline{\text{ENCK}}$	Enable Clocks	X3	I	Enables clocks in 'deactivated' state. Also during RST = 0, outputs are low impedance when $\overline{\text{ENCK}}$ = 0 and high impedance otherwise.
NT	$\overline{\text{SSP}}$	Send Single Pulses	X1	I	Test mode 1
	$\overline{\text{SCP}}$	Send Contin. Pulses	X2	I	Test mode 2
LT norm. or SLD	CONF4	Programmable Output Pin	X0	O	Programmed over monitor channel. Useful to control other devices.
LT	TS0-2	Time Slot 0 - 2	X0, 1,2	I	In MUX mode, one of eight possible time slots is selected to be read by the device (TS0 - LSB)

Figure 13
Output Clock Relationships

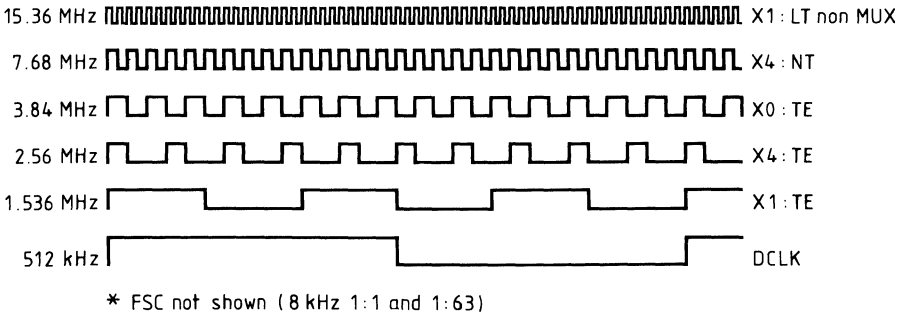


Figure 13 shows the relationship between the various clock outputs form the IBC. The crystal frequency is 15.36 MHz. All clock outputs have a duty cycle of 1:1 except 2.56 MHz (1:2). Note that the following are derived directly from the crystal oscillator; 15.36 MHz, 3.84 and 2.56 MHz. They are not synchronized to the line. Their accuracy will be, to a first order, governed by the crystal accuracy (± 100 ppm maximum).

The following clocks are derived both from the crystal and, with the help of the DPLL, from the line; 7.68 MHz, 1.536 MHz, DCLK and FSC. Synchronization may be regarded as a two stage process. Firstly, a synchronous 7.68 MHz signal is derived using the DPLL. Secondly, all other syncronous clocks are derived, by simple division, from 7.68 MHz synchronous. Because of the internal method of synchronization employed, the 7.68 MHz signal may "step forward or back" by 1 crystal period **(see figure 14)**. Hence the period of 7.68 MHz, and all synchronous clocks derived from it, may vary by one crystal period (± 65 ns). This, to a first order, gives the accuracy of the various synchronous clocks. **Table 2** to **table 6** detail the accuracy of the clock outputs with respect to the symbols.

Figure 14
Possible 7.68 MHz Clocks

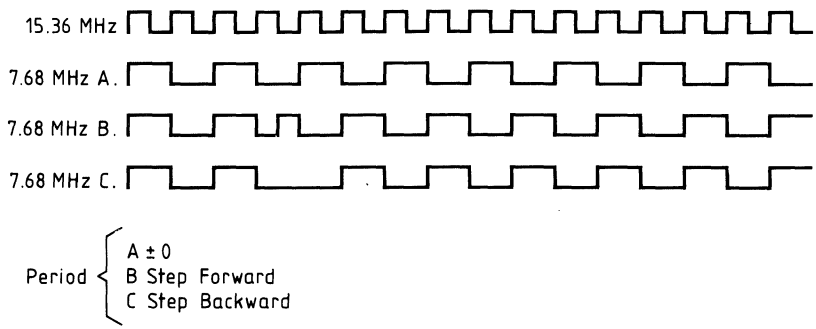


Figure 15
Clock Timing Symbols

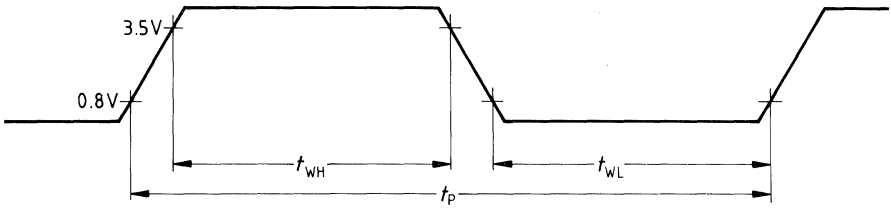


Table 2
DCLK Timing

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
TE/NT 512 kHz	t_P	1888	1953	2019	ns	Output
TE/NT 512 kHz	t_{WH}	944	977	1009	ns	
TE/NT 512 kHz	t_{WL}	944	977	1009	ns	
LT mode	t_{WH}	90			ns	Input
LT mode	t_{WL}	90			ns	

Table 3
FSC Timing

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
TE/NT 8 kHz 1:1	t_P	124.93	125	125.07	µs	Output
TE/NT 8 kHz 1:1	t_{WH}	62.46	62.5	62.54	µs	
TE/NT 8 kHz 1:1	t_{WL}	62.46	62.5	62.54	µs	
TE (SEL) 8 kHz 63:1	t_P	124.93	125	125.07	µs	
TE (SEL) 8 kHz 63:1	t_{WH}	122.08	123.05	124.02	µs	
TE (SEL) 8 kHz 63:1	t_{WL}	1888	1953	2019	ns	

Table 4
X4 Clock Timing

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
TE 2.56 MHz 1:2	t_P	−100	390	+100	ns	OSC ± 100 ppm
TE 2.56 MHz 1:2	t_{WH}	−100	130	+100	ns	OSC ± 100 ppm
TE 2.56 MHz 1:2	t_{WL}	−100	260	+100	ns	OSC ± 100 ppm
NT 7.68 MHz 1:1	t_P	65	130	196	ns	
NT 7.68 MHz 1:1	t_{WH}	65	65	131	ns	
NT 7.68 MHz 1:1	t_{WL}	65	65	131	ns	

Table 5
X1 Clock Timing

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
TE: 1.536 MHz	t_P	585	651	717	ns	
TE: 1.536 MHz	t_{WH}	260	326	391	ns	
TE: 1.536 MHz	t_{WL}	260	326	391	ns	
LT* 15.36 MHz	t_P	−100	65.1	+100	ns	OSC ± 100 ppm
LT* 15.36 MHz	t_{WH}	−100	65.1	+100	ns	OSC ± 100 ppm
LT* 15.36 MHz	t_{WL}	−100	65.1	+100	ns	OSC ± 100 ppm

* in normal and SLD modes only

Table 6
X0 Clock Timing

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
TE: 3.84 MHz	t_P	−100	260	+100	ns	OSC ± 100 ppm
TE: 3.84 MHz	t_{WH}	−100	130	+100	ns	OSC ± 100 ppm
TE: 3.84 MHz	t_{WL}	−100	130	+100	ns	OSC ± 100 ppm

Finally table 7 defined the rise and fall times of DCLK and FSC clocks in the various modes.

Table 7
DCLK/FSC Rise and Fall Timing

Parameter	Symbol	Limit Values			Unit	Mode
		min.	typ.	max.		
TRD; DCLK rise time	t_r			50	ns	NT/TE
				60	ns	LT normal
				25	ns	LT MUX
TFD; DCLK fall time	t_f			50	ns	NT/TE
				60	ns	LT normal
				25	ns	LT MUX
TFR; FSC rise time	t_r			50	ns	NT/TE
				60	ns	LT normal
				50	ns	LT MUX
TFF; FSC fall time	t_f			50	ns	NT/TE
				60	ns	LT normal
				50	ns	LT MUX

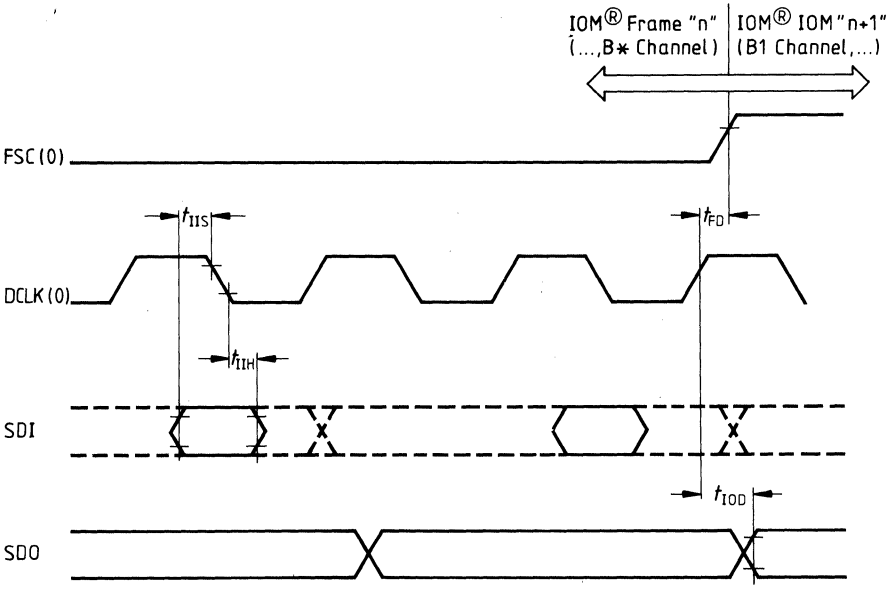
IOM Interface

Given the clock accuracies defined in the previous section, the following paragraphs define the timing relationship between the data and the DCLK and FSC clocks.

Normal Mode

Master Mode (TE/NT mode)

Normal TE/NT Mode Timing Diagram

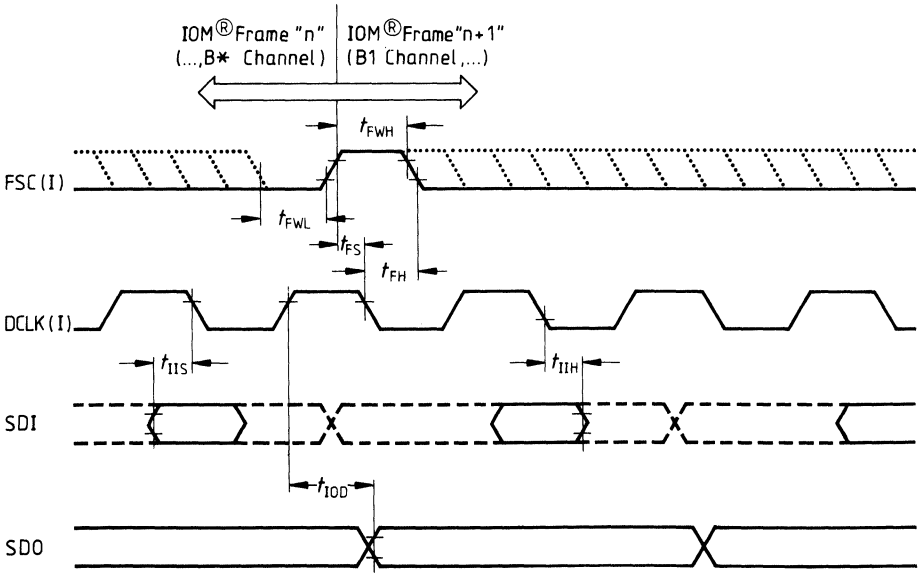


Normal TE/NT Mode Timing

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Frame sync. delay	t_{FD}	−20	20	ns	C_L = 100 pF
IOM output data delay	t_{IOD}		200	ns	C_L = 100 pF
IOM input data setup	t_{IIS}	20		ns	
IOM input data hold	t_{IIH}	50		ns	

Slave Mode (LT)

Normal LT Mode Timing Diagram

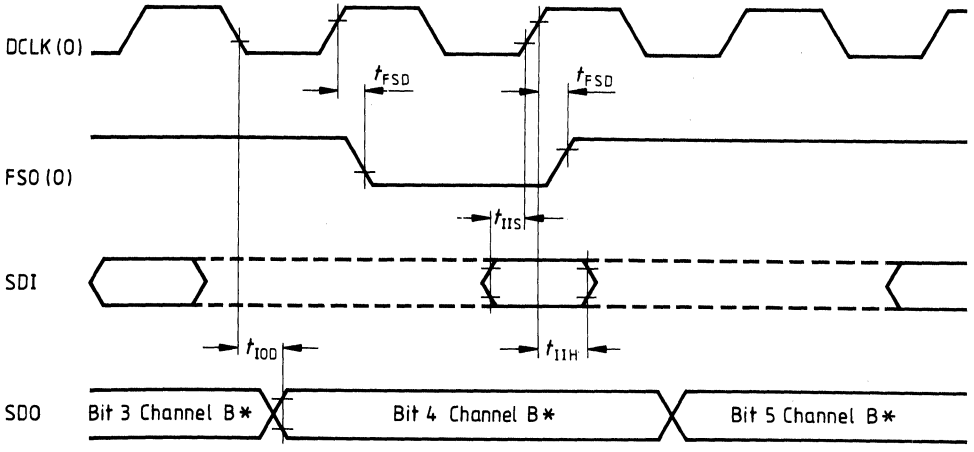


Normal LT Mode Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	30		ns
Frame sync high	t_{FWH}	80		ns
Frame sync low	t_{FWL}	2150		ns
IOM output data delay	t_{IOD}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	50		ns

TE Inverted Mode

Inverted TE Mode Timing Diagram

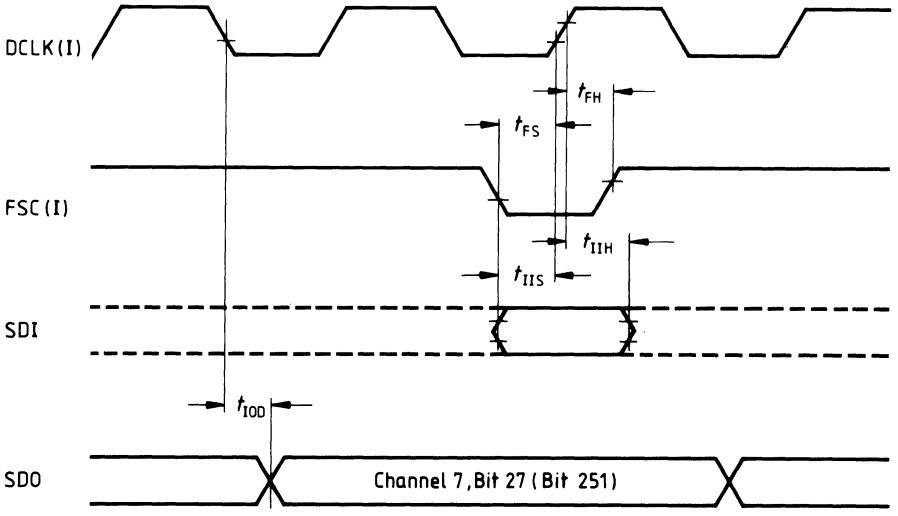


Inverted TE Mode Timing

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Frame sync delay	t_{FSD}	−20	20	ns	$C_L = 100$ pF
IOM output data delay	t_{IOD}		200	ns	$C_L = 100$ pF
IOM input data setup	t_{IIS}	20		ns	
IOM input data hold	t_{IIH}	50		ns	

LT MUX Mode

Inverted LT MUX Mode Timing Diagram



Inverted LT MUX Mode Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	20		ns
Frame sync high	t_{FH}	124.8		µs
Frame sync low	t_{EL}	70	200	ns
IOM output data delay	t_{IOM}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM output data hold	t_{IIH}	50		ns

Receiver Stage Properties

Receiver Stage Properties

Input Stage / Measured Property		dB
Line amplifier	– dynamic range	0 – 30
	– resolution (128 setting)	0.236
Anti-aliasing filter and low pass filters		
> 1.1 MHz	– minimum attenuation	30
> 1.1 MHz	– typical attenuation	35
Equalizer	– dynamic range	0 – 15.36 dB
	– resolution (8 settings)	2.194