General Description

The most challenging requirement in ISDN is full-duplex transmission at a data rate of 144 kbit/s over the existing twisted-pair telephone cables (U-interface). Among several approaches for solving this problem, ping-pong time-compression multiplexing and echo cancellation have been proposed as most suitable for VLSI implementation. Moreover, echo cancellation has proven to be the best method for public lines which typically reach lengths in the range of 8 km.

After a careful study of different transmission codes, a 4B3T block code was chosen for the IEC-T which make use of ternary coding of the binary information. A particular advantage of this code is its low frequency, DC-free performance spectrum with its energy peak at about 40 kHz. In this context, for a bit rate of 160 kbit/s the required baud rate is as low as 120 kHz. As a result transmission systems benefit from, low line attenuation low crosstalk distortion and high possible signal levels without causing EMI-problems.
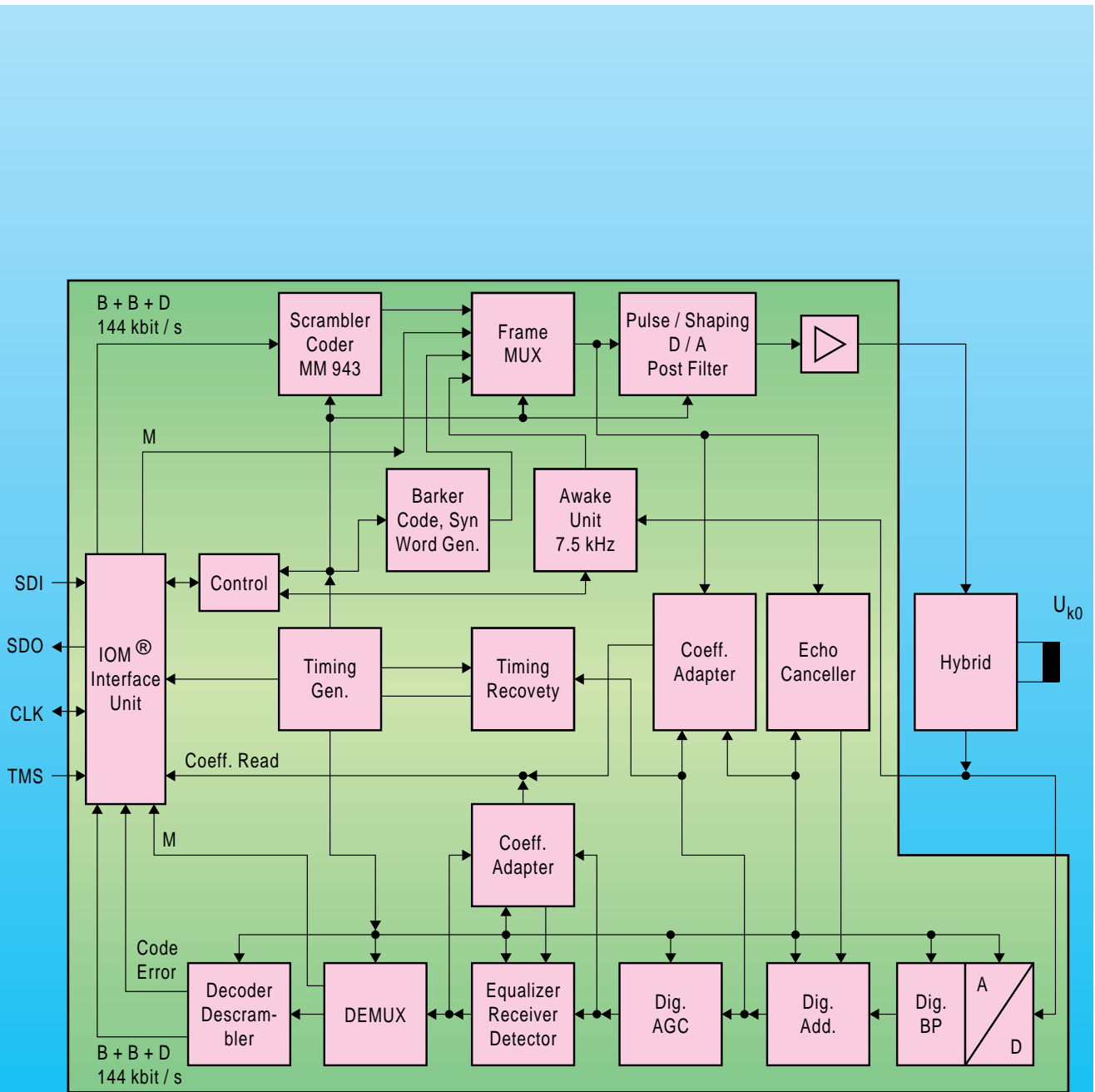
The IEC-T is offered as a two chip solution consisting of:
- Digital part, called PEB 20901
- Analog part, called PEB 20902

Type	Package
PEB 20901-N	P-LCC-44-1 (SMD)
PEB 20901-P	P-DIP-40-1 (not for new designs)
PEF 20902-N	P-LCC-28-2 (SMD)
PEB 20902-P	P-DIP-24-1 (not for new designs)
PEF 20901-N	P-LCC-28-2 (SMD)
PEF 20902-N	P-LCC-28-2 (SMD)

Features

- Full-duplex two-wire U-transceiver
- 144-kbit/s user bit rate (2B+D)
- 160-kbit/s total bit rate including maintenance and synchronization
- Low transmission frequency of 120 kbaud by using the 4B3T-ternary block code
- Adaptive echo cancellation and equalization using digital filtering (DSP)
- Recovery of clock and frame signals from the data stream
- IOM-1 interface compatible
- Transmission range up to 8 km with 0.6-mm wires
- Handling of command/indication information during activation/deactivation procedure
- Switching of test loops
- Wake-up unit for activation from power-down state
- Several operating modes including trunk applications with frame alignment
- 2-μm CMOS technology for PEB 20902, 1-μ technology for PEB 20901
- 320-mW power consumption
- Repeater mode with no external devices

Block Diagram