SIEMENS

S-Bus Interface Circuit (SBC) PEB 2080

Preliminary Data **CMOS-IC**

Type	Ordering Code	Package
PEB 2080-C	Q67100-H8329	C-DIP-22
PEB 2080-N	Q67100-H8395	PL-CC-28 (SMD)
PEB 2080-P	Q67100-H2954	P-DIP-22

The S-Bus Interface Circuit (SBC) PEB 2080 implements the four-wire S/T-interface used to link voice/data terminals to an ISDN. Through selection of operating mode, the device may be employed in all types of applications involving an S-interface. Two or more SBCs can be used to build a point-to-point, passive bus, extended passive bus or star configuration.

Specific ISDN applications of the SBC include: ISDN terminals, ISDN network termination (Central Office and PBX applications), and PBX trunk lines to Central Office.

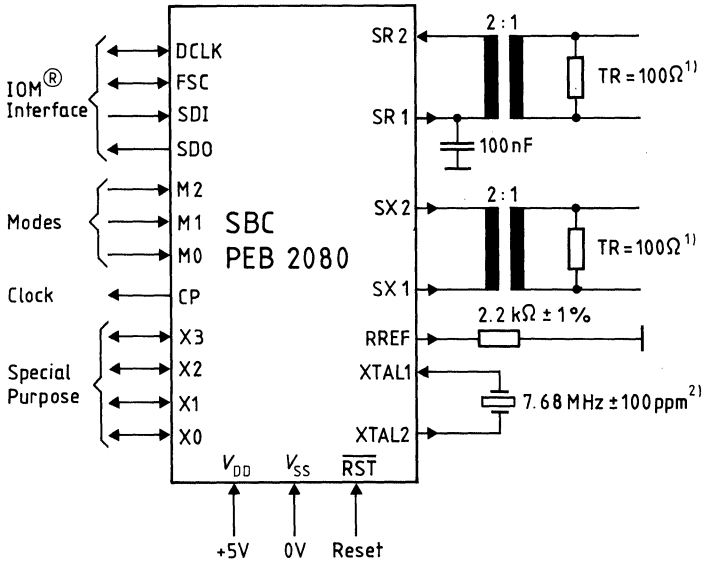
The device provides all electrical and logical functions according to CCITT recommendation I.430. These include: mode-dependent receive timing recovery, D-channel access and priority control, and automatic handling of activation/deactivation procedures. The SBC does not require direct microprocessor control.

The SBC is an IOM® compatible, 22-pin CMOS device. It operates from a single +5 V supply and features a power-down state with very low power consumption.

Features

- Full duplex 2B + D S/T-interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T and IOM interfaces
- D-channel access control
- Activation and deactivation procedures according to CCITT I.430
- Built-in wake-up unit for activation from powerdown state
- Adaptively switched receive threshold
- Control via IOM interface
- Several operating modes
- Receive timing recovery according to selected operating mode
- Frame alignment with absorption of phase wander in trunk line applications
- Switching of test loops
- Advanced CMOS technology
- Low power consumption: standby less than 4 mW
  active max 60 mW

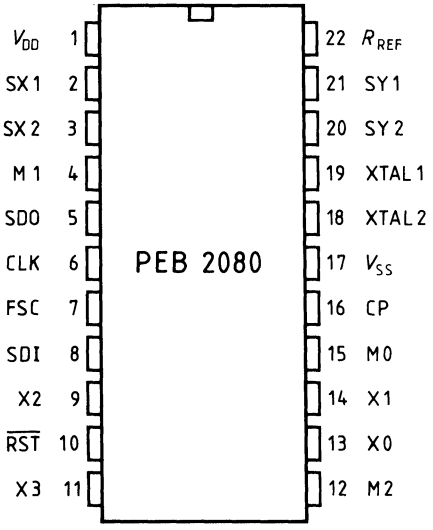
Logic Symbol



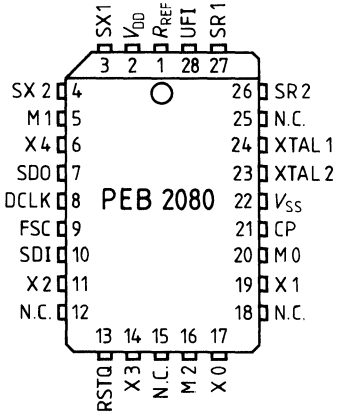
* Terminating resistors only at the far ends of the connection

Pin Configurations
(top view)

P-DIP-22; C-DIP-22



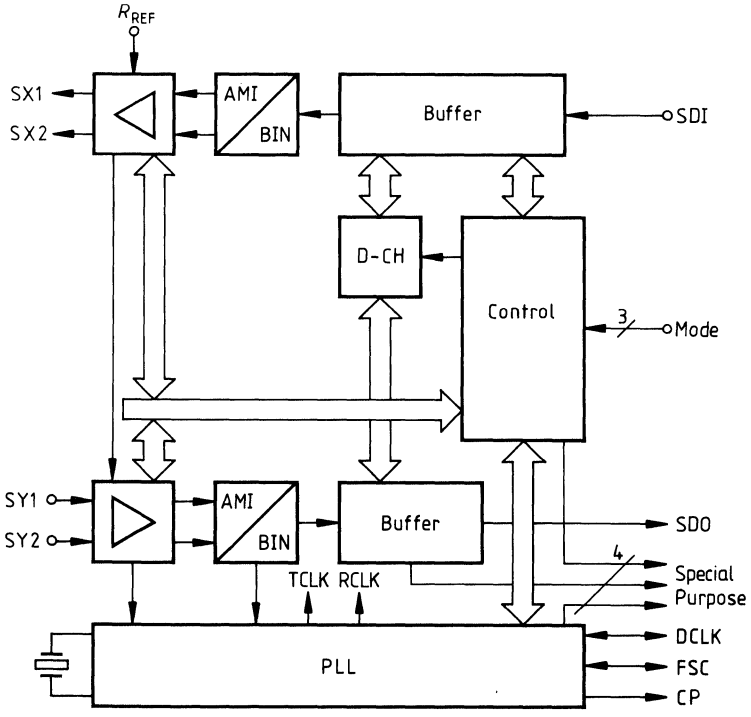
PL-CC-28



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
2	SX1	O	Positive output S-bus transmitter
3	SX2	O	Negative output S-bus transmitter
5	SDO	O	Serial data out, IOM interface
8	SDI	I	Serial data in, IOM interface
6	DCLK	I/O	Serial data clock, IOM interface
7	FSC	I/O	Frame Sync, IOM interface
12 4 15 11	M2 M1 M0 X3	I I I I	Setting of operating mode
9 14 13	X2 X1 X0	I/O I/O I/O	Functions depending on the selected operating mode **see chapter Operating Modes**
16	CP	I/O	Clock Pulse/special purpose
19	XTAL1	I	Connection for external crystal, or input for external clock generator
18	XTAL2	O	Connection for external crystal, N.C., when external clock generator is used.
20	SR2	I	S-bus Receiver, signal input
21	SR1	O	S-bus Receiver, 2.5 V reference output
22	R_{REF}	O	Connection of reference resistor to ground (2.2 kΩ ± 1%)
1	V_{DD}	I	Power supply, +5 V ± 5%
17	V_{SS}	I	Power supply, ground
10	$\overline{RST}$	I	Reset, active low

Block Diagram



System Integration

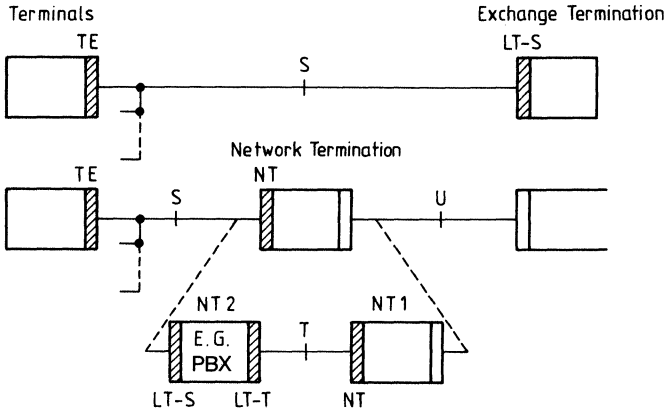
The SBC implements the four-wire S and T interfaces used in the ISDN basic access. It may be used at both ends of these interfaces.

The Applications Include

ISDN terminals (TE)
ISDN network termination (NT)
ISDN subscriber line termination (LT-S)
ISDN trunk line termination (LT-T)
(PBX connection to Central Office).

These applications are shown in **figure 1,** where the usual nomenclature as defined by the CCITT for the basic access functional blocks and reference points has been used.

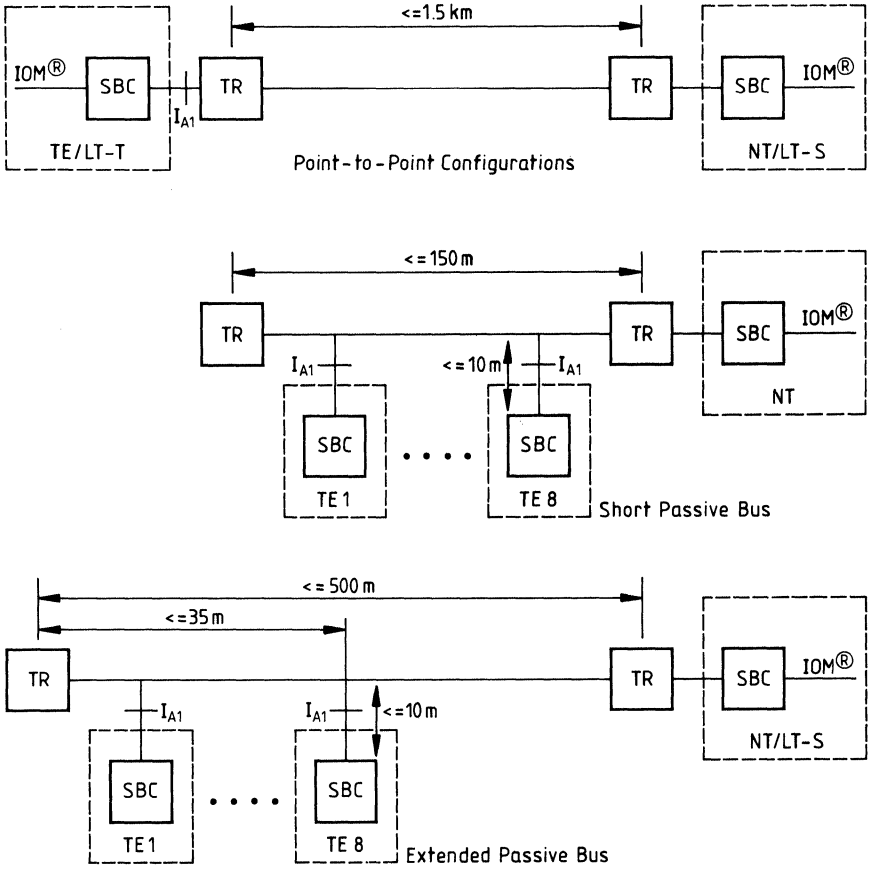
Figure 1
Applications of the SBC



Some of the S interface wiring configurations possible with the SBC are shown in **figure 2**, with approximate typical distances.

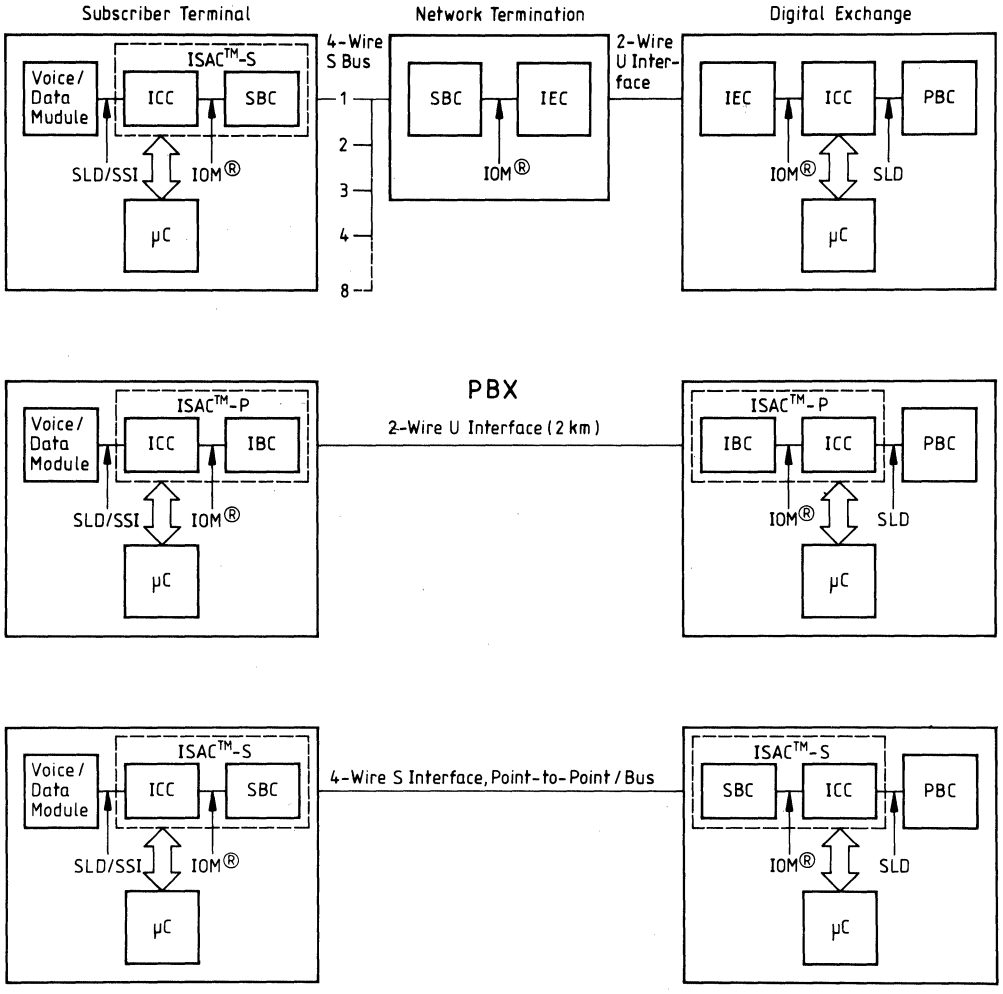
*) (N.B.: "TR" stands for terminating resistor of value 100 Ω).

Figure 2
Some S-Interface Wiring Configuration



*) The maximum line attenuation tolerated by the SBC is 15 dB at 96 kHz.

Figure 3
ISDN Oriented Modular (IOM) Architecture



PEB 2050	Peripheral Board Controller	PBC
PEB 2070	ISDN Communication Controller	ICC
PEB 2080	S Bus Interface Circuit	SBC
PEB 2085	ISDN Subscriber Access Controller (S Bus)	ISAC™-S
PEB 2090	ISDN Echo Cancellation Circuit	IEC
PEB 2095	ISDN Burst Transceiver Circuit	IBC
PEB 20950	ISDN Subscriber Access Controller (PBX, U Interface)	ISAC™-P

Figure 3 gives an example of an application of the SBC in an IOM (ISDN Oriented Modular) architecture.

By separate implementation of OSI layer-1 and layer-2 functions, and through unified control procedures, the architecture provides flexibility with respect to various transmission techniques. The IOM devices are all low-power, high integration, single +5 V supply CMOS devices. Through mode switching, each devices may be used in several applications: thus with one and the same limited set of devices all ISDN basic access configurations are covered. Note that none of the compatible layer-1 devices (SBC, IBC, IEC) requires direct microprocessor control. This is due to the fact that IOM interface provides all the necessary functions for layer-1 – layer-2 communication.

Functional Description

The S-bus interface circuit PEB 2080 performs the layer 1 functions for the S/T interface of the ISDN basic access.

General Functions and Device Architecture

The common functions for all operating modes are:

- line transceiver functions for the S interface according to the electrical specifications of CCITT I.430;
- dynamically adaptive threshold control for the receiver;
- conversion of the frame structure between IOM and S interfaces;
- conversion from/to binary to/from pseudo-ternary code.

Mode specific functions are:

- receive timing recovery;
- S timing generation using IOM timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation;
- activation/deactivation procedures, triggered by primitives received over the IOM interface or by INFO's received from the line;
- frame alignment according to CCITT Q.503;
- execution of test loops.

For a block diagram, **see figure Block Diagram**

Analog Functions

The full-bauded pseudo-ternary pulse shaping is achieved with the integrated transmitter which is realized as a voltage limited current source. A current of 7.5 mA is delivered over SX1-SX2, which yields a voltage 1.5 V over 200 Ω.

The receiver is designed as a threshold detector with adaptively switched threshold levels. Pin SR1 delivers 2.5 V as an output, which is the virtual ground of the input signal on pin SR2.

An external transformer of ratio 2:1 is needed in both receive and transmit direction to provide for isolation and transform voltage levels according to CCITT recommendations.

Digital Functions

A DPLL circuitry working with a frequency of 7.68 MHz ±100 ppm serves to generate the 192-kHz-line-clock from the reference clock delivered by the network and to extract the 192-kHz-line clock from the receive data stream.

The 7.68-MHz-clock may be generated with the use of an external crystal between pins XTAL1 and XTAL2. It may also be provided by an external oscillator, in which case XTAL2 is left unconnected.

The "Control" block includes the logic to detect layer-1 commands and to communicate with external layer-1 or layer-2 devices via the IOM interface.

An incorporated finite state machine controls ISDN layer-1 activation/deactivation.

The D-channel access procedure according to CCITT I.430 including priority management is fully implemented in the SBC. When used as an S-bus master in a multipoint configuration, the device generates the echo bits necessary for D-channel collision detection. In the NT-mode, moreover, the echo channel may be made externally available through an auxiliary pin and thus "intelligent NT's" (star configuration) may be implemented.

In terminal applications (TE) the Q channel as specified by I.430 is supported*).

The buffer memory serves to adapt the different bit rates of the S and the IOM interface. In addition, in trunk line applications it absorbs the possible deviation between two system clocks, according to CCITT Q.503 (slip detection).

Operating Modes

The operating modes are determined by pin strapping on pins M0 to M2. The four basic operating modes are: TE, NT, LT-S, LT-T.

In three of these operating modes, the IOM may be programmed to function in the normal mode, in the inverted mode (clock frequency 512 kHz) or in the inverted mux mode (clock frequency 4096 kHz). To see which IOM timing mode is applicable in the four basic operating modes, refer to **table 1.**

In **table 1**, the functions of the operating mode specific pins are given: these pins are DCLK (IOM interface data clock, input/output), FSC (IOM interface frame sync, input/output), CP (auxiliary clock/test pin), and X0 to X3.

Depending on the selected mode, pins CP, X2 and X1 provide auxiliary clocks, either asynchronous or synchronous to the S-interface:

3840 kHz
2560 kHz
1280 kHz
} clocks derived from the 7680-kHz-crystal

1536 kHz
512 kHz
} clocks synchronized to S-interface.

These auxiliary clocks may be used to drive, e.g. a codec filter, or a microprocessor system (TE applications).

*) Stepping A 6 and up. The SBC sends a binary one in FA bit position to allow another terminal to use the extra transmission capacity.

The other uses of the auxiliary pins are:

$\overline{\text{ENCK}}$	input	Enable clock. At "0", forces the SBC to deliver IOM timing at all times, regardless of SDI input level; in TE mode, pin X3.
Bus	input	At "1", specifies a bus configuration (as opposed to point to point or extended passive bus); in NT and LT-S modes, pin X3.
ECHO	output push-pull	Reproduces the E-bits received from the S-interface synchronously to IOM frame "D"-bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary "1"; in TE mode, pin X2.
$\overline{\text{SSZ}}$	input	Send Single Zeros. At "0", forces the SBC to transmit alternating pulses at 250 µs intervals (period 2 kHz) on S-interface for test purposes; X2 in NT mode.
RDY	output push pull	Ready. Provides a signal logically equal to bit 3 of monitor channel. Signals the D-channel status ("0" = occupied, "1" = free) to layer 2 component; X0 in TE mode.
CON	input	Connected. At "0", prevents the SBC from activating and transmitting on the S-interface. Indicates whether the device is connected to the S-interface or not; X0 in TE and LT-T modes.
DEX	input	External D-channel echo enable. At "1", makes the E-bit dependent on the DE (X0) input. Used in NT mode to build a star configuration; X1 in NT mode.
DE	input/ output open drain with integrated pull-up resistor	D-channel Echo. The DE outputs should be tied together (open drain) in an NT star configuration, to obtain the global echo bit; X0 in NT mode.
TS0 to TS 2	inputs	Time slot 0 to 7. IOM interface time slot to be used = 4 x TS2 + 2 x TS1 + TS0; LT-T and LT-S in IOM mux mode.

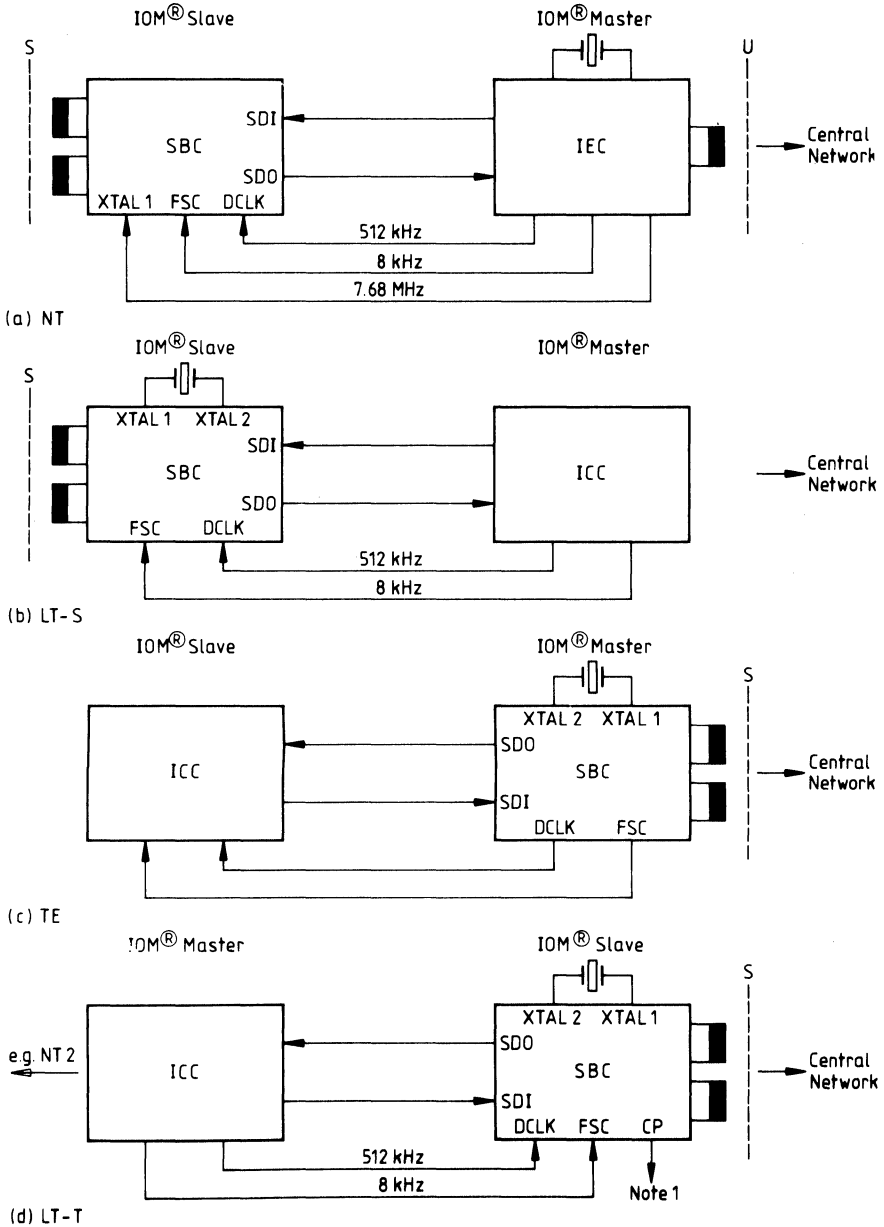
Table 1
Operating Modes and Functions of Mode Specific Pins of PEB 2080

	Application								
	TE	**TE**	**TE**	**LT-T**	**LT-T**	**NT**	**LT-S**	**LT-S**	**LT-S**
Operation of IOM Interface	Inverted Mode	Inverted Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCLK	o:512kHz*	o:512kHz*	o:512kHz*	i:4096kHz	i:512kHz	i:512kHz	I:4096kHz	i:512kHz	i:512kHz
FSC	o:8kHz*	o:8kHz*	o:8kHz*	i:8kHz	i:8kHz	i:8kHz	i:8kHz	i:8kHz	i:8kHz
CP	o: 1536kHz*	o: 1536kHz*	o: 1536kHz*	o:512kHz*	o:512kHz*	i:$\overline{\text{SCZ}}$	i: fixed at 0	i: fixed at 0	i: fixed at 0
X3	i:$\overline{\text{ENCLK}}$	i:$\overline{\text{ENCLK}}$	i:$\overline{\text{ENCLK}}$	i: fixed at 1	i: fixed at 0	I: BUS	i: BUS	i: BUS	i: BUS
X2	o: 2560kHz	o: 1280kHz	o:ECHO	i: TS2	i: fixed at 0	i:$\overline{\text{SSZ}}$	i:TS2	i: fixed at 0	o:192kHz
X1	o: 3840kHz	o: 3840kHz	o: 3840kHz	i:TS1	i: fixed at 0	i:DEX	i:TS1	o: 7680kHz	o: 7680kHz
X0	o:RDY	o:RDY	i:CON	i:TS0	i:CON	i/o:DE	i:TS0	i: fixed at 0	i:fixed at 1

*) synchronized to S i: input o: output

$\overline{\text{SCZ}}$	Send continuous binary zeros (96 kHz)
ENCLK	Enable clock at all times
BUS	Bus configuration specified
TS2-0	Time-slot number of IOM
$\overline{\text{SSZ}}$	Send single binary zeros (2 kHz)
DEX	D-channel echo external/internal
RDY	D-channel status on S-interface
CON	Connected to S bus
DE	D-channel echo bit in NT star configuration

Figure 4
Clocking of SBC in Different Operating Modes



IEC = ISDN Echo Cancellation Circuit PEB 2090
ICC = ISDN Communication Controller PEB 2070

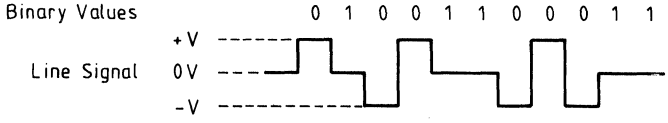
Note 1: Reference clock (512 kHz, duty cycle 1:2) may be used to drive, e.g. NT 2 clock generator

Interfaces

S Interface

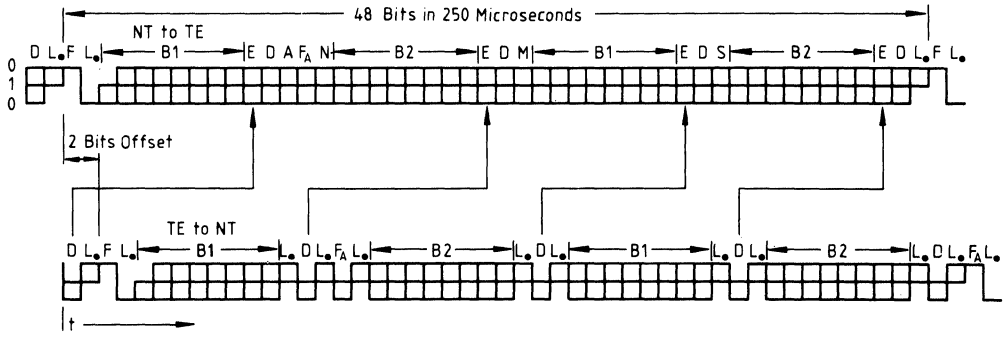
According to CCITT recommendation I.430, pseudo-ternary encoding with 100% pulse width is used on the S interface. A logical 1 corresponds to a neutral level (no current), whereas logical 0's are encoded as alternating positive and negative pulses. An example is shown in **figure 5**.

Figure 5
S Interface Line Code



One S-frame consists of 48 bits, at a nominal bit rate of 192 kbit/s. Thus each frame carries two octets of B1, two octets of B2, and four D-bits, according to the B1+B2+D structure defined for the ISDN basic access (total useful data rate: 144 kbit/s). Frame begin is marked using a code violation (no mark inversion). The frame structures (from network to subscriber, and subscriber to network) are shown in **figure 6**.

Figure 6
Frame Structure at Reference Points S and T (CCITT I.430)



F = Framing Bit
L = DC Balancing Bit
D = D-Channel Bit
E = D-Echo-Channel Bit
F = Auxiliary Framing Bit or Q-Bit
N = Bit Set to a Binary Value $N = \overline{F_A}$

B1 = Bit within B-Channel 1
B2 = Bit within B-Channel 2
A = Bit Used for Activation
S = S-Channel Bit
M = Multiframing Bit

Note: Dots Demarcate those Parts of the Frame that are Independently DC-Balanced.

Digital Interface

IOM Frame Structure

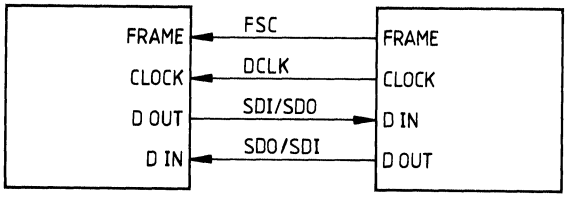
The SBC is provided with a digital interface, the IOM interface, for communication with other ISDN devices, in other words with units realizing OSI layer-1 functions (such as the ISDN Echo Cancellation Circuit IEC PEB 2090) or layer-2 functions (such as the ISDN Communication Controller ICC PEB 2070).

The IOM interface is a four-wire serial interface with: a bit clock, a frame clock and one data line per direction **(figure 7)**.

The ISDN data rate of 144 kbit/s (B1 + B2 + D) is transmitted transparently in both directions over the interface. In addition, it is necessary to interchange control information for activation and deactivation of OSI layer-1 and for switching of test loops. This information is transferred using time division multiplexing with a 125-µs total frame length.

Figure 7

IOM Interface Signals

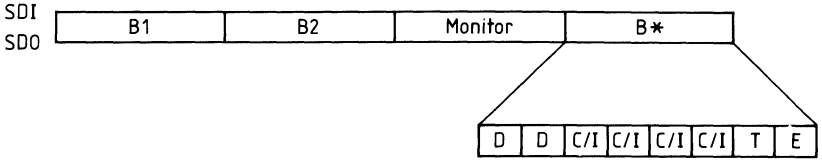


In LT-S :	SBC	ICC
In NT :	SBC	IEC
In LT-T :	SBC	ICC
In TE :	ICC	SBC

The basic frame consists of a total of 32 bits, or four octets: B1 + B2 + D (18 bits) plus 14 bits of monitor and control information. The data in both directions are synchronous and in phase **(figure 8)**.

Figure 8

IOM Interface Frame Structure



1st octet B1: B channel (64 kbit/s), most significant bit first
2nd octet B2: B channel (64 kbit/s), most significant bit first
3rd octet: monitor channel (64 kbit/s), most significant bit first
4th octet B*: 2 bit D channel (16 kbit/s)
4 bit C/I channel
T channel: not used with SBC
E bit: not used with SBC.

The C/I channel is used for communication between the SBC and a processor via a layer-2 device, to control and monitor layer-1 functions. The codes originating from layer-2 devices are called "commands", those sent by the SBC are called "indications". For a list of the C/I codes and their use, see the SBC Technical Manual.

Three modes of the IOM are distinguished. These modes differ only with respect to the physical data rate (256 or 8 x 256 kbit/s) and to polarity of the clocks.

Normal Mode

This timing mode is applicable in all operating modes of the SBC.

Nominal bit rate of data (SDI and SDO): 256 kbit/sec

Nominal frequency of DCLK: 512 kHz

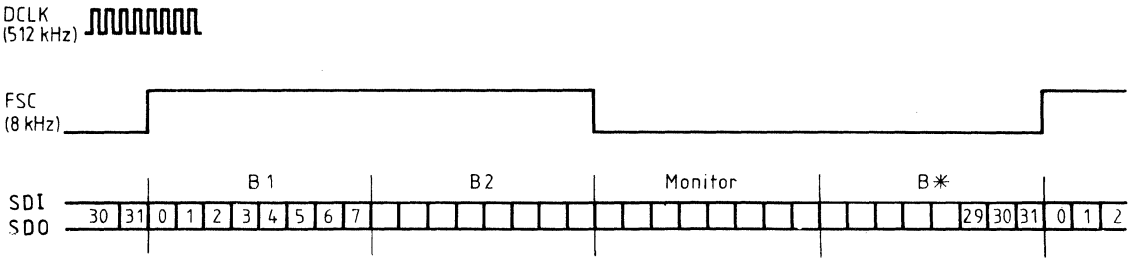
Nominal frequency of FSC: 8 kHz

Transitions of the data occur after even-numbered rising edges of DCLK. Even-numbered rising edges of the clock are defined as the second rising edge following the rising edge of FSC and every second rising edge thereafter.

The frame is earmarked by the rising edge of FSC.

Figure 9

Timing of Data and Clocks of IOM in the Normal Mode



Inverted Mode

This timing mode is only applicable in TE mode.

The characteristics are the same as above, except that FSC is not a signal with 50% duty cycle but an active low pulse, one DCLK clock period long, which occurs in the middle of bit 27 (fourth bit of B*).

Inverted Mux Mode

This timing mode is applicable in the LT-T and LT-S operating modes.

Nominal bit rate of data bursts (SDI and SDO)	2048 kbit/sec
Nominal frequency of DCLK	4096 kHz
Nominal frequency of FSC	8 kHz.

The frame clock FSC is an active low strobe clock. The strobe earmarks the second half of bit no. 251 in the frame. The low state of the strobe is detected with the rising edge of DCLK. Refer to **figure 10**.

The data at the input SDI is valid on the even-numbered rising edges of DCLK. Transitions of the data on SDO occur after even-numbered falling edges of DCLK. The rising edge earmarked by the frame strobe is an even-numbered rising edge of DCLK. The following falling edge is an even-numbered falling edge.

The bursts are allocated to consecutive time slots in a frame by the static inputs X0(TS0), X1(TS1), X2(TS2). **Table 2** indicates the allocations. **Figure 11** gives the positions of the respective frames.

Figure 10

Timing of Data and Clocks of IOM in the Inverted Mux Mode

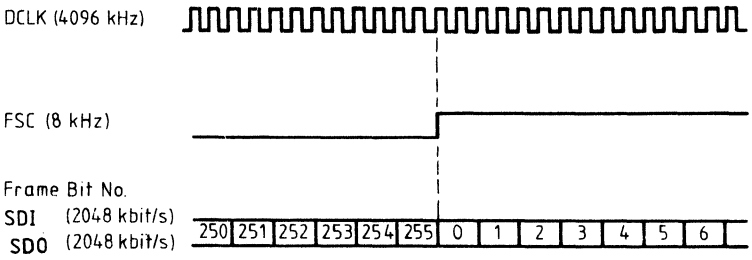


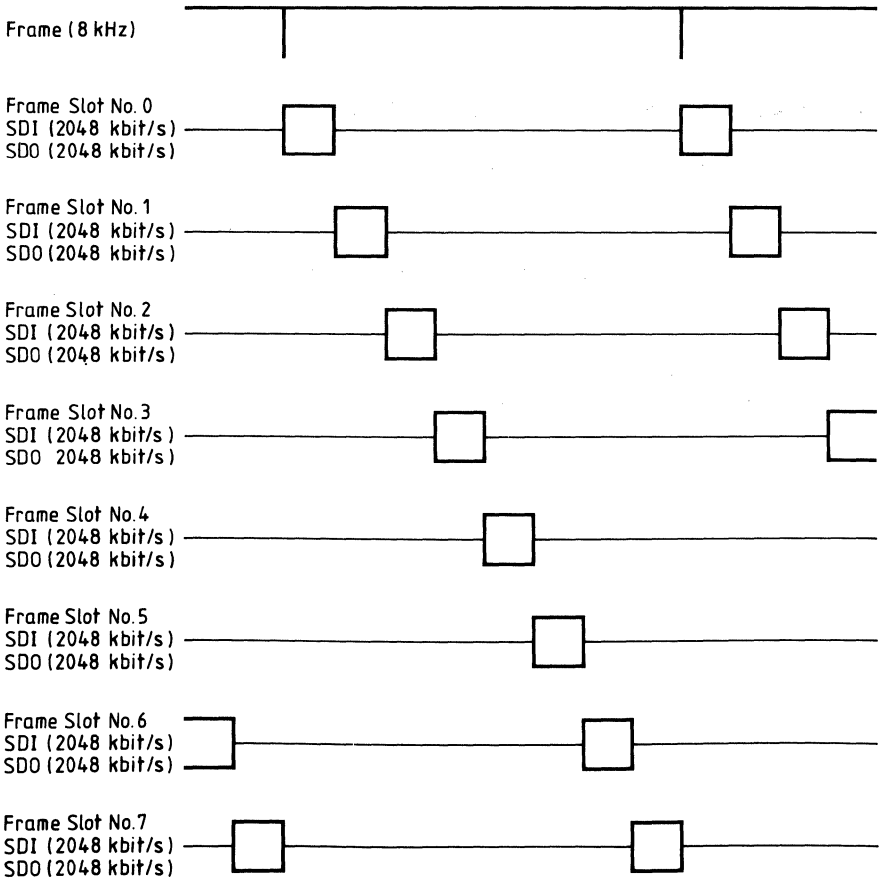
Table 2

Allocation of Time Slots

Time Slot No.	TS2	TS1	TS0	Bit No.
0	0	0	0	0 ... 31
1	0	0	1	32 ... 63
2	0	1	0	64 ... 95
3	0	1	1	96 ... 127
4	1	0	0	128 ... 159
5	1	0	1	160 ... 191
6	1	1	0	192 ... 223
7	1	1	1	224 ... 255

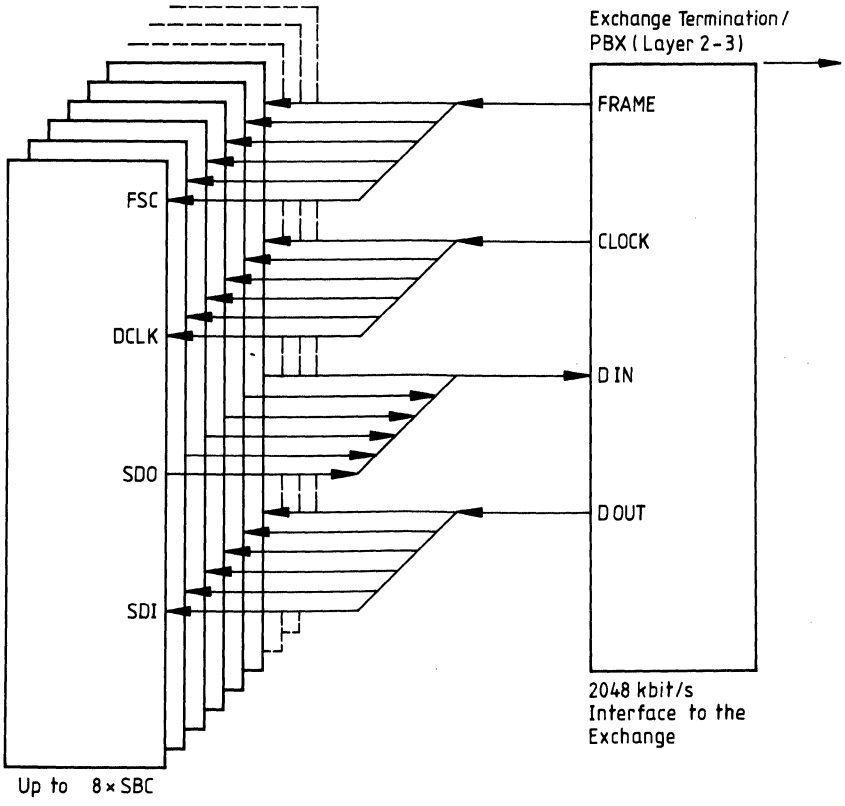
Figure 11

Position of IOM Frames as a Function of Time-Slot Allocation in Inverted Mux Mode



The mux mode may be used to link up to eight SBC's over a single 2048 kbit/s interface to an exchange or PBX **(figure 12)**.

Figure 12
IOM Interface 2048 kbit/s Mux Mode



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	-0.4 to $V_{DD}+0.4$	V
Power dissipation	P_D	1	W
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C

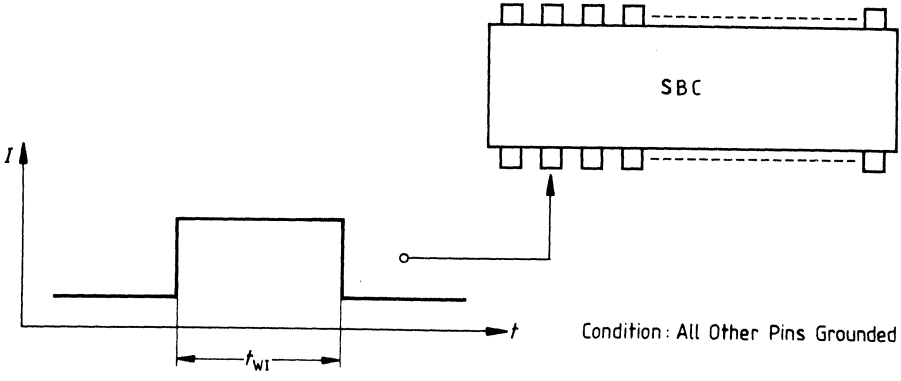
Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse **(figure 13)**.

Figure 13

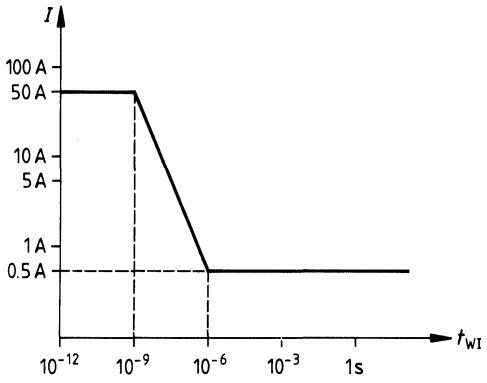
Test Condition for Maximum Input Current



Transmitter Input Current

The destruction limits are given in **figure 14.**
$R_i \geq 2\ \Omega$.

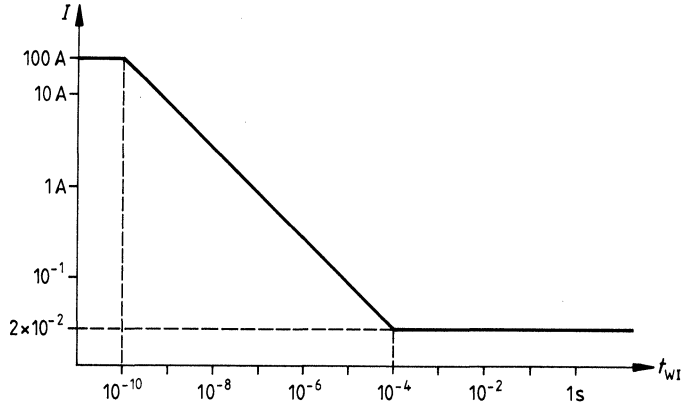
Figure 14



Receiver Input Current

The destruction limits are given in **figure 15.**
$R_i \geq 300\ \Omega$.

Figure 15



DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	
L-input voltage	V_{IL}	−0.4	0.8	V		
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V		All pins
L-output voltage L-output voltage (SDO)	V_{OL} V_{OL1}		0.45 0.45	V V	$I_{OL} = 2$ mA $I_{OL} = 7$ mA	ex-cept
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} −0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$	SX1,2 SR1,2 RREF
Power supply current — operational	I_{CC}		12	mA	$V_{DD} = 5$ V inputs at V_{SS}/V_{DD} no output loads	
Power supply current — power down	I_{CC}		0.8	mA	$V_{DD} = 5$ V inputs at V_{SS}/V_{DD} no output loads	
Input leakage current	I_{LI}		10	µA	$0\ V < V_{IN} < V_{DD}$ to 0 V	
Output leakage current	I_{LO}		10	µA	$0\ V < V_{OUT} < V_{DD}$ to 0 V	
Absolute value of output pulse amplitude (VSX2 − VSX1)	V_X	1.35 1.35 2.03 2.10	1.65 2.4 2.31 2.39	V V V V	$R_L = 50\ \Omega$ [1] $R_L = 400\ \Omega$ [1] $R_L = 50\ \Omega$ [1) 2)] $R_L = 400\ \Omega$ [1) 2)]	
Transmitter output current	I_X	7.5	13.4	mA	$R_L = 5.6\ \Omega$ [1]	SX1,2
Transmitter output impedance	R_X	10		kΩ	inactive or during binary one	
		80		Ω	during binary zero [3] $R_L = 50\ \Omega$	
Receiver output voltage	V_{SR1}	2.4	2.6	V	$I_O < 5\ \mu A$	SR1,2
Receiver threshold voltage VSR1 − VSR2	V_{TR}	225	375	mV	dependent on peak level	
Voltage at RREF	V_O	1.0	1.2	V	$R_{REF} = 2.2\ k\Omega \pm 1\%$	RREF [4]
Output current	I_O	450	550	µA	$R_{REF} = 2.2\ k\Omega \pm 1\%$	

Notes: 1) Due to the transformer, the load resistance as seen by the circuit is four times R_L.
2) From SBC A7 onwards.
3) From A7 onwards, the 80 Ω output impedance is external.
4) Applies only up to A6.

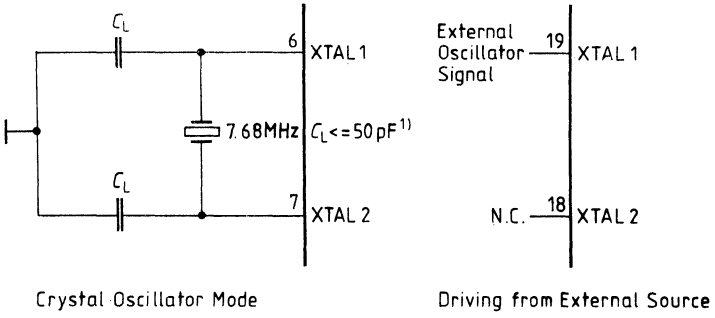
Cpacitances

$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	
Input capacitance I/O capacitance	C_{IN} C_{IO}		7 7	pF pF	All pins except SR1,2 XTAL1,2
Output capacitance against V_{SSA}	C_{OUT}		10	pF	SX1,2
Input capacitance	C_{IN}		7	pF	SR1,2
Load capacitance	C_{LD}		50*)	pF	XTAL1,2

Recommended Oscillator Circuit

Figure 16



Crystal Oscillator Mode

Driving from External Source

*) for the version up to and including A4 this value should not exceed 20 pF. This maximum capacitance is determined by the maximum oscillator startup time of 4 ms.

Table 3
Output Stages

	Application								
	TE	TE	TE	LT-T	LT-T	NT	LT-S	LT-S	LT-S
Operation of IOM Interface	Inverted Mode	Inverted Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCLK	Push/Pull	Push/Pull	Push/Pull						
FSC	Push/Pull	Push/Pull	Push/Pull						
CP	Push/Pull	Push/Pull	Push/Pull	Push/Pull	Push/Pull				
X2	Push/Pull	Push/Pull	Push/Pull						Push/Pull
X1	Push/Pull	Push/Pull	Push/Pull					Push/Pull	Push/Pull
X0	Push/Pull	Push/Pull				open drain*			
SDO	Push/Pull	Push/Pull	Push/Pull	open drain	Push/Pull	open drain*	open drain	Push/Pull	

*) with integrated Pull-up

Table 4
SBC Clock Signals

	Application								
	TE	**TE**	**TE**	**LT-T**	**LT-T**	**NT**	**LT-S**	**LT-S**	**LT-S**
Operation Of IOM Interface	Inverted Mode	Inverted Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCLK	o:512kHz* 1:2	o:512kHz* 1:2	o:512kHz* 2:1	i:4096kHz	i:512kHz	i:512kHz	i:4096kHz	i:512kHz	i:512kHz
FSC	o:8kHz* 63:1	o:8kHz* 63:1	o:8kHz*	i:8kHz	i:8kHz	i:8kHz 1:1	i:8kHz	i:8kHz	i:8kHz
CP	o: 1536kHz* 3:2	o: 1536kHz* 3:2	o: 1536kHz* 3:2	o:512kHz* 2:1	o:512kHz* 2:1				
X2	o: 2560kHz 1:2	o: 1280kHz 1:2							o: 192kHz 1:1
X1	o: 3840kHz 1:1	o: 3840kHz 1:1	o: 3840kHz 1:1					o: 7680kHz 1:1	o: 7680kHz 1:1
X0								i: fixed at 0	i: fixed at 1

*) synchronized to S line

Input and Output Pin Configurations

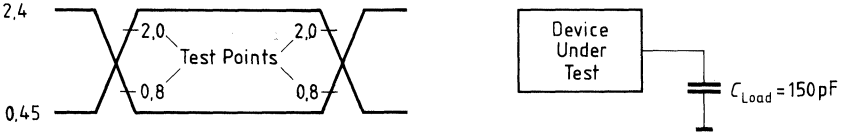
In TE, LT-T and LT-S IOM normal modes an integrated pull-up resistor is connected to SDI. For output pin configurations, **see table 3**.

AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

The AC testing input/output waveform is shown below.

Figure 17



Jitter

In TE mode, the timing extraction jitter of the SBC conforms to CCITT Recommendation I.430 (−7% to +7% of the S-interface bit period).

In the NT and LT-S applications, the clock input DCLK is used as reference clock to provide the 192-kHz-clock for the S line interface. In the case of a plesiochronous 7.68-MHz-clock generated by an oscillator, the clock DCLK should have a jitter of less than 100 ns peak-to-peak. (In the case of a zero input jitter on DCLK, SBC generates at most 130 ns "self-jitter" on S interface.)

In the case of a synchronous*) 7.68-MHz-clock (input XTAL1), the SBC transfers the input jitter of XTAL1, DCLK and FSC to the S interface. The maximum jitter of the NT/LT-S output is limited to 260 ns peak-to-peak (CCITT I.430).

*) fixed divider ratio of 15 between XTAL1 and DCLK

Clock timing

The clocks in the different operating modes are summarized in **table 4**, with duty ratios.

Clock CP is phase-locked to the receive S signal, and is derived using the internal DPLL and the 7.68 MHz ± 100 ppm crystal (TR and LT-T).

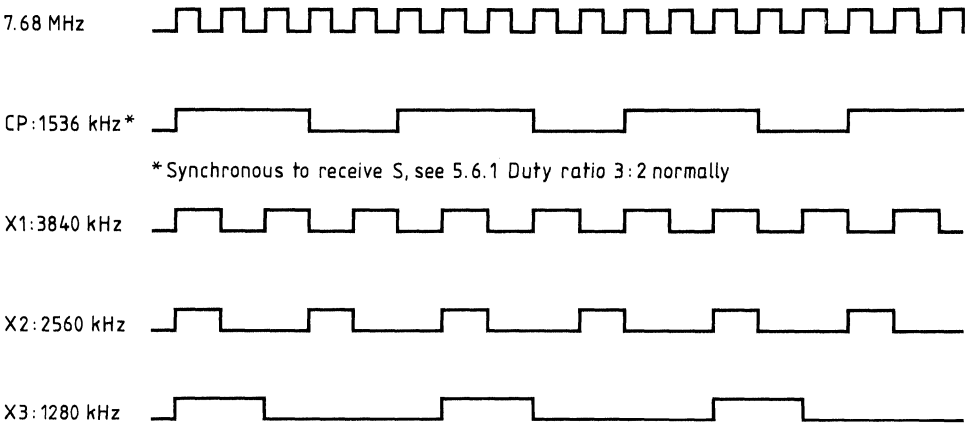
A phase tracking of CP with respect to "S" is performed once in 250 µs. As a consequence of this DPLL tracking, the high state of CP may be either reduced or extended by one 7.68-MHz-period (CP duty ratio 2:2 or 4:2 instead of 3:2) once every 250 ns.

Since DCLK and FSC are derived from CP (TE mode), the high state (FSC) or the high or low state (DCLK) may likewise be reduced or extended by the same amount once every 250 µs.*)

The phase relationships of the auxiliary clocks are shown in **figure 18**.

Figure 18

Phase Relationships of Auxiliary Clocks



*) The phase adjustment may take place either in the sixth, seventh or eight CP cycle counting from the beginning of an IOM frame in TE.

Tables 5 to 9 give the timing characteristics of the clock.

Figure 19
Definition of Clock Period and Width

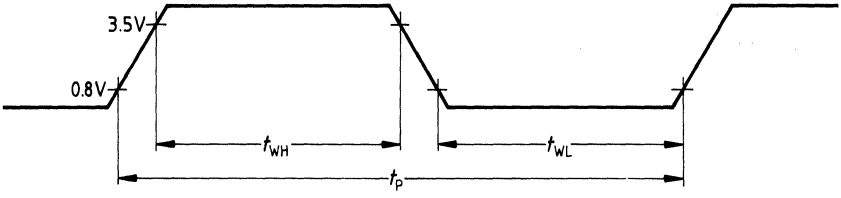


Table 5
XTAL1,2

Parameter	Symbol	Limit Values		Unit
		min.	max.	
High phase of crystal/clock	t_{WH}	20		ns
Low phase of crystal/clock	t_{WL}	20		ns

Table 6
DCLK

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 512 kHz	t_{PQ}	1822	1953	2084	ns	OSC ±100 ppm
(TE) 512 kHz 2:1	$t_{W\,HQ}$	1121	1302	1483	ns	OSC ±100 ppm
(TE) 512 kHz 2:1	$t_{W\,LQ}$	470	651	832	ns	OSC ±100 ppm
(TE) 512 kHz 1:2	$t_{W\,HQ}$	470	651	832	ns	OSC ±100 ppm
(TE) 512 kHz 1:2	$t_{W\,LQ}$	1121	1302	1483	ns	OSC ±100 ppm
(NT, LT-S, LT-T)	$t_{W\,HI}$	90			ns	
(NT, LT-S, LT-T)	$t_{W\,LI}$	90			ns	

Table 7
CP

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 1536 kHz	t_{PQ}	520	651	782	ns	OSC ±100 ppm
(TE) 1536 kHz	$t_{W\,HQ}$	240	391	541	ns	OSC ±100 ppm
(TE) 1536 kHz	$t_{W\,LQ}$	240	260	281	ns	OSC ±100 ppm
(TE, LT-T)	t_R, t_F			20 10	ns ns	C_L = 100 pF C_L = 50 pF
(LT-T) 512 kHz	t_{PQ}	1822	1953	2084	ns	OSC ±100 ppm
(LT-T) 512 kHz	$t_{W\,HQ}$	1121	1302	1483	ns	OSC ±100 ppm
(LT-T) 512 kHz	$t_{W\,LQ}$	470	651	832	ns	OSC ±100 ppm

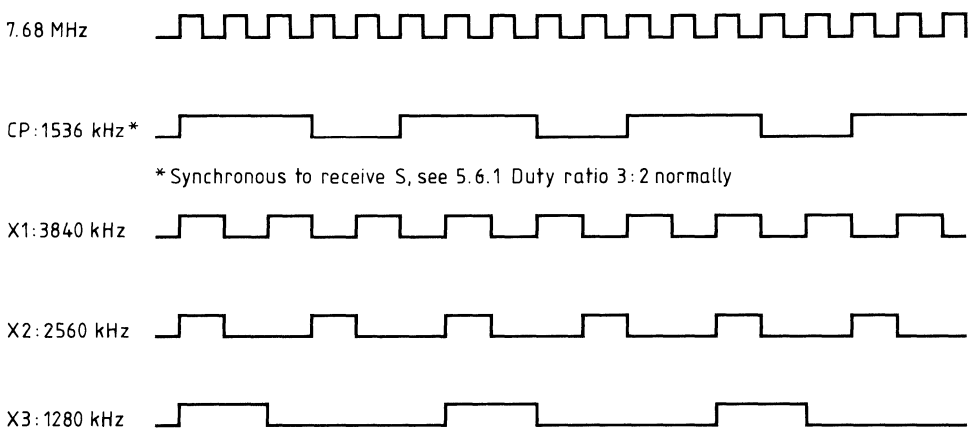
Table 8
X1

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 3840 kHz	t_{PQ}	−100 ppm	260	100 ppm	ns	OSC ±100 ppm
(TE) 3840 kHz	$t_{W\,HQ}$	120	130	140	ns	OSC ±100 ppm
(TE) 3840 kHz	$t_{W\,LQ}$	120	130	140	ns	OSC ±100 ppm

Table 9
X2

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 2560 kHz	t_{PQ}	−100 ppm	391	100 ppm	ns	OSC ±100 ppm
(TE) 2560 kHz	$t_{W\,HQ}$	110	130	150	ns	OSC ±100 ppm
(TE) 2560 kHz	$t_{W\,LQ}$	250	260	270	ns	OSC ±100 ppm
(TE) 1280 kHz	t_{PQ}	−100 ppm	781	100 ppm	ns	OSC ±100 ppm
(TE) 1280 kHz	$t_{W\,HQ}$	250	260	270	ns	OSC ±100 ppm
(TE) 1280 kHz	$t_{W\,LQ}$	511	521	531	ns	OSC ±100 ppm

CP, DCLK and FSC Relationships in IOM Master Mode

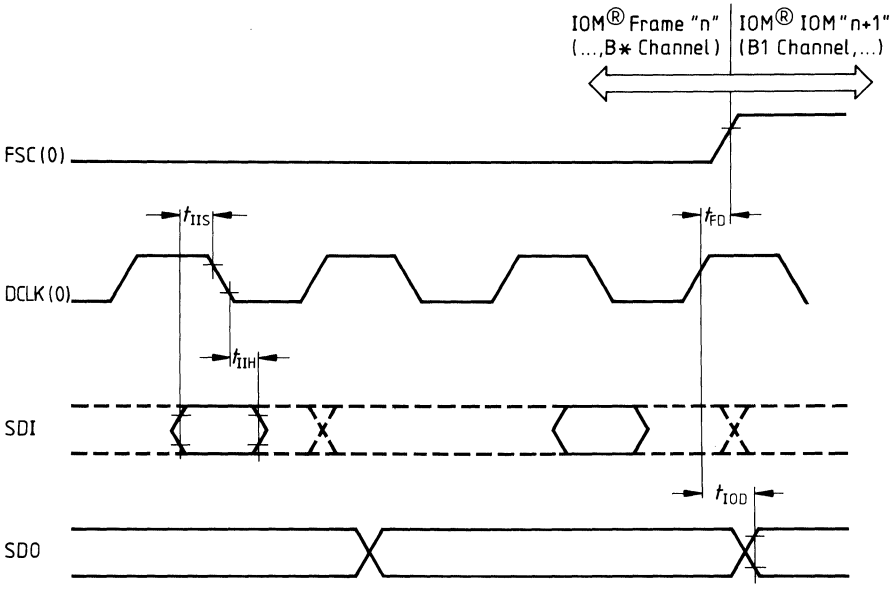


Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Clock delay CP – DCLK	t_{DC}	0	50	ns	$C_L = 100$ pF
Clock delay CP – FSC	t_{FC}	0	50	ns	$C_L = 100$ pF
Delay DCLK – FSC	t_{FD}	−20	20	ns	$C_L = 100$ pF

IOM Interface

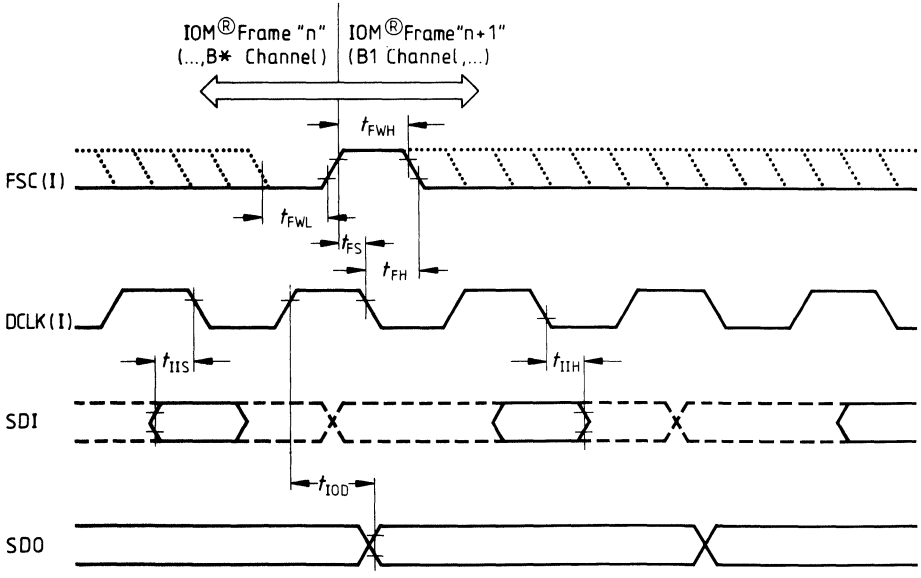
Normal mode

Master mode (TE)



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync delay C_L = 100 pF	$t_{F\,D}$	−20	20	ns
IOM output data delay C_L = 100 pF	$t_{I\,OD}$		200	ns
IOM input data setup	$t_{I\,IS}$	20		ns
IOM input data hold	$t_{I\,IH}$	50		ns

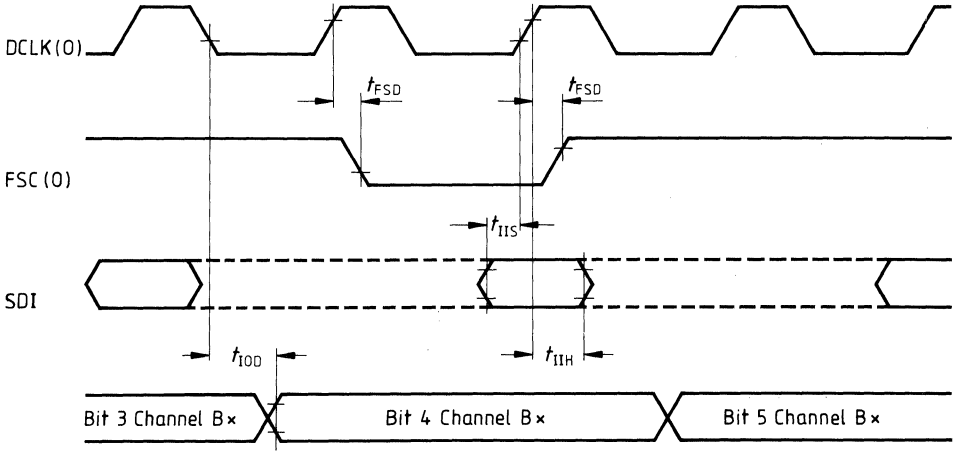
Slave Mode (NT, LT-S, LT-T)



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	$t_{F\,H}$	30		ns
Frame sync setup	$t_{F\,S}$	50		ns
Frame sync high	$t_{F\,WH}$	40		ns
Frame sync low	$t_{F\,WL}$	2150		ns
IOM output data delay	$t_{I\,OD}$		200	ns*)
IOM input data setup	$t_{I\,IS}$	20		ns
IOM input data hold	$t_{I\,IH}$	50		ns

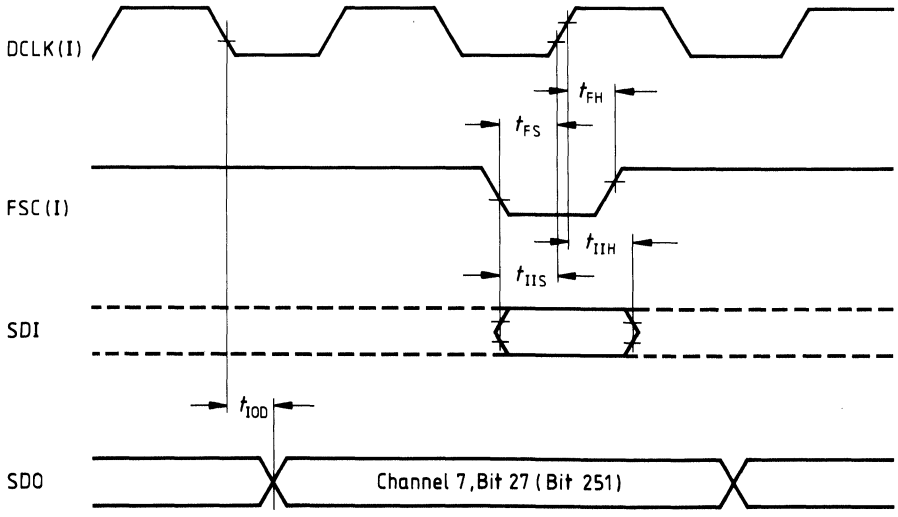
*) For push-pull output. For open drain output with integrated pull-up resistor, the maximum value is 900 ns.

Inverted Mode



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync delay C_L = 100 pF	$t_{F\,SD}$	−20	20	ns
IOM output data delay C_L = 100 pF	$t_{I\,OD}$		200	ns
IOM input data setup	$t_{I\,IS}$	20		ns
IOM input data hold	$t_{I\,IH}$	50		ns

Inverted Mux Mode



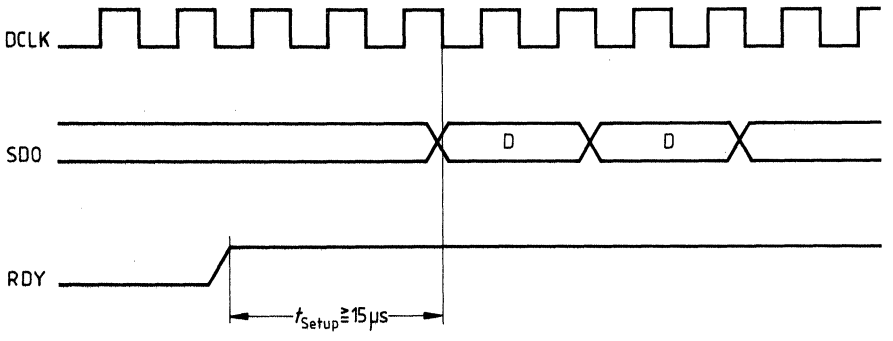
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	20		ns
Frame sync high	t_{FWH}	124.8		µs
Frame sync low	t_{FWL}	70	200	ns
IOM output data delay C_L = 150 pF; I_{OL} = 7 mA	t_{IOD}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM output data hold	t_{IIH}	50		ns

Timing of Special Function Pins

$\overline{\text{RST}}$ Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Length of active (low) state	t_{WL}	1		µs

RDY Characteristics

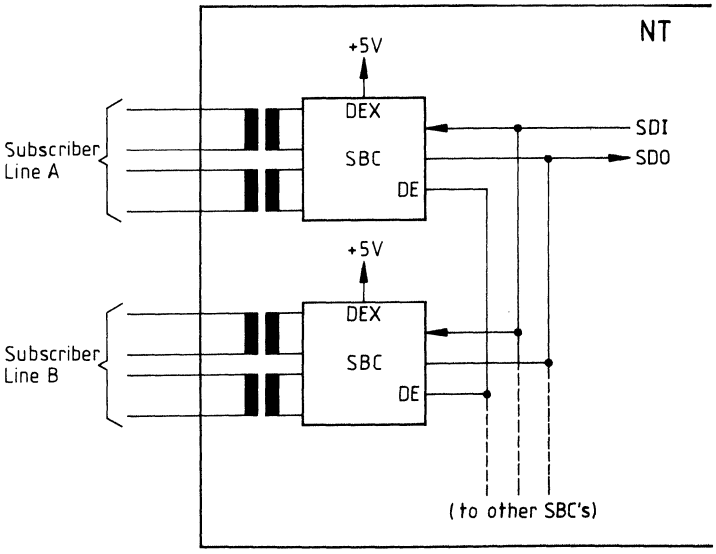


Parameter	Symbol	Limit Values		Unit
		min.	max.	
Length of low state	t_{WL}	360		µs
Length of high state	t_{WH}	60		µs

DE Characteristics

The form of the DE input/output (pin XO, NT mode) is given by **figure 20** for the case of two S interfaces having a minimum frame delay and a maximum frame delay, respectively.

Figure 20



The AC characteristics of DE output and input are shown in **figures 21** and **22** and **table 10.**

Figure 21
Timing of DE Output

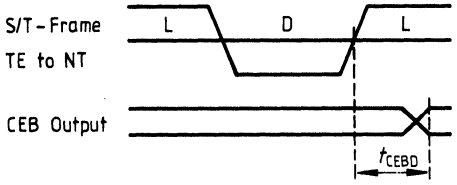


Figure 22
Timing of DE Input

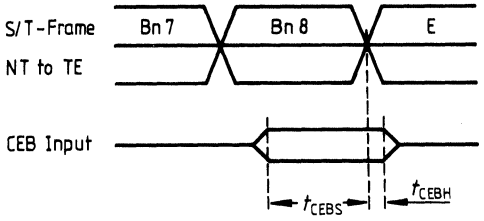


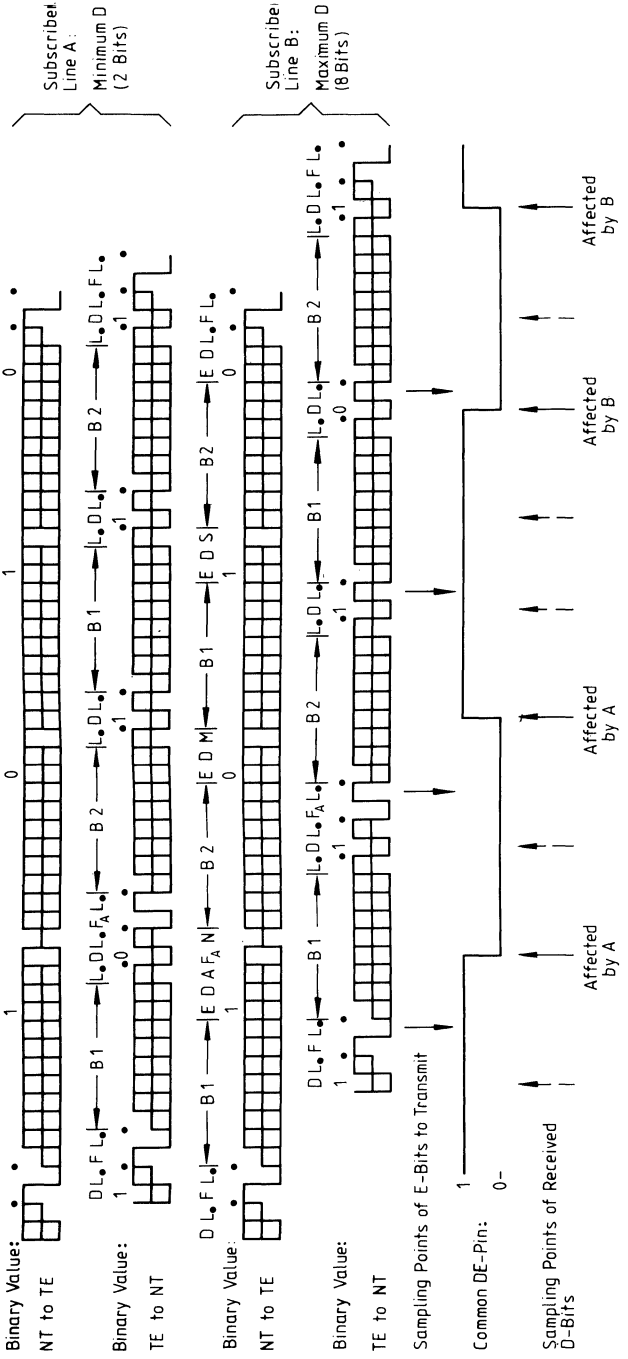
Table 10

Parameter	Symbol	Limit Values		Unit
		min.	max.	
DE delay C_L = 100 pF	t_{DED}		2	µs
DE setup	t_{DES}	5		µs
DE hold	t_{DEH}	0		µs

ECHO Characteristics

The timing of the ECHO output (pin X2, TE mode) is identical with that of output SDO: however, the signal is "1" everywhere except in bit positions 24 and 25 ("D"-bit positions) of IOM frame, where it is equal to the E-bits received from the S interface.

Figure 23
Timing of DE

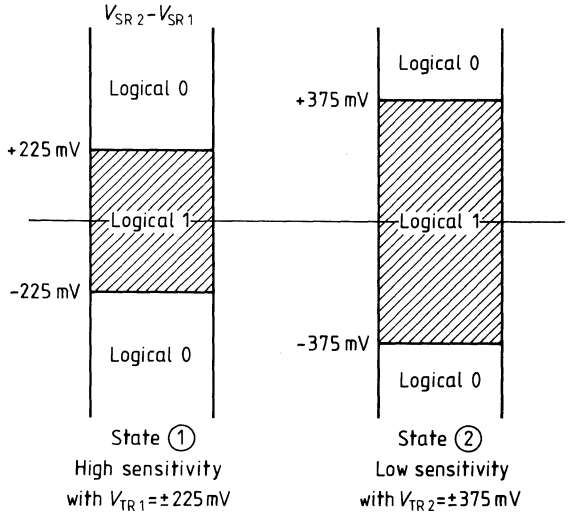


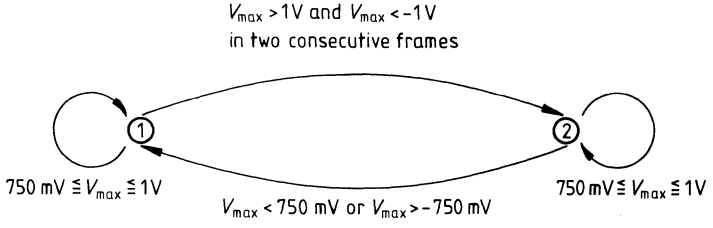
Adaptive Receiver Characteristics

The integrated receiver uses an adaptively switched threshold detector. The detector controls the switching of the receiver between two sensitivity levels. The hysteresis characteristics of the receiver are shown in **figure 23.**

Figure 24

Switching of the Receiver between High Sensitivity and Low Sensitivity





$V_{SR2}-V_{SR1}$ = Input voltage
V_{TR1}, V_{TR2} = Threshold voltages of the receiver threshold detector

V_{max} = maximum value of $V_{SR2}-V_{SR1}$ during one frame