Signal Processing Codec Filter (SICOFI) PEB 2060

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2060-P	Q67100-Z170	P-DIP-22
PEB 2060-N	Q67100-Z8393	PL-CC-28 (SMD)

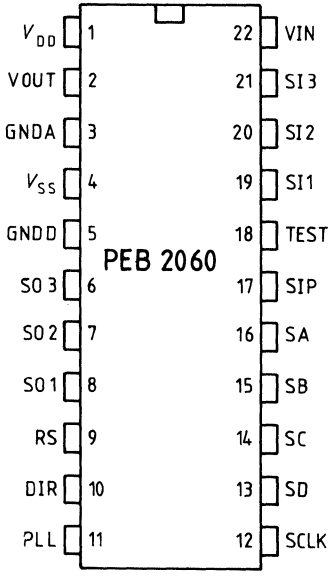
The Signal Processing Codec Filter (SICOFI®) PEB 2060 is a fully integrated PCM codec (coder/decoder) and transmit/receive filter fabricated in advanced CMOS technology for applications in digital telecommunication systems. Based on a digital filter concept, the PEB 2060 provides improved transmission performance and high flexibility. The digital signal processing approach supports software controlled adjustment of the analog behavior, including attractive features such as programmable transhybrid balancing, impedance matching, gain and frequency response correction.

Features

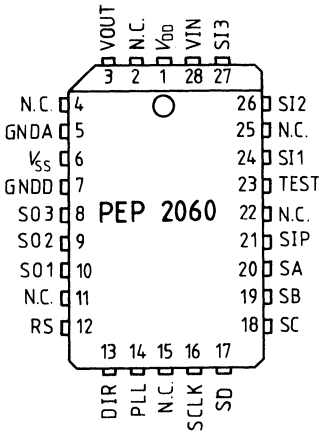
- Single chip codec and filter
- Band limitation according to CCITT and AT&T recommendations
- Digital Signal Processing techniques
- Digital voice transmission
  - PCM encoded (A-law or μ-law)
  - linear (16 bit 2s complement)
- Programmable digital filters for
  - impedance matching
  - transhybrid balancing
  - gain
  - frequency response correction
- Configurable three pin serial interface
  - 512-kHz-SLD-Bus (e.g. to PEB 2050/51)
  - burst mode with bit rates up to 8 MHz
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities
  - three digital loop back modes
  - two analog loop back modes
  - on chip sine wave generation
- No trimming or adjustments
- No external components
- Variable SICOFI Master Clock selection
- Signaling expansion possible
- Prepared for three-party conferencing
- Advanced low power 2 μCMOS technology
- Power supply +/−5 V

Pin Configuration
(top view)

P-DIP-22



PL-CC-28



Pin Definitions and Functions

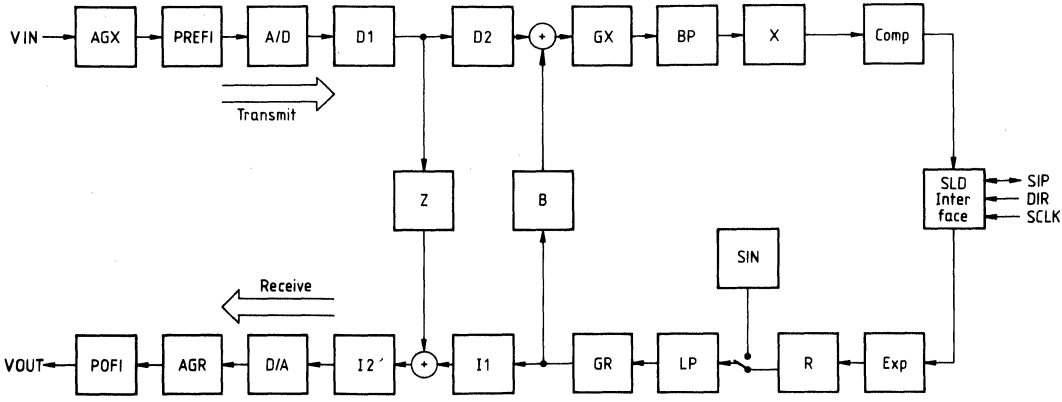
Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
1	1	V_{DD}	I	Power supply +5 V
4	6	V_{SS}	I	Power supply −5 V
3	5	GNDA	I	Ground analog, not internally connected to GNDD. All analog signals are referred to this pin.
5	7	GNDD	I	Ground digital, not internally connected to GNDA. All digital signals are referred to this pin.
22	28	VIN	I	Analog voice input to transmit path.
2	3	VOUT	O	Analog voice output of the received digital voice.
12	16	SCLK	I	Slave clock.
10	13	DIR	I	Frame synchronisation signal (direction signal).
17	21	SIP	I/O	Serial Interface Port, bidirectional serial data port.
9	12	RS	I	Reset input, active high, RS forces the SICOFI to power down mode and resets the configuration registers.
18	23	TEST	I	Test input, normally connected to GNDD.
11	14	PLL	I	Master clock selection (PLL/external clock).
19	24	SI1	I	Signaling Inputs. Data present at SI is sampled and transmitted via the serial interface.
20	26	SI2	I	
21	27	SI3	I	
8	10	SO1	O	Signaling Outputs. Data received via the serial interface is latched and fed to these outputs.
7	9	SO2	O	
6	8	SO3	O	
16	20	SA	I/O	Programmable I/O signaling pins. Each of these pins may be declared input or output individually with adequate SICOFI status settings. If 2 SICOFIs are connected to 1 serial interface, pin SA (high/low) assigns voice, control and signaling bytes.
15	19	SB	I/O	
14	18	SC	I/O	
13	17	SD	I/O	

SICOFI Principles

The SICOFI codec filter solution is a highly digital approach utilizing the advantages of digital signal processing such as excellent performance, high flexibility, easy testing, no sensitivity to fabrication and temperature variations, no problems with crosstalk and power supply rejection.

Figure 1

SICOFI Signal Flow Graph



Transmit Direction

The analog input signal is A/D converted, digitally filtered and transmitted either PCM-encoded or linear. Antialiasing is done with a 2nd order Sallen-Key prefilter (PREFI). The A/D Converter (ADC) is a modified slopeadaptive interpolative sigma-delta modulator with a sampling rate of 128 kHz. Digital downsampling to 8 kHz is done by subsequent decimation filters D1 and D2 together with the PCM bandpass filter (BP).

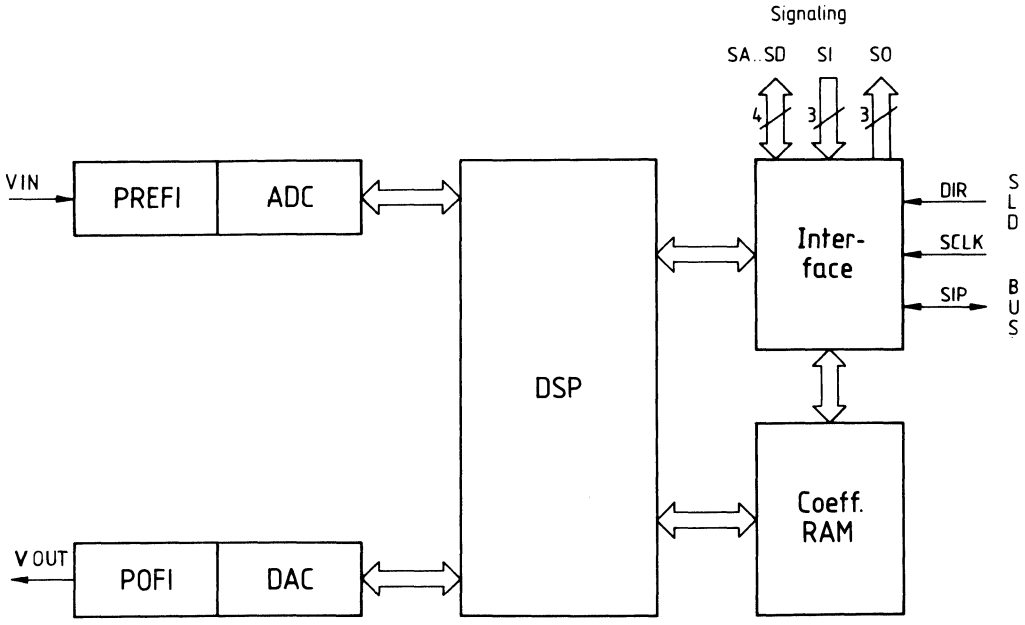
Receive Direction

The digital input signal is received PCM-encoded or linear, digitally filtered and D/A converted to generate the ananlog output signal. Digital interpolation up to 128 kHz is done by the PCM lowpass filter (LP) and the interpolation filters I1 and I2. The D/A Converter (DAC) output is fed to the 2nd order Sallen-Key postfilter (POSI).

Programmable Functions

The high flexibility of the SICOFI is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.

Figure 2
SICOFI Block Diagram



The SICOFI bridges the gap between analog and digital voice signal transmission in modern telecommunication system.

High performance oversampling analog-to-digital converter (ADC) and digital-to-analog converter (DAC) provide the conversion accuracy required. An analog antialiasing prefilter (PREFI) and smoothing postfilter (POFI) is included. The dedicated on chip digital signal processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The three pin serial SLD-Bus interface handles digital voice transmission and SICOFI feature control. Specific filter programming is done by downloading coefficients to the coefficient ram (CRAM).

The ten pin parallel signaling interface provides for a powerful per line SLIC control.

Serial Interface

The exchange of data on the SLD-Bus is based on a bidirectional, bitserial interface consisting of three pins: SIP, DIR and SCLK.

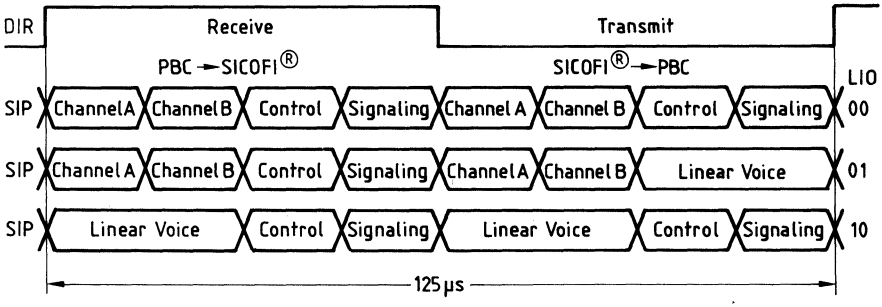
Data is written or read out on the Serial Interface Port (SIP) under control of the frame synchronisation signal DIR with a period of 125 µs*). The interface clock frequency supplied at the Slave CLocK pin SCLK is 512 kHz*). The rate of the serial data stream on the SIP pin is 512 kbit/s, that is 64 bits per each 8 kHz frame*).

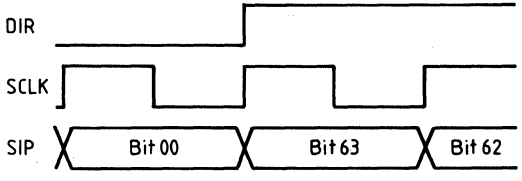
Starting with the rising edge DIR, four bytes of information are transfered on the SLD-Bus to the SICOFI, followed by four bytes from the SICOFI to the SLD-Bus.

Bit 7 is the first bit transfered and bit 0 is the last one of each byte.

Figure 3

Byte Sequence and Timing at Serial Interface Port SIP





LIO: Field LIO (Linear Operating Mode) in CR3

*) for applications with other clock rates see appendix A

Programming

A message-orientated byte transfer is used, due to the fact that the SICOFI needs extended control information. One control byte per frame and direction is transfered. With the appropriate received commands, data can be written to the SICOFI or read from the SICOFI onto the SLD-bus.

Data transfer to the SICOFI starts with a write command, followed by up to 8 bytes of data. The SICOFI responds to a read command with the requested information, starting at the next transmission period. If no status modification or data exchange is required a NOP byte is transfered **(see Programming Procedure)**.

Classes of Control Bytes

The 8-bit control bytes consist of either commands, status information or data. There are three different classes of SICOFI commands:

NOP NO OPERATION:
no status modification or data exchange

SOP STATUS OPERATION:
SICOFI status setting/monitoring

COP COEFFICIENT OPERATION:
filter coefficient setting/monitoring

The class of command is selected by bit 2 and 3 of the control byte as shown below. Due to the extended SICOFI feature control facilities, SOP- and COP-commands contain additional information.

BIT	7	6	5	4	3	2	1	0
NOP	1	1	1	1	1	1	1	1
SOP					0	1		
COP					X	0		

NOP Command

If no status modification of the SICOFI or control data exchange is required, a No Operation Byte NOP is transfered.

BIT	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	1	1

X .... don't care

SOP Command

To modify or evaluate the SICOFI status, the contents of up to four configuration registers CR1, CR2, CR3 and CR4 may be transfered to or from the SICOFI. This is done by a SOP-Command (Status Operation Command).

BIT	7	6	5	4	3	2	1	0
	AD	R/W	PU	TR	0	1	LSEL	

AD Address Information
AD = 0 A-SICOFI addressed
AD = 1 B-SICOFI addressed
This bit is evaluated if two SICOFIs are connected to one SLD-port.
A SICOFI is accessed, if AD is consistent with the level at pin SA
(see Signaling Byte, Programming Procedure).

R/W Read/Write Information
R/W = 0 Write to SICOFI
R/W = 1 Read from SICOFI
Enables reading from the SICOFI or writing information to the SICOFI.

PU Power Up/Power Down **(see also CR3)**
PU = 1 Sets the SICOFI to power-up mode (operating)
PU = 0 Resets the SICOFI to power-down (standby mode)

TR Three Party Conference
TR = 1 The received voice bytes of Channel A and Channel B are added (A+B). The result is filtered, D/A converted and transfered to Analog Output VOUT **(see also CR3)**.

LSEL Length Select Information **(see also Programming Procedure)**
This two bit field identifies the number of subsequent data bytes
LSEL = 0 0 no byte following
LSEL = 1 1 CR1 is following
LSEL = 1 0 CR2 and CR1 are following
LSEL = 0 1 CR4, CR3, CR2 and CR1 are following in this case the PU and TR bits are not overwritten.

CR1 Configuration Register 1

This configuration register is used for enabling/disabling the programmable digital filters (DB..RG) and for accessing tesmodes (TM1).

BIT	7	6	5	4	3	2	1	0
	DB	RZ	RX	RR	RG		TM1	

DB Disable B-Filter
DB = 0 : B-Filter enabled
DB = 1 : B-Filter disabled

RZ Restore Z-Filter
RZ = 0 : Z-Filter disabled
RZ = 1 : Z-Filter enabled

RX Restore X-Filter
RX = 0 : X-Filter disabled
RX = 1 : X-Filter enabled

RR Restore R-Filter
RR = 0 : R-Filter disabled
RR = 1 : R-Filter enabled

RG Restore GX-GR-Filter
RG = 0 : GX-GR-Filter disabled
RG = 1 : GX-GR-Filter enabled

TM1			TESTMODES
0	0	0	No test mode
0	0	1	Analog loop back via Z-filter (H (Z) = 1)[1]
0	1	0	Disable highpass filter (part of bandpass BP)
0	1	1	Cut off receive path
1	0	0	Initialize data ram
1	1	0	Digital loop back via B-filter (H (B) = 1)[2]
1	1	1	Digital loop back via PCM-register[3]

[1] Output of the interpolation filter 1 I1 is set to 0.
Value of transfer function of the Z-filter is 1 (not programmable).

[2] Output of the low pass decimation filter 2 D2 is set to 0.
Value of transfer function of the B-filter is 1 (not programmable).

[3] PCM in = PCM out. This testmode is also available in standby mode.

CR2 Configuration Register 2

BIT	7	6	5	4	3	2	1	0
	D	C	B	A	EL	AM	µ/A	PCS

The first four bits D...A in this register, program the four bidirectional signaling pins SD...SA. With two SICOFIs on one SLD port only pin SD can be used, pin SA is always input in this case and indicates the address of the SICOFI.

SA = 0 : A-SICOFI, SA = 1 : B-SICOFI **(see also bit AD in SOP-command).**

D	Signaling Pin SD	D = 0	SD is output
		D = 1	SD is input
C	Signaling Pin SC	C = 0	SC is output
		C = 1	SC is input
B	Signaling Pin SB	B = 0	SB is output
		B = 1	SB is input
A	Signaling Pin SA	A = 0	SA is output
		A = 1	SA is input
EL	Signaling Expansion Logic	EL = 0	No expansion logic
		EL = 1	Expansion logic provided

signaling expansion logic is only possible with one SICOFI on port
(see also Signaling Byte)

AM	Address Mode	AM = 0	Two SICOFIs on SLD port
		AM = 1	One SICOFI on SLD port

The SICOFI access to the SLD-Bus voice channel is controlled by AM and TR.

		Receive (SLD-Bus→SICOFI)		**Transmit (SICOFI→SLD-Bus)**	
AM	TR	SICOFI A	SICOFI B	SICOFI A	SICOFI B
0	0	channel A	channel B	channel A	channel B
0	1	channel B	channel A	channel B	channel A
1	0	channel A	–	channel A, B[1)]	–
1	1	channel A + B[2)]	–	channel A, B[1)]	–

µ/A	PCM-Law	µ/A = 0	A-Law
		µ/A = 1	µ-Law (µ255 PCM)
PCS	Programmed B-Filter Coefficient		
		PCS = 0	Programmed coefficients
		PCS = 1	Fixed coefficients

1) The SICOFI transmits the same byte in channel A and B.
2) Three Party Conference.

CR3 Configuration Register 3

BIT	7	6	5	4	3	2	1	0
	AGX		AGR		PU	TR	LIO	

AGX	Analog Gain Control Transmit-Path	
	AGX = 0 0	0 dB
	AGX = 0 1	6 dB amplification
	AGX = 1 0	12 dB amplification
	AGX = 1 1	14 dB amplification

AGR	Analog Gain Control Receive-Path	
	AGR = 0 0	0 dB
	AGR = 0 1	6 dB attenuation
	AGR = 1 0	12 dB attenuation
	AGR = 1 1	14 dB attenuation

PU	Power Up/Power Down[1]	
	PU = 0	Power Down (standby)
	PU = 1	Power Up (operating)

TR Three Party Conference/Reverse Operating Mode **(see CR2)**[1]

LIO	Linear Operating Mode **(see serial interface)**	
	LIO = 0 0	PCM mode
	LIO = 0 1	Linear mode 1[2]
	LIO = 1 0	Linear mode 2

(Change of linear mode becomes valid in the next DIR-cycle).

[1] The bits PU and TR may also be overwritten by a SOP command with LSEL = 0 1 (PU and TR are part of the SOP command). With LSEL = 0 1, the bits PU and TR in the SOP command are ignored.

[2] Subsequent to a SOP/COP-read command the control and signaling information is transmitted instead of linear voice.

CR4 Configuration Register 4

BIT	7	6	5	4	3	2	1	0
		TM3		0	0		TM4	

TM3	TEST MODES
0 0 0	No test mode
0 0 1	Additional + 6 dB digital gain in transmit direction (GX)
0 1 1	Additional + 12 dB digital gain in transmit direction (GX)
1 0 0	Enable on chip sine wave generation[1]
1 1 0	Far analog loop back[2]

TM4	TEST MODES
0 0 0	No test mode
1 0 0	Digital loop back via analog port ($V_{IN} = V_{OUT}$)

COP Command

With a COP command coefficients for the programmable filters can be written to the SICOFI coefficient ram or transmitted on the SLD-bus for verification.

BIT	7	6	5	4	3	2	1	0
	AD	R/W			CODE			

AD Address Information AD = 0 A-SICOFI addressed
AD = 1 B-SICOFI addressed

This bit is evaluated with two SICOFIs on one SLD-port only.
With two SICOFIs on port, a SICOFI is identified, if AD is consistent with the level at pin SA **(see Signaling Byte, Programming Procedure).**

R/W Read/Write Information R/W = 0 Write to SICOFI
R/W = 1 Read from SICOFI

This bit indicates whether filter coefficients are written to the SICOFI or read from the SICOFI.

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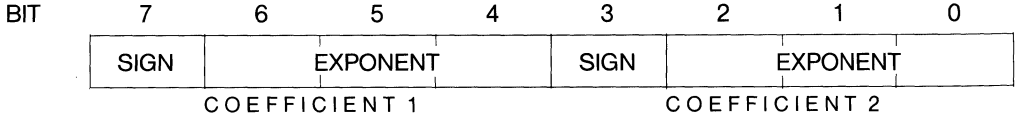
1) With the R-Filter disabled a 2 kHz, 0 dBm0 sine wave signal is fed to the input of the receive Lowpass Filter LP (other frequencies see Appendix B).
2) The output of the X-Filter is fed to the input of the R-Filter (8 kHz, 16 bit linear).

CODE

0	0	0	0	1	1	B-Filter coefficients part 1	(followed by 8 bytes of data)
0	0	1	0	1	1	B-Filter coefficients part 2	(followed by 8 bytes of data)
0	1	0	0	1	1	Z-Filter coefficients	(followed by 8 bytes of data)
0	1	1	0	0	0	B-Filter delay coefficients	(followed by 4 bytes of data)
1	0	0	0	1	1	X-Filter coefficients	(followed by 8 bytes of data)
1	0	1	0	1	1	R-Filter coefficients	(followed by 8 bytes of data)
1	1	0	0	0	0	GX- and GR-Filter coefficients	(followed by 4 bytes of data)

Other codes are reserved for future use.

Data Byte Format



Each four bit coefficient represents a factor of **SIGN x 2**$^{\text{-EXPONENT}}$

Subsequent to reading the filter coefficients form the SICOFI CR2 and CR1 are transmitted additionally!!

Signaling Byte

The signaling interface of the SICOFI consists of 10 pins.

3 transmit signaling inputs: SI1, SI2 and SI3
3 receive signaling outputs: SO1, SO2 and SO3
4 bidirectional programmable signaling pins: SA, SB, SC and SD

Data present at SI1..SI3 and possibly at some or all of SA..SD (if programmed as inputs) are sampled and transfered serially on SIP onto the SLD-bus. Data received serially on SIP from the SLD-Bus are latched and fed to SO1..SO3 and possibly to some of SA..SD if programmed as output.

The signaling field format is generally:

In Receive Direction:

BIT	7	6	5	4	3	2	1	0
	SO1	SO2	SO3	SD	SC	SB	SA	SEL

In Transmit Direction:

BIT	7	6	5	4	3	2	1	0
	SI1	SI2	SI3	SD	SC	SB	SA	SEL

where SEL is the signaling expansion bit if EL = 1 in CR2.

For the different cases possible, the signaling byte format at SIP is

	Receive Signaling Byte								**Transmit Signaling Byte**							
Bit / Case	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	SC	SB	SA	0
2	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	SC	SB	SA	Z
3	SO1	SO2	SO3	SD	SC	SB	SA	X	SI1	SI2	SI3	0	0	0	0	0
4	SO1	SO2	SO3	SD	SC	SB	SA	X	SI1	SI2	SI3	Z	Z	Z	Z	Z
5 A-SIC	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	Z	Z	Z	Z
B-SIC	X	X	X	X	SO1	SO2	SO3	X	Z	Z	Z	Z	SI1	SI2	SI3	SD
6 A-SIC	SO1	SO2	SO3	SD	X	X	X	X	SI1	SI2	SI3	0	Z	Z	Z	Z
B-SIC	X	X	X	X	SO1	SO2	SO3	SD	Z	Z	Z	Z	SI1	SI2	SI3	0

Z...high impedance, X...don't care

Signaling Byte

Cases

1 One SICOFI is connected to one SLD port, EL = 0 (no signaling expansion logic provided); SA..SD are programmed as transmit signaling inputs.

2 One SICOFI connected to one SLD port, EL = 1 (signaling expansion logic provided); SA..SD are programmed as transmit signaling inputs.

3 One SICOFI is connected to one SLD port; EL = 0 (no signaling expansion logic provided); SA..SD are programmed as receive signaling outputs.

4 One SICOFI is connected to one SLD port; EL = 1 (signaling expansion logic provided); SA..SD are programmed as receive signaling outputs.

If a signaling expansion logic is provided (see case 2 and 4), the signaling bits SA..SD which are programmed as signaling inputs or outputs can be used as additional expansion bits in receive or transmit direction, respectively. As far as SICOFI is concerned, SIP is in a high-impedance (Z) state or "don't care" (Y) state while these bits are transfered.

5 Two SICOFIs are connected to one SLD port; SD is programmed as transmit signaling input.

6 Two SICOFIs are connected to one SLD port; SD is programmed as receive signaling output.

If two SICOFIs are connected to one SLD port, no signaling expansion logic is possible. SA is programmed as input automatically, and defines the addressed SICOFI:

SA = 0 : A-SICOFI
SA = 1 : B-SICOFI.

SB and SC are not usable with two SICOFIs on one SLD port.

Programming Procedure

The following table shows some control byte sequences. If the SICOFI has to be configured completly during initialization, up to 60 bytes will be transfered.

DIR	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive

No Operation

	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP

SOP Write

LSEL = 00	SOP	NOP									
LSEL = 11	SOP	NOP	CR1	NOP							
LSEL = 10	SOP	NOP	CR2	NOP	CR1	NOP					
LSEL = 01	SOP	NOP	CR4	NOP	CR3	NOP	CR2	NOP	CR1	NOP	

SOP Read

LSEL = 00	SOP	NOP									
LSEL = 11	SOP	CR1									
LSEL = 10	SOP	CR2	X	CR1							
LSEL = 01	SOP	CR4	X	CR3	X	CR2	X	CR1			

COP Write

4 Bytes	COP	NOP	DB4	NOP	DB3	NOP	DB2	NOP	DB1	NOP
8 Bytes	COP	NOP	DB8	NOP	DB7			NOP	DB1	NOP

COP Read

4 Bytes	COP	DB4	X	DB3		DB1	X	CR2	X	CR1
8 Bytes	COP	DB8	X	DB7		DB1	X	CR2	X	CR1

X .... don't care

DB1, DB2...DB8...coefficient Data Byte 1..8

Operating Modes

Basic Setting

Upon initial application of V_{DD} or reseting pin RS to "1" while operating, the SICOFI enters a basic setting mode. Basic setting means, that the SICOFI configuration registers CR1...CR4 are initialized. All CR1 bits are set to "0" (all programmable filters are disabled except the B-Filter where fixed coefficients are used, no test mode); CR2 is set to "1" (SA...SD are inputs, signaling expansion logic is provided, one SICOFI on SLD-port, μ-law chosen and fixed B-Filter coefficients used). All CR3 and CR4 bits are reset to "0" (no additional amplification or attenuation, no linear mode, power down, no test mode). Receive signaling registers are cleared. SIP is in high-impedance state, the analog output V_{OUT} and the receive signaling outputs SO1...SO3 are forced to ground.

The serial interface is active to receive commands starting with the next 8-kHz SLD-bus frame. The serial interface port SIP remains tristate until CR2 has been defined.

If two SICOFIs are connected to one SLD port, both SICOFIs get the same SOP and CR2 information during initialization. The subsequent CR1 byte is assigned to the addressed SICOFI only. If the two SICOFIs need different CR2 information, the SOP-CR2 sequence has to be provided once again (each SICOFI knows its address now).

Standby Mode

Upon reception of a SOP command to load CR2 from the basic setting, the SICOFI enters the standby mode (basic setting replaced by individual CR2). Being in the operating mode, the SICOFI is reset to standby mode with a Power-Up bit PU = 0 (in CR3 or in the SOP-command directly). The serial interface is active to receive and transmit new commands and data.

Operating Mode

From the standby mode, the operating mode is entered upon recognition of a Power-Up bit PU = 1 (in CR3 or in the SOP-command directly).

Gain Adjustment

The transmit gain values are digitally programmable in the range of 0 to 8 dB in steps of ≤ 0.25 dB.

The receive gain values are digitally programmable in the range of 0 to −8 dB in steps of ≤ 0.25 dB.

Transmission Characteristics – Preliminary

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing: B; line termination: Z; frequency-response correction: X, R) needs a complete knowledge of the SICOFI®'s analog environment. Unless otherwise stated, the programmable filters have the following transfer functions:

$H(Z) = H(B) = 0$; $H(X) = H(R) = 1$; $H(Gx) = 0$ dB to 8 dB
$H(GR) = 0$ dB to -8 dB; $H(AGX) = 0$ dB to 14 dB; $H(AGR) = 0$ dB to -6 dB;

A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms.
A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V. (A-law,[μ-law]).

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain (either value) Gain absolute $R_L > 1$ kΩ 1000 Hz at 0dBm0 300 Ω $< R_L <$ 1 kΩ	G	-0.2 -0.3	± 0 -0.05	0.2 0.20	dB
Gain variation with supply voltage and temperature 1000 Hz at 0dBm0	G_V	-0.2	0	0.2	dB
Total harmonic distortion[1]	THD			-44	dB
Intermodulation $2f_1-f_2$ [2] $2f_1-f_2$ [3]	IMD			-42 -56	dB
Crosstalk Transmit to receive 0dBm0 $f = 300$ Hz to 3400 Hz Receive to transmit 0dBm0 $f = 300$ Hz to 3400 Hz	CT_{XR} CT_{XR}			-70 -70	dB dB
Idle channel noise psophometric weighted Transmit, VIN = 0 V Receive, idle code +0	N_{RP} N_{RP}			-67 -78	dBm0p dBm0p

[1]) Single-frequency components between 300 Hz and 3400 Hz produced by a 0 dBm0 sine wave in the range between 300 Hz and 3400 Hz.
[2]) Equal input levels in the range between -4 dBm0 and -21 dBm0; different frequencies in the range between 300 Hz and 3400 Hz.
[3]) Input level -9 dBm0, frequency range 300 Hz to 3400 Hz and -23 dBm0, 50 Hz.

Attenuation Distortion

Attenuation deviations stay within the limits in the figures below.

Figure 3

Receive: Reference frequency 1 kHz, input signal level 0 dBm0

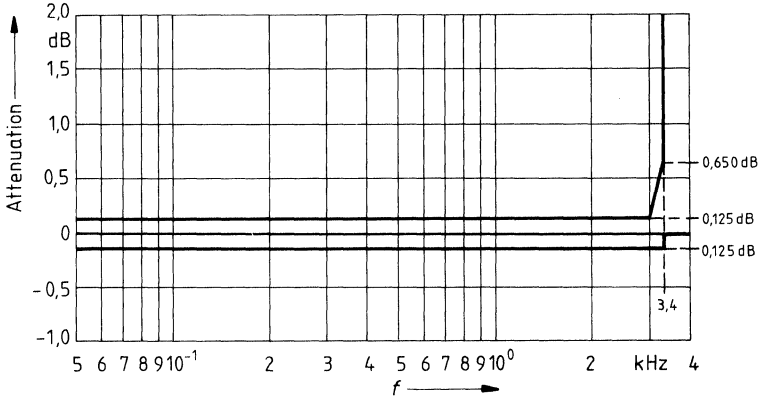
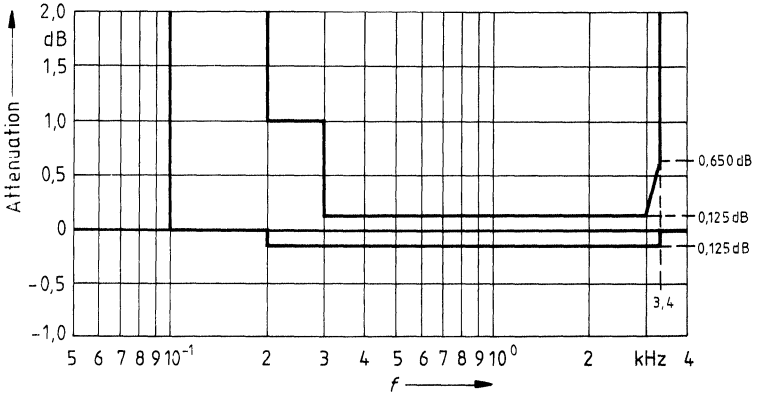


Figure 4

Transmit: Reference frequency 1 kHz, input signal level 0 dBm0



Group Delay

Maximum delays for operating the SICOFI with H(B) = H(Z) = 0 and H(R) = H(X) = 1, including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

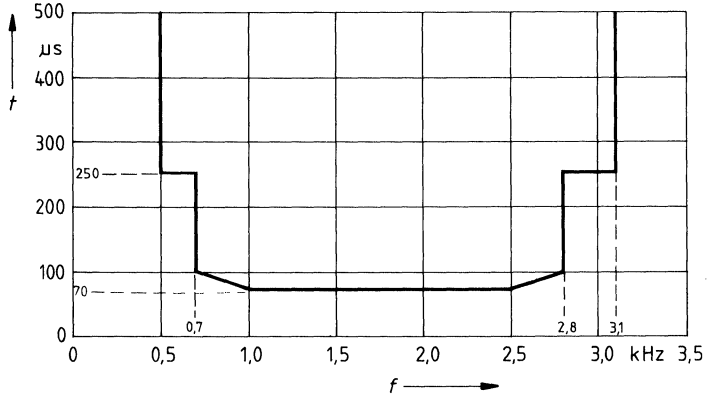
Group delay deviations stay within the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Transmit Delay $f = 1.4$ kHz	D_{XA}			300	µs
Receive Delay $f = 300$ Hz	D_{RA}			240	µs

Figure 5

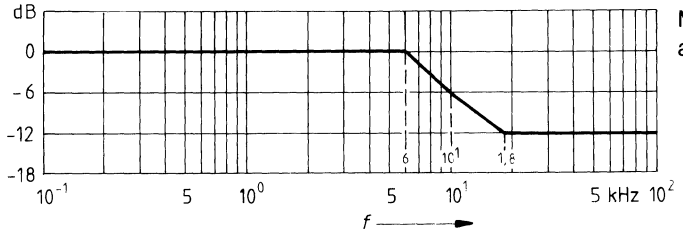
Group Delay Distortion: Input signal level 0 dBm0



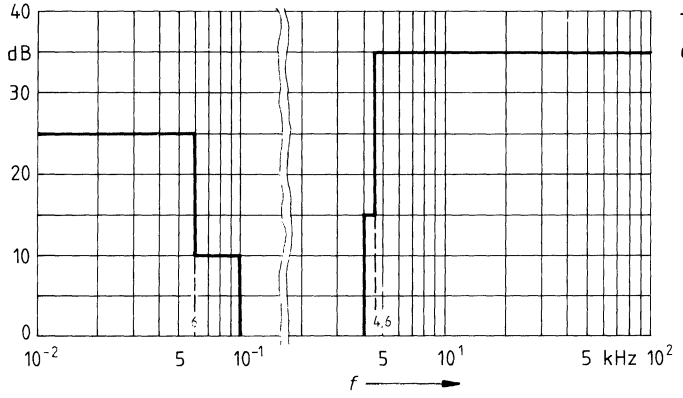
Out-of-Band Signals at Analog Input

With an out-of-band sine wave signal with frequency *f* and level A applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below level A.

Figure 6



Maximum input level A at analog input

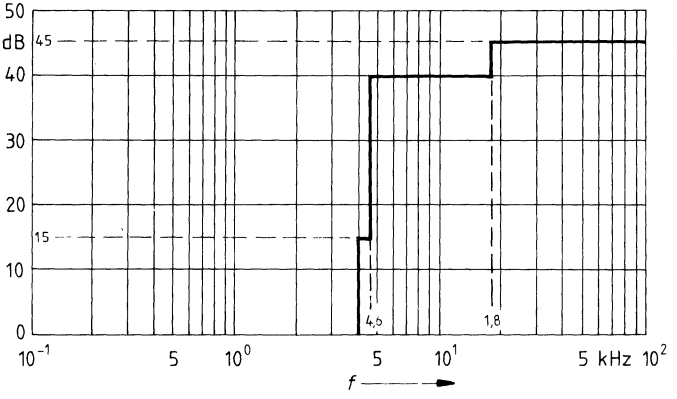


Transmit out-of-band discrimination X

Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave of frequency *f* applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

Figure 7



Receive out-of-band discrimination X

Gain Tracking (receive and transmit)

The gain deviations stay within the limits in the figures below.

Figure 8

Gain Tracking: Measured with noise signal according to CCITT recommendations
Reference level is −10 dBm0

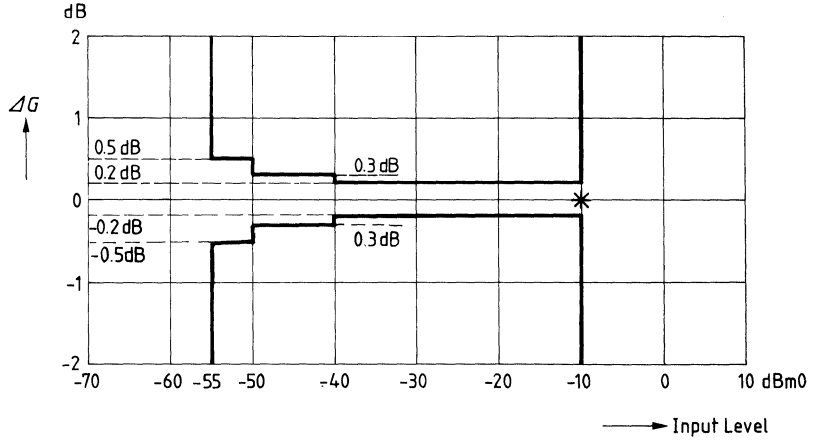
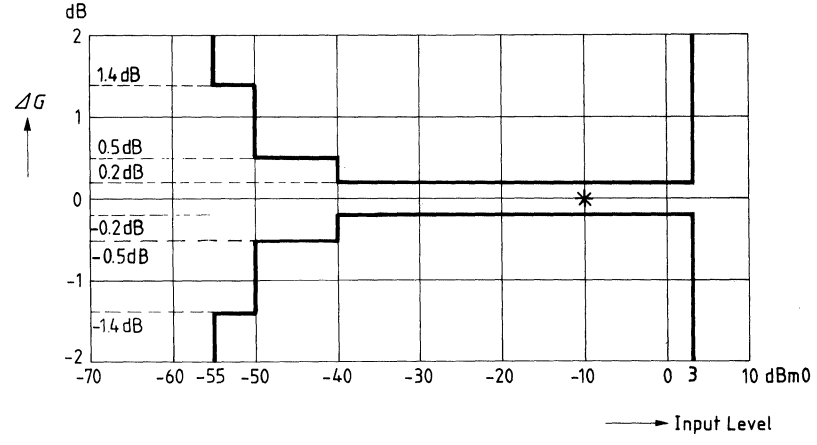


Figure 9

Gain Tracking: Measured with sine wave in the range 700 to 1100 Hz
Reference level is −10 dBm0



Total Distortion (The signal-to-distortion ratio exceeds the limits in the following figures).

Figure 10

Receive: Measured with noise signal according to CCITT recommendations

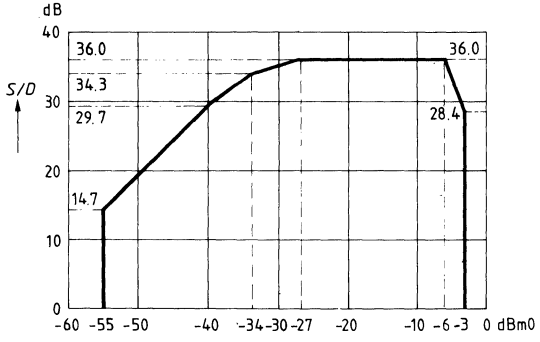


Figure 11

Transmit: Measured with noise signal according to CCITT recommendations

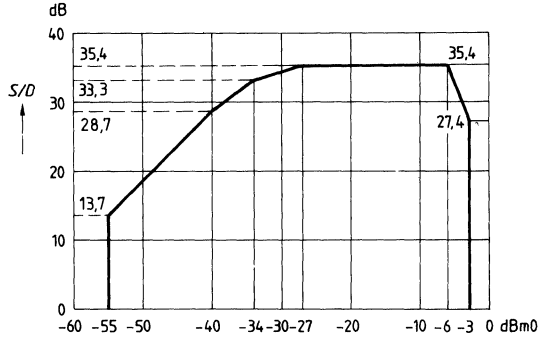
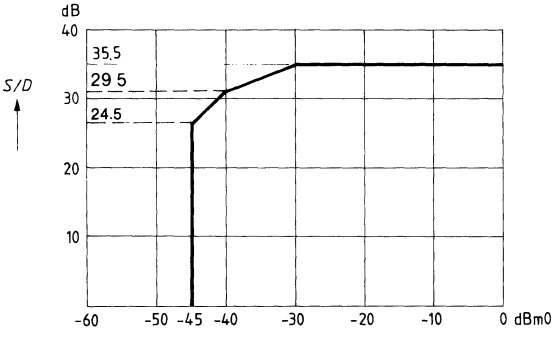


Figure 12

Receive & Transmit: Measured with sine wave in the range 700 to 1100 Hz excluding submultiples of 8 kHz



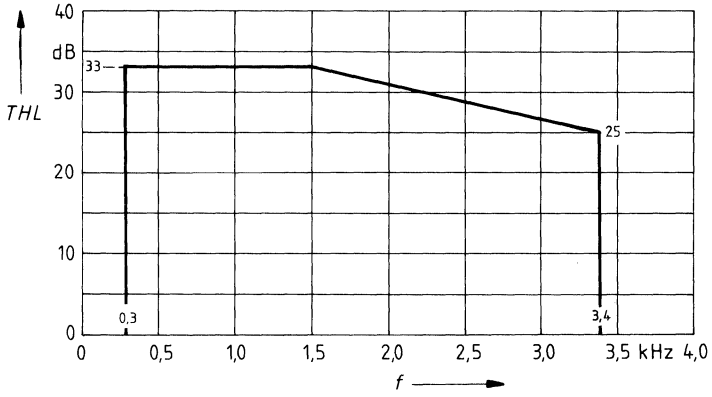
Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay-deviations inherent to the SICOFI A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP's etc.).

The SICOFI transhybrid-loss is measured the following way: A sine wave signal with level A and a frequency in the range of 300-3400 Hz is applied to the digital input. The resulting analog output signal at pin V_{OUT} is directly connected to V_{IN}, e.g. with the SICOFI testmode "Digital Loop Back via Analog Port" **(see CR4).** The programmable filters R, Gr, X, Gx and Z are disabled, the balancing filter B is enabled with coefficients optimized for this configuration ($V_{OUT} = V_{IN}$).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the following figure.

Figure 13



Note:

B-filter coefficients recommended for transhybrid loss measurement ($V_{OUT} = V_{IN}$)
B-filter part 1 (03) = DE, 12, 2B, 23, 15, 21, 31, D1
B-filter part 2 (03) = 00, 14, 4E, 5B, AC, DB, 1B, A3
B-filter delay (18) = 19, 19, 11, 19

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
V_{DD} referred to GNDD		−0.3	5.5	V
V_{SS} referred to GNDD		−5.5	0.3	V
GNDA to GNDD		−0.3	0.3	V
Analog input and output voltage				
referred to $V_{DD} = 5$ V; $V_{SS} = -5$ V	V_{IN}	−10.3	0.3	V
referred to $V_{SS} = -5$ V; $V_{DD} = 5$ V	V_{IN}	−0.3	10.3	V
All digital input voltages				
referred to GNDD = 0 V; $V_{DD} = 5$ V	V_{IN}	−0.3	5.3	V
referred to $V_{DD} = 5$ V; GNDD = 0 V	V_{IN}	−5.3	0.3	V
Power dissipation	P_D		1	W
Storage temperature	T_{stg}	−60	125	°C
Ambient temperature under bias	T_A	−10	80	°C

Operating Range

$T_A = 0$ to 70 °C; $V_{DD} = 5$ V ± 5%; $V_{SS} = -5$ V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
V_{DD} supply current	I_{DD}					
standby			2.1	4	mA	± 5% supply
operating			8	12	mA	± 5% supply
V_{SS} supply current	I_{SS}					
standby			1.7	3	mA	± 5% supply
operating			5	8	mA	± 5% supply
Power supply rejection (of either supply/direction)	*PSRR*	35			dB	1 kHz 80 mV_{rms} ripple
Power dissipation standby	P_{Ds}		20	37	mW	± 5% supply
Power dissipation operating	P_{Do}		70	105	mW	± 5% supply

Digital Interface

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = -5\ V \pm 5\%$; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
L-input voltage	V_{IL}	−0.3	0.8	V
H-input voltage	V_{IH}	2.0	V_{DD} +0.3	V
L-output voltage $I_O = -2$ mA	V_{OL}		0.45	V
H-output voltage $I_O = 400\ \mu A$		2.4		V
Input leakage current $-0.3 \le V_{IN} \le V_{DD}$	I_{IL}		±1	µA

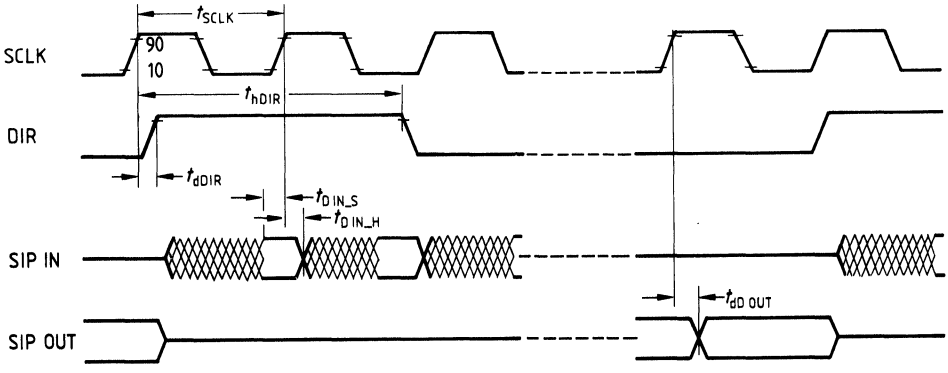
Analog Interface

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = -5\ V \pm 5\%$; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Analog input resistance	R_I	10		MΩ
Analog output resistance	R_O		10	Ω
Input offset voltage	V_{IO}		±50	mV
Output offset voltage	V_{OO}		±50	mV
Input voltage range	V_{IR}		±3.2	V
Output voltage range $R_L \ge 300\ \Omega$; $C_L \le 10$ pF	V_{OR}	±3.1		V

SIP Interface Timing (SLD-Bus)

Figure 14

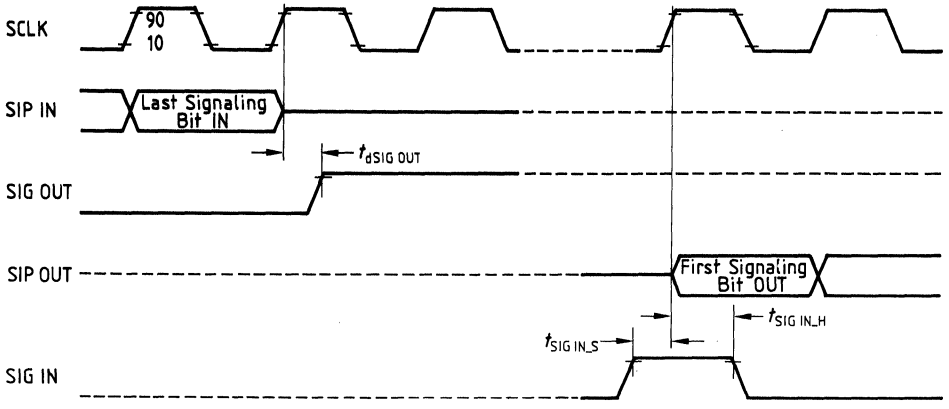


Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period SCLK	t_{SCLK}	−10%	1/512 kHz	+10%	
Duty Cycle		10		90	%
Period DIR	t_{DIR}		125		µs
DIR delay time	t_{dDIR}	−20		80	ns
DIR high time	t_{hDIR}	500			ns
SIP data in setup time	$t_{DIN\ S}$	50			ns
SIP data in hold time	$t_{DIN\ H}$	20			ns
SIP data out delay	t_{dDOUT}			200	ns
SIP data out tristate delay vs. SCLK				50	ns
RS high time		250			ns

Signaling Interface Timing

Figure 15



Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Delay signaling out vs. SCLK[1])	$t_{dSIGout}$			200	ns
SIG in setup time[2])	$t_{SIGin\ S}$	50			ns
SIG in hold time[2])	$t_{SIGin\ H}$	100			ns

[1]) Pins SO1..SO3; Pins SA..SD as output
[2]) Pins SI1..SI3; Pins SA..SD as input

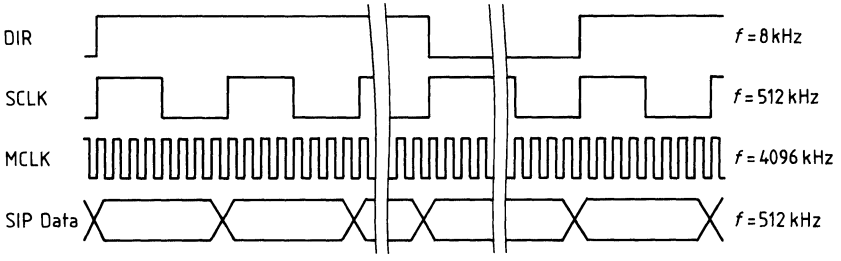
Appendix A

The SICOFI can be used with three different SLD-bus type interfaces.
A specific interface type is selected with three pins: TEST, SI3 and PLL.

Figure 16

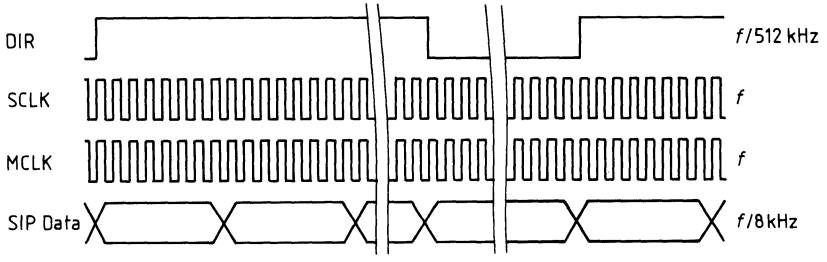
1) SLD-bus Interface[1)]

TEST	SI3	PLL
0	X	X



2) SLD-bus Interface with Variable Clock-frequencies[2)]

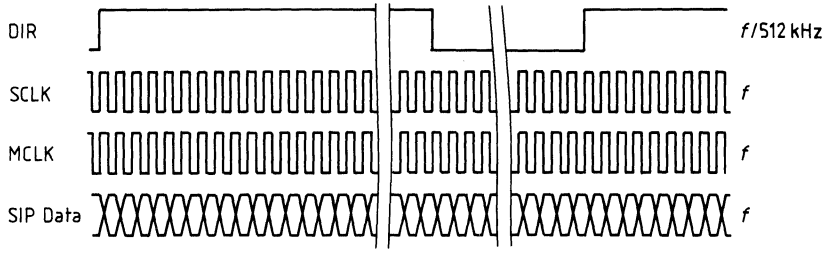
TEST	SI3*	PLL
1	0	0



3) Burst Mode Interface[2)]

TEST	SI3*	PLL
1	0	1

*) SI3 cannot be used as Signalling pin

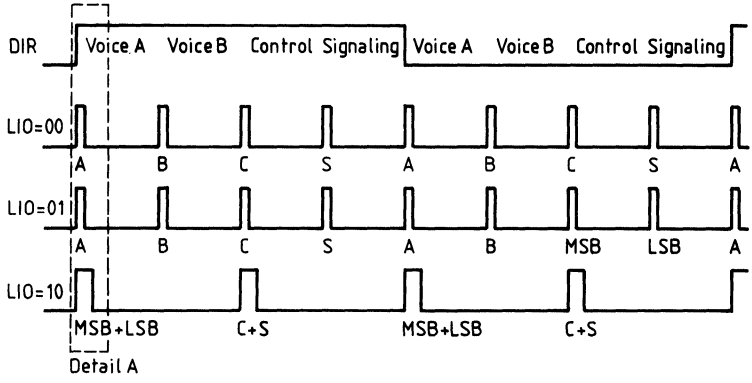


1) 4096-kHz Masterclock MCLK is generated from 512-kHz SCLK by on chip PLL
2) Maximum MCLK-frequency = 8 MHz

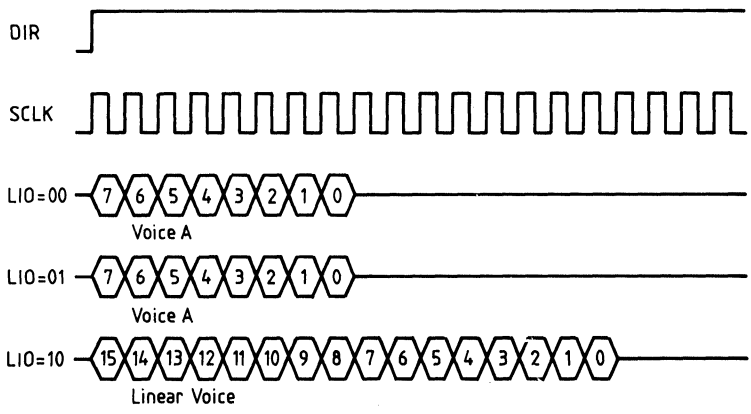
Appendix A (cont'd)

In burst-mode 8- or 16-bit bursts are received or transmitted, depending on the linear mode selected (**see** field LIO in **CR3**).

Figure 17



Detail A



A... voice A C...control
B... voice B S...signaling
MSB... bit 15 – 18 of linear in- or output
LSB... bit 7 – 0 of linear in- or output

Appendix B

On Chip Sine-Wave Generation

By setting field TM3 in CR4 to '100' the on-chip sine-wave generator is activated with a fixed frequency of 2 kHz. The frequency f_{SIN} may be programmed via the R-filter coefficients (R-filter enabled) in the range of 0..4 kHz. The gain may be adjusted with the programmable GR-filter.

The trapezoidal sine-wave generation algorithm used, provides for a harmonic distortion better than 27 dB.

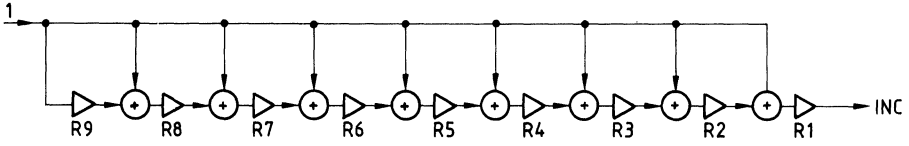
Calculation of the R-filter Coefficients:

f_{SIN}: $= 8192 * INC/f_{MCLK}$ with f_{MCLK}, f_{SIN} [kHz]

$INC := S_{R1} * 2^{-EXP_{R1}} * (1 + S_{R2} * 2^{-EXP_{R2}} * (1 + S_{R3} * 2^{-EXP_{R3}} * (..(.. (1 + S_{R9} * 2^{-EXP_{R9}})..))$

S...SIGN, EXP...EXPONENT

Figure 18



$A_1 = INC$

FOR i: = 1 TO 9 DO

FIND S_i, EXP_i : FOR $(|A_i - S_i * 2^{-EXPi}|) = MIN$; $S_i \epsilon (-1,1)$, $EXP_i \epsilon (0...7)$

$A_{i+1} := (A_i/S_i * 2^{-EXPi}) - 1$

$R_i := [(-S_i + 1)/2), BIN(EXP_i)]$ (to be transfered to the SICOFI)

NEXT i

Programming Byte Sequence for Selected Frequencies

Frequency	2000	1000	800	697	700	852	941	1209	1336	1477	1633
COP write	AB	AB	AB	AB	AB	AB	AB	AB	AB	AB	AB
X	00	00	00	00	00	00	00	00	00	00	00
X X	00	00	00	00	00	00	00	00	00	00	00
X X	00	00	00	00	00	00	00	00	00	00	00
R_1 X	00	10	10	20	10	10	10	10	10	10	00
R_3 R_2	8F	8F	AA	A1	CA	3B	CC	B2	22	D1	1B
R_5 R_4	8F	8F	AA	2B	32	C1	BB	22	A1	C1	5C
R_7 R_6	8F	8F	AA	4B	2D	BB	12	5F	5F	BB	CA
R_9 R_8	8F	8F	AA	B1	B3	12	DA	8F	1B	12	13

X... don't care