SIEMENS

Extended PCM Interface Controller (EPIC-1) PEB 2055

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2055-C	Q67100-H6034	C-DIP-40
PEB 2055-N	Q67100-H6035	PL-CC-44 (SMD)
PEB 2055-P	Q67100-H6036	P-DIP-40

Information from subscriber lines needs to be transferred to time slots on system internal PCM communication highways. The EPIC™ concentrates the circuitry necessary to do this interfacing for a large number of transmission lines on a single IC. Therefore, it is not necessary to repeat this PCM interface circuitry for every line. Since the system cost of the EPIC is divided by the number of lines it controls, powerful and comfortable functions can be economically performed.

The basic functions of the EPIC were defined by the system houses of ALCATEL, Siemens Plessey and ITALTEL as part of their ISDN cooperation.

Features

- PCM interface controller for up to 32 ISDN or 64 analog subscribers
- Time-slot assignment freely programmable for all subscribers
- Non-blocking switch for 128 channels
- Switching of 16-, 32-, 64-kbit/s channels (128-kbit/s via two consecutive 64-kbit/s channels)
- Two serial interfaces: PCM and configurable (IOM®-1, IOM®-2, SLD, PCM)
- Interfacing with four full-duplex PCM highways (2, 4 or 8 Mbit/s)
- Data rates of PCM and configurable interfaces independent of each other
- Change detection ("last-look") logic for C/I or feature control channels
- 16-byte FIFO for monitor or signaling channels
- Standard µP interface with multiplexed (P-DIP-40) or demultiplexed (PL-CC-40) address/data bus
- Advanced low power CMOS technology

General

Up Stream Direction from the subscriber to the PCM highways in the exchange.

Down Stream Direction from the PCM highways to the subscribers.

Time Slot Defined period of time the PCM, IOM or SLD frame consisting of 8 bits. Time slots are allocated to the frames in such away that the time slot boundaries coincide with the frame boundaries. The time slots do not overlap. The lowest time-slot number is 0. This time slot is the first in the frame.

Sub Time Slot A quarter or half a time slot. These are allocated to the time slots in such a way that time slot and subtime slot boundaries match. The subtime slots are non overlapping.

Channel Sequence of bits which is exchanged between the subsriber, the exchange equipment and/or the microprocessor. It occupies a definied number of bits at a definied position within a frame as long as a connection pervails. Both time slots and subtime slots are channels and hence a channel may offer a bandwidth of 16, 32 or 64 kbit/s.

Bit Numbering The bits in a slot are numbered 7 (MSB) through 0 (LSB). Bit 7 is the first bit to be transmitted or received, bit 0 the last.

General Device Overview

The Extended PCM Interface Controller EPIC (PEB 2055) is a monolithic switching device for the path control of up to 128 channels of 16, 32 or 64 kbit/s bandwidth. Two consecutive 64 kbit/s channels may also be handled as a quasi single 128 kbit/s channel. For these channels the EPIC performs nonblocking space time switching between two serial interfaces, the system and the configurable interface.

Both interfaces can be programmed to operate data rates between 8 and 8192 kbit/s. The system interface consists of up to four duplex ports with a tristate indication signal for each output line. The configurable interface can be selected to incorporate either four duplex or eight bidirectional I/O ports (SLD).

The EPIC can therefore be programmed to communicate either with SLD or with IOM (ISDN Oriented Modular) compatible devices. In both cases the device handles the layer-1 functions buffering the C/I and monitor channels for IOM compatible devices and the feature control and signaling channels for SLD compatible devices.

Due to its capability to switch channels of different bandwidths, the EPIC can handle up to 32 ISDN subscribers with their 2B+D channel structure in IOM configuration or up to 16 subscribers in SLD configuration. Since its interfaces can operate at different data rates, the EPIC is an ideal device for data rate adaption.

Moreover, the EPIC is one of the fundamental building blocks for networking with either central, decentral or mixed signaling and packet data handling architectures. The other key devices are the IDEC™ (ISDN D-channel Exchange Controller, PEB 2075) and the HSCX (High-Level Serial Communication Controller Enhanced, SAB 82525).

Applications of the EPIC include communication multiplexers, concentrators, central switches as well as peripheral ISDN and analog line cards.

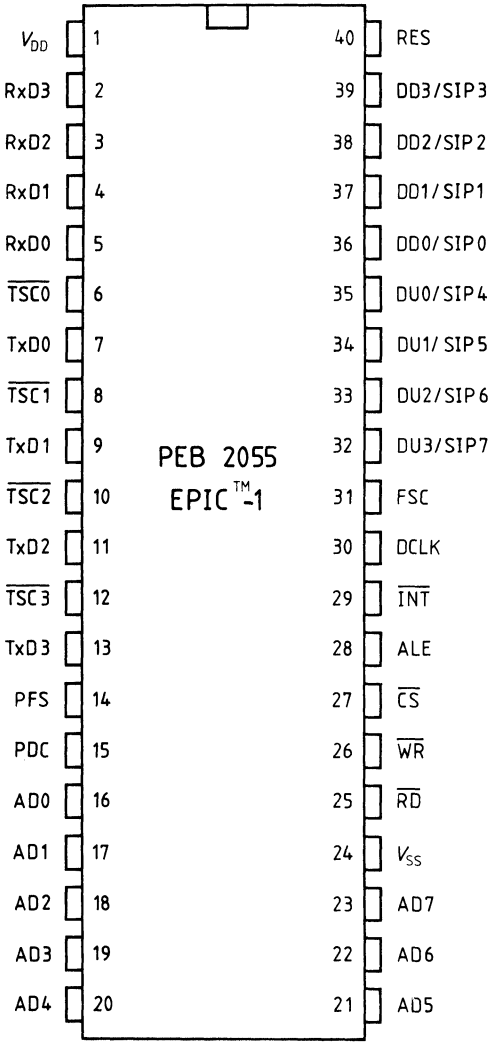
The EPIC is available in a P-DIP-/C-DIP 40 or a PL-CC-44 package.

The P-DIP/C-DIP-40 version is controlled by a standard 8-bit-parallel microprocessor interface with a multiplexed address-data bus. In the PL-CC-44 package the device may optionally be controlled by separate address and data buses.

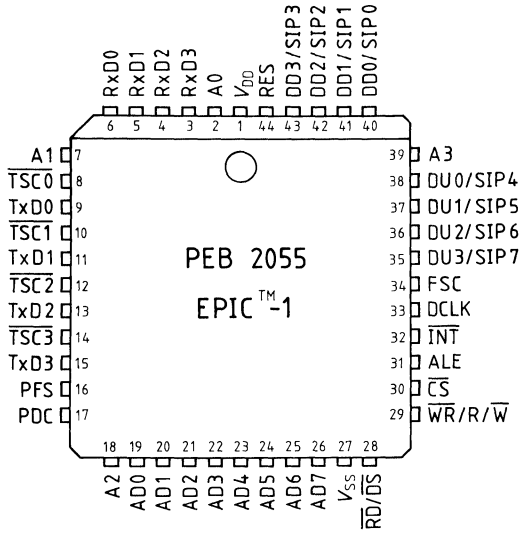
The PEB 2056 EPIC-2 is a smaller version of the EPIC-1. The EPIC-2 has been optimized for digital line cards with up to eight subscriber lines. In contrast to the EPIC-1, the EPIC-2 has only one IOM interface, only two PCM highway connections and comes in P-DIP-28 or PL-CC-44 packages.

Pin Configuration
(top view)

P-DIP-40



PL-CC-44



Pin Defintions and Functions

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O) In/Output (IO) Open Drain (OD)	Function
1	1	V_{DD}		Supply Voltage 5 V ± 5%
	2	A0	I	**Address Bus Bit 0:** This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provides in the PL-CC package and only active if a demultiplexed µP interface mode is selected.
2 3 4 5	3 4 5 6	RxD3 RxD2 RxD1 RxD0	I	**Receive PCm Interface Data:** Serial data is received at these lines at standard TTL or CMOS levels.
	5	A1	I	**Address Bus Bit 1:** This input interfaces to the system's address but to select an internal register for a read or write access. This pin is only provides in the PL-CC package and only active if a demultiplexed µP interface mode is selected.
6 8 10 12	8 10 12 14	$\overline{TSC0}$ $\overline{TSC1}$ $\overline{TSC2}$ $\overline{TSC3}$	O	Tristate control for the PCM interface. These lines are low when the corresponding TxD outputs are valid.
7 9 11 13	9 11 13 15	TxD0 TxD1 TxD2 TxD3	O	**Transmit PCM Interface Data:** Serial data is sent by these lines at standard TTL or CMOS levels. These pins can be tristated.
14	16	PFS	I	PCM interface frame synchronization pulse.
15	17	PDC	I	PCM interface data clock, signle or double rate.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O) In/Output (IO) Open Drain (OD)	Function
–	18	A2	I	**Address Bus Bit 2:** This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provides in the PL-CC package and only active if a demultiplexed µP interface mode is selected.
16 17 18 19 20 21 22 23	19 20 21 22 23 24 25 26	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O	**Address Data Bus.** If the multiplexed address/data µP interface bus mode is selected these pins transfer data and commands between the µP and the EPIC. If a demultiplexed mode is used, these bits interface with the system data bus.
24	27	V_{SS}	I	**Ground:** 0 V
25	28	$\overline{RD}$	I	**Read:** The signal indicates a read operation, active low.
26	29	$\overline{WR}$	I	**Write:** This signal indicates a write operation, active low.
27	30	$\overline{CS}$	I	**Chip Select.** A low on this line selects the EPIC for a read/write operation.
28	31	ALE	I	**Address Latch Enable.** In the Intel type multiplexed µP interface mode a logical high on this line indicates an address of an EPIC internal register on the external address/data bus. In the Intel type multiplexed µP interface mode this line is fixed to logical 0, in the demultiplexed Motorola type µP interface mode it should connected to 5 V.
29	32	$\overline{INT}$	OD	Interrupt line, active low
30	33	DCLK	IO	Data Clock input or output in IOM/slave clock in SLD configuration.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol Output (O)	Input (I) In/Output (IO) Open Drain (OD)	Function
31	34	FSC	IO	Frame Synchronization input or output in IOM configuration / Direction indication signal in SLD configuration.
32 33 34	35 36 37	DU3/SIP7 DU2/SIP6 DU1/SIP5	O/IO	Data Upstream outputs in IOM configuration. Serial interface port 4, 5, 6 and 7 in bidirection configuration.
–	39	A3	I	**Address Bus Bit 3:** This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provides in the PL-CC package and only active if a demultiplexed µP interface mode is selected.
36 37 38 39	40 41 42 43	DD0/SIP0 DD1/SIP1 DD2/SIP2 DD3/SIP3	I/IO	Data Downstream inputs in IOM configuration. Serial interface ports 0, 1, 2 and 3 in bidirectional configuration.
40	44	RES	I	**Reset.** A logical high on this input forces the EPIC into the reset state.

Logic Symbol

Figure 1
Functional Symbol for the Duplex Configuration

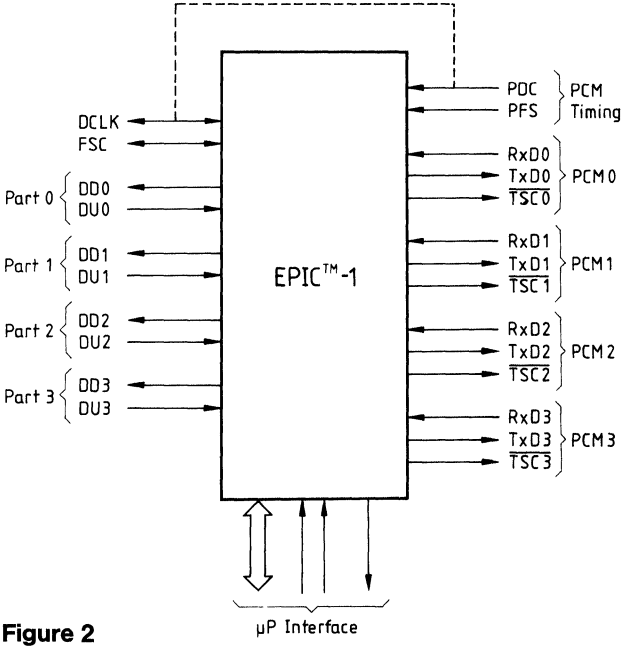
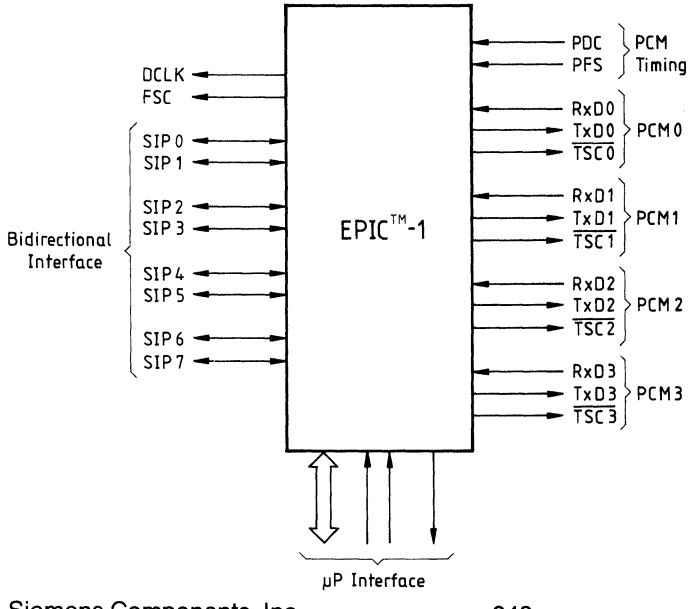


Figure 2
Functional Symbol for the Bidirectional Configuration



System Integration

Communication Multiplexers

The nonblocking switching capability for various bandwidth implemented in the EPIC makes the circuit suitable for use in communication multiplexers. Due to the data rate programmability of the configurable and PCM interfaces, data rate adaption (e.g. between 1544 and 2048 kbit/s systems can be accomplished.

Concentrators

Due to the high data rates of up to 8192 kbit/s, the EPIC can be used in concentrator applications.

Central Switches

The EPIC is a nonblocking switch for up to 128 channels per direction. The channel bandwidth can be programmed to 16, 32 or 64 kbit/s. The PCM and configurable interfaces are programmable for a wide variety of data rates from 8 to 8192 kbit/s. PCM and configurable interfaces can be operated with different clock frequences. Thus, the EPIC can be used in central switches and for data rate adaption.

Line Cards

The EPIC is designed to operate in 3 digital or analog line card architectures. For a schematic summary of these possible line card configuration refer to **figure 3.**

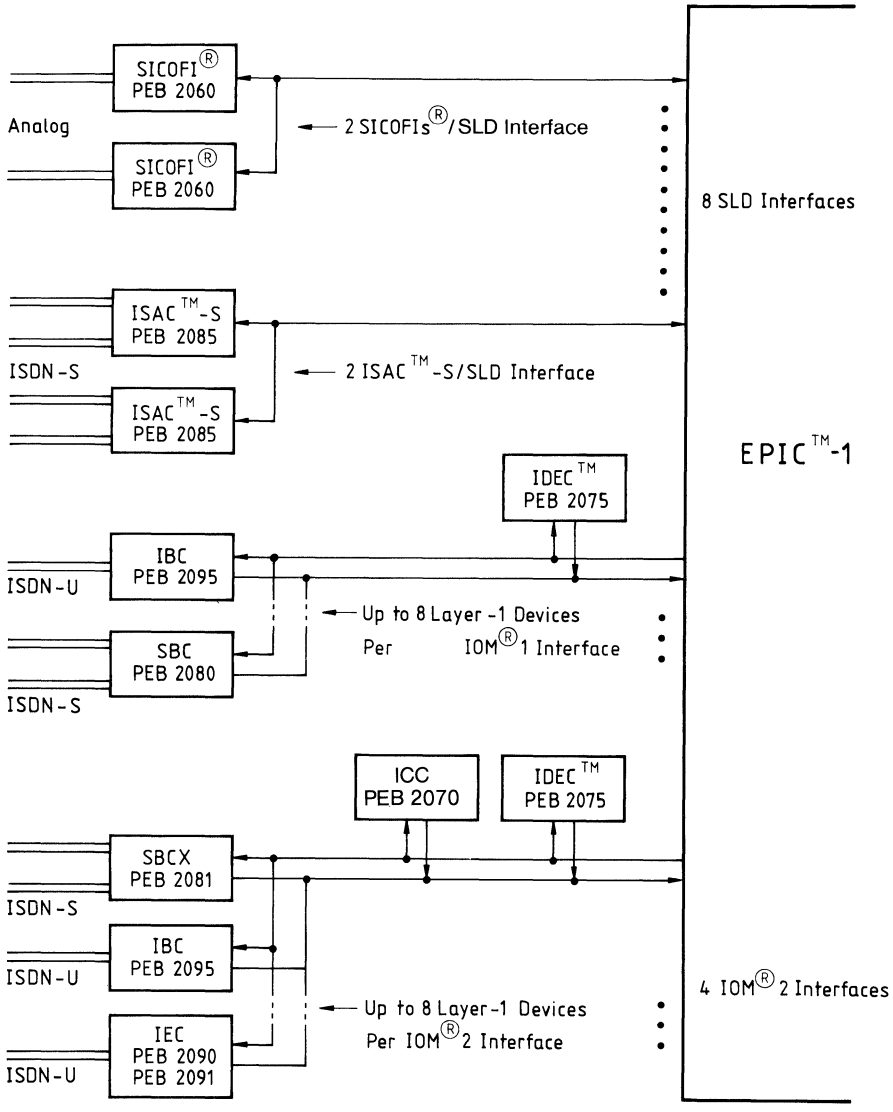
With its **configurable interface** being programmed as a **SLD interface**, it can communicate with SLD compatible devices (e.g. Siemens Codec Filter, SICOFI®, PEB 2060 or ISDN Subscriber Access Controller ISAC™-S, PEB 2085). Connected to up to 16 SICOFIs, the EPIC can serve up to 16 analog lines. Used together with ISAC-S, the EPIC provides the signals for up to 16 ISAC-S, to support up to 16 S-interfaces.

Alternately, the configurable interface may be selected as **IOM interface**, which is compatible to both the **multiplexed IOM-1** and the **IOM-2 interface**.

In the **multiplexed IOM-1 interface** is chosen, the EPIC supports up to 32 ISDN subscribers on the digital line card. The interface lines are then connected to the EPIC, an IOM-1 compatible layer-1 device e.g. the S-bus controller (SBC, PEB 2080), the ISDN Burst Transceiver Circuit (IBC, PEB 2095) or the ISDN Echo Cancellation Circuit (IEC, PEB 2090) and, optionally, an IOM-1 compatible layer-2 device e.g. the ISDN D Channel Exchange Controller (IDEC, PEB 2075).

In the case of an **IOM-2 interface**, the EPIC supports up to 32 ISDN or 64 voice subscribers. They are connected via the SBCX (PEB 2081), IBC (PEB 2095) or IEC (PEB 20901 and PEB 20902) and a digital loop. In both cases, either the ICC (PEB 2070) or the IDEC (PEB 2075) may perform the D channel handling.

Figure 3
Schematic Summary of the Line Card



Analog Line Card

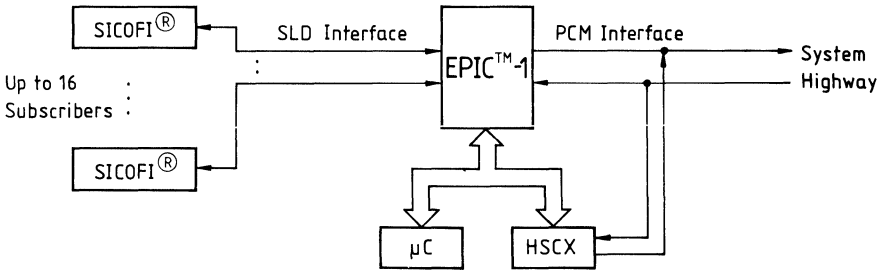
In analog line cards, the EPIC controls the signaling, voice and data paths of 64 kbit/s channels.

In combination with SLD compatible devices e.g. the highly flexible Siemens codec filter (PEB 2060), it forms an optimized analog subscriber line board architecture as shown in **figure 4.** The HSCX (High Level Serial Communication Controller, SAB 82525) handles the signaling information contained in a time slot of programmable bandwidth at the PCM interface or on a dedicated signaling highway.

Moreover, the EPIC controls the feature control and signaling channels and buffers these channels to the µC.

Figure 4

Example of an Analog Line Card Architecture



Digital Line Cards

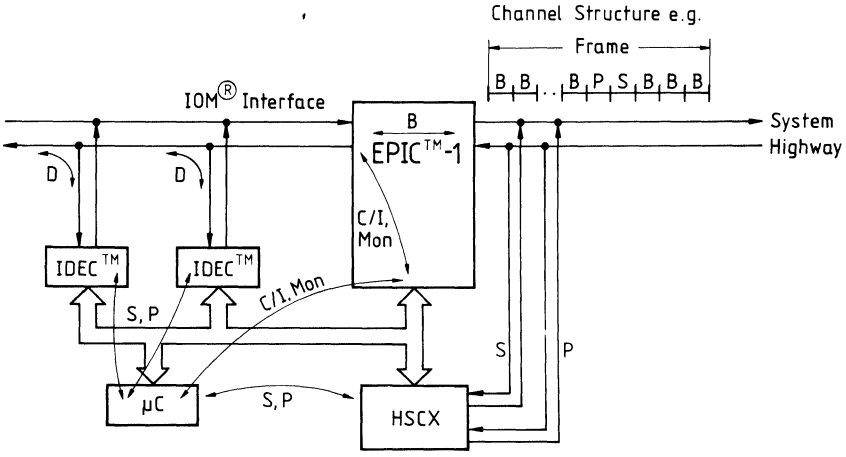
On digital line cards, the EPIC performs the switching function for up to 32 ISDN subscribers between the PCM system highways and the IOM interfaces. Moreover, it has the layer-1 controlling capability of buffering the C/I and monitor channels of the IOM interface.

The EPIC can be operated in tandem, i.e. one device is active, another one is a backup device. The backup device can instantaneously take over from the active device when the active device fails. Due to this tandem operation capability and the high number of ISDN subscribers which can be connected to one EPIC, the use of single line cards is feasable.

Several architectures are possible.

In **completely decentral** D channel processing architectures **(figure 5),** the processing capacity of a line card is usually dimensioned to avoid blocking situations even under maximum conceivable D channel traffic conditions. In such an architecture, the EPIC switches the B channels and performs C/I and monitor channel control. The IDECs handle the layer-2 functions for signaling and data packets in the D channel and transfer the extracted data via the µP and an HDLC controller, e.g. the HSCX (High Level Serial Communication Controller Enhanced SAB 82525) to the system. One of the channels of the HSCX may be used for example for the signaling information, the other for data packets. The HSCX may access either a time slot of programmable bandwidth on one of the system highways **(figure 5)** or a separate signaling highway **(figure 6).** In both cases, the highway capacity used for packet traffic can be shared among several line cards due to the statistical multiplexing capabilities of the HSCX.

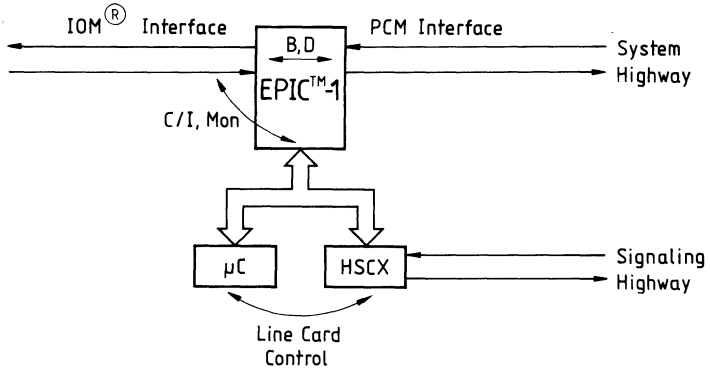
Figure 5
Completely Decentral Packet Switching Digital Line Card Architecture



In an architecture with **completely central** D channel handling **(figure 6)**, the EPIC switches the B and D channels and performs the C/I and monitor channel control functions.

The line card microcontroller programs the EPIC and is connected to the group control via a signaling highway and an HSCX. Moreover the EPIC controls the layer-1 protocol on the IOM interface, buffering the C/I and monitor channels to the microprocessor.

Figure 6
Digital Line Card Architecture with a Completely Central D Channel Handling



A third possibility is a **mixed architecture** with central packet data and decentral signal handling. This is a very flexible architecture which reduces the dynamic load of central processing units by evaluating the signaling information on the line card. For this case, any increase of packet data traffic does not necessitate any changes in the architecture since the line cards do not have to be modified. The central packet handling unit can simply be expanded.

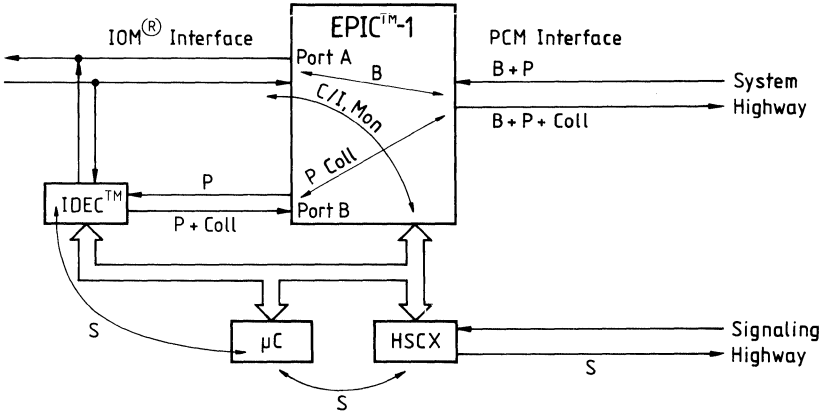
For such an architecture, the EPIC performs B and D channel switching in addition to C/I and monitor channel control. The IDECs handle the signaling data of the D channel. These messages are transferred to the group controller via the microprocessor and an HDLC controller. The packet data of the D channel are switched to the system highways and processed by the central packet unit.

In this architecture, the EPIC switches the B channels from IOM port A **(figure 7)** to the PCM interface. The IDEC works in a master/slave configuration. Therefore, an additional collision resolution line is needed. The IDEC separates signaling from data packets. The signaling messages are transferred to the µC, which in turn hands them over to the group controller using the HSCX.

The packet data are processed differently. Together with the collision resolution line they are handled by the IDEC at another IOM port (port B). The EPIC switches the channels of these ports to the PCM interface as shown in **figure 7.**

Figure 7

Line Card Architecture for Mixed Packet Handling, 2 IOM Ports of the EPIC

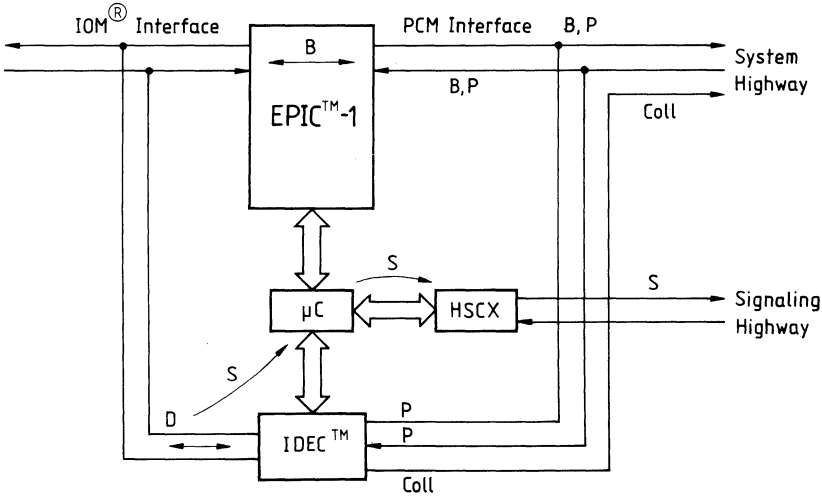


In such a configuration, the p packets and the collision resolution signal occupy one of the IOM ports available at the configurable interface. This reduces the total switching capability of the EPIC to 24 ISDN subscribers.

Alternately, the packet data and the collision line can be directly exchanged between the IDEC and the PCM highway. The EPIC then simply switches the B channels **(see figure 8)**. The packet data are separated by the IDEC and placed on the PCM highway. Thus, the full 32 subscriber switching capability of the EPIC is retained.

Figure 8

Digital Line Card Architecture for Mixed Packet Handling Using a Collision Highway



Packet Handlers

The EPIC is an important building block for networks based on either central, decentral or mixed signaling and packet data handling architectures. Its flexibility allows for the modification of the packet handling architecture according to the changing needs.

Thus, it may be useful to add central packet handling groups to a network originally based on decentral signaling packet handling. This may be the case if growing data packet traffic exceeds the initial capacity of the network. The result is a mixed architecture.

On the other hand, increasing packet handling demand on a few dedicated subscriber lines calls for solutions which back up the capacity at these few decentral line cards.

In both of these cases and several other applications, the EPIC is a powerful device for solving the problem of packet handling. In most applications,it is used together with the IDEC (ISDN D Channel Exchange Controller).

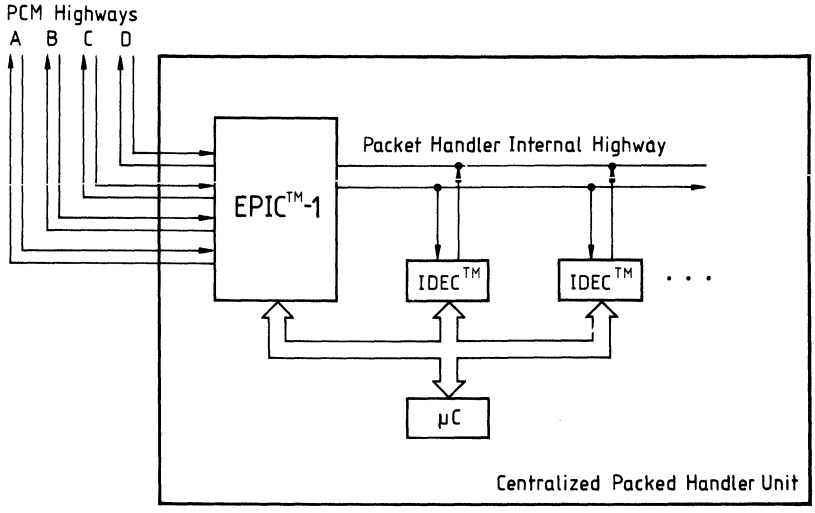
Decentralized and mixed packet handling has already been covered in the line card chapter. In the following, the centralized signaling/data packet handlers built up with the EPIC will be described.

Central packet handling is used if many subscribers with a generally low demand for packet switching are to be connected to a system. Concentrating the packet servers for multiple users eliminates the need to provide a packet server channel for every user. The overall number of packet server channels can thus be reduced.

In such a central packet handling group, the EPIC performs the switching and concentrator function. It connects a variable number of PCM highways to the packet handler internal highway. HDLC controllers are also connected to this internal highway as illustrated in **figure 9.**

Figure 9

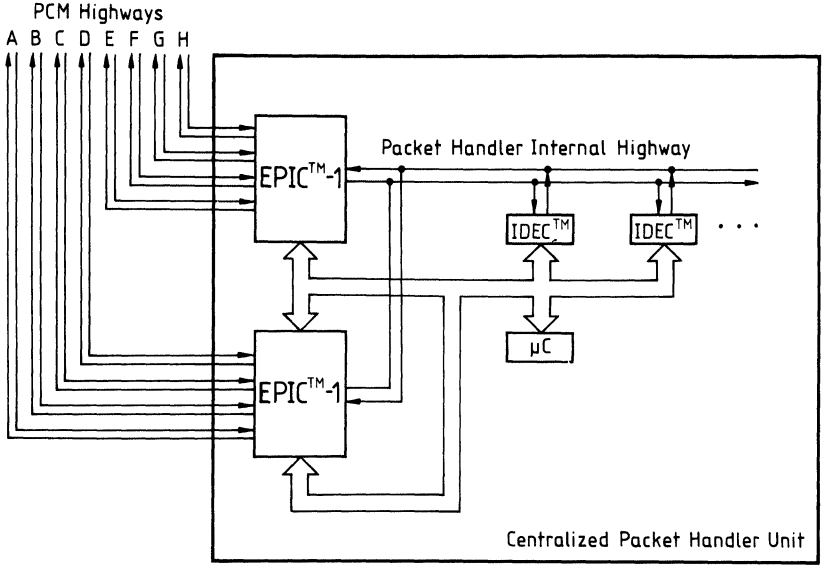
Centralized Packet Handler with a Single Internal Highway Connected to 4 PCM Highways



This figure shows one EPIC connecting four PCM highways to one packet handler internal highway. These highways are accessed by the IDECs (ISDN D channel Exchange Controller) which are 4 channel HDLC controllers and handle the packets. If more than four PCM highways shall be connected to the centralized packet handler, further EPICs are necessary. Such a situation is shown in **figure 10**, where 8 highways are switched to one packet handler internal highway. In this case the two EPICs are connected in parallel at the packet handler internal side.

Figure 10

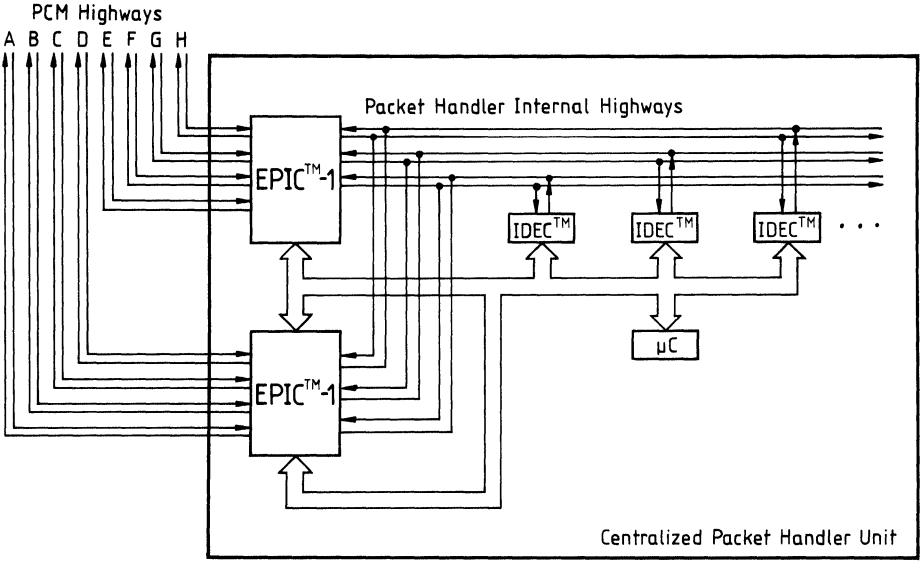
Centralized Packet Handler with 1 Internal Highway Connected to 8 PCM Highways



The data rate of the packet handler internal highway can be up to 4096 kbit/s. If this capacity is not sufficient, other packet handler internal highways may be added as shown in **figure 11.**

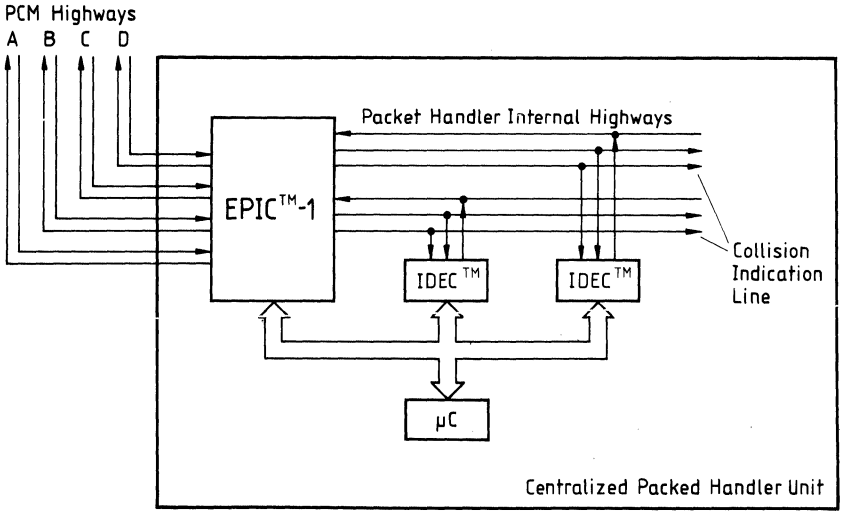
Figure 11

Centralized Packet Handler with 3 Internal Highways



In some applications an additional collision resolution signal is required for the HDLC controllers. This information can be demultiplexed from the PCM highways to a third line for each packet handler internal highway **(see figure 12).**

Figure 12
Centralized Packet Handler with Internal Collision Line



The applications illustrated apply equally to centralized signaling as well as to data packet handlers.

Functional Description

The EPIC is a peripheral board controller. It combines the nonblocking switching function between the PCM and the configurable interfaces for 128 channels per direction with the layer-1 control function for connection set-up/termination/maintenance on one chip.

A general block diagramm of the EPIC is shown in **figure 13.**

In the downstream direction, the input information of a complete frame is stored in the data memory. The incoming channels are written in sequence into fixed positions in the data memory. This is controlled by the downstream input counter with an 8-kHz-repetition rate. A cyclic write sequence results.

For the downstream switching, the control memory (CM) is read in sequence. The addressed location contains a pointer to a location in the data memory. The byte in this data memory location is read into the current configurable interface time slot, resulting in a random read sequence.

The read access of the control memory is controlled by the downstream output counter, correlating the data memory read operations with the downstream output time-slot sequence.

In the upstream direction, the data is written to the data memory randomly, under CM control and read from there cyclically.

Hence, for the desired connection the control memory needs to be programmed beforehand using the MAAR, MADR and MACR registers **(see chapter Memory Access Register)**. The control memory address corresponds to one particular configurable interface time slot and line number. The contents of this control memory address point to a particular PCM interface time slot and line number now resident in the data memory.

For upstream output, four control bits per time-slot are provided in the data memory. These control the output driver state of any possible subtime slot.

Besides the data memory address, each CM address also points to four code bits determining the bandwidth of the switched channel. These code bits are also used to mark the signaling channels at the CFI.

The EPIC can be used in two different set-ups:

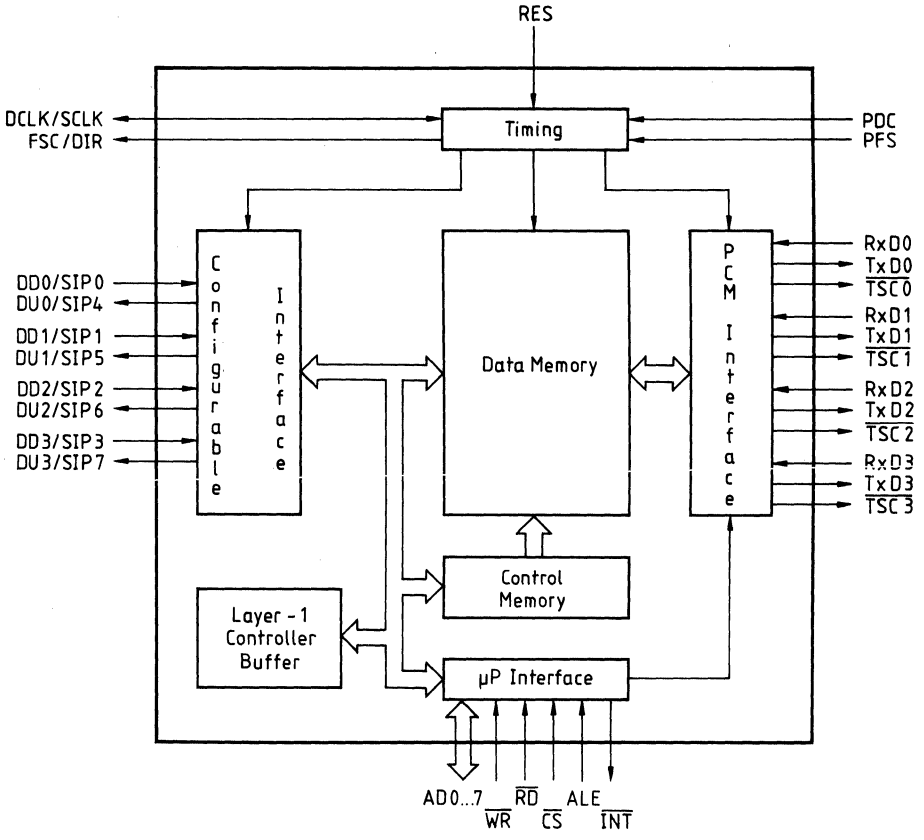
- In the bidirectional set-up, every channel at the configurable interface can be programmed to be either input or output. 8 equivalent bidirectional ports at the configurable interface result.
- In the duplex set-up, 4 of the 8 lines of the configurable interface are predetermined as outputs, 4 as inputs. 4 duplex ports result.

In both of these set-ups, the EPIC provides a switching capability for up to 128 channels and direction.

The IOM and the SLD configurations previously mentioned are special cases of these set-ups:

- In the IOM, the EPIC switches the B and D channels of up to 32 subscribers working in the duplex set-up. Additionally, the device handles the monitor and C/I channel buffering to the µP.
- In the SLD configuration, the EPIC switches up to sixty four 64 kbit/s channels operating in bidirectional set-up. Additionally, the device handles the feature control and signaling channels buffering to the µP.

Figure 13
Functional Block Diagram of the EPIC



In the IOM configuration, upon proper programming, the EPIC checks the incoming C/I channels and generates interrupts if changes occur. In the case of the bidirectional configuration, it implements the double last look algorithm with a period adaptable to a wide range of system needs.

For handling the monitor or feature control channel, the EPIC is equipped with a FIFO buffering up to 16 bytes of information. The contents can be transferred or received upon a special command. Or, they can be dealt with largely autonomously according to the IOM handshake procedure.

Operational Description

Principles

Every time slot at the configurable interface is controlled by a control memory entry. Thus, the functionality of every time slot may be chosen from the choices of **table 1**.

Table 1
CFI Time Slot Functionality Choices

Functionality			Application
Transparent	64 kbit/s 32 kbit/s 16 kbit/s	to/from PCM interface	Switching
Transparent	64 kbit/s	from µP interface	Idle code
Signaling channel bits 5..2			IOM C/I channel
Signaling channel bits 7..2			e.g. analog IOM channel
Signaling channel bits 7..0			e.g. SLD signaling channel
MFFIFO channel			Monitor channel in IOM Feature control channel in SLD

Every channel may be selected in either upstream or downstream direction. The selections for the time slots are nearly independent of each other.

The only restriction is that MFFIFO and signaling channels must be programmed to adjacent time slots, starting with the MFFIFO channel at the even time slot.

The choices of **table 1** may be programmed independently of the selected mode.

By programming the time slots, the configurable interface may be configured e.g. as a

- transparent PCM interface (plain switching function)
- IOM interface
- SLD interface

Register Description*

The following symbols are used throughout this chapter

x... don't care

u... used to ensure the intended function

n... not used. It has to be set to logical 0 in write accesses but may be switched by the EPIC to either logical level in read accesses.

Table 2
Register Set

Group	Register Name	Access Write (WR) Read (RD)	µP Interface Mode MUX. AD7..AD0	DEMUX. A3..A0/RBS	Reset Value	Register Content
PCM	PMOD	RD/WR	20_H	$0_H/1$	00	PCM Mode Register
	PBNR	RD/WR	22_H	$1_H/1$	FF	PCM Bit Number Register
	POFD	RD/WR	24_H	$2_H/1$	00	PCM Offset Downstream Register
	POFU	RD/WR	26_H	$3_H/1$	00	PCM Offset Upstream Register
	PCSR	RD/WR	28_H	$4_H/1$	00	PCM Clock Shift Register
	PICM	RD/WR	$2A_H$	$5_H/1$	–	PCM Input Comparison Mismatch Register
CFI	CMD1	RD/WR	$2C_H$	$6_H/1$	00	CFI Mode Register 1
	CMD2	RD/WR	$2E_H$	$7_H/1$	00	CFI Mode Register 2
	CBNR	RD/WR	30_H	$8_H/1$	FF	CFI Bit Number Register
	CTAR	RD/WR	32_H	$9_H/1$	00	CFI Time Slot Adjustment Register
	CBSR	RD/WR	34_H	$A_H/1$	00	CFI Bit Shift Register
	CSCR	RD/WR	36_H	$B_H/1$	00	CFI Subchannel Register
MAR	MACR	RD/WR	00_H	$0_H/0$	–	Memory Access Control Register
	MAAR	RD/WR	02_H	$1_H/0$	–	Memory Access Address Register
	MADR	RD/WR	04_H	$2_H/0$	–	Memory Access Data Register

* For a detailed register description, refer to the EPIC Data Sheet 10/88

Group	Register Name	Access Write (WR) Read (RD)	µP Interface Mode mux. AD7..AD0	µP Interface Mode demux. A3..A0/RBS	Reset Value	Register Content
STR	STDA	RD/WR	06_H	$3_H/0$	–	Synchron Transfer Data Register A
	STDB	RD/WR	08_H	$4_H/0$	–	Synchron Transfer Data Register B
	SARA	RD/WR	$0A_H$	$5_H/0$	–	Synchron Transfer Receive Address Register A
	SARB	RD/WR	$0C_H$	$6_H/0$	–	Synchron Transfer Receive Address Register B
	SAXA	RD/WR	$0E_H$	$7_H/0$	–	Synchron Transfer Transmit Address Register A
	SAXB	RD/WR	10_H	$8_H/0$	–	Synchron Transfer Transmit Address Register B
	SRCR	RD/WR	12_H	$9_H/0$	00	Synchron Transfer Control Register
MFCH	MFAIR	RD	14_H	$A_H/0$	Undef.	MF Channel Actice Indication Register
	MFSAR	WR	14_H	$A_H/0$	Undef.	MF Channel Subscriber Address Register
	MFFIFO	RD/WR	16_H	$B_H/0$	Empty	MF Channel FIFO
SCR	C/I FIFO	RD	18_H	$C_H/0$	Validity 0	Signaling Channel FIFO
	TIMR	WR	18_H	$C_H/0$	00	Timer Register
	STAR	RD	$1A_A$	$D_H/0$	05	Status Register
	CMDR	WR	$1A_H$	$D_H/0$	00	Command Register
	ISTA	RD	$1C_H$	$E_H/0$	00	Interrupt Status Register
	MASK	WR	$1C_H$	$E_H/0$	00	Mask Register
	OMDR	RD/WR	$1E_H/3E_H$	F_H/X	00	Operation Mode Register
	VNSR	RD	$3A_H$	$D_H/1$		Version Number Register

Note: In the multiplexed µP interface mode AD0 is not used for address coding.

Absolute Maximum Ratings

Description	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5$ V, $V_{SS} = 0$ V

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V	
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA
H-output voltage	V_{OH}	2.4		V	$I_{OH} = -400$ µA
H-output voltage	V_{OH}	V_{DD} −0.5		V	$I_{OH} = -100$ µA
Operational power supply current					$V_{DD} = 5$ V, input at 0 V or V_{DD}, no output loads
	I_{CC}		9.5	mA	clock frequency > 4096 kHz
	I_{CC}		6.5	mA	clock frequency ≤ 4096 kHz
Input leakage current	I_{LI}		10	µA	$0 V < V_{IN} < V_{DD}$ to 0 V
Output leakage current	I_{LO}		10	µA	$0 V < V_{OUT} < V_{DD}$ to 0 V

Capacitances

$T_A = 25\,°C$; $V_{DD} = 5\,V$, $V_{SS} = 0\,V$

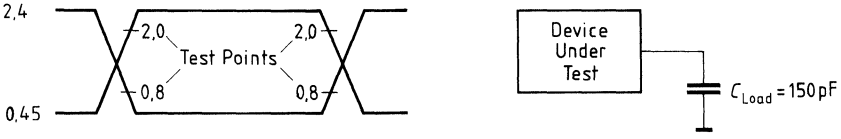
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
I/O capacitance	C_{IO}		20	pF
Output capacitance	C_{OUT}		15	pF

AC Characteristics

Ambient temperature under bias range, $V_{DD} = 5\,V \pm 5\%$

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

Figure 21
I/O Waveform for AC Tests

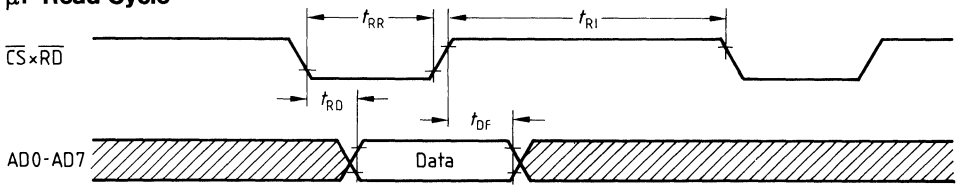


Microprocessor Interface Timing Parameters

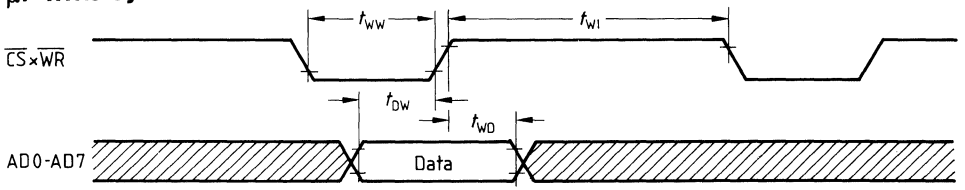
Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	30		ns
Address setup time to ALE	t_{AL}	10		ns
Address hold time form ALE	t_{LA}	20		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	25		ns
$\overline{RD}$ delay after WR setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		100	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ + $\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}$ + $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

INTEL Bus Mode

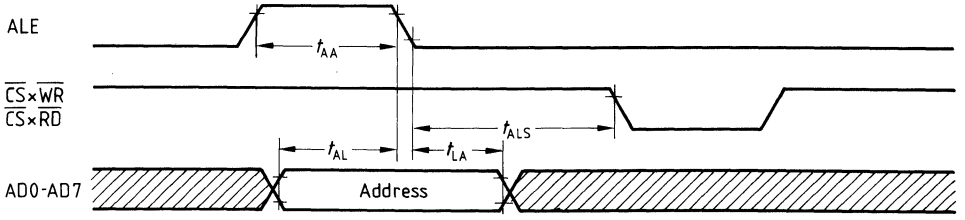
µP Read Cycle



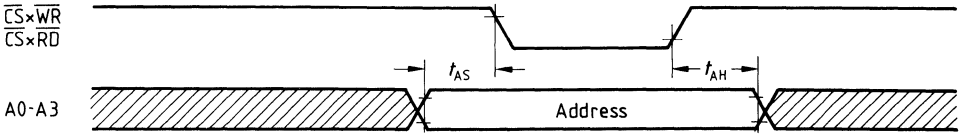
µP Write Cycle



Multiplexed Address Timing

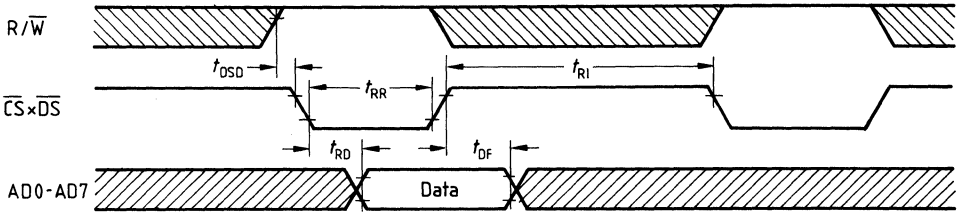


Demultiplexed Address Timing

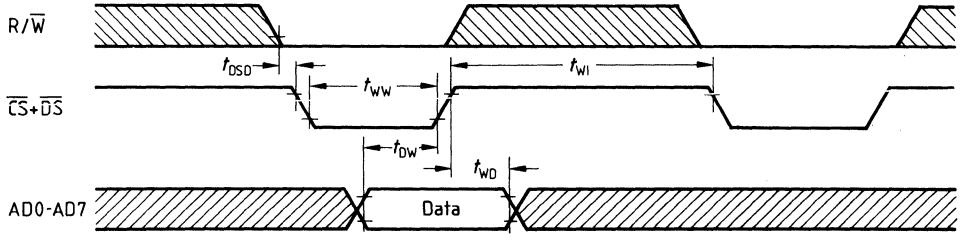


Motorola Bus Mode

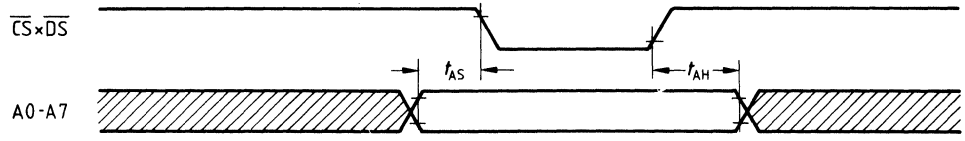
µP Read Cycle



µP Write Cycle



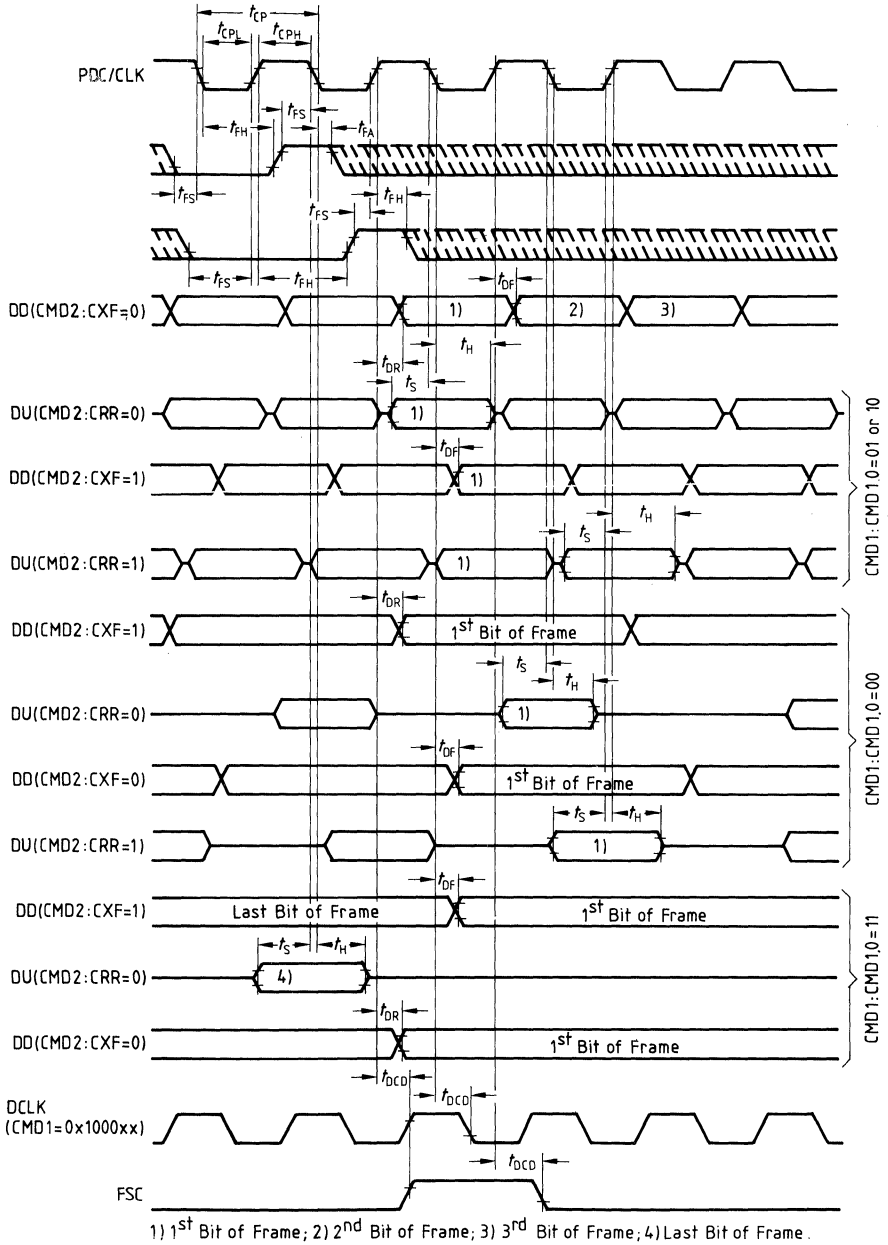
Address Timing



Timing of PCM and Configurable Interfaces

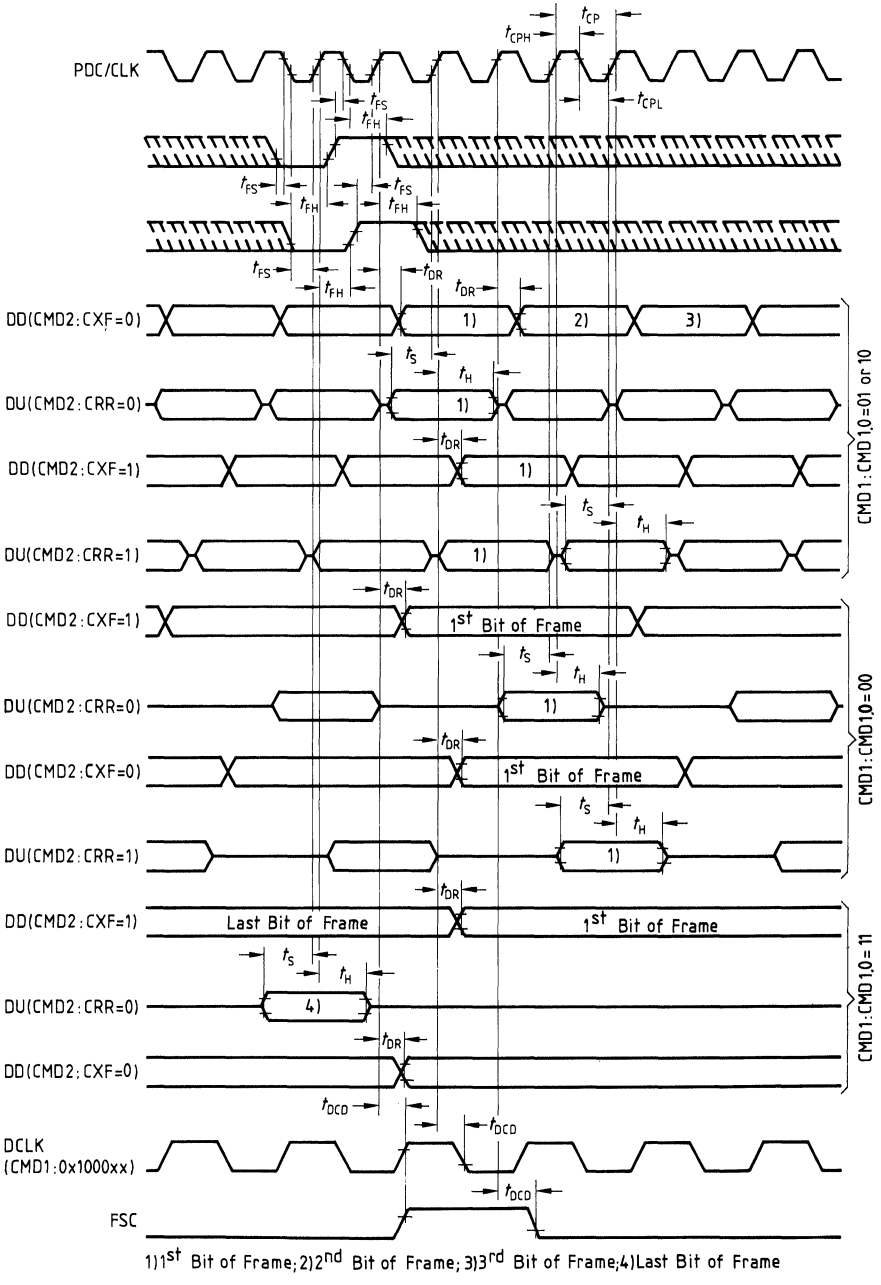
Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Conditions
Clock period Clock period low Clock period high	t_{CP} t_{CPL} t_{CPH}	240 80 100		ns ns ns	clock frequency ≤ 4096 kHz
Clock period Clock period low Clock period high	t_{CP} t_{CPL} t_{CPH}	120 50 50		ns ns ns	clock frequency > 4096 kHz
Frame setup time Frame hold time	t_{FS} t_{FH}	15 50		ns ns	
Data clock delay time	t_{DCD}		125	ns	
Serial data input setup time Serial data input hold time	t_S t_H	5 35		ns ns	PCM input data frequency > 4096 kbit/s
Serial data input setup time Serial data input hold time	t_S t_H	15 50		ns ns	PCM input data frequency ≤ 4096 kbit/s
Serial data input setup time Serial data input	t_S t_H	15 50		ns ns	CFI input data frequency > 4096 kbit/s
Serial data input setup time Serial data input hold time	t_S t_H	0 75		ns ns	CFI input data frequency ≤ 4096 kbit/s
PCM serial data output delay time	t_D		55	ns	
Tristate control delay	t_T		60	ns	
CFI serial data output delay time (falling clock edge)	t_{DF}		60	ns	
CFI serial data output delay time (rising clock edge)	t_{DR}		80	ns	

AC Characteristics at the CFI with CMD: CSP 1.0 = 10 (Prescaler Divisor = 1)



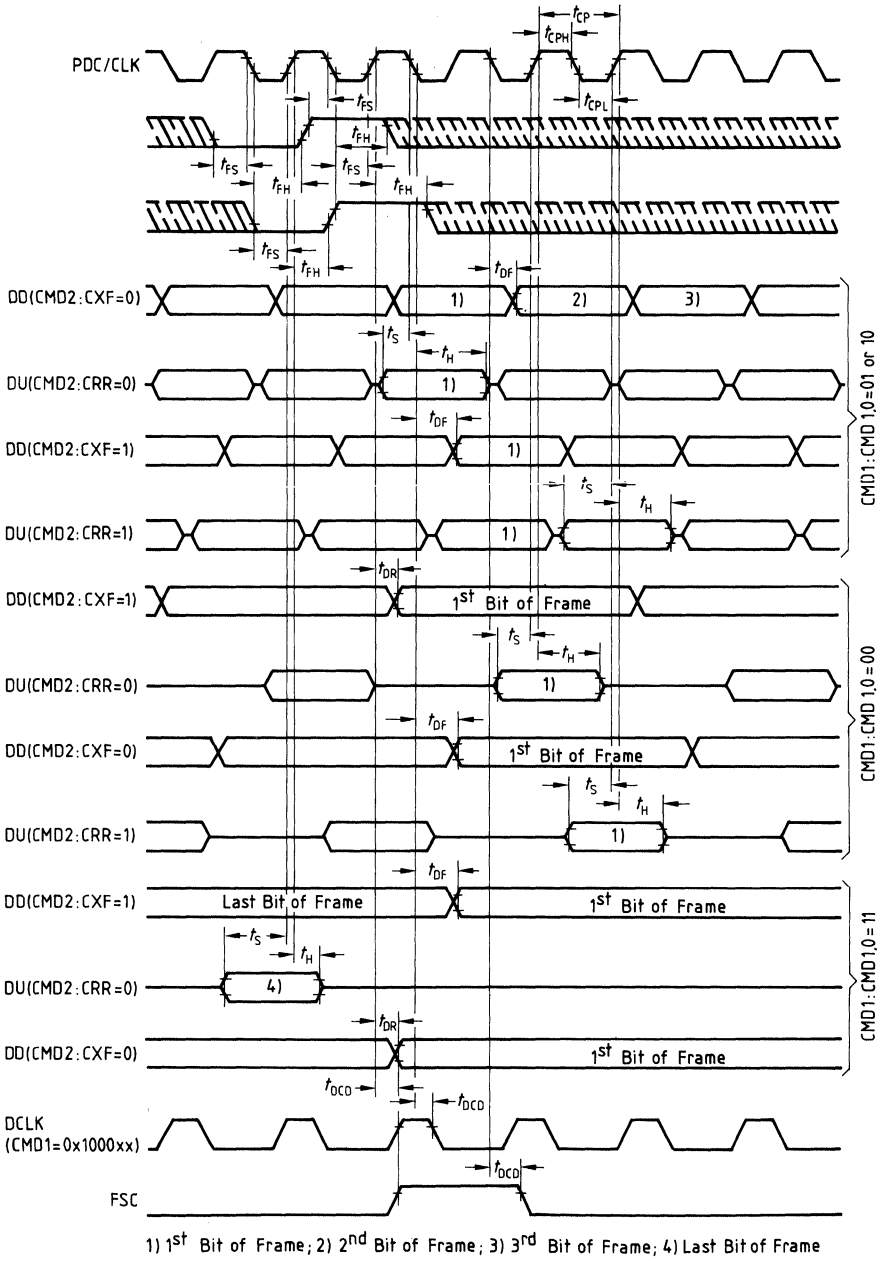
1) 1st Bit of Frame; 2) 2nd Bit of Frame; 3) 3rd Bit of Frame; 4) Last Bit of Frame.

AC Characteristics at the CFI with CMD: CSP 1.0 = 00 (Prescaler Divisor = 2)



1)1st Bit of Frame; 2)2nd Bit of Frame; 3)3rd Bit of Frame; 4)Last Bit of Frame

AC Characteristics at the CFI with CMD1:CSP = 01 (Prescaler Divisor)



1) 1st Bit of Frame; 2) 2nd Bit of Frame; 3) 3rd Bit of Frame; 4) Last Bit of Frame

AC Characteristics at the PCM Interface