

## PCM Interface Controller (PIC)

## PEB 2052

Preliminary Data

CMOS IC

Type	Ordering Code	Package
PEB 2052-C	Q67100-H6059	C-DIP-40
PEB 2052-N	Q67100-H6060	PL-CC-44 (SMD)
PEB 2052-P	Q67100-H6061	P-DIP-40

The PCM interface controller PEB 2052 is a device for the control of voice, data, and signaling paths of up to 16 subscribers on peripheral component boards in digital telephone systems. In combination with the highly flexible Signal Processing Codec Filter (SICOFI® PEB 2060) it forms an optimized analog subscriber-line board architecture. Its flexibility allows operation as general-purpose controller for data switching and MUX/De MUX applications.

The PIC controls space and time switching functions between subscriber-line devices and time-division multiplex highways. Further, it controls the flow of information between the subscriber interface ports and a local line card processor.

To meet the different requirements the PIC PEB 2052 provides the following interfaces:

- 8 serial, bidirectional I/O ports for the transfer of voice, data, control, and signaling information between the PBC and codec filters (e.g. SICOFI PEB 2060), digital interface circuits or signal processors.
- Double-constructed PCM interface.
- Bit-parallel interface for the connection of 8-bit standard microcomputers such as the SAB 8051.

The PIC PEB 2052 is pin and software compatible with PEB 2050 and is optimized for applications without an HDLC signaling link. It is fabricated using Siemens ACMOS 3 technology.

### Features

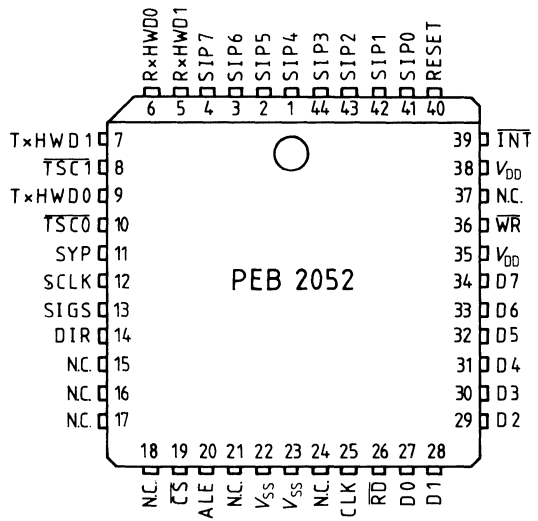
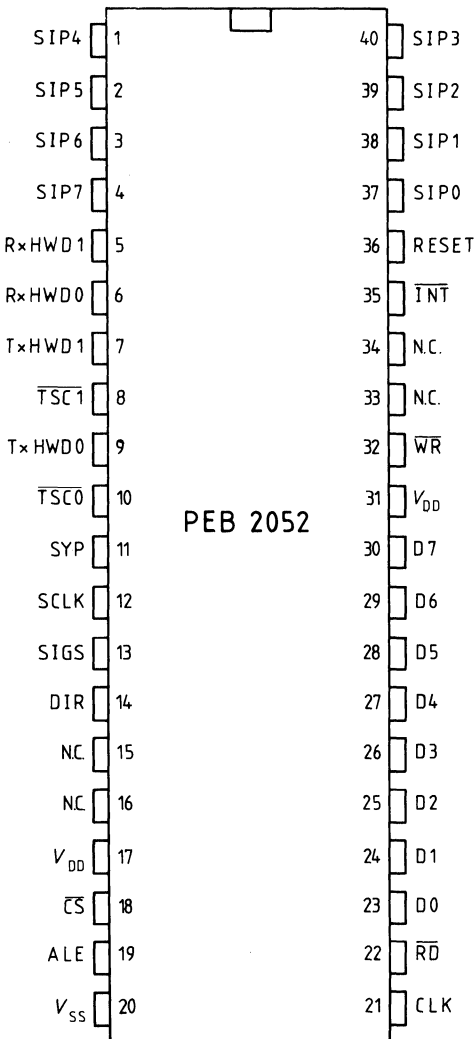
- Board controller for up to 16 subscribers of a digital switching system
- Designed for different PCM systems
- Time-slot assignment freely programmable for all subscribers connected
- Control of voice, data, signaling and line board parameters to minimize hardware requirements and to simplify software
- Provides two full duplex PCM highways for the system interface
- Pin and software compatible with PEB 2050
- Standard  $\mu$ P interface
- $\mu$ P access to all internal data streams including time-slot oriented data streams
- Support of subscriber circuits by generating timing signals
- Single +5 V power supply
- Advanced CMOS technology
- Low power consumption

**Pin Configurations**

(top view)

**P-DIP**

**PL-CC**



## Pin Definitions and Functions

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
1 . . . 4	1 . . . 4	SIP 4 . . . SIP 7	Subscriber interface port (input/output)	These interface ports are used for bi-directional, bit-serial transfer of speech, data and control words to and from the signal processing codec filter (SICOFI) or standard codec. Corresponding with the direction signal, the PIC PEB 2052 is transmitting during the high level of DIR within the first half of a 125 $\mu$ s frame.
5 6	5 6	RxHWD 1 RxHWD 0	Receive highway data (input) Receive highway data (input)	Receive PCM highway 1 interface. Receive PCM highway 0 interface. The PIC serially receives a PCM word (8 bits) through one of these leads at the programmed time slot.
7	7	TxHWD 1	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 1 (serial bus). The 8-bit PCM word is serially sent out on this pin at the programmed time slot. Tristate output.
8	8	TSC 1	Tristate control (output, active low)	Normally high, this signal goes low while the PIC is transmitting an 8-bit PCM word on the PCM highway 1.
9	9	TxHWD 0	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 0.
10	10	TSC 0	Tristate control (output, active low)	Tristate control of highway 0.
11	11	SYP	Synchronization	SYP is a frame synchronization pulse which resets the on-chip time-slot counters.
12	12	SCLK	Slave clock (output)	Clock output for the peripheral devices. The signals between the codec filter and the PIC are latched and transmitted with the rising edge of SCLK.
13	13	SIGS	Signal strobe (output, active high)	The SIGS output supplies a programmable strobe signal.

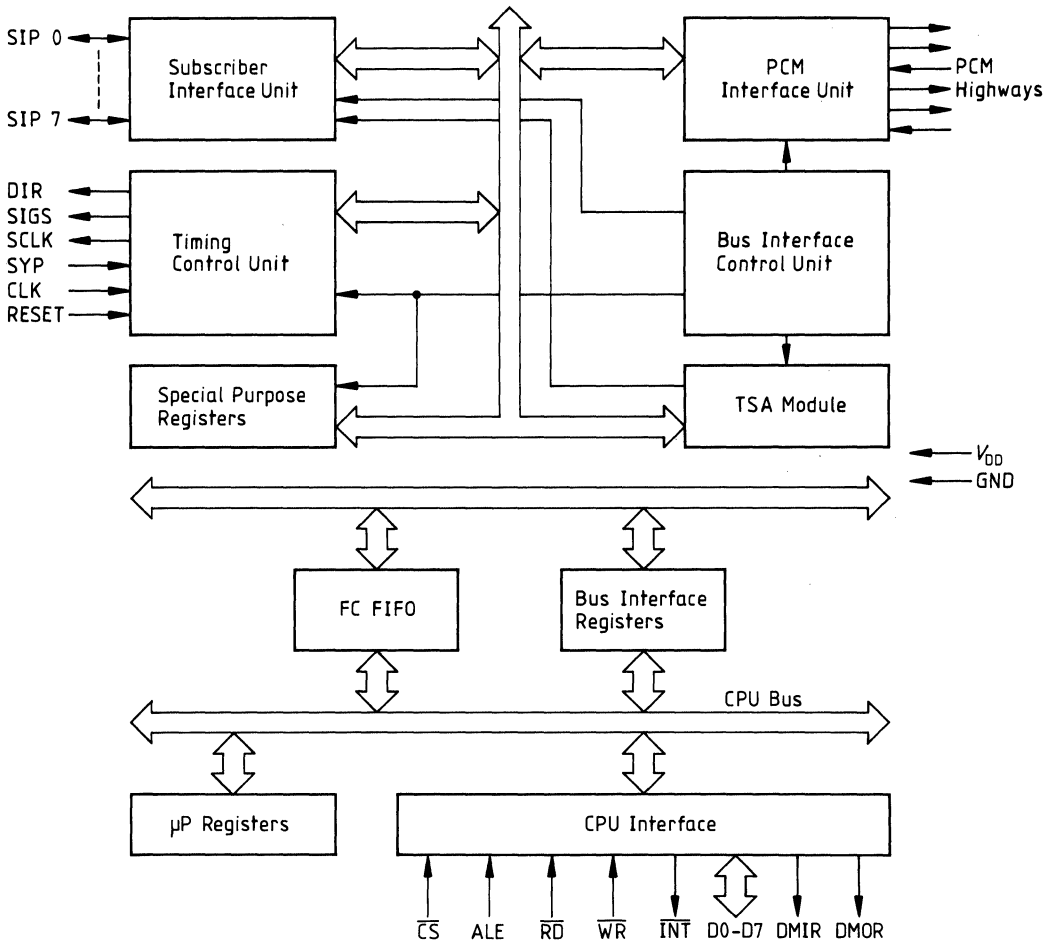
## Pin Definitions and Functions (cont'd)

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
14	14	DIR	Direction (output, active high)	DIR is an 8-kHz-symmetric frame signal which controls the direction of data transfer from and to the peripheral devices. The PIC is able to receive data during the low state of DIR.
15	15	N.C.		Not connected
16	16	N.C.		Not connected
38	17	$V_{DD}$		Power supply: $V_{DD} = 5.0 \text{ V} \pm 0.25 \text{ V}$
19	18	$\overline{CS}$	Chip select (input, active low)	CS is used to address the PIC. A low level at this input enables the PIC to accept commands or data from a $\mu\text{P}$ within a write cycle, or to transmit data during a read cycle.
20	19	ALE	Address latch enable (input, active high)	A high level at this input indicates that the data on the external bus is an address selecting one of the PIC-internal sources or destinations. Latching into the address latch occurs during the high-low transition.
22, 23	20	$V_{SS}$		Ground (0 V)
25	21	CLK	Clock (input)	A standard TTL clock provides the basic timing of the controller. The clock is synchronous to the PCM clock.
26	22	$\overline{RD}$	Read strobe (input, active low)	$\overline{RD}$ is used together with $\overline{CS}$ to transfer data from the PBC to a $\mu\text{P}$ or memory.
27 . . . . . .	23 . . . . . .	D0 . . . . . .	System data bus	The data bus transfers data and commands between the $\mu\text{P}$ or memory and the PIC.
34	30	D7		
35	31	$V_{DD}$		Power supply: $V_{DD} = 5.0 \pm 0.25 \text{ V}$

## Pin Definitions and Functions (cont'd)

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
36	32	$\overline{WR}$	Write strobe (input, active low)	During the low state of $\overline{WR}$ data can be transferred from the $\mu P$ or memory to the PBC.
37	33 34	N.C. N.C.		Not connected Not connected
39	35	$\overline{INT}$	Interrupt request (output, active low)	The signal is pulled down, when the PIC is requesting an interrupt. In that case, the $\mu P$ should enter an interrupt routine for reading status register 1.
40	36	RESET	Reset (input, active high)	A high on this input forces the P/C into reset state. The minimum reset pulse is 16 complete clock cycles.
41 . . . . . .	37 . . . . . .	SIP 0 . . . . . .	Subscriber interface port (input/output)	These interface ports are used for bi-directional, bit-serial transfer of speech, data and control words to and from the Signal Processing Filter (SICOFI) or standard codec. Corresponding with the direction signal, the PIC PEB 2052 is transmitting during the high level of DIR within the first half of a 125 $\mu s$ frame.
44	40	SIP 3		

**Block Diagram**



**Description of the Functional Blocks**

The PIC has been designed especially for use in peripheral subscriber boards, but its functional flexibility also permits its application in various parts of a digital exchange telecommunications system.

Used in peripheral subscriber boards it performs two essential functions:

- 1) Exchange of control data between an on-board processing unit and individual subscriber connections.
- 2) The time-slot controlled transfer of PCM data (64-Kbaud channels) between the PCM highways and the subscriber connections. Data transfers between both parts, such as the access of the on-board  $\mu$ P to 64-Kbaud channels, are considerably simplified by the IC.

**The PIC Consists of the Following Functional Blocks**

- Subscriber Interface Unit
- PCM Interface Unit
- TSA Module (Contents-Addressable Memory)
- Timing Control Unit
- $\mu$ P Interface
- $\mu$ P Control and Status Register
- Feature Control FIFO (16 byte)
- Bus Interface Register

**Maximum Ratings**

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Storage temperature	$T_{stg}$	-65	125	°C

**Range of Operation**

Operating temperature	$T_A$	0	70	°C
Voltage at any pin referred to ground	$V_S$	-0.5	7	V
Total power consumption	$P_{tot}$		35	mW

**DC Characteristics**

$T_A = 0$  to  $70$  °C;  $V_{CC} = 5$  V  $\pm$  0.25 V; GND = 0 V

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
L-input voltage	$V_{IL}$	-0.5		0.8	V
H-input voltage	$V_{IH}$	2.0		5.5	V
L-output voltage $I_{OL} = +1.6$ mA	$V_{OL}$			0.45	V
H-output voltage $I_{OH} = -400$ $\mu$ A	$V_{OH}$	2.4			V
Input leakage current $V_{IN} = V_{CC}$ to 0 V	$I_{IL}$	-10		10	$\mu$ A
Output leakage current $V_{OUT} = V_{CC}$ to 0 V	$I_{OL}$	-10		10	$\mu$ A
$V_{CC}$ supply current $V_{CC} = 5$ V	$I_{CC}$			7	mA

**Capacitance**

$T_A = 25$  °C;  $V_{CC} =$  GND = 0 V

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input capacitance $f_C = 1$ MHz	$C_{IN}$		5	10	pF
Input/output capacitance	$C_{I/O}$		10	20	pF
Output capacitance unmeasured pins returned to GND	$C_{OUT}$		8	15	pF



**AC Characteristics**

$T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$ ;  $\text{GND} = 0\text{ V}$

**Microprocessor Interface**

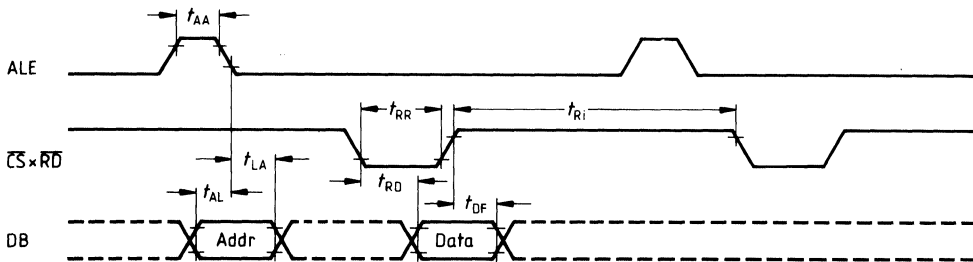
**Read Cycle**

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address hold after ALE	$t_{LA}$	20		ns
Address to ALE setup	$t_{AL}$	30		ns
Data delay from $\overline{\text{RD}}$	$t_{RD}$		120	ns
$\overline{\text{RD}}$ pulse width	$t_{RR}$	120		ns
Output float delay	$t_{DF}$		25	ns
$\overline{\text{RD}}$ control interval	$t_{RI}$	80		ns
ALE pulse width	$t_{AA}$	60		ns

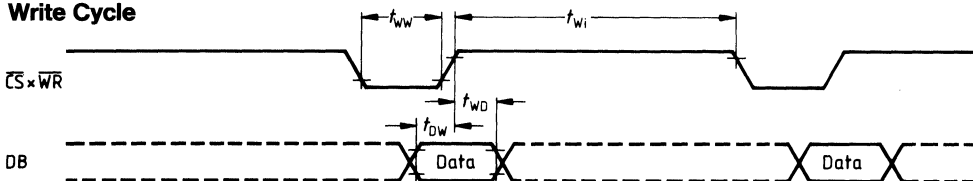
**Write cycle**

$\overline{\text{WR}}$ pulse width	$t_{WW}$	100		ns
Data setup to $\overline{\text{WR}}$	$t_{DW}$	50		ns
Data hold after $\overline{\text{WR}}$	$t_{WD}$	25		ns
$\overline{\text{WR}}$ control interval	$t_{WI}$	50		ns

**Read Cycle**



**Write Cycle**



**Clock Timing**

Parameter	Symbol	Limit Values		Unit
		min.	max.	

**System Clock**

System clock frequency	$f_{CLK}$		4.2	MHz
Duty cycle		40	60	%
Sync pulse period	$t_{SPP}$	125	$N \times 125$	$\mu$ s
Sync pulse width	$t_{SYP}$	60	$t_{CLK}$	ns
Pulse delay to CLK	$t_{dSYP}$	10		ns
Setup time to CLK	$t_{sSYP}$	50		ns

**Slave Clock**

Clock frequency	$f_{SCLK}$	512	512	kHz
Clock delay time	$t_{dSCLK}$		150	ns

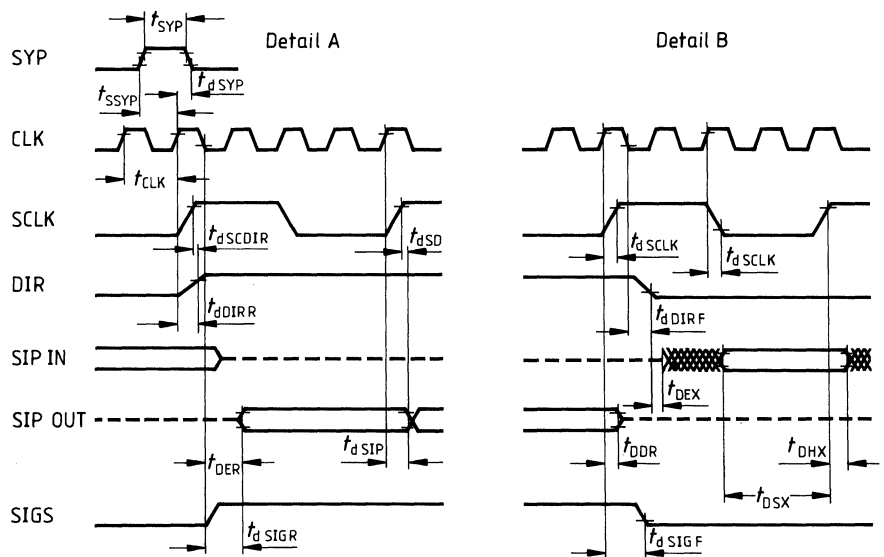
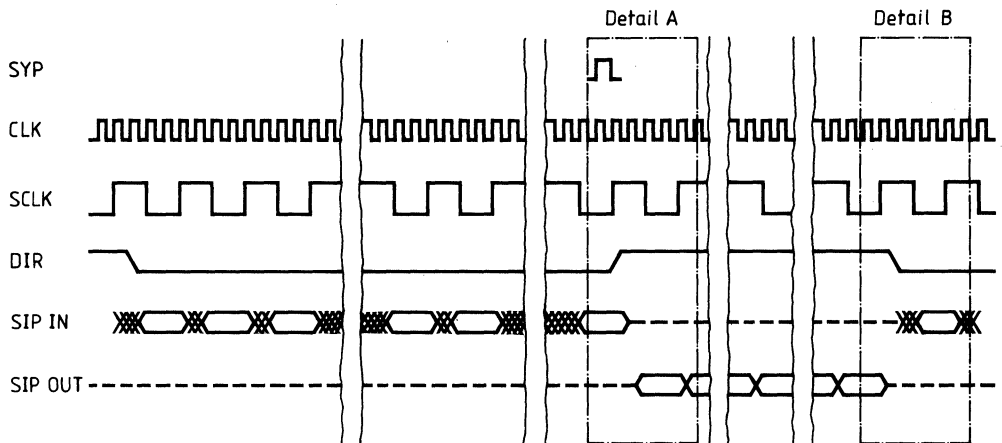
**DIR Clock**

Delay time to CLK (rising edge)	$t_{dDIR R}$		150	ns
Delay time to CLK (falling edge)	$t_{dDIR F}$		110	ns

**SIU Interface**

SIP data delay	$t_{dSIP}$		200	ns
Data enable receive	$t_{DER}$		120	ns
Data disable receive	$t_{DDR}$		120	ns
Data enable transmit	$t_{DEX}$	0		ns
Data hold transmit	$t_{DHX}$	0		ns
Data setup transmit (control data)	$t_{DSX}$	$CP/2 + 200$		ns
Data setup transmit	$t_{DSX}$	100		ns
Signaling strobe delay (falling edge)	$t_{DSIG F}$		150	ns
Signaling strobe delay (rising edge)	$t_{DSIG R}$		150	ns

SIP Interface Timing



**Serial Port Timing**

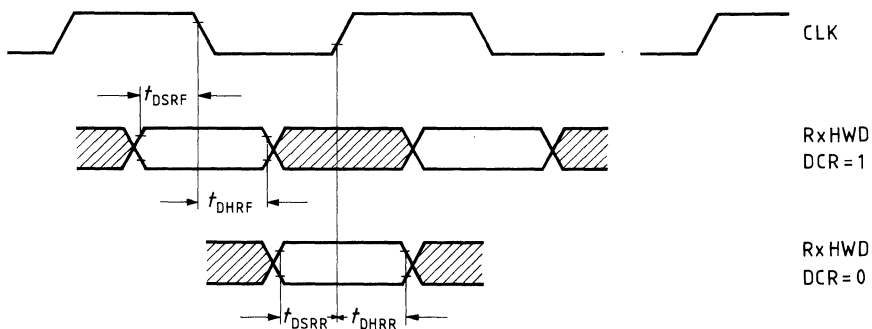
**PCM Interface**

Parameter	Symbol	Limit Values		Unit
		min.	max.	

**Receive Timing**

Receive data setup DCR = 1	$t_{DSRF}$	20		ns
Receive data setup DCR = 0	$t_{DSRR}$	40		ns
Receive data hold DCR = 1	$t_{DHRF}$	40		ns
Receive data hold DCR = 0	$t_{DHRR}$	10		ns

**Receive Timing**



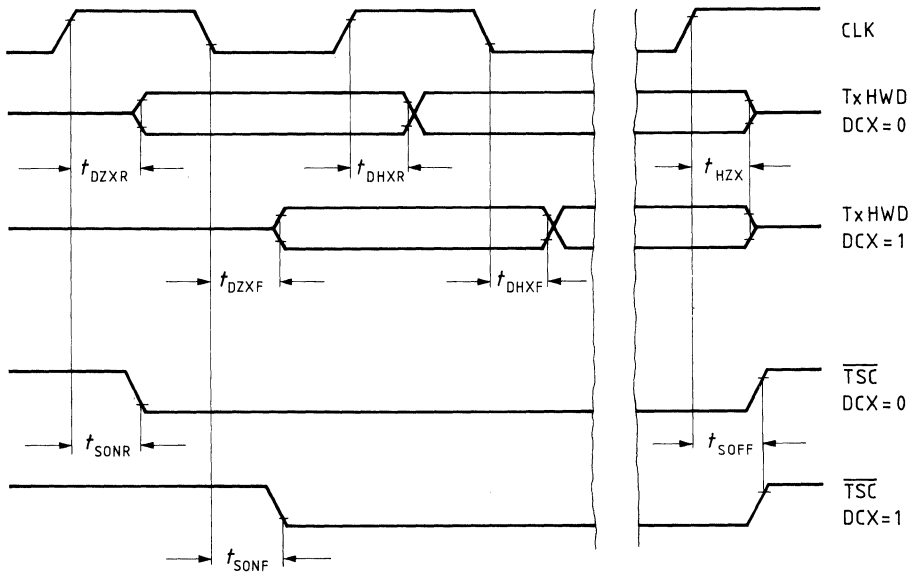
**PCM Interface (cont'd)**

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		

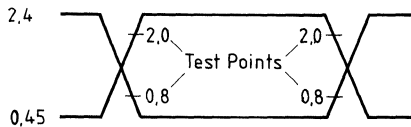
**Transmit Timing**

Data enable DCX = 0	$t_{DZXR}$		160	ns	$C_L = 200$ pF
Data enable DCX = 1	$t_{DZXF}$		100	ns	$C_L = 200$ pF
Data hold time DCX = 0	$t_{DHXR}$		160	ns	$C_L = 200$ pF
Data hold time DCX = 1	$t_{DHXF}$		100	ns	$C_L = 200$ pF
Data float on TS EXIT	$t_{HZX}$		80	ns	$C_L = 150$ pF
Time slot x to enable DCX = 0	$t_{SONR}$		130	ns	$C_L = 150$ pF
Time slot x to enable DCX = 1	$t_{SONF}$		100	ns	$C_L = 150$ pF
Time slot x to disable	$t_{SOFF}$		100	ns	$C_L = 150$ pF

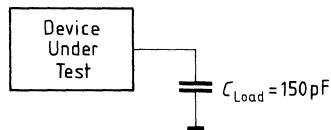
**Transmit Timing**



**AC Testing Input, Output Waveform**



**AC Testing Load Circuit**



AC testing: inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".