SIEMENS

Advanced CMOS Frame Aligner (ACFA) PEB 2035

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2035-C	Q67100-H8358	C-DIP 40
PEB 2035-N	Q67100-H8684	PL-CC 44
PEB 2035-P	Q67100-H8359	P-DIP 40

Introduction (PEB 2035; Version A)

The Advanced CMOS Frame Aligner PEB 2035 (ACFA) is a monolithic CMOS device which implements the interface to primary rate PCM carriers. It may be programmed to operate in 24-channel (T1) and 32-channel (CEPT) carrier systems.

The ACFA features include: selectable multiframe (six multiframe formats), error checking (CRC4, CRC6), multiple line codes (HDB3, B8ZS, AMI), and programmable signaling paths. The device meets the newest CCITT recommendations for primary rate interfaces and the AT&T Digital Multiplexed Interface specifications (DMI). Controlling and monitoring of the device is performed via a parallel eight-bit microprocessor bus.

The circuit contains a two-frame elastic memory which ensures wander absorption between the PCM carrier and a synchronous, system internal highway.

All signaling types – CCS, CAS and bit-robbed signaling – are supported by the ACFA. In addition, the ACFA allows flexible access to facility data link and service channels. Extensive testing capabilities are included.

The ACFA is suitable for use in a wide range of voice and data applications such as the connection of digital switches and PABX's to host computers (S1/S2 interfaces), the implementation of primary ISDN subscriber loops, and the connection to primary rate fibre optical transmission systems.

The ACFA is available in either 40 pin DIP or 44 pin PL-CC packages. As with all of the ISDN circuits from Siemens, the ACFA has been implemented in advanced CMOS technology. Total power consumption is less than 100 mW.

Features

Serial Interface to Line Interface Unit

- Frame alignment/synthesis for 2048 kbit/s (CEPT, PCM 30) and 1544 kbit/s (T1, PCM 24) PCM
- Meets newest CCITT Rec's (G703, 704, 732, 733, Nov. 1984) and AT&T technical advisories (DMI, April 1985)
- Programmable formats for: PCM 30: Doubleframe, CRC Multiframe
  PCM 24: 4-Frame Multiframe (F4), 12-Frame Multiframe (F12, D3/4), Extended Superframe (ESF), Remote Switch Mode (F72)
- Selectable line codes (HDB3, B8ZS, AMI with ZCS)
- Unipolar NRZ for interfacing fibre optical transmission routes
- Error checking via CRC4 or CRC6 procedures
- Insertion and extraction of alarms and facility signaling

Serial Interface to System Internal Highway

- System clock frequency of either 4096 kHz or 8192 kHz
- Selectable 2048/4096 kbit/s system internal highway with programmable receive/transmit shifts
- Two-frame deep elastic receive memory for receive route clock wander and jitter compensation
- One frame elastic transmit memory (PCM 24 mode only) for transmit route clock wander and jitter compensation
- Two different time-slot assignment procedures in PCM 24 mode
- Support for different signaling schemes
- Channel loop back capabilities
- Channel parity error monitoring

Microprocessor Interface

- Parallel, demultiplexed microprocessor interface for random access to control and status registers
- Alarm interrupt capabilities
- Access to different signaling information:
  -Sn, Si-bits (register)
  -SN-bits (5 byte stack)
  -FDL bits with the possibility of mixed insertion
  -CCS, CAS-CC (common channel), CAS-BR (bit robbing) via 2/3 byte stacks
  with DMA/interrupt support
- Extensive test and diagnostic capabilities

General

- Advanced CMOS technology
- Low power consumption (<100 mW)
- Packaging: 40-pin DIP/DIC, 44-pin PL-CC

Important Remarks

If it is planned to use future design versions of the ACFA (e.g. ACFA- VB1) which will meet newest CCITT recommendations and actual requirements of the market, SOFTWARE development should take into account that

- **unused control bits** have to be programmed with a **logical '0'**, although they are set to logical '1' when reading the assignend registers,
- future design versions will have **more status bits** than now,
- future design versions **will no longer** support the **HDB3 Full Error Detection** mode.

Introduction; (PEB 2035; Version B)

In addition to the features of PEB 2035 (ACFA) version A, the version B includes functions which meet the newest CCITT and FTZ recommendations plus some additional features requested by the market.

The most important new functions are the clear channel capability (PCM 24) and the extented support of the synchronization algorithm recommended by FTZ (PCM 30, Deutsche Bundespost).

There are no differences in packaging, pin functions or hardware interfaces between the ACFA's version A and version B.

General

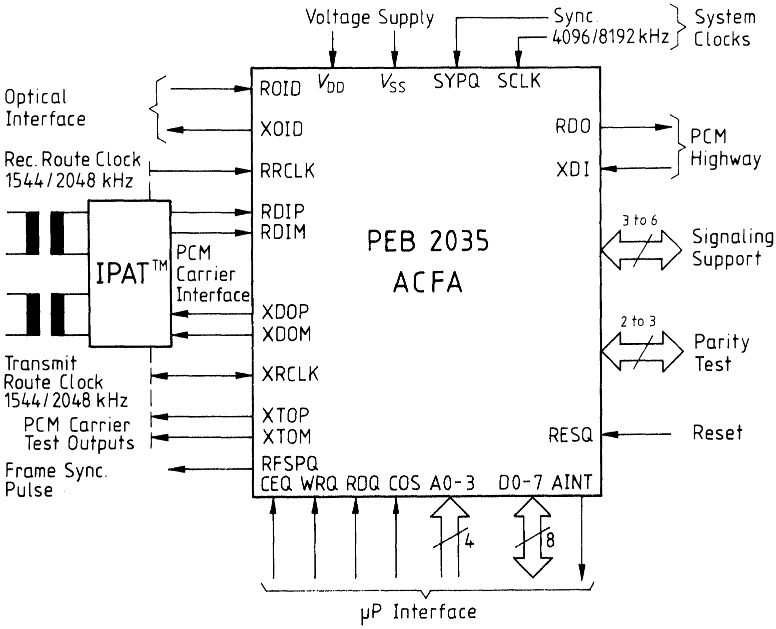
Additions to PCM 30 Mode

- Slip direction indication [RSR.SDI].
- Extended HDB3 error detection ['0000' string detection, CCR.EXTD]. HDB3 full detection mode no longer supported.
- Indication of a CRC error in received submultiframes [SEI.SI1, SEI.SI2] and selectable automatic insertion in Si bit position of outgoing CRC multiframe [XSP.AXS].
- Multiframe synchronous updating of Si bit information.
- Additional alarm interrupt sources for start of transmit and receive CRC multiframes [XSP.MXMB,XSP.MRMB] in conjunction with auto-reset multiframe status flags enable multiframe synchronous access to Si and Sn bit information.
- Extension of CRC error counting (switchable 10-bit counter) simplifies CRC error limit detection [CECX,CE8,CECX.CE9,RC0.ECE].
- Two transparent modes for time-slot 0 in transmit direction [XSP.TT0,XSP.TT0S] extend test capabilities and access to Sn and Si bit information via the system interface.
- Improved sychronization procedures.
- Single frame mode [LOOP.SFM] of receive speech memory for short data delays in master/slave applications.
- Error on receive line [ARS.ERL] flags that signals at line inputs RDIP, RDIM) are both active. This alarm may occur if line interface unit (e.g. PEB 2235, IPAT) detects bad signal levels on receive line.
- Repeated transmission of the signaling information (last byte of XSIG, transmit signaling stack) simplifies realization of HDLC procedures via board processor.

Additions to PCM 24 Mode

- Clear channel capabilities for applications in mixed voice/data or data-only environments, especially when using bit robbing signaling schemes and pure AMI line coding with zero code suppression (B7 stuffing). Selection of 'clear' channels is done by programming three byte register bank CCB1 ... CCB3 [enabled by CPY.SWTCH].
- Extension of CRC error counting (switchable 10-bit counter) simplifies CRC error limit detection [CECX,CE8, CECX.CE9, RC0.ECE].
- Error on receive line [ARS.ERL] flags that signals at line inputs RDIP, RDIM are both active. This alarm may occur if line interface unit (e.g. PEB 2235, IPAT) detects bad signal levels on receive line.
- Repeated transmission of the last signaling information (last byte of XSIG, transmit signaling stack) simplifies realization of HDLC procedures via board processor.

Logic Symbol

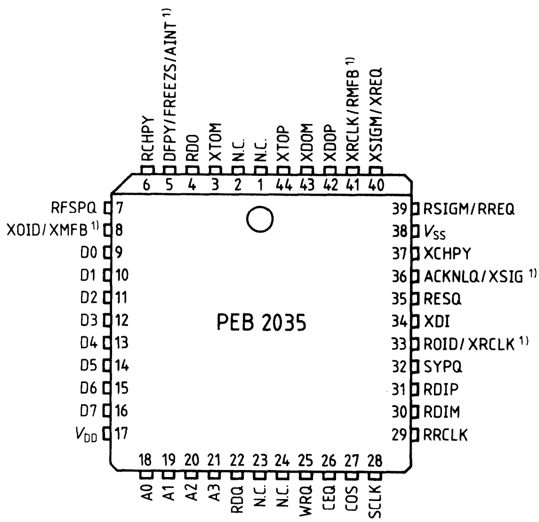


ISDN Primary Access Transceiver (IPAT) PEB 2235 for receive line clock recovery, TTL/line voltage translation and pulse shaping.

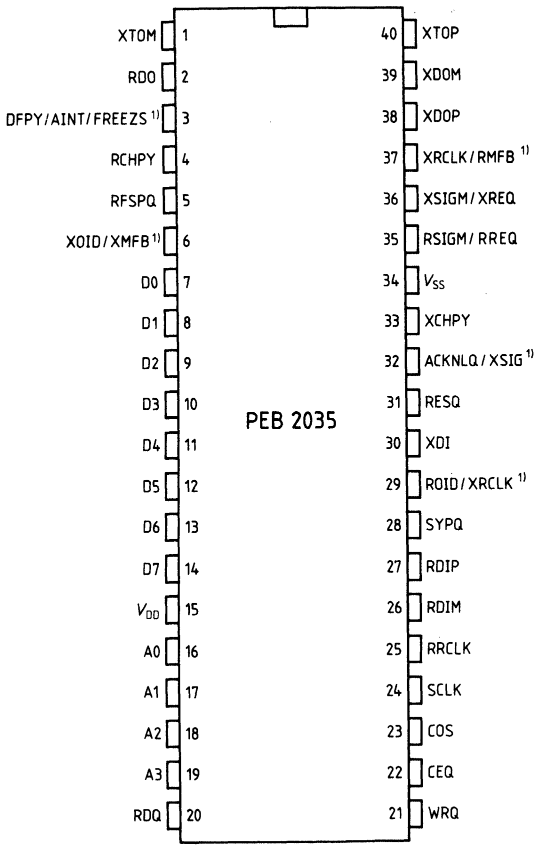
Note: Some pins have mode dependent functions and thus may appear more than once in the logic symbol.

Pin Configurations
(top view)

PL-CC-44



P-DIP-40



1) The function of the pin is mode dependent (2048/1544 kbit/s PCM)

Pin Definitions and Functions

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
44 3	40 1	XTOP XTOM	O	**Transmit Text Data OUT Plus** **Transmit Test Data OUT Minus** **PCM** (+) and **PCM** (–) output signals which may be used for diagnostic loopback. Data will continue to be transmitted during AIS transmission at XDOP/XDOM. The line code is determined by the bits MODE.PMOD and MODE.CODE. Output sense is selected via bit XC0.XTDS (after RESET: active low). Timing specifications are equivalent to XDOP/XDOM.
4	2	RDO	O	**Receive Data OUT** Received data which is sent to the system internal highway with 4096 kbit/s or 2048 kbit/s (bit MODE.IMOD). Data is clocked with the falling edge of SCLK. The delay between the beginning of time-slot 0 and the initial edge of SCLK (after SYPQ goes active) is determined by the values of Receive Time-slot Offset RC1.TRO and Receive Clock Offset RC0.RCO. Additionally for PCM 24, the time-slot assignment between route and system side is selected via bit MODE.CTM.
5	3	DFPY FREEZS AINT	O	**PCM 30: Doubleframe Parity** Every parity signal which supplements the number of ones of a received doubleframe to an even quantity. The parity signal is sent out during the following doubleframe (data changes four SCLK cycles before the next doubleframe begins). **PCM 24: Freeze Signaling** Synchronization status signal which informs the signaling processor that current signaling should be frozen. This signal goes actife if – one or more framing bit errors are found in a superframe, – loss or receiver synchronization, or – a receipe slip is detected It is cleared after an error-free superframe. FREEZS will be inhibited by setting bit RC0. DFRZ. During alarm simulation, this signal goes active during simulation steps 2 and 6 if not disabled via RCO.DFRZ.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
5	3	AINT	O	**Alarm Interrupt** Setting bit CCR.AINT switches the output to the Alarm Interrupt function. It is triggered by any of the alarm sources which are enabled via register MASK. Acknowledging is done by writing a "1" to bit LOOP.AIA.
6	4	RCHPY	O	**Receive Channel Parity** Even/Odd parity signal which supplements the number of ones of a received channel to an even/odd quantity while sending channel data to output RDO. The parity type is programmed by bit RCO.RPYS.
7	5	RFSPQ	O	**Receive Frame Synchronous Pulse** (Active Low) Framing pulse derived from the received PCM route signal. During loss of synchronization (bit RSR.LOS), this pulse is suppressed (not influenced during alarm simulation). Pulse Frequency: 8 kHz Pulse Width: 488 ns [PCM 30] 648 ns [PCM 24]
8	6	XOID/ XMFB	O	**PCM 30: Transmit Optical Interface Data** Unipolar NRZ data sent to fiber optical interface with 2048 kbit/s. The output sense is programmed via bit XCO.XDOS. Data is clocked with the rising edge of XRCLK. **PCM 24: Transmit Multiframe Begin** Marks the beginning of every transmitted superframe (used for synchronizing). Additional pulses are provided which mark – frame 13 of the ESF-format to allow access to the data link channel. The flag MRF.XMB marks the multiframe begin. – every 12 frames when using the F72 format. The additional status flag MFR.XRS marks the beginning of the DL-channel. The pulses which are normally two frames long may be reset by writing a "1" to the acknowledge bit XFDL.XMAK.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function Bus
9 10 11 12 13 14 15 16	7 8 9 10 11 12 13 14	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Data Bus** 8-bit bi-directional tristate data lines which interface with the system's data bus. These lines carry data and control/status information to and from the ACFA.
17	15	V_{DD}	I	**Power** +5 V Power Supply
18 19 20 21	16 17 18 19	A0 A1 A2 A3	I	**Address Bus** These inputs interface with four lines of the system's address bus to select one of the internal registers. Write access to address "0E" and "0F" is not allowed.
22		RDQ	I	**Read Enable** (Active Low) This signal indicates a read operation. If both CEQ and RDQ are active, status information of the registers selected via A0-A3 will be read from the ACFA. If access to the internal signaling stacks is enabled by setting bit XC0.ISIG, the data from the stack: RSIG may be read when ACKNLQ and RDQ are active.
25	21	WRQ	I	**Write Enable** (Active Low) This signal indicates a write operation. If both CEQ and WRQ are active control information may be written to the registers selected via A0-A3. If access to the internal signaling stacks is enabled by setting bit XC0.ISIG data may be written to the stack XSIG when ACKNLQ and WRQ are active.
26	22	CEQ	I	**Chip Enable** (Active Low) A low signal enables normal read/write access to the internal registers.
27	23	COS	I	**Carrier OUT of Service** A high signal at this input enables transmission of AIS via outputs XDOP, XDOM, and XOID without any framing structure.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
28	24	SCLK	I	**System Clock** Working clock for the ACFA with a frequency of 4096 kHz or 8192 kHz (selected by bit MODE.SCLK)
29	25	RRCLK	I	**Receive Route Clock** Extracted from the incoming data pulses by the line interface unit (e.g., IPAT, PEB 2235). Clock Frequency: 2048 kHz [PCM 30] 1544 kHz [PCM 24]
30 31	26 27	RDIM RDIP	I	**Receive Data in Minus** **Receive Data in Plus** Inputs for received dual rail PCM (+) and PCM (–) route signals which will be latched on negative transitions of RRCLK. Input sense is selected by bit RC0.RDIS (after RESET: active low). Signal decoding depends on the PCM mode selected via bit MODE.PMOD: - PCM 30: HDB3 line code with 2048 kbit/s - PCM 24: If optical interface mode is disabled the selected line code with 1544 kbit/s depends on bit MODE.CODE (B8ZS or AMI with B7 stuffing). After enabling optical interface mode via bit MODE.OPT port RDIP will be switched to input for single rail unipolar data. In this case, port RDIM has no function.
32	28	SYPQ	I	**Synchronous Pulse** Defines the beginning of time-slot 0 at system highway ports RDO, and XDI in conjunction with the values of registers RC0.RCO, RC1.RTO, CX0.CXO, and XC1.XTO. Pulse Cycle: Integer multiple of 125 μs.
33	29	ROID	I	**PCM 30: Receive Optical Interface Data** Unipolar data received from fiber optical interface with 2048 kbit/s. The input sense is programmed via bit RC0.RDIS. Data is clocked on the falling edge of RRCLK if optical interface mode is enabled via bit MODE.OPT.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
33	29	XRCLK	I	**PCM 24: Transmit Route Clock** Input for 1544 kHz transmit route clock provided from an external clock generator. To avoid transmit slips it must be phase locked to a common submultiple of the system clock SCLK such as 8 kHz. In case of an error condition reported via bit ASR.XSLP the transmit time-slot counter has to be set to its initial start position by programming its offset value XC1.XTO.
34	30	XDI	I	**Transmit Data IN** Transmit data received from the system internal highway with 4096 kbit/s or 2048 kbit/s (bit MODE.IMOD). Data is clocked on the falling edge of SCLK. The delay between the beginning of time slot 0 and the initial edge of SCLK (after SYPQ goes active) is determined by the values of Transmit Time-Slot Offset XC1.XTO and Transmit Clock-Slot Offset XC0.XCO. Additionally, for PCM 24 the channel/time slot correspondence between route and system side ist selected via bit MODE.CTM.
35	31	RESQ	I	**RESET** (Active Low) A low signal will initialize all internal flipflops. The ACFA is switched to PCM 30 mode. All output stages are tristated while RESQ is active.
36	32	ACKNLQ	I	**DMA Acknowledge** (Active Low) If access to internal signaling stacks is enabled via bit XCO.ISIG this input acts as an "access enable" to the internal stacks RSIG and XSIG in conjunction with a read/write command without the need of generating the chip enable signal CEQ. In this case is should be connected to the acknowledge output of the DMA controller to enable I/O-to-memory transfers. **PCM 30** No function if XCO.ISIG is set to "0". In that case this input has to be fixed either to V_{DD} or to V_{SS}.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
36	32	XSIG	I	**PCM 24: Transmit Signaling Data** If XCO.ISIG is set to "0" the external signaling mode is enabled. This port acts as input for the signaling data requested by the marker XSIGM. Data is clocked on the falling edge of SCLK. If not used port XSIG should be tied to port XDI.
37	33	XCHPY	I	**Transmit Channel Parity** Externally generated even/odd parity signal which supplements the number of ones of each transmit channel on XDI to an even/odd quantity. Latching of data on XCHPY is coincident with latching of the LSB (bit 8) of the corresponding time slot if the external transmit channel parity mode is enabled via bit XCO.EPY. The parity type is programmed by bit XC0.EPYS. **NOTE:** To avoid difficulties for external parity generation the parity signal related to channels with signaling information is adjusted internally.
38	34	V_{SS}	I	**GND** (0 V)
39	35	RSIGM	O	**Receive Signaling Marker** – **PCM 30:** Marks time slot 16 of every received frame at pin RDO. – **PCM 24:** When using CCS or CAS-CC signaling schemes (bit MODE.SIGM = 0) RSIGM marks a) time slot 31 (speech channel 24) in channel translation mode 0 (bit MODE.CTM = 0) b) time slot 23 (speech channel 24) in channel translation mode 1. Setting bit FMR.SM24 shifts the marker to time slot 16 (speech channel 17). When using the CAS-BR signaling scheme, every six frames the robbed bit of each channel is marked.

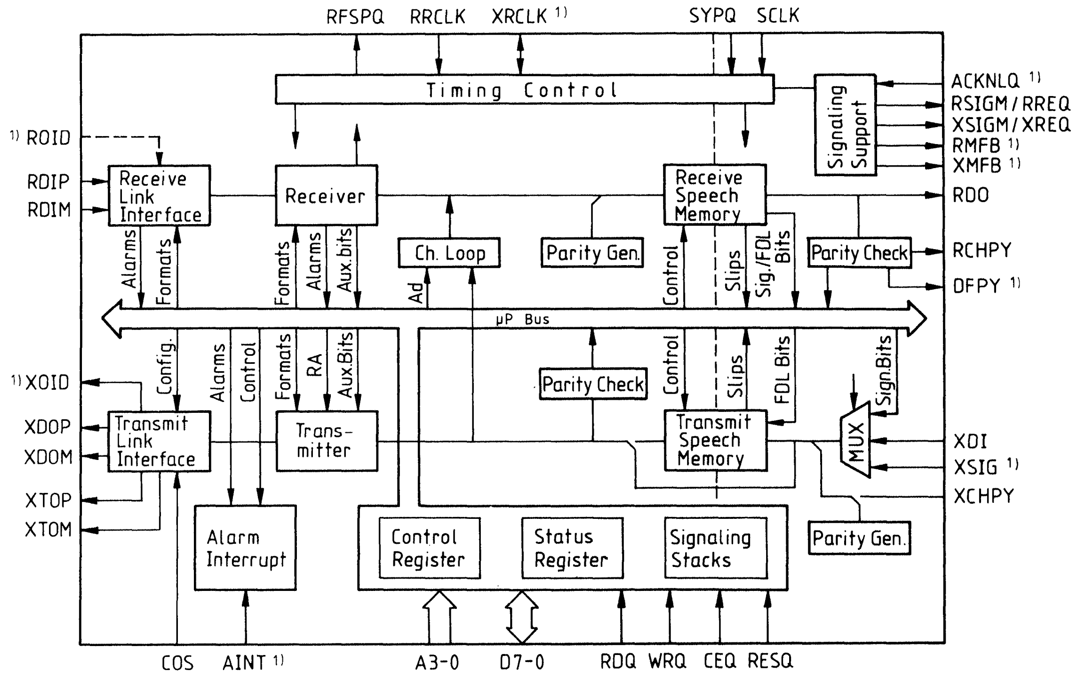
Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
39	35	RREQ	O	**Receive Request** If access to the internal signaling stacks RSIG and XSIG is enabled via bit XC0.ISIG, this pin acts as a DMA or interrupt request. It requires the controller to read the stack RSIG. RREQ will be held active until the first read access to RSIG is finished. It will be generated – **PCM 30:** once a double frame – **PCM 24:** every three frames in CCS/CAS-CC mode, or once a signaling frame (every six frames) at CAS-BR mode. The output will be cleared with the first read access to RSIG.
40	36	XSIGM/ XREQ	O	**Transmit Signaling Marker** Its function is equivalent to RSIGM for the data stream at ports XDI and XSIG (XSIG: PCM 24 mode only). **Transmit request** Its function is equivalent to RREQ for writing data to the stack XSIG.
41	37	XRCLK/ RMFB	O	**PCM 30: Transmit Route Clock** 2048 kHz clock derived from the internal clock of 4086 kHz. **PCM 24: Receive Multiframe Begin** Marks the beginning of every received super-frame (used for synchronizing). Additional pulses are provided which mark – frame 13 of the ESF format to allow access to the data link channel. The flag MFR.RMB marks the multiframe begin. – every 12 frames when the F72 format is used. The additional status flag MFR.RRS signals that the first six bits of the DL-channel have been received (RMFB goes active with the beginning of frame 37 of the F72 multiframe). The pulses which normally are two frames long may be reset by writing a "1" to the acknowledge bit XFDL.RMAK.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
42	38	XDOP	O	**Transmit Data OUT Plus**
43	39	XDOM		**Transmit Data OUT Minus** Outputs for transmitted dual rail PCM (+) and PCM (–) route signals which will be clocked on rising edge of XRCLK. Output sense is selected by bit XC0.XDOS (after RESET: active low). Signal encoding depends on the selected PCM mode (MODE.PMOD): – **PCM 30:** HDB3 line code with 2048 kbit/s – **PCM 24:** If optical interface mode is disabled the selected line code with 1544 kbit/s depends on programming bit MODE.CODE (B8ZS or AMI with B7 stuffing). After enabling optical interface mode via bit MODE.OPT port XDOP will be switched to output single rail unipolar data with 100% duty cycle.

Block Diagram



The ACFA comprises complete paths for receive and transmit direction for connecting the primary access line interface unit to the system internal PCM highway:

The receive/transmit link interface with encoder/decoder and alarm detectors connects the ACFA to the line interface unit (e.g. IPAT, PEB 2235).

The receiver/transmitter perform frame alignment/synthesis, CRC checking/generation, alarm and signaling extraction/insertion.

The receive/transmit speech memory compensates the wander and jitter of the assigned route clock. Time-slot assigment to the system internal highway is also handled via this memory.

The parallel microprocessor interface can be used for controlling and monitoring of all functions and alarms as well as extraction and insertion of signaling data. Additionally, a Direct Memory Access (DMA) interface and bundel of specific signals enable powerfull support for a varity of possible external signaling controllers.

Functional Description

General Functions and Device Architecture

1 Receive Path

Receive Link Interface

For data input, two different data types with selectable input sense are supported:

- Dual rail data (PCM[+], PCM[–]) at ports RDIP, RDIM received from a line interface unit (e.g. PEB 2235, Siemens ISDN Primary Access Transceiver, IPAT)
- Unipolar data at port ROID (PCM 30) or at port RDIP (PCM 24) received from a fibre optical interface.

Latching of data is done using the falling edges of the Receive Route Clock (RRCLK, 2048 kHz or 1544 kHz) recovered from the PCM receive data stream. Dual rail data is subsequently converted into a single rail, unipolar bit stream. In PCM 30 mode, the HDB3 line code is used along with double violation detection or full code violation detection (selectable). In PCM 24 mode, a selection between B8ZS or simple AMI (ZCS) coding is provided. In this case, all code violations that do not correspond to zero substitution rules will be detected.

These errors increment the code violation counter.

When using the unipolar input mode, the decoder is by-passed and no code violations will be detected.

Additionally, the receive link interface comprises the alarm detection for AIS (Alarm Indication Signal: unframed bit stream with constant logical 'one') and NOS (no signal: input signal with an insufficient bit rate or an insufficient density of ones).

The single rail bit stream is then processed by the receiver.

Receiver

For both the PCM 30 mode and the PCM 24 mode the following functions are performed:

- Synchronization on pulse frame
- Synchronization on multiframe
- Error indication when synchronization is lost. In this case, AIS is sent to the system side.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This may be automatically done by the ACFA, or user controlled via the microprocessor interface.
- Detection of remote alarm indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Generation of control signals to synchronize the CRC checker, the parity generator, and the receive speech memory write control unit.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC submultiframe (or ESF multiframe) according to either the CRC 4 procedure (PCM 30, refer to CCITT Rec. G704 § 2.3.3) or the CRC 6 procedure (PCM 24, refer to CCITT Rec. G704 § 3.1.1.3). These bits are compared with those check bits that are received during the next CRC (sub-)multiframe. If there is at least one mismatch, the CRC error counter will be incremented.

Receive Speech Memory

The speech memory is organized as a two-frame elastic buffer with a size of 64 x 9 bit or 48 x 9 bit for PCM 30 or PCM 24, respectively (8-bit channel data plus one parity bit).

The functions are:

- Clock adaption between system clock (SCLK) and route clock (RRCLK).
- Compensation of input wander and jitter. Maximum of wander amplitude:
  PCM 30: 95 UI (1 UI = 488 ns)
  PCM 24: 63 UI in channel translation mode 0
  39 UI in channel translation mode 1
  (1 UI = 644 ns)
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, channel-serial data which is circularly written to the speech memory using the receive route clock (RRCLK). At the same time, a parity signal is generated over each channel and also stored in the speech memory.

Reading of stored data is controlled by the system clock (SCLK) and the synchronous pulse (SYPQ) in conjunction with the programmed offset values for the receive time-slot/ clock-slot counters. After conversion into a serial data stream and parity checking (errors are reported via the status registers), the data is given out via port RDO. Channel parity information is output at port RCHPY with selectable output sense. In PCM 24 mode, two channel translation modes are provided (refer to § 2.3.4). Unequipped time-slots will be set to 'FF' hex. For both PCM modes, two bit rates (2048/4096 kbit/s) are selectable via the microprocessor interface.

A slip condition is detected when the write address pointer and the read address pointer of the speech memory are nearly coincident. In this case, a negative slip (the next received frame is skipped) or a positive slip (the previous received frame is read out twice) is performed, depending on the difference between RRCLK and SCLK.

2 Transmit Path

The inverse functions are performed for the transmit direction.

The PCM data is received from the system internal highway at port XDI with 2048 kbit/s or 4096 kbit/s. The channel assignment is equivalent to the receive direction. All unequipped time-slots will be ignored. Latching of data is controlled by the system clock (SCLK) and the synchronous pulse (SYPQ) in conjunction with the programmed offset values for the transmit time slot/clock-slot counters.

Transmit Speech Memory

The transmit speech memory is operational only in the PCM 24 mode. This one-frame elastic buffer with a size of 24 x 9 bit (8-bit channel data plus 1 parity bit) serves as a temporary store for the PCM data to adapt the system clock (SCLK) to the externally generated transmit route clock (XRCLK), and to re-translate channel structure used in the system to that of the line side. Its optimal start position is initiated when programming the above offset values. Normally, XRCLK has to be phase locked to a common submultiple of SCLK such as 8 kHz. A difference in the effective data rates of system side and transmit side may lead to an overflow/underflow of the transmit speech memory: thus, errors in data transmission to the remote end may occur. This error condition (transmit slip) is reported to the microprocessor via the status registers. It signals that the external clock generation is defective.

Maximum wander amplitude in PCM 24 mode:

- Channel translation mode 0: 29 UI
- Channel translation mode 1: 23 UI

(1 UI = 644 ns)

Because this is, under normal circumstances, a rare error condition no automatic action is taken by the transmit speech memory as opposed to the receive speech memory in the case of a positive or negative slip. In this case the ACFA requires a re-initialization of the transmit memory by re-programming of the transmit time-slot counter. After that, this memory has its optimal start position.

In PCM 30 mode, the transmit route clock (XRCLK) is derived directly from the system clock by an internal clock divider. Consequently, the data received from the system interface is switched through without the need of intermediate storage.

The parity generation/checking mechanism is symmetrical to the receive path. The channel data is checked with the channel parity information generated internally or externally (input at port XCHPY with selectable input sense). Errors are reported to the microprocessor interface. To avoid difficulties with external parity generation, the parity signal for non-speech data (e.g. signaling data or channels with bit robbing information) is computed internally.

Transmitter

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the six selectable framing formats
- Insertion of service and data link information
- Remote alarm generation

Transmit Link Interface

Similar to the receive link interface two different data types with selectable output sense are supported:

- Dual rail data (PCM[+], PCM[–]) at ports XDOP, XDOM with 50% duty cycle transmitted to a line interface unit (e.g. PEB 2235, Siemens ISDN Primary Access Transceiver, IPAT). Single rail data is converted into a dual rail bit stream. In PCM 30 mode, the HDB3 line code is employed. In PCM 24 mode, selection between B8ZS or simple AMI coding with zero code suppression (B7 stuffing) is provided.
- Unipolar data at port XOID (PCM 30) or at port XDOP (PCM 24) with 100% duty cycle transmitted to a fibre optical interface.

Clocking of data is done with the positive transitions of the transmit route clock: XRCLK (2048 kHz or 1544 kHz). In PCM 30 mode, XRCLK is generated by the ACFA, whereas in PCM 24 mode it must be generated by an external clock generator.

Additionally, the dual rail outputs XTOP and XTOM are provided for test applications.

3 Additional Functions

Signaling Support

Generation of all supporting signals to achieve simple access to signaling information (CCS, CAS-CC, CAS-BR, FDL) at the system interface. In PCM 24 mode, the additional input XSIG is provided for connection to a bit-robbed signaling controller. Furthermore, the controlling of the internal signaling stacks is done by this unit.

Alarm Interrupt

Normally, the control of data transmission via the PCM line is done by polling the internal status registers of the ACFA at equidistant time intervals.

However, for fast error handling the option exists to configure a specific output port as interrupt port (AINT). This signal may be connected to an interrupt input of the board processor. Triggering of this output may be caused by up to eight maskable interrupt sources.

Single Channel Loop Back

As one of the extended test options, the single channel loop back enables reflection of a selected channel back to the system interface at port RDO.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 V to V_{DD} +0.4 V	V

DC Characteristics

$T_A = 0$ to $70\,°C$; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V	
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} −0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$
Power supply current	I_{CC}		18	mA	$V_{DD} = 5$ V Inputs at 0 V/V_{DD}, no output loads
Input leakage current Output leakage current	I_{LI} I_{LO}		10	μA	$0\ V < V_{IN} < V_{DD}$ to 0 V $0\ V < V_{OUT} < V_{DD}$ to 0 V

Characteristics

$T_A = 25\,°C$; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}	5	10	pF
Output capacitance	C_{OUT}	10	20	pF
I/O	C_{IO}	8	15	pF

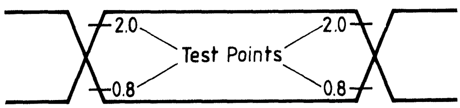
AC Characteristics

$T_A = 0$ to $70\,°C$; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$

Inputs are driven to 2.4 V for a logical '1' and to 0.4 V for a logical '0'. Timing measurements are made at 2.0 V for a logical '1' and at 0.8 V for a logical '0'.

The AC testing input/output waveforms are shown in the **figure 1**.

Figure 1
Input/Output Waveform for AC Tests

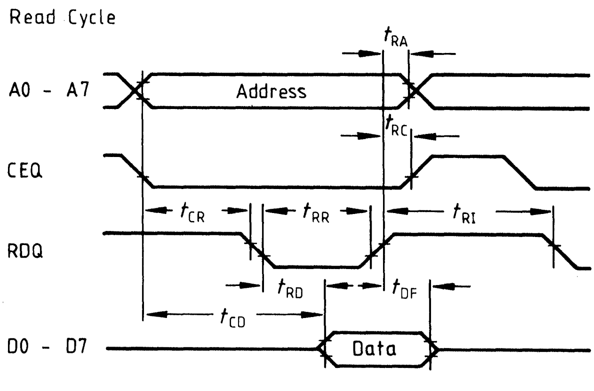


Output load: 150 pF load capacitance in connection with resistive loads for $I_{OL} = 2$ mA and $I_{OH} = -100$ uA.

Rise/fall times: 20 ns max.

µP Interface Timing

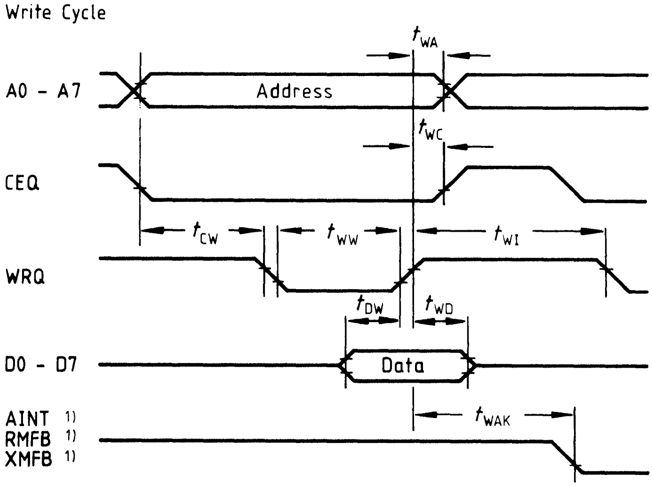
Figure 2
µP Read Timing



µP Read Timing

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
CEQ and ADDRESS valid to DATA valid	t_{CD}		120	ns
CEQ and ADDRESS stable before RDQ	t_{CR}	0		ns
RDQ to DATA valid	t_{RD}		110	ns
RDQ pulse width	t_{RR}	120		ns
DATA float after RDQ	t_{DF}	10	30	ns
CEQ hold after RDQ	t_{RC}	0		ns
ADDRESS hold after RDQ	t_{RA}	0		ns
RDQ control interval	t_{RI}	70		ns

Figure 3
µP Write Timing

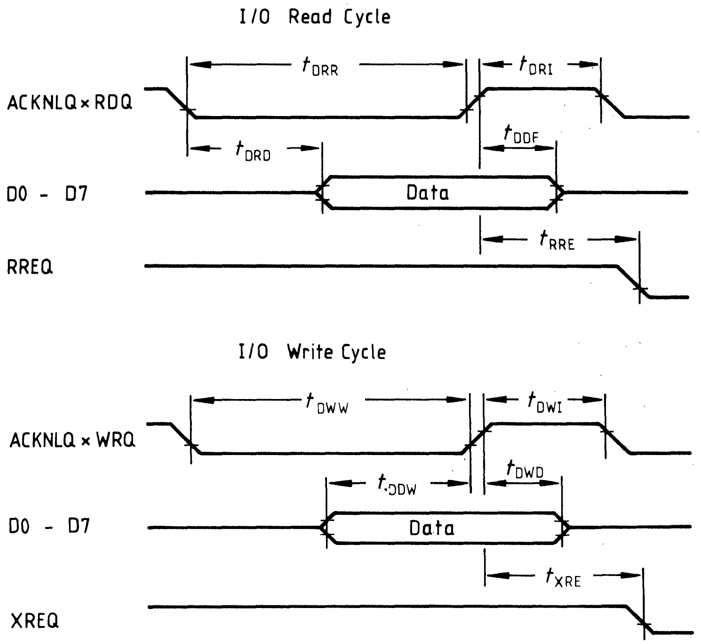


1) : In connection with assigned values of A0-A3 and D0-D7

µP Write Timing

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
CEQ and ADDRESS valid to WRQ valid	t_{CW}	30		ns
DATA setup before end of write	t_{DW}	30		ns
DATA hold after WRQ	t_{WD}	10		ns
WRQ pulse width	t_{WW}	70		ns
CEQ hold after WRQ	t_{WC}	10		ns
ADDRESS hold after WRQ	t_{WA}	10		ns
WRQ control interval	t_{WI}	70		ns
Interrupt acknowledge delay	t_{WAK}		$2 \times t_{CP4} + 60$ $4 \times t_{CP8} + 80$	ns

Figure 4
DMA Timing

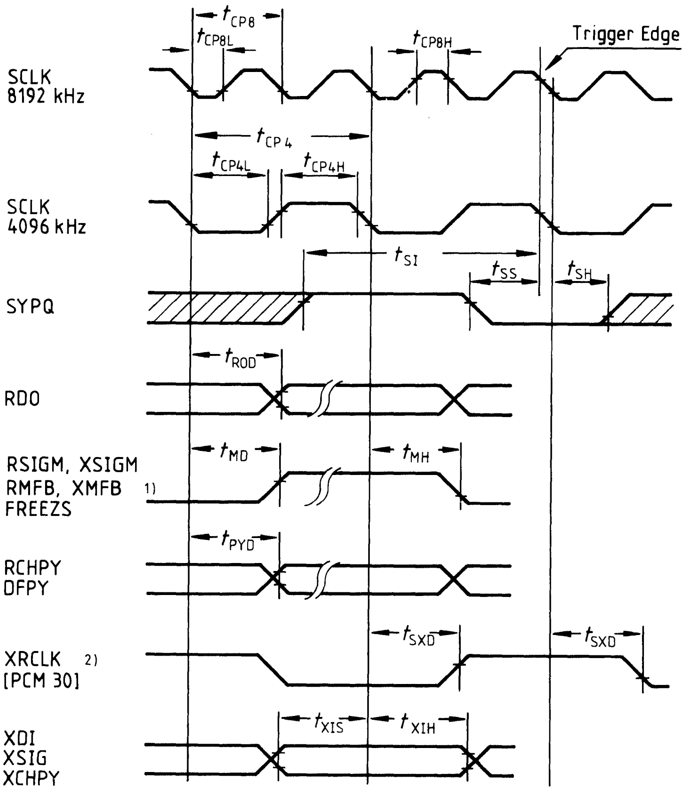


DMA Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RDQ to DATA valid	t_{DRD}		110	ns
DATA float after RDQ	t_{DDF}	10	30	ns
RDQ pulse width	t_{DRR}	120		ns
RDQ control interval	t_{DRI}	70		ns
RREQ reset after RDQ	t_{RRE}		130	ns
DATA setup before end of write	t_{DDW}	30		ns
DATA hold after WRQ	t_{DWD}	10		ns
WRQ pulse width	t_{DWW}	70		ns
WRQ control interval	t_{DWI}	70		ns
XREQ reset after WRQ	t_{XRE}		130	ns

Serial Interface Timing

Figure 5
System Interface Timing



1) : If not Reset via µP Interface

2) : For Even Values of XCO.XCO, Otherwise Inverted

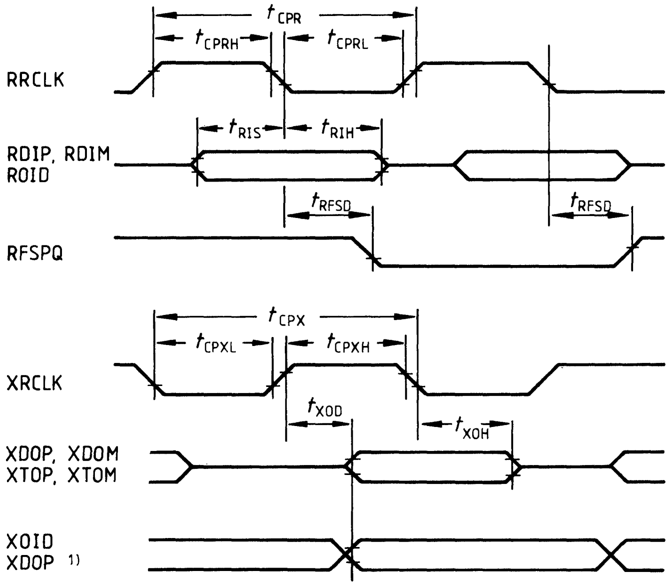
System Interface Timing

Parameter	Symbol	Limit Values				Unit
		4096 kHz SCLK		8192 kHz SCLK		
		min.	max.	min.	max.	
SCLK period 8 MHz	t_{CP8}			typ. 122		ns
SCLK period 8 MHz low	t_{CP8L}			40		ns
SCLK period 8 MHz high	t_{CP8H}			40		ns
SCLK period 4 MHz	t_{CP4}	typ. 244				ns
SCLK period 4 MHz low	t_{CP4L}	110				ns
SCLK period 4 MHz high	t_{CP4H}	110				ns
SYPQ setup time	t_{SS}	40	$t_{CP4} - 30$	$t_{CP8} - 40$	$t_{CP8} + 40$	ns
SYPQ hold time	t_{SH}	40		40		ns
SYPQ inactive setup	t_{SI}	$t_{CP4} + 30$		$2 x t_{CP8} + 30$		ns
RDO propagation delay	t_{ROD}		90		110	ns
Marker propagation delay	t_{MS}		100		120	ns
Marker hold	t_{MH}		100		120	ns
Parity propagation delay	t_{PYD}		100		120	ns
XRCLK to SCLK delay	t_{SXD}		110		130	ns
Transmit data setup	t_{XIS}	30		30		ns
Transmit data hold	t_{XIH}	30		30		ns

Reset Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RESQ low	t_{REL}	2000		ns

Figure 6
Line Interface Timing



1) : PCM 24, Optical Interface Mode

Line Interface Timing

Parameter	Symbol	Limit Values				Unit
		PCM 30		PCM 24		
		min.	max.	min.	max.	
RRCLK clock period	t_{CPR}	typ. 488		typ. 648		ns
RRCLK clock period low	t_{CPRL}	220		300		ns
RRCLK clock period high	t_{CPRH}	220		300		ns
Receive data setup	t_{RIS}	30		30		ns
Receive data hold	t_{RIH}	30		30		ns
RFSPQ propagation delay	t_{RFSD}		130		130	ns
XRCLK clock period	t_{CPX}	$2 \times t_{CP4}$ $4 \times t_{CP8}$		typ. 648		ns
XRCLK clock period low	t_{CPXL}			300		ns
XRCLK clock period high	t_{CPXH}			300		ns
Transmit data output delay	t_{XOD}		50		90	ns
Transmit data output hold	t_{XOH}	0*	50	20*	90	ns

* Test conditions: 0 °C, C_L = 50 pF