SIEMENS

ICs for Communications

Advanced CMOS Frame Aligner
ACFA

PEB 2035

Data Sheet 01.94

PEB 2035 **Revision History:** **Current Version: 01.94**		
Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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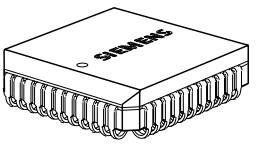
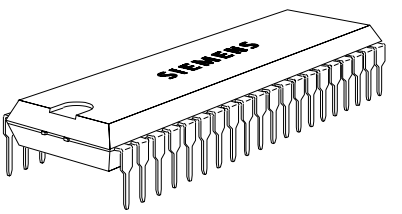
Advanced CMOS Frame Aligner (ACFA) PEB 2035

CMOS IC

1 Features



P-LCC-44



P-DIP-40

Serial Interface to Line Interface Unit

- Frame alignment/synthesis for 2048 kbit/s (CEPT, PCM 30) and 1544 kbit/s (T1, PCM 24)
- Meets newest CCITT Rec's (Blue Book), FTZ Rec's and AT&T technical advisories (DMI, August 1986)
- Programmable formats for
  PCM 30: Doubleframe, CRC Multiframe
  PCM 24: 4-Frame Multiframe (F4), 12-Frame Multiframe (F12, D3/4), Extended Superframe (ESF), Remote Switch Mode (F72)
- Selectable conditions for loss of sync
- Selectable line codes (HDB3, B8ZS, AMI with ZCS)
- Unipolar NRZ for interfacing fibre optical transmission routes
- Error checking via CRC4 or CRC6 procedures
- Insertion and extraction of alarms and facility signaling
- IDLE code insertion for selectable channels

Serial Interface to System Internal Highway

- System clock frequency of either 4096 kHz or 8192 kHz
- Selectable 2048/4096 kbit/s system internal highway with programmable receive/transmit shifts
- Two-frame deep elastic receive memory for receive route clock wander and jitter compensation (can be reduced to one-frame length for PCM 30 master-slave applications)
- One frame elastic transmit memory (PCM 24 mode only) for transmit route clock wander and jitter compensation
- Two different time-slot assignment procedures in PCM 24 mode
- Support for different signaling schemes
- Channel loop back capabilities
- Channel parity error monitoring
- Clear channel capabilities in PCM 24 mode

Type	Version	Ordering Code	Package
PEB 2035-N	V4.1	Q67100-H6289	P-LCC-44 (SMD)
PEB 2035-P	V4.1	Q67100-H6290	P-DIP-40

Microprocessor Interface

- Parallel, demultiplexed microprocessor interface for random access to control and status registers
- Alarm interrupt capabilities
- Access to different signaling information:
  – S_a-, E, S_i -bits (register)
  – S_a-bits (5-byte stack)
  – FDL bits with the possibility of mixed insertion
  – CCS, CAS-CC (common channel), CAS-BR (bit robbing) via 2/3-byte stacks with DMA/ interrupt support
- Extensive test and diagnostic capabilities

General

- Advanced CMOS technology
- Low power consumption (< 100 mW)
- Packaging: P-DIP-40, P-LCC-44

1.1 Introduction

The Advanced CMOS Frame Aligner PEB 2035 (ACFA) is a monolithic CMOS device which implements the interface to primary rate PCM carriers. It may be programmed to operate in 24-channel (T1) and 32-channel (CEPT) carrier systems.

The ACFA features include: selectable multiframe (six multiframe formats), error checking (CRC4, CRC6), multiple line codes (HDB3, B8ZS, AMI), and programmable signaling paths. The device includes functions which meet newest CCITT (Blue Book) and FTZ recommendations for primary rate interfaces and the AT&T Digital Multiplexed Interface specifications (DMI) plus some additional features requested by the market. Controlling and monitoring of the device is performed via a parallel eight-bit microprocessor bus.

The circuit contains a two-frame elastic memory which ensures wander absorption between the PCM carrier and a synchronous, system internal highway.

All signaling types - CCS, CAS and bit-robbed signaling in conjunction with Clear Channel Capability - are supported by the ACFA. In addition, the ACFA allows flexible access to facility data link and service channels. Extensive testing capabilities are included.

The ACFA is suitable for a wide range of voice and data applications. Below you find a list of equipment as described by the CCITT which potential ACFA applications.

2048 kbit/s Applications

– PCM Multiplex equipment according to G.732, G.735, G.738.
– Digital Multiplex equipment according to G.736
– Digital Multiplex equipment according G.742, G745
– External Access equipment according to G.737, G.739
– Digital Exchange equipment according to G.705, Q.511, Q512
– Transmultiplex equipment according to G.793

– Video Conferencing according to H120, H130
– Transcoder equipment according to G.761
– Digital circuit multiplication equipment according to G.763
– Digital section/line system according to G.921, G.952, G.956

1544 kbit/s

– PCM Multiplex equipment according to G.733
– Digital Multiplex equipment according to G.734
– Digital Multiplex equipment according G.743
– Digital Exchange equipment according to G.705, Q.511, Q512
– Transmultiplex equipment according to G.793
– Video Conferencing according to H.120, H.130
– Transcoder equipment according to G.762
– Digital circuit multiplication equipment according to G.763
– Digital section/line system according to G.951, G.955
– ADPCM multiplex equipment according to G.724

The ACFA is available in either P-DIP-40 or P-LCC-44 packages. As with all of the ISDN circuits from Siemens, the ACFA has been implemented in advanced CMOS technology. Total power consumption is less than 100 mW.

– External Access equipment according to G.739

Conventions

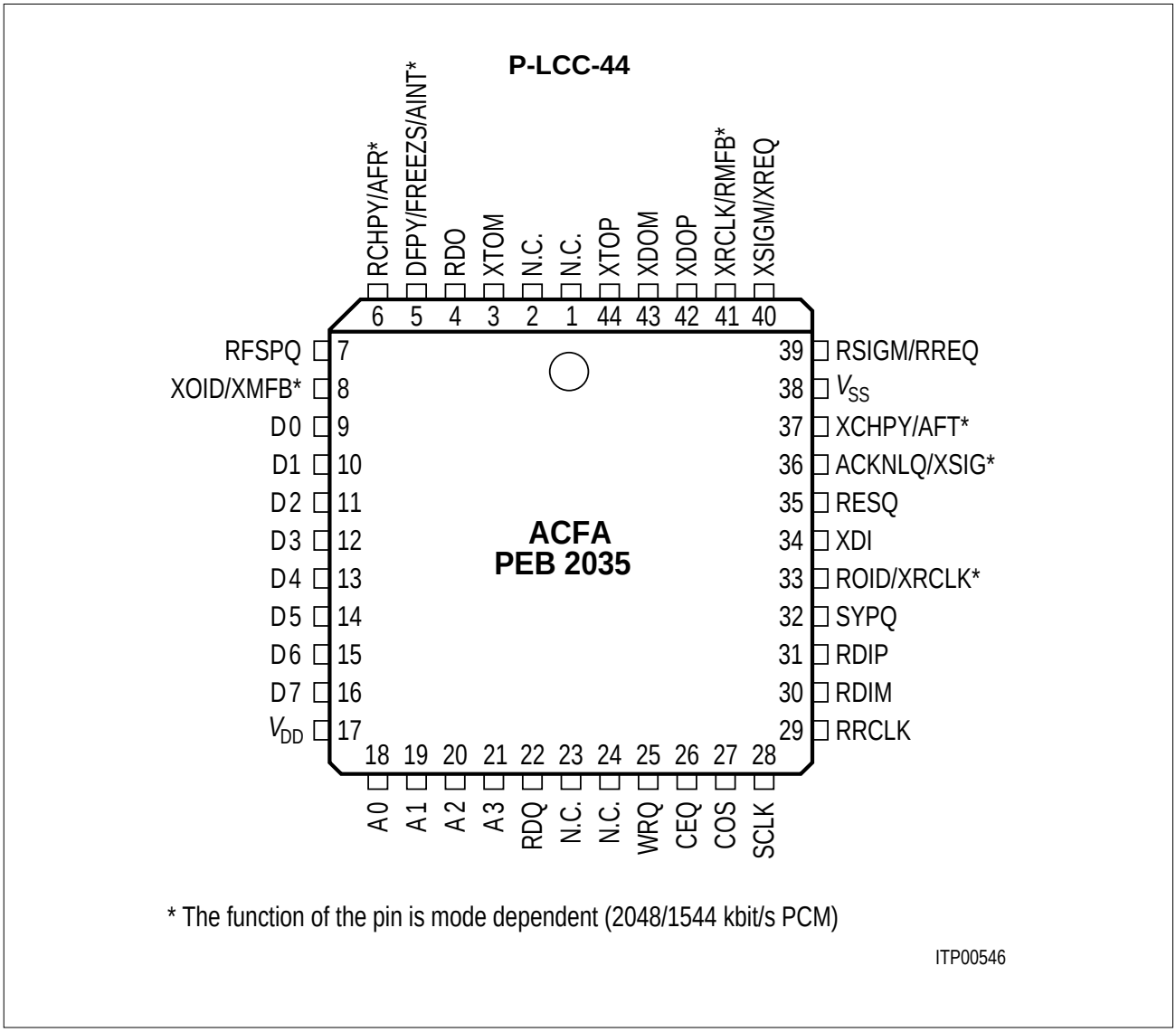
Register bits are designated in the text as follows: X.Y, where X is the register name and Y is the bit of that register in question (e.g. MODE.PMOD). PCM mode specific functions are marked with **PCM 30** or **PCM 24**.

In chapters 1, 2, 4 and 5 all additional features of the version 4

– in comparison to the PEB 2035 version B are marked with a black line, and
– in comparison to the PEB 2035 version 3 (version C) are marked with a grey line.

1.2 Pin Configurations

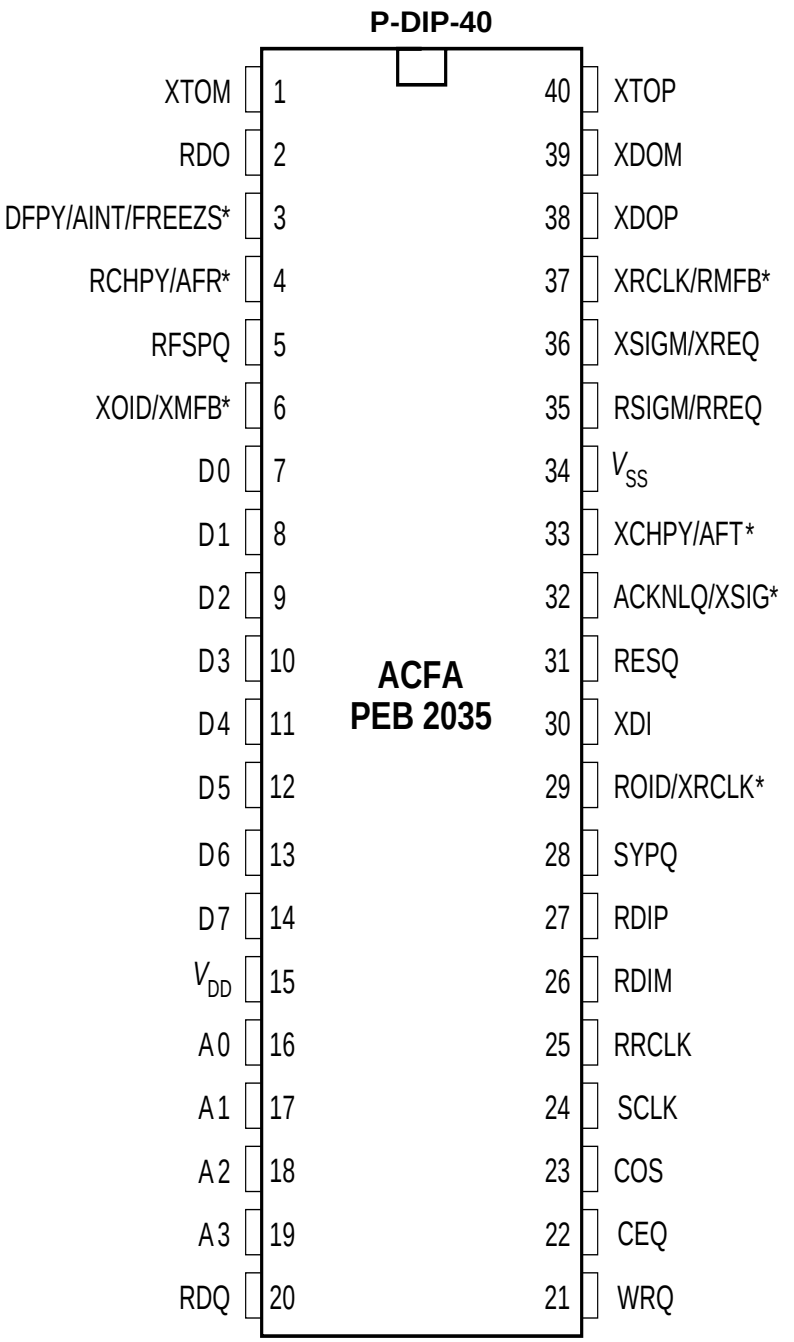
(top view)



* The function of the pin is mode dependent (2048/1544 kbit/s PCM)

ITP00546

Pin Configurations (cont'd)
(top view)



*The function of the pin is mode dependent (2048/1544 kbit/s PCM)

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1.3 Pin Definitions and Functions

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
44 3	40 1	XTOP XTOM	O O	**Transmit Test Data Out Plus** **Transmit Test Data Out Minus** PCM(+) and PCM(–) output signals which may be used for diagnostic loopback. Data will continue to be transmitted during AIS transmission via XDOP/ XDOM. The line code is determined by the bits MODE.PMOD and MODE.CODE. Output sense is selected via bit XC0.XTDS (after RESET: active low). Timing specifications are equivalent to XDOP/XDOM.
4	2	RDO	O	**Receive Data Out** Received data which is sent to the system internal highway with 4096 kbit/s or 2048 kbit/s (bit MODE.IMOD). Clocking off data is done with the falling edge of SCLK. The delay between the beginning of time-slot 0 and the initial edge of SCLK (after SYPQ goes active) is determined by the values of Receive Time-slot Offset RC1.RTO5 … 0 and Receive Clock-slot Offset RC0.RCO2 … 0. Additionally for PCM 24, the time-slot assignment between route and system side is selected via bit MODE.CTM.

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
5	3	DFPY / FREEZS / AINT	O	**PCM 30: Doubleframe Parity** Even parity signal which supplements the number of ones of a received doubleframe to an even quantity. The parity signal is sent out during the following doubleframe (data changes 4 SCLK cycles before the next doubleframe begins). **PCM 24: Freeze Signaling** Synchronization status signal which informs the signaling processor that current signaling should be frozen. It goes active if – one or more framing bit errors are found in a superframe, – loss of receiver synchronization, or – a receive slip is detected. It is cleared after an error-free superframe. FREEZS will be inhibited by setting bit RC0.DFRZ. During alarm simulation, this signal goes active during simulation steps 2 and 6 if not disabled via RCO.DFRZ. **Alarm Interrupt** Setting bit CCR.AINT switches the output to the Alarm Interrupt function. It is triggered by any of the alarm sources which are enabled via mask bits. Acknowledging is done by writing a '1' to bit LOOP.AIA.

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
6	4	RCHPY / AFR	O	**Receive Channel Parity** Even/odd parity signal which supplements the number of ones of a received channel to an even/ odd quantity while sending channel data to output RDO. The parity type is programmed by bit RC0.RPYS. **PCM 24: Additional Function Receive** If enabled via bit ACR.DLC, this output provides a 4-kHz signal which marks the DL-bit position within the data stream on RDO. It can be used as receive strobe signal for external data link controllers.
7	5	RFSPQ	O	**Receive Frame Synchronous Pulse** (active low) Framing pulse derived from the received PCM route signal. During loss of synchronization (bit RSR.LOS), this pulse is suppressed (not influenced during alarm simulation). Pulse frequency: 8 kHz Pulse width: 488 ns [PCM 30] 648 ns [PCM 24]

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
8	6	XOID / XMFB	O	**PCM 30: Transmit Optical Interface Data** Unipolar data sent to fibre optical interface with 2048 kbit/s. The output sense is programmed via bit XC0.XDOS. Clocking off data is done with the rising edge of XRCLK with 100 % duty cycle. **PCM 24: Transmit Multiframe Begin** The function depends on programming bit ACR.MFBS: **MFBS = 1**: XMFB marks the beginning of every transmitted multiframe (XDI). **MFBS = 0**: Marks the beginning of every transmitted superframe. Additional pulses every 12 frames are provided when using ESF or F72 format. Status bits MFR.XMB and MFR.XRS specify multiframe begin and the beginning of the DL channel (F72 only). In both cases the pulses which normally are two frames long can be reset by writing a '1' to the acknowledge bit XFDL.XMAK. **Note**: If signal AFT is supplied for 'External Multiframe Synchronization' and a **new** multiframe position is enforced, signal XMFB may be (for one time) three or four frames long before the new multiframe position has been settled.
9 10 11 12 13 14 15 16	7 8 9 10 11 12 13 14	D0 D1 D2 D3 D4 D5 D6 D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Data Bus** 8-bit bi-directional tristate data lines which interface with the system's data bus. These lines carry data and control/status information to and from the ACFA.
17	15	V_{DD}	I	**Power** + 5 V power supply

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
18 19 20 21	16 17 18 19	A0 A1 A2 A3	I I I I	**Address Bus** These inputs interface with four lines of the system's address bus to select one of the internal registers. Write access to address '0E' and '0F' is not allowed.
22	20	RDQ	I	**Read Enable** (active low) This signal indicates a read operation. If both CEQ and RDQ are active, status information of the registers selected via A0 … A3 will be read from the ACFA. If access to the internal signaling stacks is enabled by setting bit XC0.ISIG, the data from the stack: RSIG may be read when ACKNLQ and RDQ are active.
25	21	WRQ	I	**Write Enable** (active low) This signal indicates a write operation. If both CEQ and WRQ are active control information may be written to the registers selected via A0 … A3. If access to the internal signaling stacks is enabled by setting bit XC0.ISIG data may be written to the stack XSIG when ACKNLQ and WRQ are active.
26	22	CEQ	I	**Chip Enable** (active low) A low signal enables normal read/write access to the internal registers.
27	23	COS	I	**Carrier Out of Service** A high signal at this input enables transmission of AIS via outputs XDOP, XDOM, and XOID without any framing structure.
28	24	SCLK	I	**System Clock** Working clock for the ACFA with a frequency of 4096 kHz or 8192 kHz (selected by bit MODE. SCLK)
29	25	RRCLK	I	**Receive Route Clock** Extracted from the incoming data pulses by the line interface unit (e.g. IPAT, PEB 2235/PEB 2236). Clock frequency: 2048 kHz [PCM 30] 1544 kHz [PCM 24]

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
30 31	26 27	RDIM RDIP	I I	**Receive Data In Minus** **Receive Data In Plus** Inputs for received dual rail PCM(+) and PCM(–) route signals which will be latched on negative transitions of RRCLK. Input sense is selected by bit RC0.RDIS (after RESET: active low). Signal decoding depends on the PCM mode selected via bit MODE.PMOD: – **PCM 30**: HDB3 line code with 2048 kbit/s. – **PCM 24**: If optical interface mode is disabled the selected line code with 1544 kbit/s depends on bit MODE.CODE (B8ZS or AMI with B7 stuffing). After enabling optical interface mode via bit MODE.OPT port RDIP will be switched to input for single rail unipolar data. In this case, port RDIM has no function.
32	28	SYPQ	I	**Synchronous Pulse** Defines the beginning of time-slot 0 at system highway ports RDO, and XDI in conjunction with the values of registers RC0.RCO, RC1.RTO, XC0.XCO, and XC1.XTO. Pulse Cycle: Integer multiple of 125 µs.
33	29	ROID / XRCLK	I	**PCM 30: Receive Optical Interface Data** Unipolar data received from fibre optical interface with 2048 kbit/s. The input sense is programmed via bit RC0.RDIS. Latching of data is done with the falling edge of RRCLK if optical interface mode is enabled via bit MODE.OPT. **PCM 24: Transmit Route Clock** Input for 1544-kHz transmit route clock provided from an external clock generator. To avoid transmit slips it must be phase locked to a common submultiple of the system clock SCLK such as 8 kHz. In case of an error condition reported via bit ASR.XSLP the transmit time-slot counter has to be set to its initial start position by programming its offset value XC1.XTO5 … 0.

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
34	30	XDI	I	**Transmit Data In** Transmit data received from the system internal highway with 4096 kbit/s or 2048 kbit/s (bit MODE.IMOD). Latching of data is done with negative transitions of SCLK. The delay between the beginning of time-slot 0 and the initial edge of SCLK (after SYPQ goes active) is determined by the values of transmit time-slot offset XC1.XTO5 … 0 and transmit clock-slot offset XC0 . XCO2 … 0. Additionally, for PCM 24 the channel/time-slot correspondence between route and system side is selected via bit MODE.CTM.
35	31	RESQ	I	**Reset** (active low) A low signal will initialize all internal flip flops. The ACFA is switched to PCM 30 mode. All output stages are tristated while RESQ is active.
36	32	ACKNLQ / XSIG	I	**DMA Acknowledge** (active low) If access to internal signaling stacks is enabled via bit XCO.ISIG this input acts as an 'access enable' to the internal stacks RSIG and XSIG in conjunction with a read/write command without the need of generating the chip enable signal CEQ. In this case it should be connected to the acknowledge output of the DMA controller to enable IO-to-memory transfers. **PCM 30** No function if XCO.ISIG is set to '0'. In that case this input has to be fixed either to V_{DD} or to V_{SS}. **PCM 24: Transmit Signaling Data** If XCO.ISIG is set to '0' the external signaling mode is enabled. This port acts as input for the signaling data requested by the marker XSIGM. Latching of data is done with negative transitions of SCLK. If not used port XSIG should be tied to port XDI.

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
37	33	XCHPY / AFT	I	**Transmit Channel Parity** Externally generated even/odd parity signal which supplements the number of ones of each transmit channel on XDI to an even/odd quantity. Latching of data on XCHPY is coincident with latching of the LSB (bit 8) of the corresponding time-slot if the external transmit channel parity mode is enabled via bit XCO.EPY. The parity type is programmed by bit XC0.EPYS. **NOTE**: To avoid difficulties for external parity generation the parity signal related to channels with signaling information is adjusted internally.
			I/O	**PCM 24: Additional Function Transmit** If enabled via bit ACR.DLC (bit ACR.EXMF = 0), this **output** provides a 4 kHz signal which marks the DL-bit position within the data stream on XDI. It can be used as transmit strobe signal for external data link controllers. Additionally, this port can operate as **input** for External Transmit Multiframe Synchronization which defines frame 1 of the Multiframe on XDI (ACR.EXMF = 1, ACR.DLC = x). Minimum pulse length is 244 ns. Latching is done equivalent to latching data via XDI. The signal has to be issued during frame 1 and has to be reset at least one bit before begin of frame 2. Recommended: AFT begins with the first bit of time-slot 0, frame 1 of XDI. **Notes**: A new multiframe position has been settled at least one multiframe after pulse AFT has been supplied. If old and new multiframe position differ from each other, signal XMFB may be up to four frames long. Moreover, if stack XSIG is enabled (DMA mode), a re-initialisation for DMA transmit direction is recommended.
38	34	V_{SS}	I	**Ground** (0 V)

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
39	35	RSIGM / RREQ	O	**Receive Signaling Marker** – **PCM 30**: Marks time-slot 16 of every received frame at port RDO. – **PCM 24**: When using CCS or CAS-CC signaling schemes (bit MODE.SIGM = 0) RSIGM marks a) Time-slot 31 (speech channel 24) in channel translation mode 0 (bit MODE.CTM = 0) b) Time-slot 23 (speech channel 24) in channel translation mode 1. Setting bit FMR.SM24 shifts the marker to time-slot 16 (speech channel 17). When using the CAS-BR signaling scheme, the robbed bit of each channel every six frames is marked. **Receive Request** If access to the internal signaling stacks RSIG and XSIG is enabled via bit XC0.ISIG, this port acts as a DMA or interrupt request. It requires the controller to read the stack RSIG.RREQ will be held active until the first read access to RSIG is finished. It will be generated – **PCM 30**: once a doubleframe – **PCM 24**: every three frames in CCS/CAS-CC mode, or once a signaling frame (every six frames) at CAS-BR mode. In dependance of bit EMOD.EDMA signal RREQ will be cleared – EDMA = 0: at the end of the first read access to stack RSIG (rising edge of RDQ); – EDMA = 1: with the beginning of the second (PCM 30) or third (PCM 24) read access to stack RSIG (falling edge of RDQ).

1.3 Pin Definitions and Functions (cont'd)

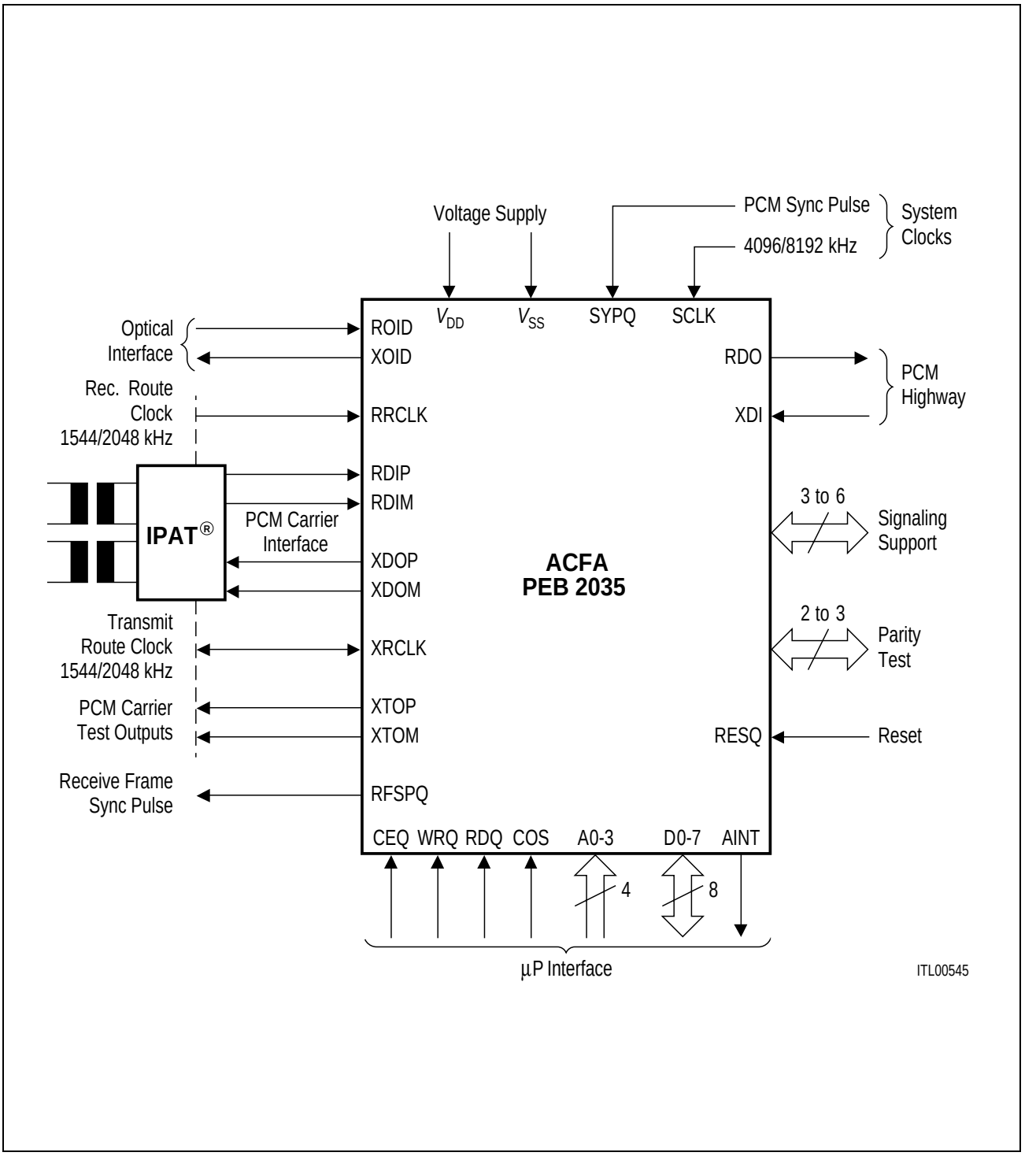
P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
40	36	XSIGM / XREQ	O	**Transmit Signaling Marker** Its function is equivalent to RSIGM for the data stream at ports XDI and XSIG (XSIG: PCM 24 mode only). **Transmit Request** Its function is equivalent to RREQ for writing data to the stack XSIG. In dependance of bit EMOD.EDMA signal XREQ will be cleared – EDMA = 0: at the end of the first write access to stack XSIG (rising edge of WRQ); – EDMA = 1: with the beginning of the second (PCM 30) or third (PCM 24) write access to stack XSIG.XREQ is reset with the falling edge of ACKNLQ or CEQ and remains reset if a write cycle to stack XSIG follows. Otherwise, it becomes active again until the second or third access to XSIG is provided.

1.3 Pin Definitions and Functions (cont'd)

P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
41	37	XRCLK / RMFB	O	**PCM 30: Transmit Route Clock** 2048-kHz clock derived from the internal clock of 4096 kHz. **PCM 24: Receive Multiframe Begin** The function depends on programming bit ACR.MFBS: MFBS = 1: RMFB marks the beginning of every received multiframe (RDO). MFBS = 0: Marks the beginning of every received superframe. Additional pulses every 12 frames are provided when using ESF or F72 format. Status bits MFR.RMB and MFR.RRS specify multiframe begin and the beginning of the DL channel (F72 only). In both cases the pulses which normally are two frames long can be reset by writing a '1' to the acknowledge bit XFDL.RMAK.

1.3 Pin Definitions and Functions (cont'd)

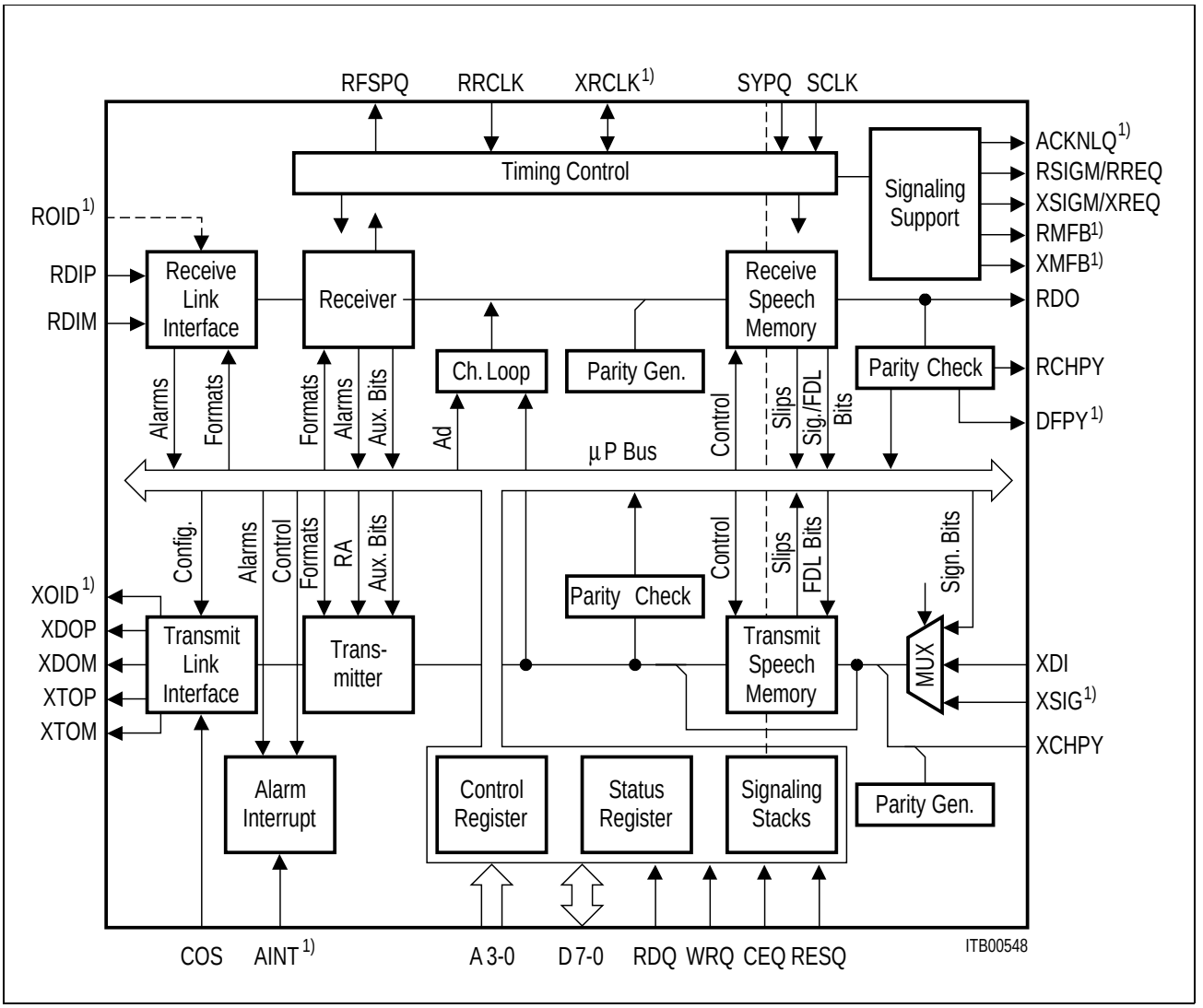
P-LCC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
42 43	38 39	XDOP XDOM	O O	**Receive Channel Parity Transmit Data Out Plus Transmit Data Out Minus** These outputs for transmitted dual rail PCM(+) and PCM(–) route signals can provide – half bauded signals with 50 % duty cycle (bit EMOD.XFB = 0), or – full bauded signals with 100 % duty cycle (bit EMOD.XFB = 1). The data will be clocked off on positive transitions of XRCLK in both cases. Output sense is selected by bit XC0.XDOS (after RESET: active low). Signal encoding depends on the selected PCM mode (MODE.PMOD): – **PCM 30**: HDB3 line code with 2048 kbit/s – **PCM 24**: If optical interface mode is disabled the selected line code with 1544 kbit/s depends on programming bit MODE.CODE (B8ZS or AMI with B7 stuffing). After enabling optical interface mode via bit MODE.OPT port XDOP will be switched to output single rail unipolar data with 100 % duty cycle.



Logic Symbol

(*) ISDN Primary Access Transceiver (IPAT®) PEB 2235/PEB 2236 for receive line clock recovery, TTL/line voltage translation and pulse shaping.

Note: Some pins have mode dependent functions and thus may appear more than once in the logic symbol.



Block Diagram

The ACFA comprises complete paths for receive and transmit direction for connecting the Primary Access Line Interface Unit to the system internal PCM highway:

The Receive/Transmit Link Interface with encoder/decoder and alarm detectors connects the ACFA to the Line Interface Unit (e.g. IPAT, PEB 2235/PEB 2236).

The Receiver/Transmitter perform frame alignment/synthesis, CRC checking/generation, alarm and signaling extraction/insertion.

The Receive/Transmit Speech Memory compensates the wander and jitter of the assigned route clock. Time-slot assignment to the system internal highway is also handled via this memory.

The parallel microprocessor interface can be used for controlling and monitoring of all functions and alarms as well as extraction and insertion of signaling data. Additionally, a Direct Memory Access (DMA) interface and bundel of specific signals enable powerful support for a varity of possible external signaling controllers.

2 System Integration

The Advanced CMOS Frame Aligner provides the interface between a primary rate PCM (T1 or CEPT) transmission line and any digital system that connects to a 2048- or 4096-kbit/s PCM highway. An example is given in **figure 1**, where the system interface is handled by a space-time switch, in this case the Siemens PEB 2045 (MTSC). This figure shows an optimized implementation of a complete Primary Access Interface (with CCS signaling) consisting of four CMOS circuits:

ACFA: Advanced CMOS Frame Aligner
HSCX: High-Level Serial Communication Controller Extended
MTSC: Memory Time Switch CMOS
IPAT: ISDN Primary Access Transceiver

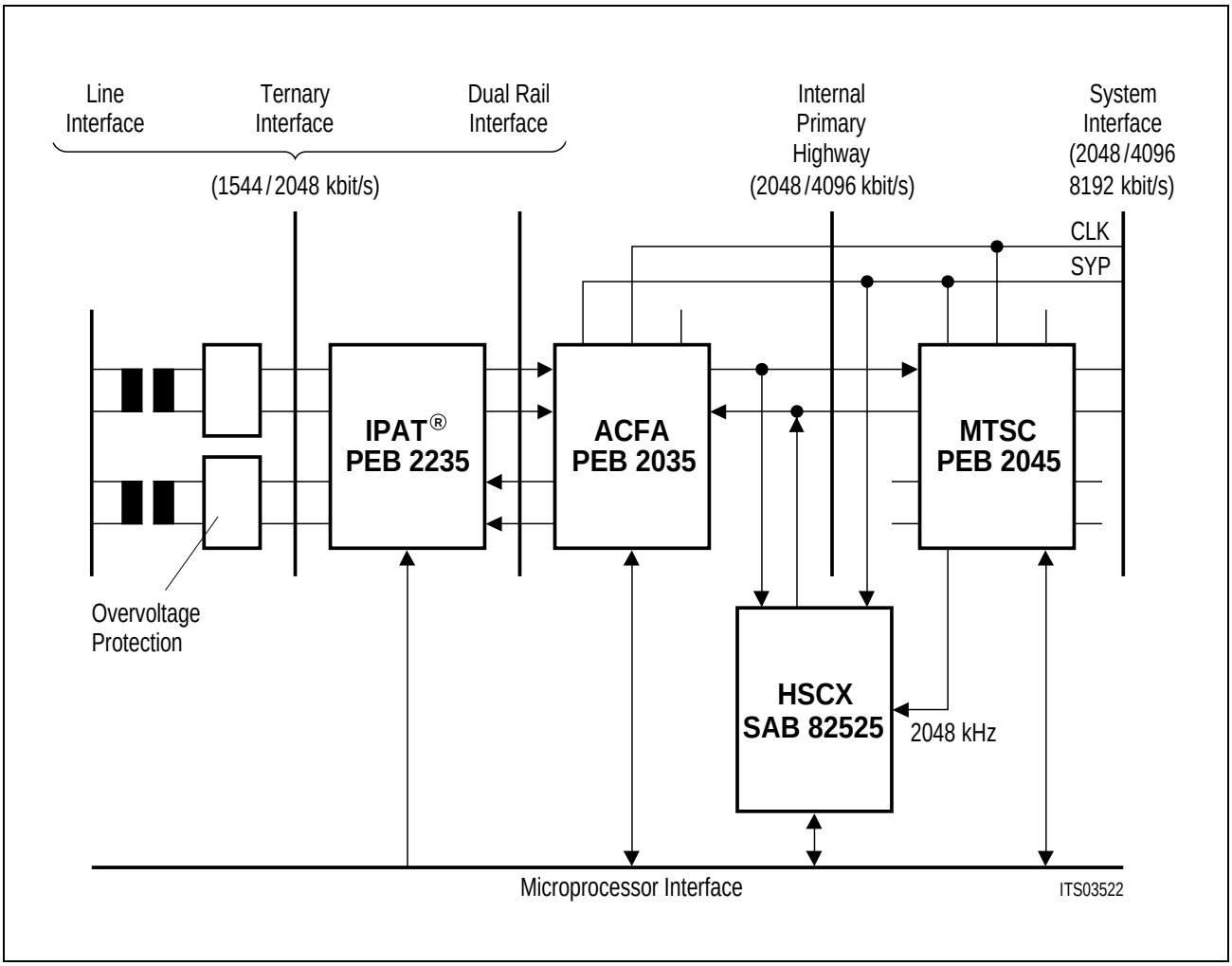


Figure 1
Primary Access Interface

The ACFA provides several ways of accessing the signaling data which it extracts from/inserts into the PCM carrier data stream. The example in **figure 1** shows a case where signaling is sent to the system internal highway in one of the (otherwise) unequipped time-slots, to be processed by an autonomous signaling controller. In the case of message oriented common channel signaling

(CCS), an integrated solution is provided by the CMOS High-Level Serial Communication Controller HSCX (SAB 82525).

This controller is able to extract and insert signaling messages in programmable one-bit steps up to 256-bit time-slots, and thus requires no extra hardware.

Since the CMOS Memory Time Switch is a switch for 256-output channels and the HSCX is actually a dual channel controller, a quad primary access interface unit with non-blocking switch requires only 11 devices:

4	ACFA	PEB 2035
4	IPAT	PEB 2235
2	HSCX	SAB 82525
1	MTSC	PEB 2045,

as shown in **figure 2**.

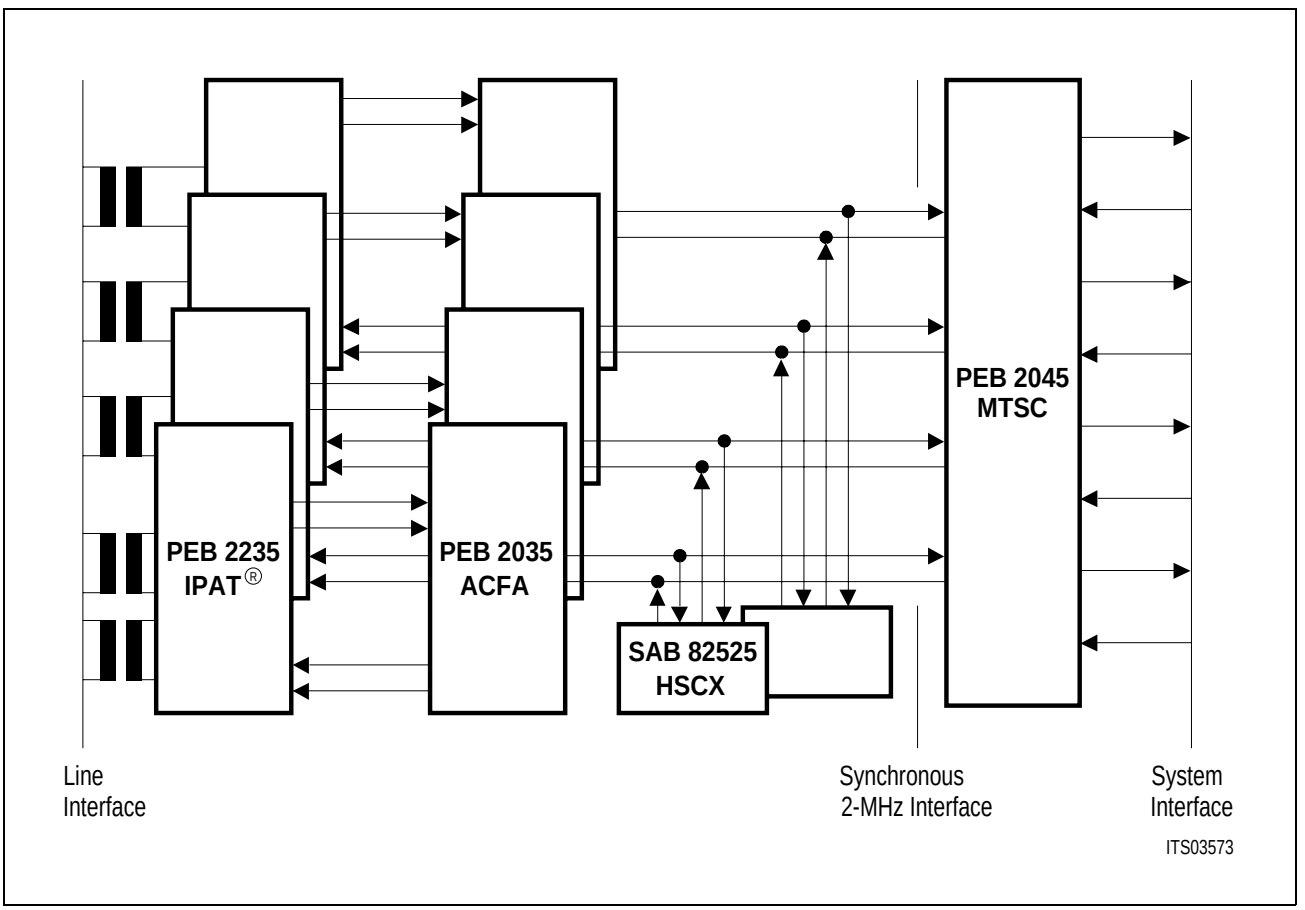


Figure 2
Quad Primary Access Interface

3 Functional Description

General Functions and Device Architecture

1. Receive Path

Receive Link Interface
For data input, two different data types with selectable input sense are supported:

- Dual rail data (PCM[+], PCM[–]) at ports RDIP, RDIM received from a line interface unit (e.g. PEB 2235/PEB 2236, Siemens ISDN Primary Access Transceiver, IPAT).
- Unipolar data at port ROID (PCM 30) or at port RDIP (PCM 24) received from a fibre optical interface.

Latching of data is done using the falling edges of the Receive Route Clock (RRCLK, 2048 kHz or 1544 kHz) recovered from the PCM receive data stream. Dual rail data is subsequently converted into a single rail, unipolar bit stream. In PCM 30 mode, the HDB3 line code is used along with double violation detection or extended code violation detection (selectable). In PCM 24 mode, a selection between B8ZS or simple AMI (ZCS) coding is provided. In this case, all code violations that do not correspond to zero substitution rules will be detected.
These errors increment the code violation counter (8 or 10 bits length).

Note: In PCM 30 mode, this counter can also be used to count sub-multiframe error indications instead of code violations.

When using the unipolar input mode, the decoder is by-passed and no code violations will be detected.

Additionally, the receive link interface comprises the alarm detection for AIS (Alarm Indication Signal: unframed bit stream with constant logical 'one') and NOS (No Signal: input signal with an insufficient bit rate or an insufficient density of ones).

The single rail bit stream is then processed by the receiver.

Receiver
For both the PCM 30 mode and the PCM 24 mode the following functions are performed:

- Synchronization on pulse frame
- Synchronization on multiframe
- Error indication when synchronization is lost. In this case, AIS is automatically sent to the system side (this function can be disabled).
- Initiating and controlling of resynchronization after reaching the asynchronous state. This may be automatically done by the ACFA, or user controlled via the microprocessor interface.
- Detection of remote alarm indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Generation of control signals to synchronize the CRC checker, the parity generator, and the receive speech memory write control unit.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC submultiframe (or ESF multiframe) according to either the CRC 4 procedure (PCM 30, refer to CCITT Rec. G704) or the CRC 6 procedure (PCM 24, refer to CCITT Rec. G704). These bits are compared with those check bits that

are received during the next CRC (sub-)multiframe. If there is at least one mismatch, the CRC error counter will be incremented. As addition, this 8-bit counter (default) can be extended to 10-bit length.

As an extension of the alarm interrupt capabilities, the occurrence of a CRC error can be defined as interrupt source for triggering interrupt port AINT.

Receive Speech Memory

The speech memory is organized as a two-frame elastic buffer with a size of 64 × 9 bit (PCM 30) or 48 × 9 bit (PCM 24) 9 bit include 8-bit channel data plus one parity bit.

The functions are:

- Clock adaption between system clock (SCLK) and route clock (RRCLK).
- Compensation of input wander and jitter. Maximum of wander amplitude (peak-to-peak):
  PCM 30: 190 UI (1 UI = 488 ns)
  PCM 24: 126 UI in channel translation mode 0 (bit ACR.SLM reset)
  142 UI in channel translation mode 0 (bit ACR.SLM set)
  78 UI in channel translation mode 1
  (1 UI = 644 ns)
  For detailed information on the channel translation modes.
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, channel-serial data which is circularly written to the speech memory using the Receive Route Clock (RRCLK). At the same time, a parity signal is generated over each channel and also stored in the speech memory.

Reading of stored data is controlled by the System Clock (SCLK) and the Synchronous Pulse (SYPQ) in conjunction with the programmed offset values for the receive time-slot/clock-slot counters. After conversion into a serial data stream and parity checking (errors are reported via the status registers), the data is given out via port RDO. Channel parity information is output at port RCHPY with selectable output sense. In PCM 24 mode, two channel translation modes are provided. Unequipped time-slots will be set to 'FF' hex. For both PCM modes, two bit rates (2048/ 4096 kbit/s) are selectable via the microprocessor interface.

Figure 3 gives an idea of operation of the receive speech memory:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the write pointer is within the slip limits (S +, S –). The values of S + and S – depend on the selected PCM mode, on the channel translation mode and on the value of bit ACR.SLM. If a slip condition is detected, a negative slip (the next received frame is skipped) or a positive slip (the previous received frame is read out twice) is performed at the system interface, depending on the difference between RRCLK and SCLK, i.e. on the position of pointer R and W within the memory.

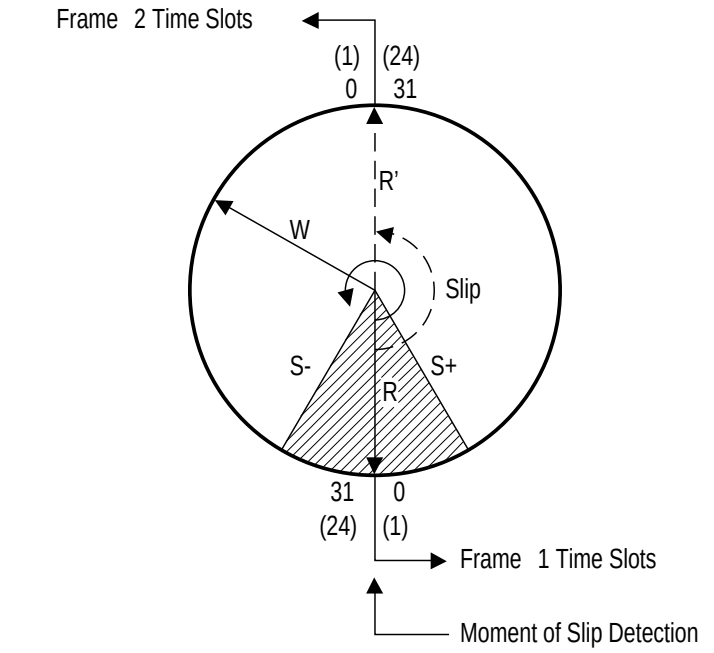


Figure 3
The Receive Speech Memory as Circularly Organized Memory

Additionally in PCM 30 mode the receive speech memory can be switched to one frame length (LOOP.SFM). This feature is useful for master-slave applications to reduce the delay between line interface and system interface. For correct operation, System Clock SCLK and Synchronous Pulse SYPQ have to be derived from the Receive Route Clock RRCLK and the Receive Frame Synchronous Pulse RFSPQ (PLL application). In single frame mode, however, it is not possible to perform a slip after the slip condition has been detected. Thus, values of receive time-slot/clock-slot offset (RC0, RC1) have to be specified great enough to prevent too great approach of frame begin (line side) and frame begin (system side).

2. Transmit Path

The inverse functions are performed for the transmit direction.

The PCM data is received from the system internal highway at port XDI with 2048 kbit/s or 4096 kbit/s. The channel assignment is equivalent to the receive direction. All unequipped time-slots will be ignored.

The contents of selectable channels (time-slots) can be overwritten by the pattern defined via register IDLE. The selection of 'idle channels' is done by programming the three/four-byte register bank ICB1 … ICB3, ICB4.
In PCM 24 mode, additional signaling information can be provided on a separate input (XSIG). Internal multiplexing of (speech) data and signaling data can be disabled on a per channel basis (Clear Channel Capability). This is also valid when using the internal signaling stack.

Latching of data is controlled by the System Clock (SCLK) and the Synchronous Pulse (SYPQ) in conjunction with the programmed offset values for the Transmit Time-slot/Clock-slot Counters.

Transmit Speech Memory

The transmit speech memory is operational only in the PCM 24 mode. This one-frame elastic buffer with a size of 24×9 bit (8 bit channel data plus 1 parity bit) serves as a temporary store for the PCM data to adapt the system clock (SCLK) to the externally generated Transmit Route Clock (XRCLK), and to re-translate channel structure used in the system to that of the line side. Its optimal start position is initiated when programming the above offset values. Normally, XRCLK has to be phase locked to a common submultiple of SCLK such as 8 kHz. A difference in the effective data rates of system side and transmit side may lead to an overflow/underflow of the transmit speech memory: thus, errors in data transmission to the remote end may occur. This error condition (transmit slip) is reported to the microprocessor via the status registers. It signals that the external clock generation is defective.

Maximum wander amplitude in PCM 24 mode (peak-to-peak):

- Channel translation mode 0: 58 UI
- Channel translation mode 1: 46 UI

(1 UI = 644 ns)

Because this is, under normal circumstances, a rare error condition no automatic action is taken by the transmit speech memory as opposed to the receive speech memory in the case of a positive or negative slip. In this case the ACFA requires a re-initialization of the transmit memory by re-programming of the transmit time-slot counter. After that, this memory has its optimal start position.

In PCM 30 mode, the Transmit Route Clock (XRCLK) is derived directly from the system clock by an internal clock divider. Consequently, the data received from the system interface is switched through without the need of intermediate storage.

The parity generation/checking mechanism is symmetrical to the receive path. The channel data is checked with the channel parity information generated internally or externally (input at port XCHPY with selectable input sense). Errors are reported to the microprocessor interface. To avoid difficulties with external parity generation, the parity signal for non-speech data (e.g. signaling data or channels with bit robbing information) is computed internally.

Transmitter
The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the six selectable framing formats
- Insertion of service and data link information
- Remote alarm generation
- CRC generation and insertion of CRC bits
  Note: As addition in PCM 24 mode, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe (function is enabled via bit GCR.CRCI).

In PCM 24 mode, the transmitter of the ACFA can be synchronized externally for multiframe begin (port XCHPY, bit ACR.EXMF). This feature is required if the bit-robbed signals are routed through the switching network and are inserted in transmit direction via the system interface.

Transmit Link Interface
Similar to the receive link interface two different data types with selectable output sense are supported:

- Dual rail data (PCM[+], PCM[–]) at ports XDOP, XDOM with 50 % or 100 % duty cycle (bit EMOD.XFB) transmitted to a line interface unit, e.g. PEB 2235, Siemens ISDN Primary Access Transceiver, IPAT. Single rail data is converted into a dual rail bit stream. In PCM 30 mode, the HDB3 line code is employed. In PCM 24 mode, selection between B8ZS or simple AMI coding with zero code suppression (B7 stuffing) is provided. B7 stuffing can be disabled on a per channel basis (clear channel capability).
- Unipolar data at port XOID (PCM 30) or at port XDOP (PCM 24) with 100 % duty cycle transmitted to a fibre optical interface.

Clocking off data is done with the positive transitions of the transmit route clock: XRCLK (2048 kHz or 1544 kHz). In PCM 30 mode, XRCLK is generated by the ACFA, whereas in PCM 24 mode it must be generated by an external clock generator.

Additionally, the dual rail outputs XTOP and XTOM are provided for test applications.

3. Additional Functions

Signaling Support

Generation of all supporting signals to achieve simple access to signaling information (CCS, CAS-CC, CAS-BR, FDL) at the system interface. In PCM 24 mode, the additional input XSIG is provided for connection to a bit-robbed signaling controller. Furthermore, the controlling of the internal signaling stacks is done by this unit.

For support of common PCM 24 applications, clear channels can be specified via the 3-byte register bank CCB1 … CCB3.

Alarm Interrupt

Normally, the control of data transmission via the PCM line is done by polling the internal status registers of the ACFA at equidistant time intervals.

However, for fast error handling the option exists to configure a specific output port as interrupt port (AINT). This signal may be connected to an interrupt input of the board processor. Triggering of this output may be caused by up to 11 (PCM 30) or 9 (PCM 24) maskable interrupt sources.

Single Channel Loop Back

As one of the extended test options, the single channel loop back enables reflection of a selected channel back to the system interface at port RDO.

Idle Code Insertion

In transmit direction, the contents of selectable channels can be overwritten by the pattern defined via register IDLE. The selection of 'idle channels' is done by programming the three/four-byte register bank ICB1 … ICB3, ICB4.

Operating Modes

The operating mode of the ACFA is selected by programming the carrier data rate, line code, multiframe structure, and signaling scheme.

The ACFA implements all of the standard and/or common framing structures for both PCM 30 (CEPT, 2048 kbit/s) and PCM 24 (T1, 1544 kbit/s) carriers. These are summarized in table 1, along with the signaling types applicable in each of the multiframe formats. 'General signaling' refers to the support the ACFA provides for handling the data link or service bits, as the case may be, in the multiframe.

Table 1
Summary of ACFA Framing and Supported Signaling Modes

	PCM 30		PCM 24			
	Double-Frame	**CRC-Multi-Frame**	**4-Frame Multiframe**	**12-Frame Multiframe**	**Extended Multiframe**	**Remote Switch M.**
CRC	–	❑ CRC4	–	–	❑ CRC6	–
Signaling						
CCS	❑ e.g. TS16	❑ e.g. TS16	❑ e.g. Ch24	❑ e.g. Ch24	❑ e.g. Ch24	❑ e.g. Ch24
CAS-CC	❑ e.g. TS16	❑ e.g. TS16	❑ e.g. Ch24	❑ e.g. Ch24	❑ e.g. Ch24	❑ e.g. Ch24
CAS-BR	–	–	–	❑	❑	❑
General Signaling	❑ S bits	❑ S bits	❑ FS bits	–	❑ DL bits	❑ FS bits

CCS = Common Channel Signaling
CAS-CC = Channel Associated Signaling (Common Channel)
CAS-BR = Channel Associated Signaling (Bit Robbing)

For CCS, CAS-CC, and CAS-BR, different types of support are provided.

Note: All signaling procedures (e.g. HDLC), signaling frame synchronization and synthesis have to be performed by an external controller (e.g. SAB 82525, HSCX for CCS).

The next pages give a general description of the PCM modes and their assigned framing formats. After RESET, the ACFA is switched to PCM 30 doubleframe format automatically.

PCM 30 Mode

Bit: MODE.PMOD = 0

General

PCM line bit rate	:	2048 kbit/s ± 50 ppm
Single frame length	:	256 bit, No. 1 … 256
Framing frequency	:	8 kHz
Organization	:	32 time-slots, No. 0 … 31 with 8 bits each, No. 1 … 8

time-slot 0 is reserved for frame alignment word and service information. Switching between the two applicable framing formats (doubleframe/CRC-multiframe) is done via bit MODE.CRC.

Line Interfacing

- Dual rail data with HDB3 coding in conjunction with double violation detection or extended code violation detection (CCR.EXTD). Errors can be counted by the Code Violation Counter CVC with 8- or 10-bit length (selectable via bit EMOD.ECVE).
- Single rail unipolar data (MODE.OPT) with no zero suppression algorithm.

General Alarms

- AIS: Detection is flaggered by bit RSR.AIS. Transmission is enabled via port COS or bit MODE.XAIS.
- NOS: Detection is flagged by bit RSR.NOS.
- RAI: Remote Alarm Indication is flagged by bit RSR.RRA and RSW.RRA. Transmission is enabled via bit XSW.XRA.

Channel Assignment

The channel (time-slot) assignment from the PCM line to the system internal highway is performed without any changes of channel numbering (TS0 ↔ TS0, … , TS31 ↔ TS31). In receive direction, the contents of time-slot 0 are switched through transparently. In transmit direction, contents of time-slot 0 of the outgoing PCM frame are normally generated by the ACFA. Additionally, one of three transparent modes (XSP.TT0S, XSP.TT0, EMOD.TT0X) can be selected to achieve transparency either for S_n -, S_i -bit information of for the complete time-slot 0.

General Signaling

- S_a bits in accordance with CCITT Blue Book G.704.
- E bits in accordance with CCITT Blue Book G.704.

Signaling

- CCS
  For Common Channel Signaling the use of time-slot 16 is recommended. The use of CCS is allowed with both the doubleframe and the CRC-multiframe format.
- CAS-CC
  For Channel Associated Signaling the use of time-slot 16 is recommended. The autonomous CAS multiframe structure is not related to a doubleframe or a CRC-multiframe structure (refer to CCITT G.704).

Note: CAS multiframe synchronization and synthesis is not performed by the ACFA.

Doubleframe Format

The framing structure is defined by the contents of time-slot 0 (**refer to table 2**).

Table 2
Allocation of Bits 1 to 8 of Time-Slot 0

Alternate Frames \ Bit Number	1	2	3	4	5	6	7	8
Frame Containing the Frame Alignment Signal	S_i	0	0	1	1	0	1	1
	Note 1	Frame Alignment Signal						
Frame not Containing the Frame Alignment Signal	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	Note 1	Note 2	Note 3	Note 4				

Notes: 1. S_i bits: reserved for international use. If not used, these bits should be fixed to '1'. Access to received information via bits RSW.RSIS and RSP.RSIF. Transmission is enabled via bits XSW.XSIS and XSP.XSIF.
2. Fixed to '1'. Used for synchronization.
3. Remote alarm indication: In undisturbed operation '0'; in alarm condition '1'.
4. S_a bits: Reserved for national use. If not used, they should be fixed at '1'. Access to received information via bits RSW.RY0 … RY4. Transmission is enabled via bits XSW.XY0 … XY4. (*)

(*) **Note**: As a special extension for double frame format, the S_n -bit stack may be used optionally.

For transmit direction, contents of time-slot 0 are additionally determined by the selected transparent mode:

Transparent Mode	Source for			
	Framing	A Bit	S_a Bits	S_i Bits
–	(int. generated)	XSW.XRA	XSW.XY0..4 [1]	XSW.XSIS , XSP.XSIF
XSP.TT0	via pin XDI	via pin XDI	via pin XDI	via pin XDI
XSP.TTOS	(int. generated)	XSW.XRA	via pin XDI	via pin XDI
EMOD.TT0X	(int. generated)	XSW.XRA	via pin XDI	via pin XDI

[1] **Note**: As a special extension for double frame format, the S_n-bit stack may be used optionally.

S_a - Bit Access

As an extension for access to S_a-bit information via registers RSW and XSW a new option is implemented to allow the usage of internal S_a-bit stacks RSN and XSN in doubleframe format.

This function is enabled by setting MODE.CRC = 1, MODE.ENSN = 1 **and** EMOD.DFSN = 1.

The new function uses an internal 16-frame structure but no CRC multiframe alignment/generation is performed although MODE.CRC is set to one. For more details refer to chapter CRC-Multiframe and to description of status flags RFLG and XFLG.

Synchronization Procedure

Synchronization status is reported via bit RSR.LOS. Framing errors are counted by the Framing Error Counter (FEC). Asynchronous state is reached after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (bit $2 \neq 1$ in time-slot 0 of every other frame not containing the frame alignment word), the selection is done via bit RC1.ASY4. Additionally, the service word condition can be disabled.

In asynchronous state, counting of framing errors will be stopped and AIS is automatically sent to the system internal highway (can be disabled via bit EMOD.DAIS).

The resynchronization procedure starts automatically after reaching the asynchronous state. Additionally, it may be invoked user controlled via bit: CCR.FRS (Force Resynchronization: the FAS word detection is interrupted. In connection with the above conditions this will lead to asynchronous state. After that, resynchronization starts automatically).

Synchronous state is reached after detecting:

– a correct FAS word in frame n,
– the presence of the correct service word (bit 2 = 1) in frame n + 1
– a correct FAS word in frame n + 2.

Undisturbed operation starts with the beginning of the next doubleframe.

CRC-Multiframe

The multiframe structure shown in **table 3** is enabled by setting bit: MODE.CRC.

Multiframe	:	2 submultiframes = 2 × 8 frames
Frame alignment	:	refer to section Doubleframe Format
Multiframe alignment	:	bit 1 of frames 1, 3, 5, 7, 9, 11 with the pattern '001011'
CRC bits	:	bit 1 of frames 0, 2, 4, 6, 8, 10, 12, 14
CRC block size	:	2048 bit (length of a submultiframe)
CRC procedure	:	CRC4, according to CCITT Rec. G704

Table 3
CRC-Multiframe Structure

	Sub-Multiframe	Frame Number	Bits 1 to 8 of the frame							
			1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Multiframe	I	0	C1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		2	C2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		4	C3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		6	C4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	II	8	C1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		10	C2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		12	C3	0	0	1	1	0	1	1
		13	E*	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		14	C4	0	0	1	1	0	1	1
		15	E*	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

E: Spare bits for international use. Access to received information via bits RSP.RS13 and RSP.RS15. Transmission is enabled via bits XSP.XS13 and XSP.XS15. Additionally, automatic transmission for submultiframe error indication is selectable.
S_a: Spare bits for national use. Additionally, the 5-byte stacks RSN and XSN are provided.
C1..C4: Cyclic redundancy check bits
A: Remote alarm indication

For transmit direction, contents of time-slot 0 are additionally determined by the selected transparent mode:

Transparent Mode	Source for			
	Framing + CRC	A Bit	S_n Bits	E Bits
–	(int. generated)	XSW.XRA	XSW.XY0..4[1]	XSP.XS13/XS15[2]
XSP.TT0	via pin XDI	via pin XDI	via pin XDI	via pin XDI
XSP.TTOS	(int. generated)	XSW.XRA	via pin XDI	via pin XDI
EMOD.TT0X	(int. generated)	XSW.XRA	via pin XDI	XSP.XS13/XS15[2]

Notes:
1) The S_a-bit stack XSN may be used optionally.
2) Additionally, automatic transmission of submultiframe error indication is selectable.

The CRC procedure is automatically invoked when the multiframe structure is enabled. CRC errors in the received data stream are counted by the CRC Error Counter CEC (one error per submultiframe, maximum). This 8-bit counter is extendable to 10-bit length (XSP.AXS, CECX).
As an extension of the alarm interrupt capabilities, the occurrence of a CRC error can be defined as interrupt source (XC1.MCA) for triggering interrupt port AINT.

Synchronization Procedure

Multiframe alignment is assumed to have been lost if doubleframe alignment has been lost (flagged at bit RSR.LOS and bit RSR.CAL).

The multiframe resynchronization procedure starts when Doubleframe alignment has been regained. For Doubleframe synchronization refer to section Doubleframe Format. It may also be invoked by the user by setting

– bit CCR.FRS for complete Doubleframe **and** multiframe re-synchronization

– bit MODE.MFCS for multiframe re-synchronization only.

The CRC checking mechanism will be enabled after the first correct multiframe pattern has been found. However, CRC errors will not be counted in asynchronous state.

The (multiframe) synchronous state is reached after detecting two correct multiframe alignment patterns at an interval of $n \times 2$ ms (n = 1,2,3 …). The CRC4 flag RSR.CAL will be reset. Checking the multiframe pattern is disabled when the receiver is in the synchronous state.

Automatic Force Resynchronization
As addition, a search for Doubleframe alignment is automatically initiated if two multiframe pattern with a distance of $n \times 2$ ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained (bit MODE.AFR).

S_a - Bit Access

Due to new signaling procedures using the five S_a bits (S_{a4} … S_{a8}) of every other frame of the CRC multiframe structure, two possibilities of access via the microprocessor are implemented.

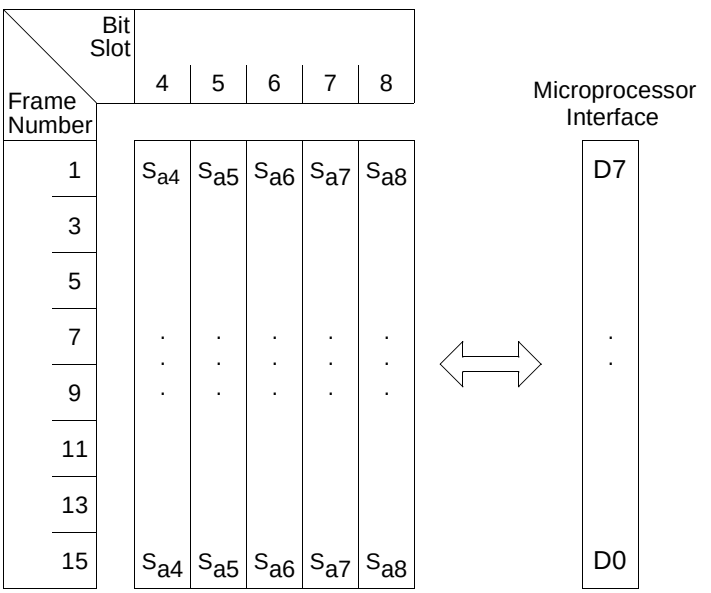
- The standard procedure allows reading/writing the S_a-bit registers RSW, XSW without further support. The S_a-bit information will be updated every other frame.
- The advanced procedure, enabled via bit MODE.ENSN, allows reading/writing two S_a-bit stacks RSN, XSN with a size of 5 bytes. The two status bits RSP.RFLG and RSP.XFLG require updating the stack information by reading/writing five bytes per multiframe from/to the assigned stack address.To avoid loss of information, the status bits should be monitored at time intervals less than 2 ms (1.5 ms recommended). With the first access to a stack, the associated status bit will be reset.
  Additionally, a transmit or receive multiframe begin interrupt is provided if alarm interrupt mode is enabled (CCR.AINT) and bits XSP.MXMB or XSP.MRMB are set.

Organization of the Stacks

The sequently received S_a bits (S_{a4} up to S_{a5}) of odd numbered frames of the multiframe structure are re-organized to bytes containing the S_a-information of the same level (S_{a4} byte up to S_{a8} byte). The S_{a8} byte is the first byte to read or to write via the microprocessor interface (**refer to table 4**).

Moreover, S_a bits may be processed via the system interface. Setting bit XSP.TT0S or EMOD.TT0X enables transparency for S_n bits in transmit direction (**refer to table 3**).

Table 4
Organization of the Sn-Bit Stacks



E-Bit Access

Due to newest signaling requirements, the E bits of frame 13 and frame 15 of the CRC multiframe can be used to indicate received errored submultiframes:

Submultiframe I status	→	E-Bit located in frame 13
Submultiframe II status	→	E-Bit located in frame 15
no CRC error	:	E = 1
CRC error	:	E = 0

Standard Procedure

After reading the Submultiframe Error Indication SEI.SI1 and SEI.SI2, the microprocessor has to update contents of register XSP (XS13, XS15). Access to these registers has to be synchronized to assigned multiframe begin. This can be done by evaluating the Transmit/Receive Multiframe Flags (RSP.XFLG, RSP.RFLG) or by activating Transmit/Receive Multiframe Begin Interrupts (CCR.AINT, XSP.MXMB, XSP.MRMB).

Automatic Mode

By setting bit XSP.AXS status information of received submultiframes is automatically inserted in E-bit position of the outgoing CRC Multiframe without any further interventions of the microprocessor.

Submultiframe Error Indication Counter

If programmed via bit EMOD.ESEI, counter CVC (8 or 10 bits) counts zeros in E-bit position of frame 13 and 15 of every received CRC Multiframe. This counter option gives information about the outgoing transmit PCM line if the E bits are used by the remote end for submultiframe error indication.

Note: E bits may be processed via the system interface. Setting bit XSP.TT0S enables transparency for E bits (and S_a bits) in transmit direction (**refer to table 3**).

PCM 24 Mode

Activated with bit MODE.PMOD = 1.

General

PCM line bit rate	:	1544 kbit/s ± 50 ppm
Single frame length	:	193 bit, No. 1 … 193
Framing frequency	:	8 kHz
Organization	:	24 time-slots, No. 1 … 24 with 8 bits each, No. 1 … 8 and one preceding F bit

Selection of one of the four permissible framing formats is performed by bits GSR.FM0 and GSR.FM1. These formats are:

F4	:	4-frame multiframe
F12	:	12-frame multiframe (D3/D4)
ESF	:	Extended Superframe
F72	:	72-frame multiframe (remote switch mode)

Line Interfacing

- Dual rail data with B8ZS or AMI (ZCS) coding (selection via bit MODE.CODE). All code violations which do not correspond to zero code substitution rules are registrated by the Code Violation Counter (CVC) with 8- or 10-bit length (selected via bit EMOD.ECVE).
  If AMI coding with zero code suppression (B7-stuffing) is selected, '**clear channels**' without B7-stuffing can be defined by programming registers CCB1 … CCB3.
- Single rail unipolar data with no zero suppression algorithm (MODE.OPT = 1).

General Aspects of Synchronization

Synchronization status is reported via bit RSR.LOS (Loss Of Synchronization). Framing errors (pulse frame and multiframe) are counted by the Framing Error Counter FEC.
Asynchronous state is reached if
2 out of 4 (bit RC1.SLC reset), or
2 out of 5 (bit RC1.SLC set)
framing bits (terminal framing or multiframing) are incorrect. If auto-mode is enabled, counting of framing errors is interrupted.

The resynchronization procedure can be controlled by either one of the following procedure:

- automatically (GCR.AUTO = 1). Additionally, it may be triggered by the user by setting/resetting one of the bits CCR.FRS (Force Resynchronization) or CCR.EXLS (External Loss of Frame).
- user controlled, exclusively, via above control bits in the non-auto-mode (GCR.AUTO = 0).

Addition for F12 and F72 Format

FT and FS bit conditions, i.e. pulse frame alignment and multiframe alignment can be handled separately if programmed via bit EMOD.SSP. Thus, a multiframe re-synchronization can be automatically initiated after detecting 2 errors out of 4/5 consecutive multiframing bits without influencing the state of the terminal framing.

In the synchronous state, the setting of CCR.FRS or CCR.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.

In asynchronous state, the function of CCR.EXLS is the same as above. Setting bit CCR.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. Otherwise, a new frame search is started. This is useful in case the framing pattern that defines the pulseframe position is imitated periodically by a pattern in one of the speech/data channels. The F-bit Error History (FSR.FEH5 … 0) may be used in the decision whether to initiate resynchronization.

The updating of these bits depends on the resynchronization mode:

- Auto mode: updating only during the synchronous state.
- Non-auto-mode: updating during the synchronous state and
  until one of the above control bits are set during the asynchronous state.

The control bit CCR.EXLS should be used first because it starts the synchronizer to search for a definite framing candidate.
To observe actions of the synchronizer, the Frame Search Restart Flag RSR.FSRF is implemented. It toggles at the start of a new frame search if no candidate has been found at previous attempt.

When resynchronization is initiated, the following values apply for the time required to achieve the synchronous state in case there is one definite framing candidate within the data stream:

Table 5
Resynchronization Timing

Frame Mode	Avg.	Max.	Units
F4 F12 ESF F72	1.0 3.5 3.4 13.0	1.5 4.5 6.125 17.75	ms

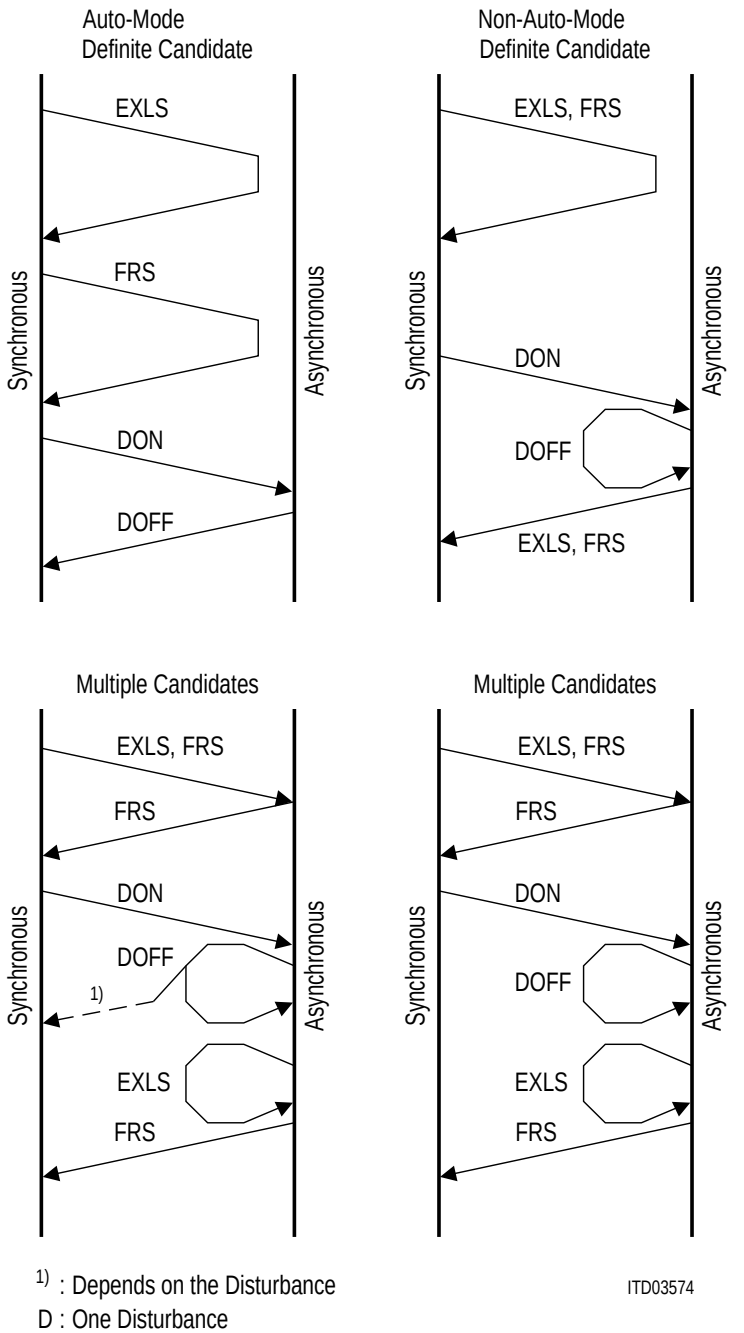


Figure 4
Influences on Synchronization Status

Figure 4 gives an overview of influences on synchronization status for the case of different external actions. Activation of auto-mode and non-auto-mode is performed via bit GSR.AUTO. Generally, for initiating resynchronization it is recommended to use bit: CCR.EXLS first. In case where the synchronizer remains in the asynchronous state, bit CCR.FRS may be used to enforce it to lock onto the next framing candidate, although it might be a simulated one.

General Alarms

- AIS: Detection is flagged by bit RSR.AIS. Transmission is enabled via port COS or bit MODE.XAIS.
- NOS: Detection is flagged at bit RSR.NOS.
- RAI: Remote Alarm Indication is flagged at bit RSR.RRA. Transmission is enabled via bit GCR.XRA. The type of remote alarm indication depends on the selected multiframe format.

Channel Assignment

Two possibilities are provided for converting the 24 speech channels to the 32 time-slots on the system internal highway (refer to section Interface to System Internal Highway). The selection is performed via bit MODE.CTM. Transparent mode setting bit GCR.TM switches the ACFA in transparent mode:

– In transmit direction bit 8 of the FS/DL time-slot from the system internal highway (XDI) is inserted
  in the F-bit position of the outgoing frame.
– In receive direction the framing bit is also forwarded to RDO and inserted in the FS/DL time-slot. Bit RDCF (bit 1 of FS/DL time-slot) indicates a DL bit.

General Signaling

For data link or signaling applications, it may be necessary to have external access to the FS bits (F4 and F72 format) or to the DL bits of the extended superframe. Two methods of access are provided:

- in a defined FS/DL time-slot of the PCM data stream on the system internal highway
- by reading and writing special registers via the microprocessor interface (RFDL, XFDL).

Simultaneous use of both of these modes is permitted. For this application, FS/DL subchannels for transmit direction may be programmed on a bit-by-bit basis over 12 frames via the additional mask register FMR. They are accessed via the microprocessor interface while the other subchannels are passed transparently from the system internal highway to the FS/DL-bit position of the assigned outgoing 193-bit frame.

A combination of the two accessing methods only makes sense when using the more complex multiframing formats (ESF, F72) to get a defined FS/DL subchannel assignment. For the 4-frame multiframe structure, all mask bits are normally to be set to the same logical level.

Additional Support: 4-kHz DL clock

If programmed via bit ACR.DLC, ports RCHPY and XCHPY provide signals which mark the DL-bit position within the data stream at RDO and XDI.

Signaling

The selection of the signaling scheme is done via bit MODE.SIGM.

- **CCS**
  MODE.SIGM = 0
  For Common Channel Signaling, the use of time-slot 24 is recommended. In channel translation mode 1 channel 17 (corresponding to time-slot 16 on the system internal highway) may be selected instead of channel 24 by programming the bit FMR.SM24. The use of CCS is permitted for all multiframe formats.
- **CAS-CC**
  MODE.SIGM = 0
  Instead of CCS the above channels may be used for carrying CAS information. For positioning of the CAS multiframe with respect to the selected multiframe structure, refer to DMI, part III, § 12.1.
  Note: Synchronization to and synthesis of the CAS multiframe is not performed by the ACFA. The use of CAS-CC is permitted for all multiframe formats.
- **CAS-BR**
  MODE.SIGM = 1
  The use of CAS bit robbing mode is applicable to F12, ESF, and F72 multiframe format.

Especially when using the CAS-BR signaling schemes it could be necessary to define '**clear channels**' for data transmission. By programming registers CCB1 … CCB3 they can be selected on a per channel basis.

4-Frame Multiframe

The allocation of the FT bits (bit 1 of frames 1 and 3) for frame alignment signal is shown in **table 6**.

The FS bit may be used for signaling.
Remote alarm is indicated by setting bit 2 to '0' in each channel.

Table 6
4-Frame Multiframe Structure

Frame Number	F_T	F_S
1	1	
2	–	Service bit
3	0	
4	–	Service bit

Synchronization Procedure

For multiframe synchronization, the terminal framing bits (FT bits) are observed. The synchronous state is reached if at least one terminal framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (CCR.FRS).

12-Frame Multiframe

Normally, this kind of multiframe structure only makes sense when using the CAS bit robbing mode. In addition, CCS and CAS-CC are also allowed. The multiframe alignment signal is located at the FS-bit position of every other frame (**refer to table 7**).

There are two possibilities of remote alarm indication:

- bit 2 = 0 in each channel of a frame, selected with bit CCR.SRAF= 0
- the last bit of the multiframe alignment signal (bit 1 of frame 12) changes from '0' to '1', selected with bit CCR.SRAF = 1.

Synchronization Procedure

In the synchronous state terminal framing (FT bits) and multiframing (FS bits) are observed, independently. Further reaction on framing errors depends on the selected sync/resync procedure (via bit EMOD.SSP):

- EMOD.SSP = '0': terminal frame and multiframe synchronization are combined.
  Two errors within four/five framing bits (via bit RC1.SLC) of one of the above will lead to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit RSR.LOS, loss of multiframe alignment is reported via bit FSR.MLOS.
  The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulseframing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- EMOD.SSP = '1': terminal frame and multiframe synchronization are separated
  Two errors within four/five terminal framing bits will lead to the same reaction as described above for the 'combined' mode.
  Two errors within four/five multiframing bits will lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported via bit FSR.MLOS. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 7
12-Frame Multiframe Structure

Frame Number	F_T	F_S	Signaling Channel Designation
1	1	–	
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	A
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0	B

Extended Superframe

The use of the first bit of each frame for the multiframe alignment word, the data link bits, and the CRC bits is shown in **table 8**.

Table 8
Extended Superframe Structure

Multiframe Frame Number	F Bits				Signaling Channel Designation
	Multiframe Bit Number	Assignments			
		FAS	DL	CRC	
1	0	–	m	–	
2	193	–	–	e_1	
3	386	–	m	–	
4	579	0	–	–	
5	772	–	m	–	
6	965	–	–	e_2	A
7	1158	–	m	–	
8	1351	0	–	–	
9	1544	–	m	–	
10	1737	–	–	e_3	
11	1930	–	m	–	
12	2123	1	–	–	B
13	2316	–	m	–	
14	2509	–	–	e_4	
15	2702	–	m	–	
16	2895	0	–	–	
17	3088	–	m	–	
18	3231	–	–	e_5	C
19	3474	–	m	–	
20	3667	1	–	–	
21	3860	–	m	–	
22	4053	–	–	e_6	
23	4246	–	m	–	
24	4439	1	–	–	D

The CRC6 checking algorithm is enabled via bit MODE.CRC. If not enabled, all check bits in the transmit direction are set to ‘1’.

Additions: CRC6 Inversion

If enabled via bit GCR.CRCI, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe.

CRC Alarm Interrupt

As an extension of the alarm interrupt capabilities, the occurrence of a CRC error can be defined as interrupt source (XC1.MCA) for triggering interrupt port AINT.

Remote alarm is indicated by the periodical pattern ‘1111 1111 0000 0000 …’ in the DL bits.

All signaling schemes are applicable for this multiframing structure. For external access to the DL bits, refer to section General.

Synchronization Procedure

For multiframe synchronization the FAS bits are observed. Synchronous state is reached if at least one framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (CCR.FRS).

72-Frame Multiframe

As a special kind of the 12-frame structure, an alternate use of the FS-bit pattern is defined for carrying data link information. This is done by stealing some of redundant multiframing bits after the transmission of the 12-bit framing header (**refer to table 9**). The position of A and B signaling channels (bit robbing mode) is defined by zero-to-one and one-to-zero transitions of the FS bits and is continued when the FS bits are replaced by the data link bits. The use of this 24-bit data link channel, however, is not specified by the ACFA. For access to these bits refer to section General.

Remote Alarm is indicated by setting bit 2 to zero in each channel. An additional use of the D bits for alarm indication is user defined and must be done externally.

In addition to CAS-BR, CCS and CAS-CC are also applicable to this multiframe structure.

Synchronization Procedure

In the synchronous state terminal framing (FT bits) and multiframing (FS bits of the framing header) are observed independently. Further reaction on framing errors depends on the selected sync/ resync procedure (via bit EMOD.SSP):

- EMOD.SSP = ‘0’: terminal frame and multiframe synchronization are combined
  Two errors within four/five framing bits (via bit RC1.SLC) of one of the above will lead to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit RSR.LOS, loss of multiframe alignment is reported via bit FSR.MLOS.
  The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulseframing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- EMOD.SSP = ‘1’ : terminal frame and multiframe synchronization are separated
  Two errors within four/five terminal framing bits will lead to the same reaction as described above for the ‘combined’ mode.
  Two errors within four/five multiframing bits will lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported via bit FSR.MLOS. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 9
72-Frame Multiframe Structure

Frame Number	F_T	F feS	Signaling Channel Designation
1	0	–	
2	–	0	B
3	1	–	
4	–	0	
5	0	–	
6	–	0	
7	1	–	
8	–	1	A
9	0	–	
10	–	1	
11	1	–	
12	–	1	
13	0	–	
14	–	0	B
15	1	–	
16	–	0	
17	0	–	
18	–	0	
19	1	–	
20	–	1	A
21	0	–	
22	–	1	
23	1	–	
24	–	1	
25	0	–	
26	–	D	B
27	1	–	
28	–	D	
.	.	.	
.	.	.	
67	1	–	
68	–	D	A
69	0	–	
70	–	D	
71	1	–	
72	–	D	

4 Interfaces

Interface to Primary Rate PCM Carriers

Receive Direction

RDIP	I	Receive Data In Plus
RDIM	I	Receive Data In Minus
RRCLK	I	Receive Route Clock

Transmit Direction

XDOP	O	Transmit Data Out Plus
XDOM	O	Transmit Data Out Minus
XRCLK		Transmit Route Clock
	O	**PCM 30**: provided by the ACFA
	I	**PCM 24**: Generated externally

The above signals are to be used for the connection to a Line Interface Unit (LIU) such as the Siemens PEB 2235/PEB 2236, IPAT. Latching data on RDIP/RDIM is done on the falling edge of RRCLK. Normally, RRCLK is extracted from the incoming data stream by the LIU. Clocking off data at XDOP/XDOM is done on positive transitions of XRCLK with 50 % or 100 % duty cycle (selectable via bit EMOD.XFB). To simplify different types of line interface units, the input sense of RDIP/RDIM and the output sense of XDOP/XDOM are selectable via bits RC0. RDIS and XC0.XDOS.

Line Codes	PCM 30:	HDB3	
	PCM 24:	B8ZS	(MODE.CODE = 1)
		AMI (ZCS)	(MODE.CODE = 0)

Interface to Fibre Optical System

The use of the fibre optical interface is alternative to the use of the PCM carrier interface. Its activation is performed via bit MODE.OPT, which enables reception and transmission of unipolar uncoded data.

Receive Direction

ROID	I	**PCM 30**: Receive Optical Interface Data RDIP/RDIM are ignored.
RDIP	I	**PCM 24**: Receive Data In Plus RDIM has no function.
RRCLK	I	as above

Transmit Direction

XOID	O	**PCM 30**: Transmit Optical Interface Data
XDOP	O	**PCM 24**: Transmit Data Out Plus XDOM should be ignored.
XRCLK	I/O	as above

The inputs for unipolar data (ROID, RDOP) are latched on the falling edge of RRCLK. Outputs XOID and XDOP are clocked off on positive transitions of XRCLK with 100 % duty cycle. The input/output sense is selectable via the same control bits (RC0.RDIS, XC0.XDOS) as for the PCM carrier interface ports. However, in the PCM 30 mode, the sense for ROID and XOID is opposite to RDIP/ RDIM and XDOP/XDOM.

Interface to Clock Generator

SCLK	I	System (station) Clock with 4096/8192 kHz. Selection is performed by bit XC1.SCLK
SYPQ	I	Synchronous Pulse defines the beginning of the frame on the receive/transmit system internal highway in conjunction with the values of the assigned time-slot/clock-slot counters (RC0.RCO, RC1.RTO, XC0.XCO, XC1.XTO).
XRCLK	I	**PCM 24**: as above
RFSPQ	O	Receive Frame Synchronous Pulse 8-kHz framing pulse derived from the received PCM route signal. It may be used for PLL applications in master-slave configurations.

Interface to System Internal Highway

SCLK	I	as above
SYPQ	I	as above
RDO	O	Receive Data Out system internal receive 2048/4096 kbit/s highway. clocking off of the data is done on negative transitions of SCLK. The beginning of time-slot 0 is defined by SYPQ and the offset values of the Receive Clock-slot and Time-slot Counters RC0.RCO, RC1.RTO (**refer to figure 5**).
XDI	I	Transmit Data In system internal transmit 2048/4096 kbit/s highway. Latching of the data is done on negative transitions of SCLK. The beginning of time-slot 0 is defined by SYPQ and the offset values of the Transmit Clock-slot and Time-slot Counters: XC0.XCO, XC1.XTO (**refer to figure 6**).

The selection of the data is performed via bit MODE.IMOD.

In PCM 24 mode, only 24 of the 32 time-slots on RDO and XDI are used. The rest of the unequipped time-slots are set to ‘FF’ hex (RDO) or ignored (XDI), except time-slot 0 or 31 which is used to carry FS/DL information. The two possible channel translation modes are shown in **table 10**.

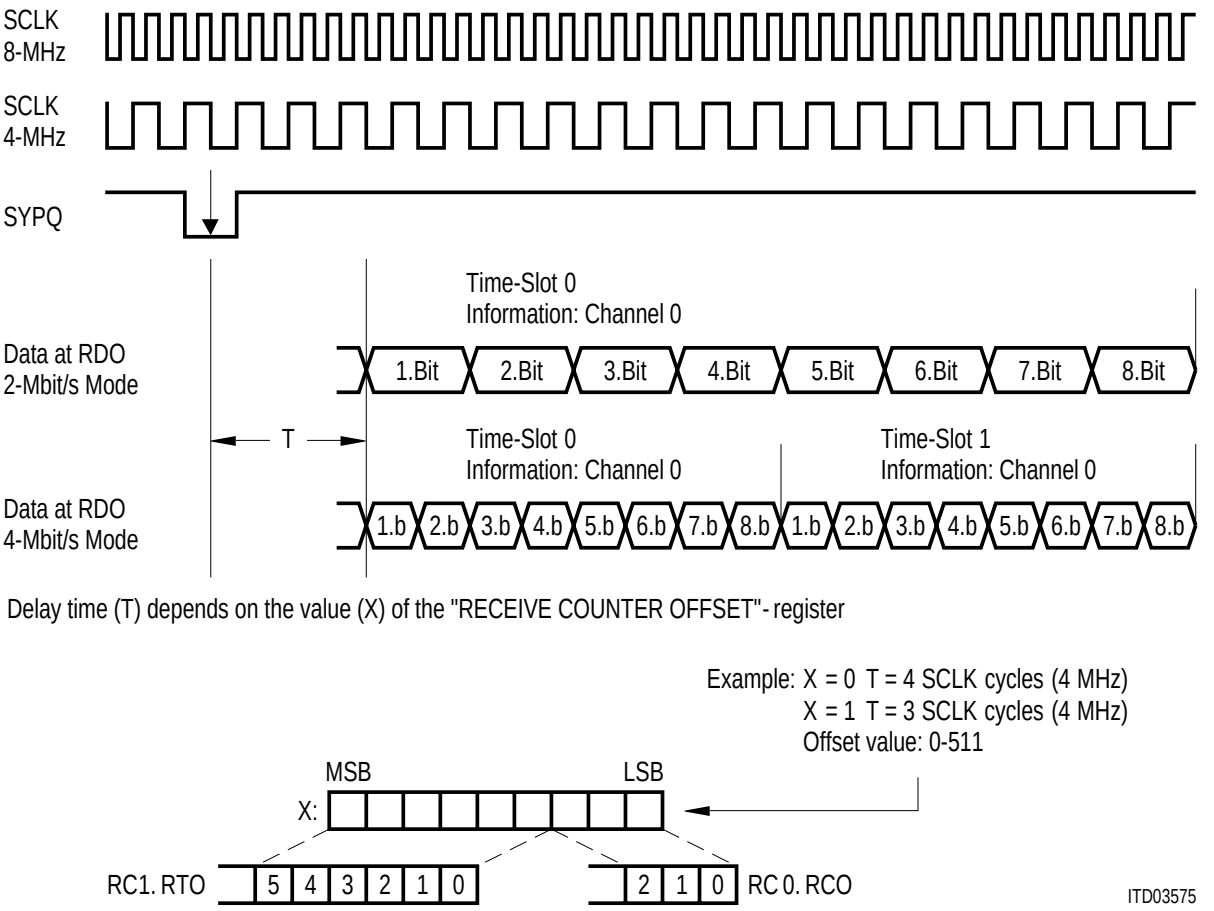


Figure 5
Data on RDO

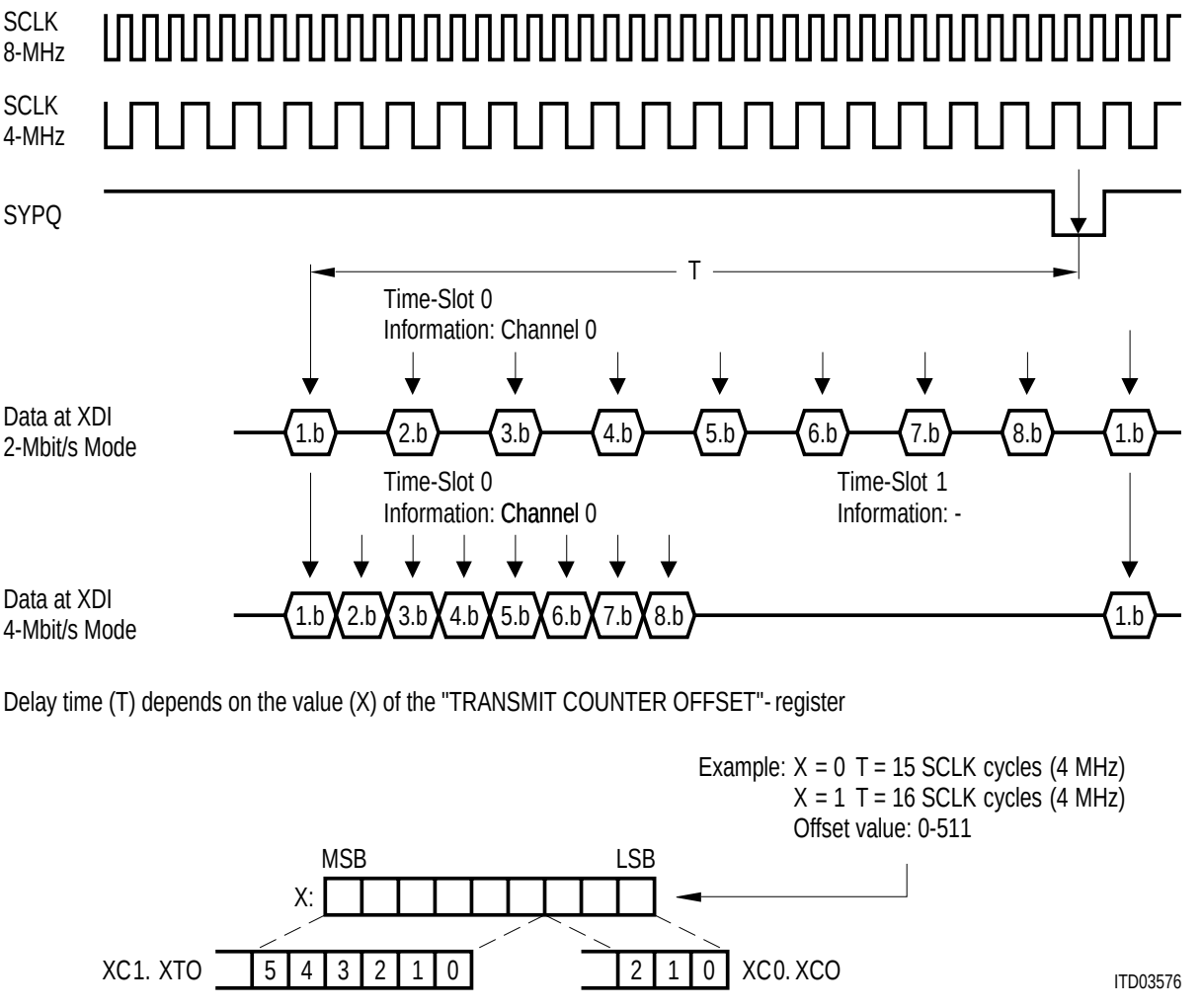


Figure 6
Data on XDI

Table 10
Channel Translation Modes for PCM 24

Speech Channels		Time-Slots
C. Translation Mode 0	C. Translation Mode 1	
FS/DL	1	0
1	2	1
2	3	2
3	4	3
–	5	4
4	6	5
5	7	6
6	8	7
–	9	8
7	10	9
8	11	10
9	12	11
–	13	12
10	14	13
11	15	14
12	16	15
–	17 --- S	16
13	18	17
14	19	18
15	20 or	19
–	21	20
16	22	21
17	23	22
18	24 --- S	23
–	–	24
19	–	25
20	–	26
21	–	27
–	–	28
22	–	29
23	–	30
S --- 24	FS/DL	31

S: CCS/CAS-CC signaling channel
The formats for FS/DL data transmission via the system interface are as follows:

Receive Direction

FS/DL bits on system internal receive highway (RDO), time-slot 0 to 31

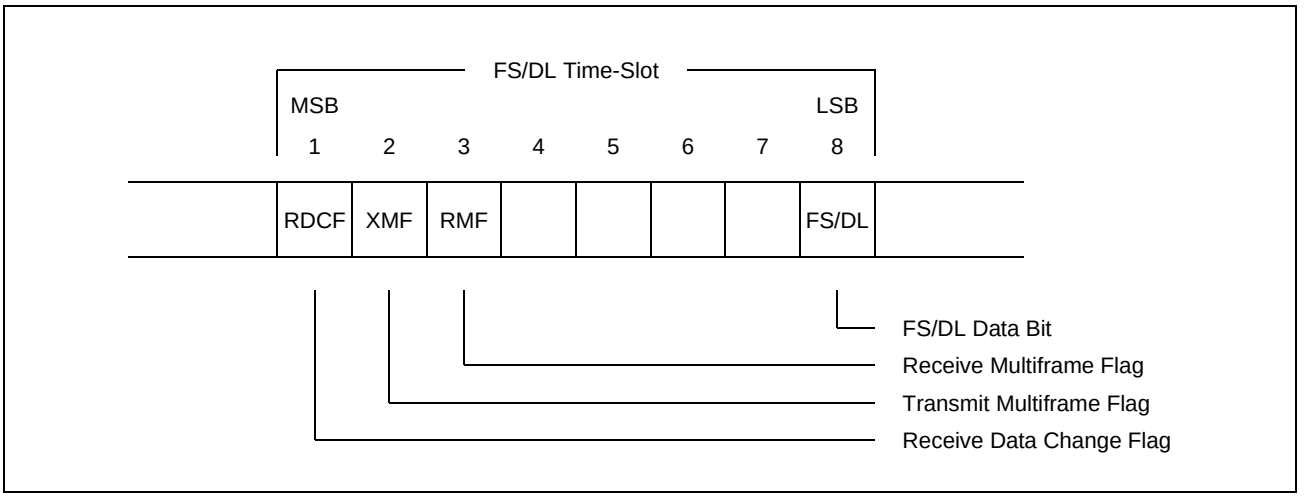


Figure 7
Receive FS/DL Bits on RDO

Each data bit is repeated for two frames. The reception of a new FS/DL bit is indicated by the **R**eceive **D**ata **C**hange **F**lag (normal operation: RDCF toggles; transparent mode enabled via bit GCR.TM: RDCF is set, if the FS/DL bit-slot contains valid DL information). For further support in locating optionally defined subchannels, the Receive Multiframe Flag and the Transmit Multiframe Flag are provided for marking the beginning of the multiframe. In addition, the signals RMFB and XMFB may be used for that purpose.

Transmit Direction

FS/DL data on system internal transmit highway (XDI), time-slot 0 or 31

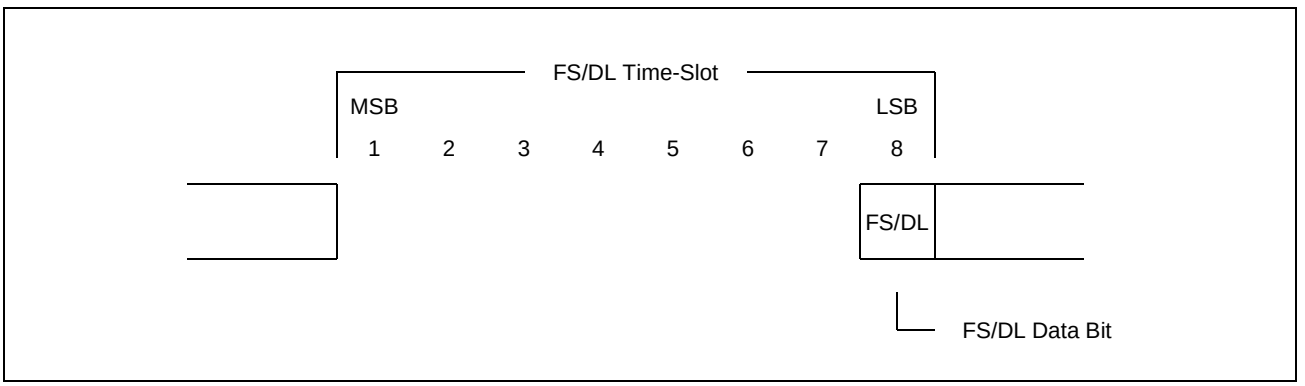


Figure 8
Transmit FS/DL Bits on XDI

The FS/DL bit of every second frame is inserted into the transmit FS/DL-bit location of the assigned outgoing 193-bit frame.

Interface to Signaling Controller

SCLK	I	as above
SYPQ	I	as above
RDO	O	as above
XDI	I	as above
RSIGM	O	Receive Signaling Marker It marks all signaling bits on RDO.
XSIGM	O	Transmit Signaling Marker It marks all signaling bits on XDI.
RREQ	O	Receive DMA/Interrupt Request Enabled via bit XC0.ISIG. It requires read access to the internal Receive Signaling Stack RSIG.
XREQ	O	Transmit DMA/Interrupt Request Enabled via bit XC0.ISIG. It requires write access to the internal Transmit Signaling Stack XSIG.
ACKNLQ	I	DMA/Interrupt Acknowledge Enabled via bit XC0.ISIG. This input acts as access enable to the signaling stacks for I/O-to-memory DMA applications.
XSIG	I	**PCM 24**: Transmit Signaling Data Additional system internal transmit highway input for signaling data. Used if the switching network circuits are not able to tri-state their outputs. Normally, this will be used for CAS-BR applications.
RMFB	O	**PCM 24**: Receive Multiframe Begin It marks the beginning of every received multiframe on RDO. Additional pulses every twelve frames are provided in ESF and F72 format to enable easy access to FS/DL information which may be used for synchronizing an external controller. Generation of these additional pulses can be disabled via bit ACR.MFBS. For interrupt applications, the internal status bits MFR.RRS and MFR.RMB may be used in conjunction with the acknowledge bit XFDL.RMAK.
XMFB	O	**PCM 24**: Transmit Multiframe Begin Its function is equivalent to RMFB for the transmit direction. Associated bits: MFR.XRS, MFR.XMB, XFDL.XMAK and also ACR.MFBS.
FREEZS	O	**PCM 24**: Freeze Signaling Synchronization status signal which informs the signaling controller that current signaling should be frozen.

AFR	O	**PCM 24**: Additional Function Receive If enabled via bit ACR.DLC, this signal provides a 4-kHz DL clock which marks the DL-bit position within the data stream at RDO.
AFT	O	**PCM 24**: Additional Function Transmit If bit ACR.EXMF is reset, its function is equivalent to AFR for the transmit direction.
	I	If bit ACR.EXMF is set, this **input** signal can be used to synchronize the transmitter of the ACFA externally for multiframe begin.

Signaling Support

The above signals may be used to support different signaling applications for CCS, CAS-CC, or CAS-BR. For each method, different ways of access to signaling data are implemented:

Access via

a. an intelligent controller without the need of supporting signals (e.g. SAB 82525, HSCX)

b. a controller supported by the ACFA

c. a DMA controller

d. the board microprocessor

a. Access via an Intelligent Controller

Applications: CCS, (CAS-CC)

The intelligent controller is able to locate the signaling data on the system internal highway by itself when supplied with the synchronous pulse SYPQ of the system (**see figure 9**). In PCM 24 applications, the normally unused input XSIG has to be connected to XDI.

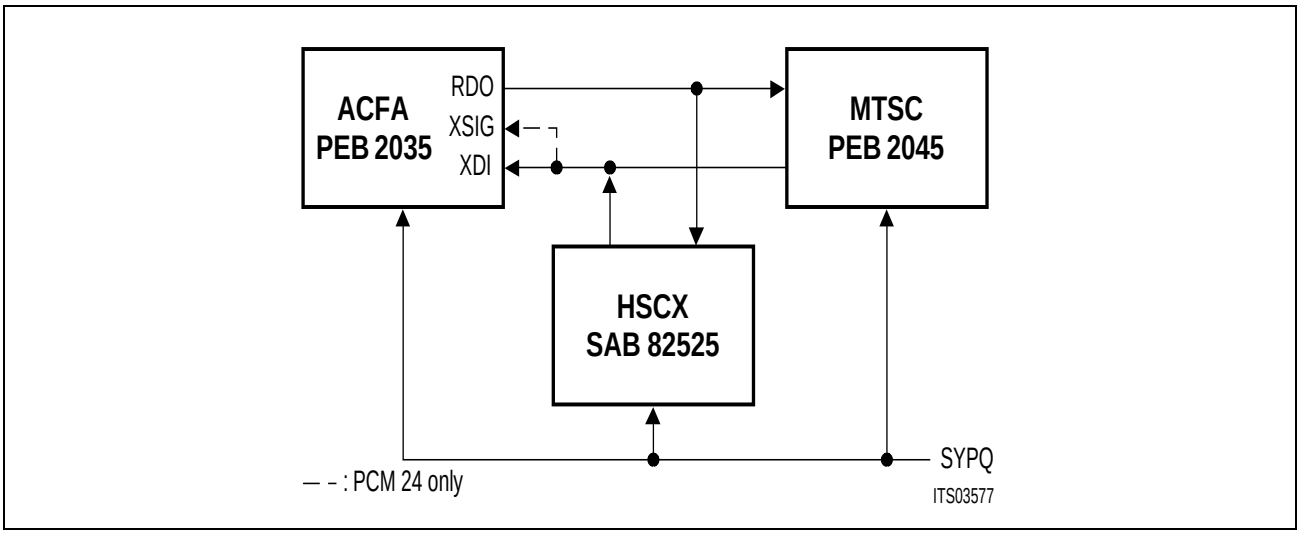


Figure 9
Connection of an Intelligent Signaling Controller

b. Access via a Signaling Controller Supported by the ACFA

Applications: CCS, CAS-CC, CAS-BR

The supporting signals enable easy access to signaling data on the system internal highway (**see figures 10 to 14**).

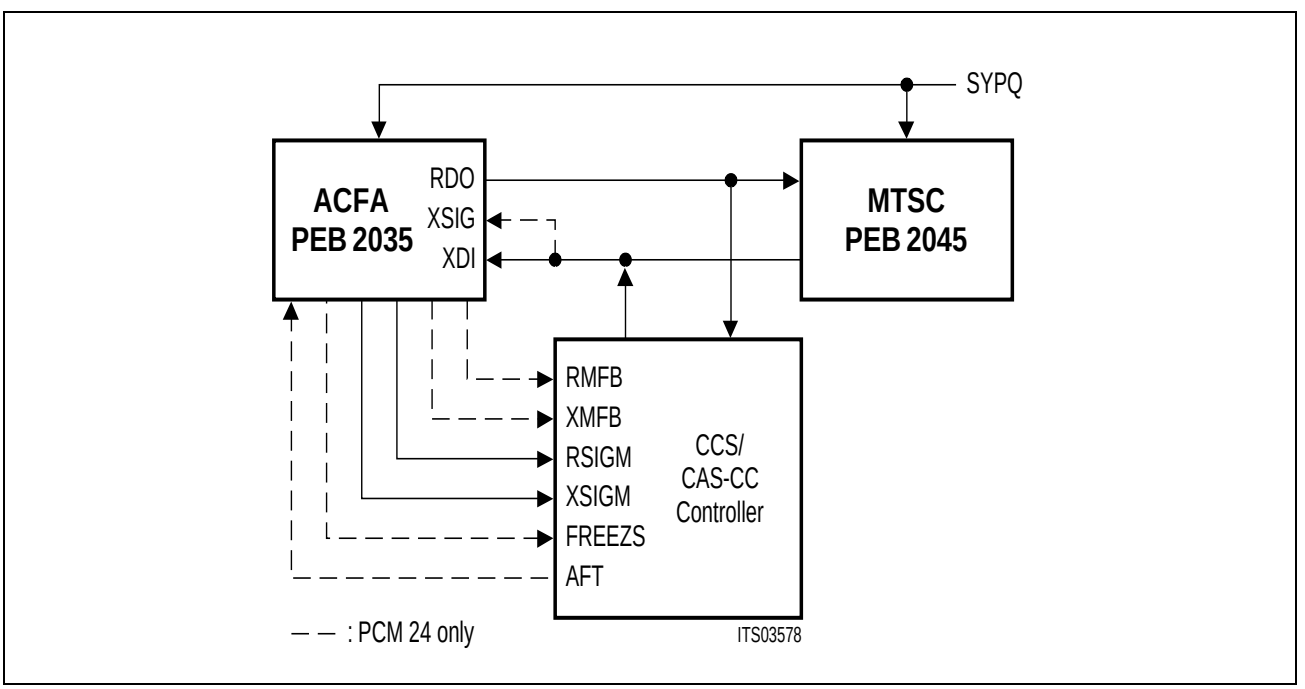


Figure 10
Connection of a Supported CCS/CAS-CC Controller

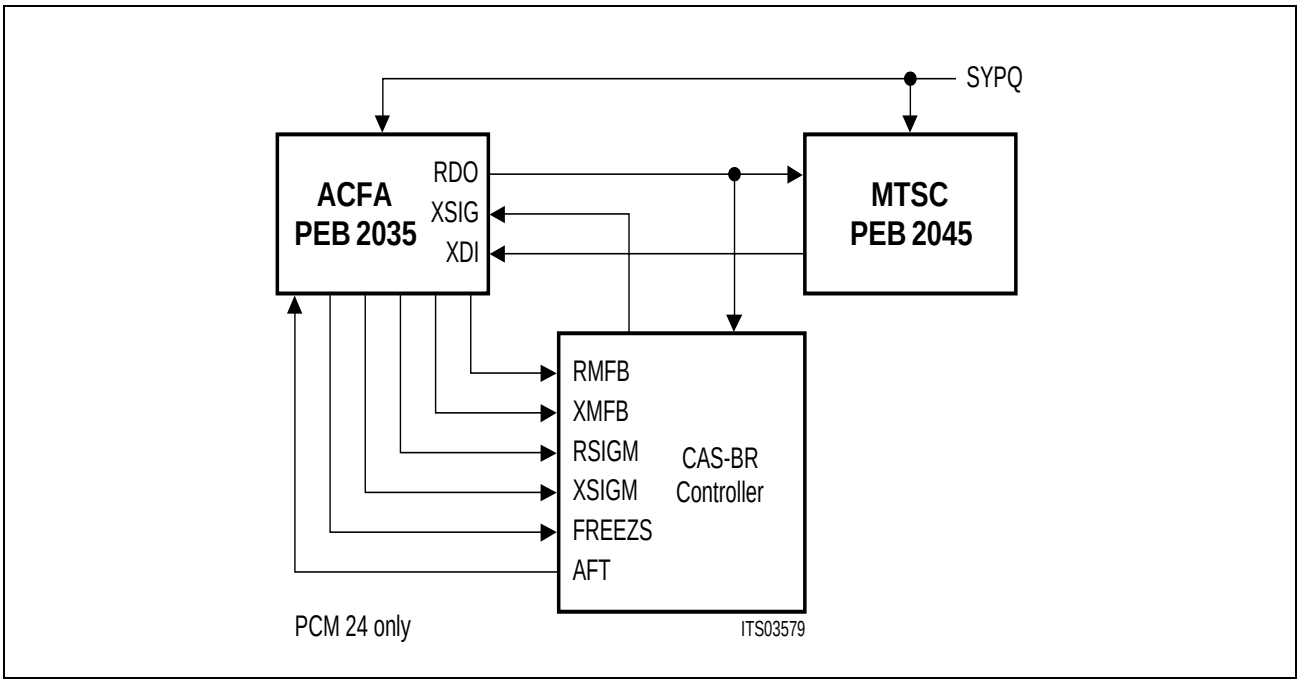
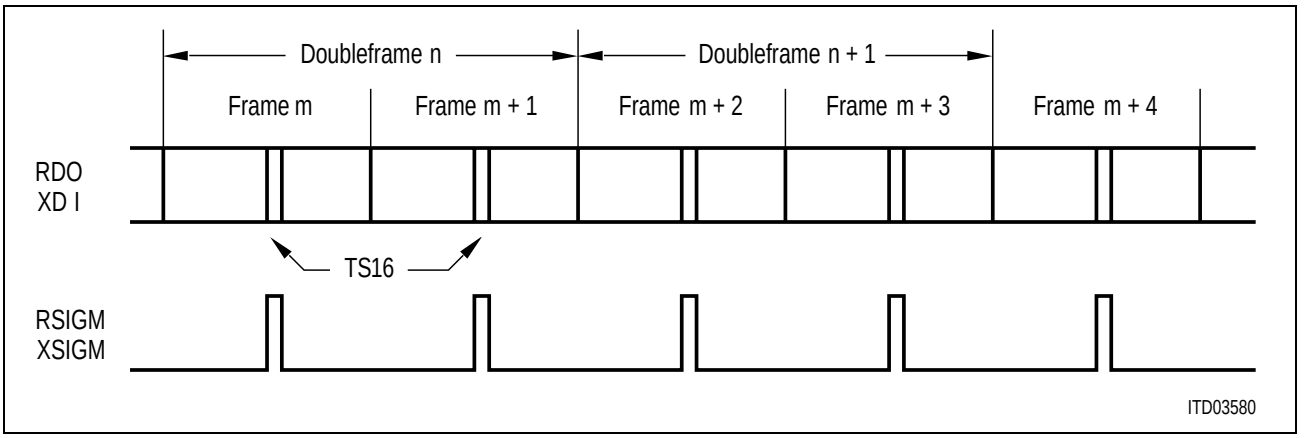


Figure 11
Connection to a CAS-BR Controller (PCM 24 mode only)



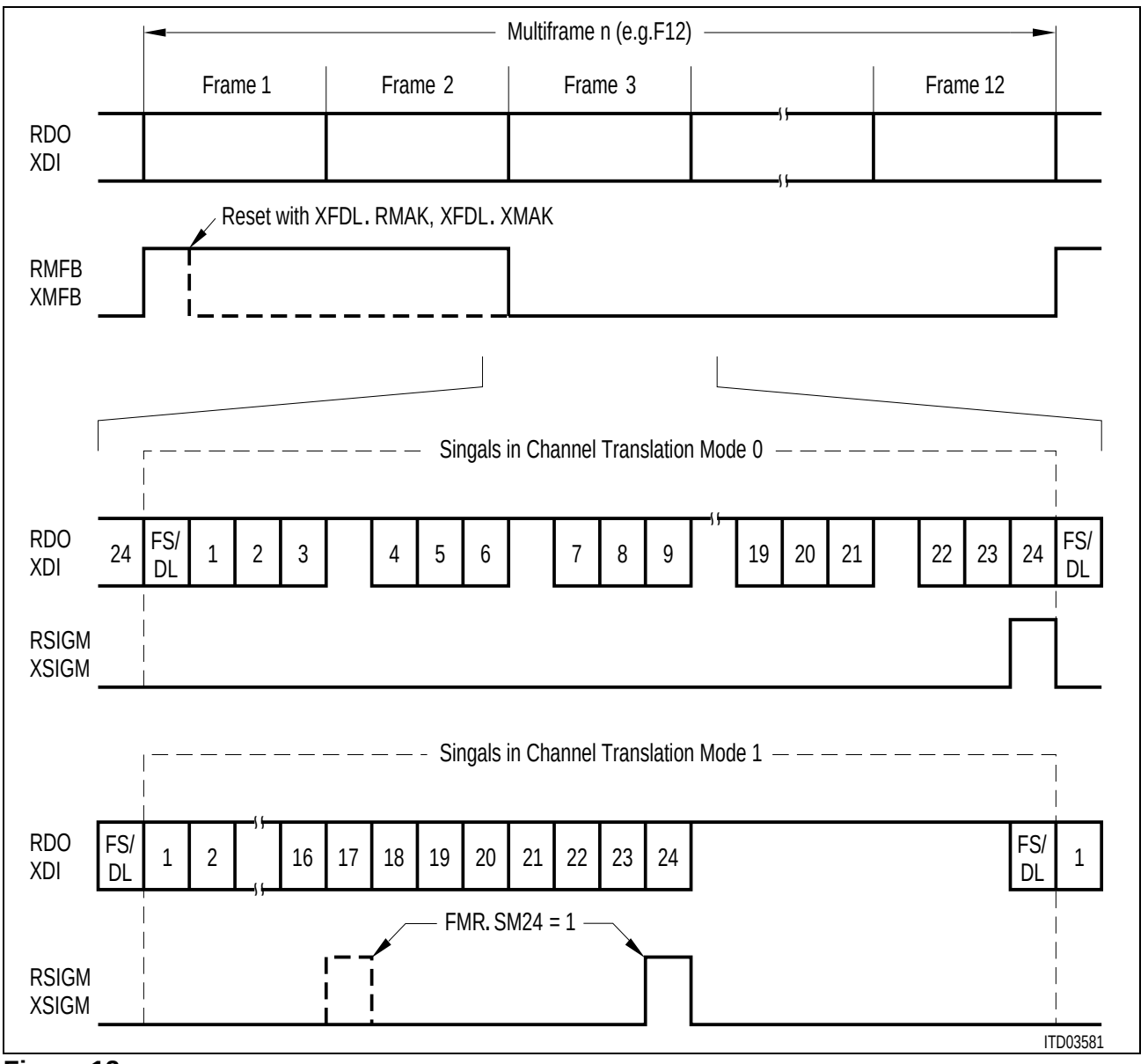


Figure 12
Supporting Signals for CCS/CAS-CC Applications

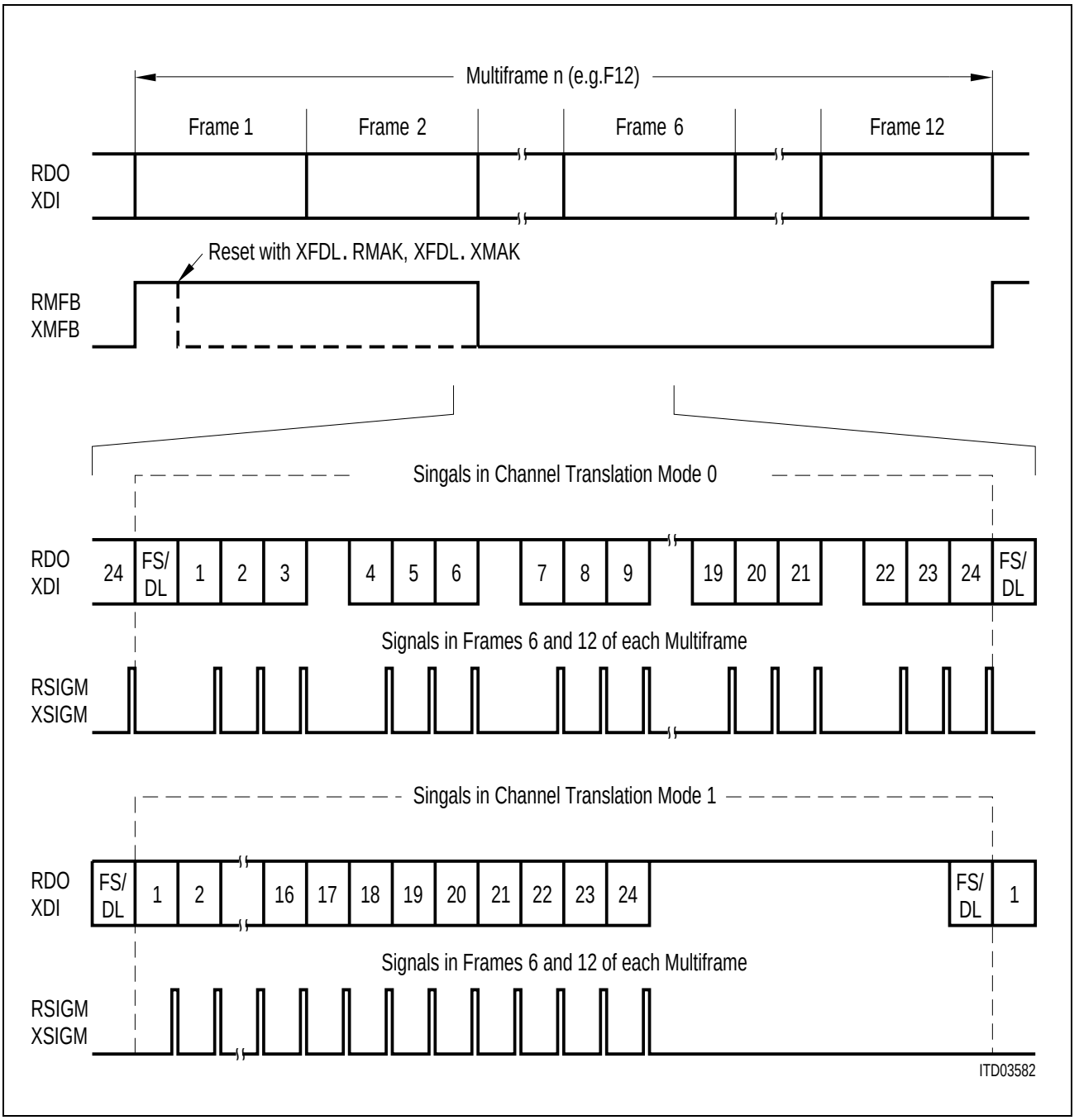
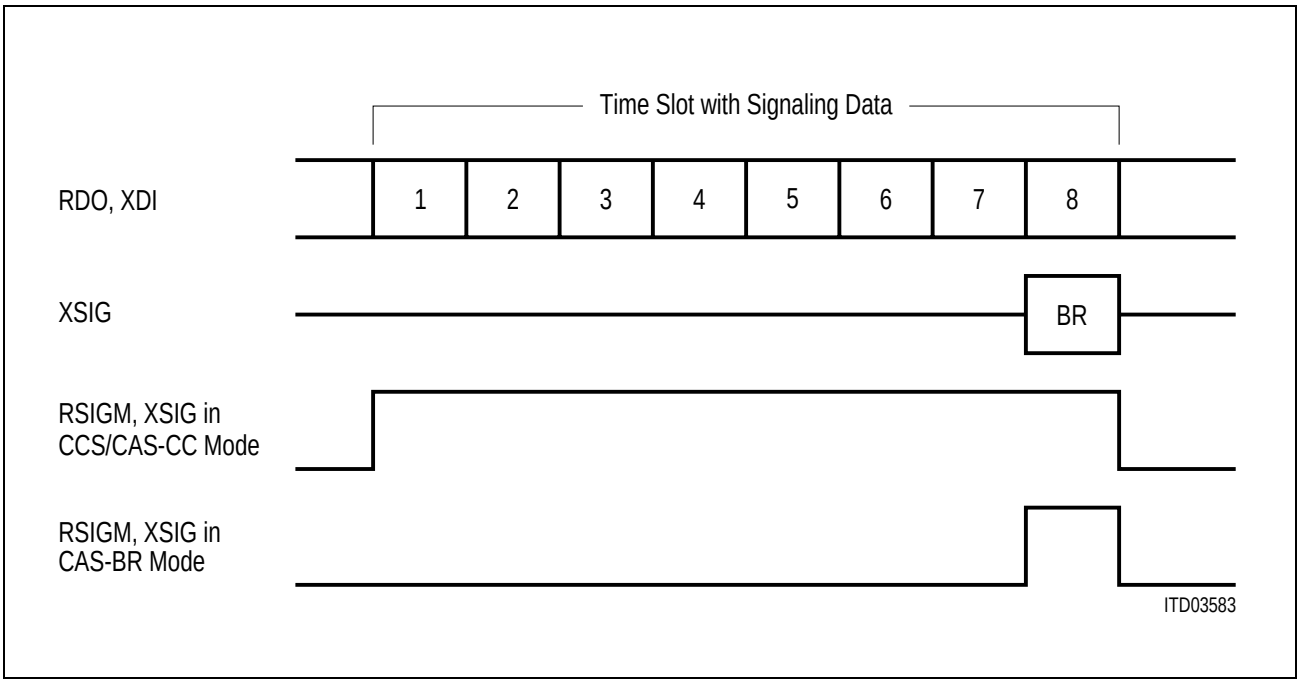


Figure 13
Supporting Signals for CAS-BR Applications (PCM 24 mode only)



Signaling Markers in 2/4-Mbyte/s System Interface Mode
2-Mbyte/s Interface Mode

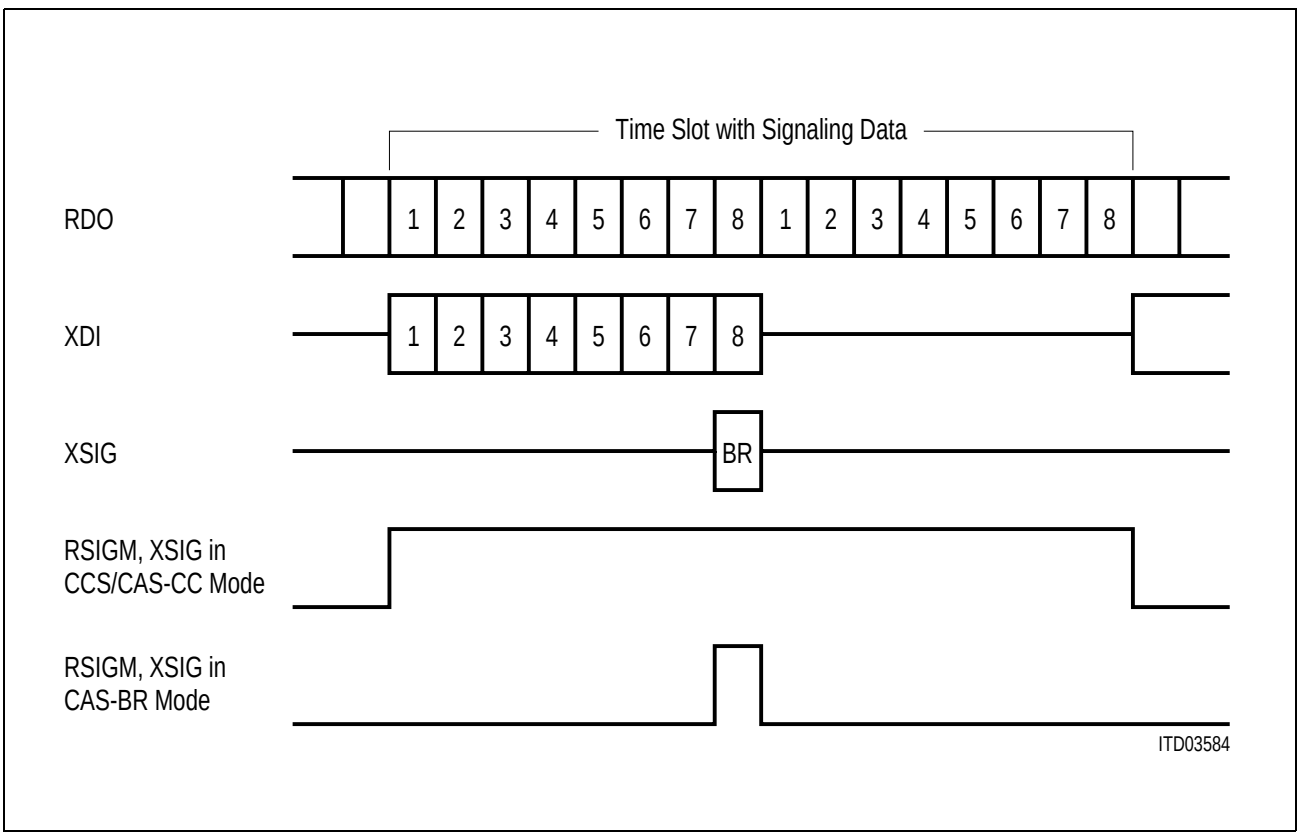


Figure 14
4-Mbyte System Interface Mode

In the PCM 24 mode an additional possibility exists for using the FS/DL bits for signaling, e.g. for CCS (**see figure 14**). For synchronizing this controller to the multiframe structure

– the time-slot internal flags
– the signals RMFB and XMFB, and
– the signals AFR and AFT (4-kHz DL clock)

may be used.

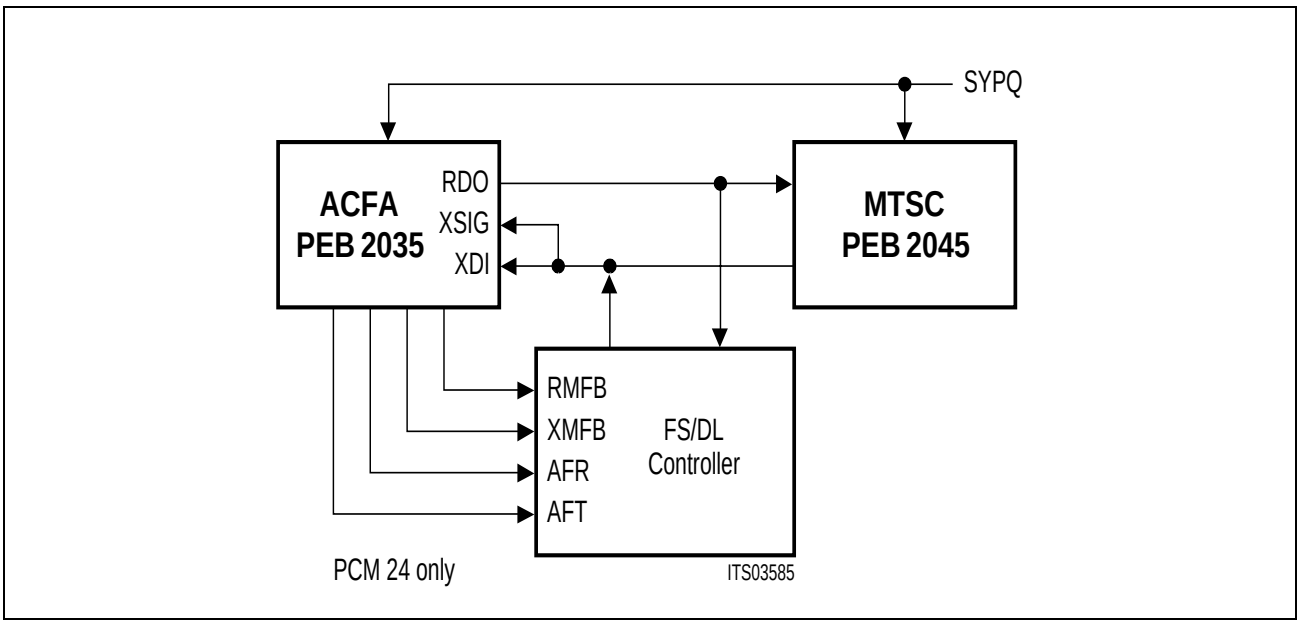


Figure 15
Connection to a Controller in FS/DL-Bit Application

c. Support for Direct Memory Access

Applications: CCS, CAS-CC, CAS-BR

After a DMA request, reading from and writing to the assigned stack must be done twice in the case of PCM 30 mode and three times when PCM 24 mode is enabled.

Further handling of the signaling information is done automatically by the ACFA. In addition to the signals for transfer control (RREQ, XREQ, ACKNLQ), the signals RMFB and XMFB may be used for synchronization.

Acknowledging and clearing pending requests is done in one of the following ways:

XREQ bit EMOD.EDMA = ‘0’: at the end of the first write access to stack XSIG (rising edge of WRQ).
bit EMOD.EDMA = ‘1’: with the beginning of the second (PCM 30) or third (PCM 24) write access to stack XSIG.XREQ is reset with the falling edge of ACKNLQ or CEQ and remains reset if a write cycle to stack XSIG follows. Otherwise, it becomes active again until the second or third access to stack XSIG is provided.

This stack is addressed by
1. address ‘A’ and write command (memory-to-memory DMA transfer)
2. signal: ACKNLQ and write command (memory-to-I/O DMA transfer)

RREQ bit EMOD.EDMA = ‘0’: at the end of the first read access to stack RSIG (rising edge of RDQ).
bit EMOD.EDMA = ‘1’: with the beginning of the second (PCM 30) or third (PCM 24) read access to stack RSIG (falling edge of RDQ).

This stack is addressed by
1. address ‘7’ and a read command (memory-to-memory DMA transfer)
2. signal: ACKNLQ and read command (I/O-to-memory DMA transfer)

Both requests may be triggered at the same time. The sequence of service is determined by the user.

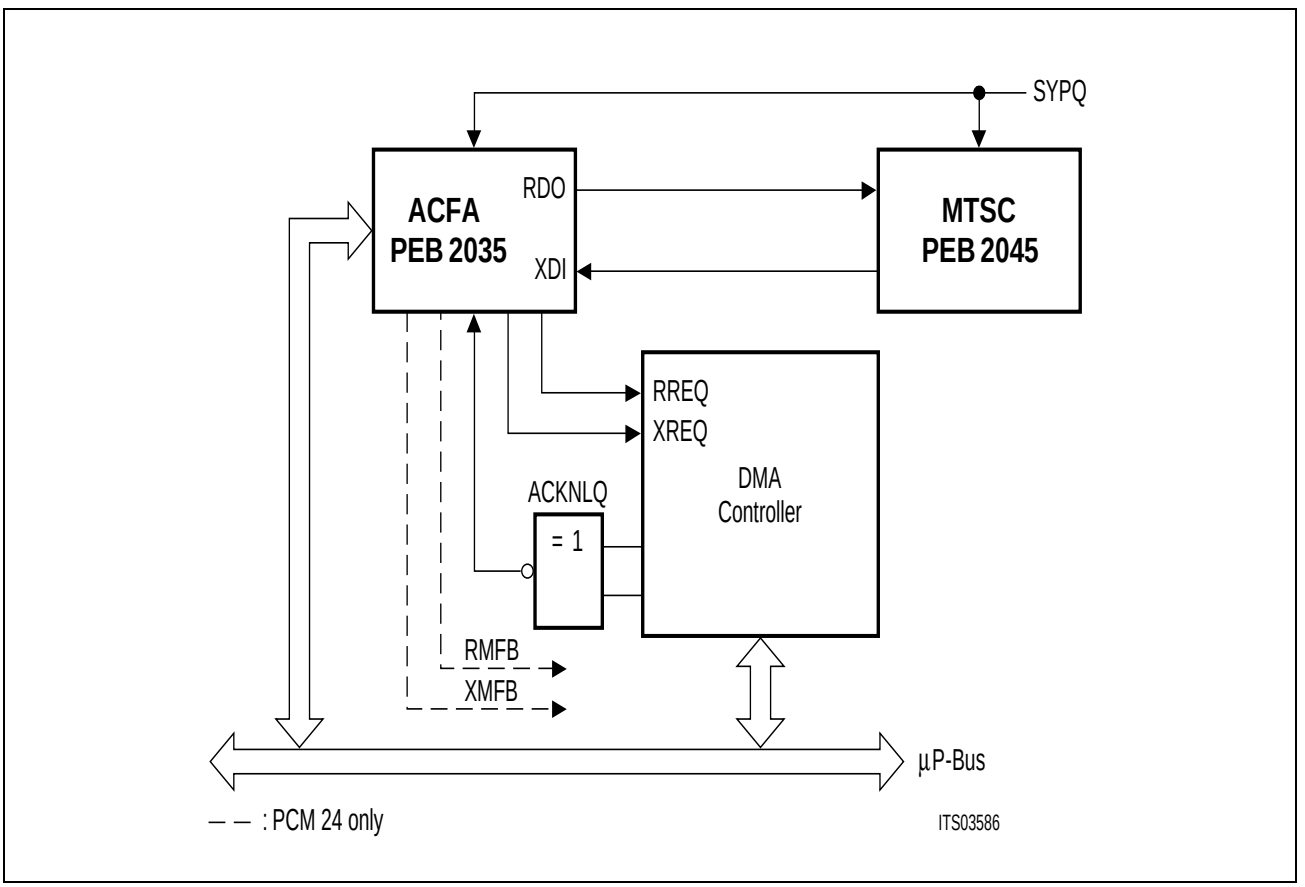


Figure 16
Connection to a DMA Controller

d. Access via Microprocessor

In principle, the use of the microprocessor for signaling tasks is similar to memory-to-memory DMA applications. The request signals RREQ and XREQ indicate the meaning of interrupt requests.

Additionally, in PCM 24 mode the possibility exists to use FS/DL bits for carrying signaling information. In this case, the signals RMFB and XMFB are used as interrupt requests. Acknowledging is done by programming the two interrupt acknowledge bits XFDL.RMAK and XFDL.XMAK.

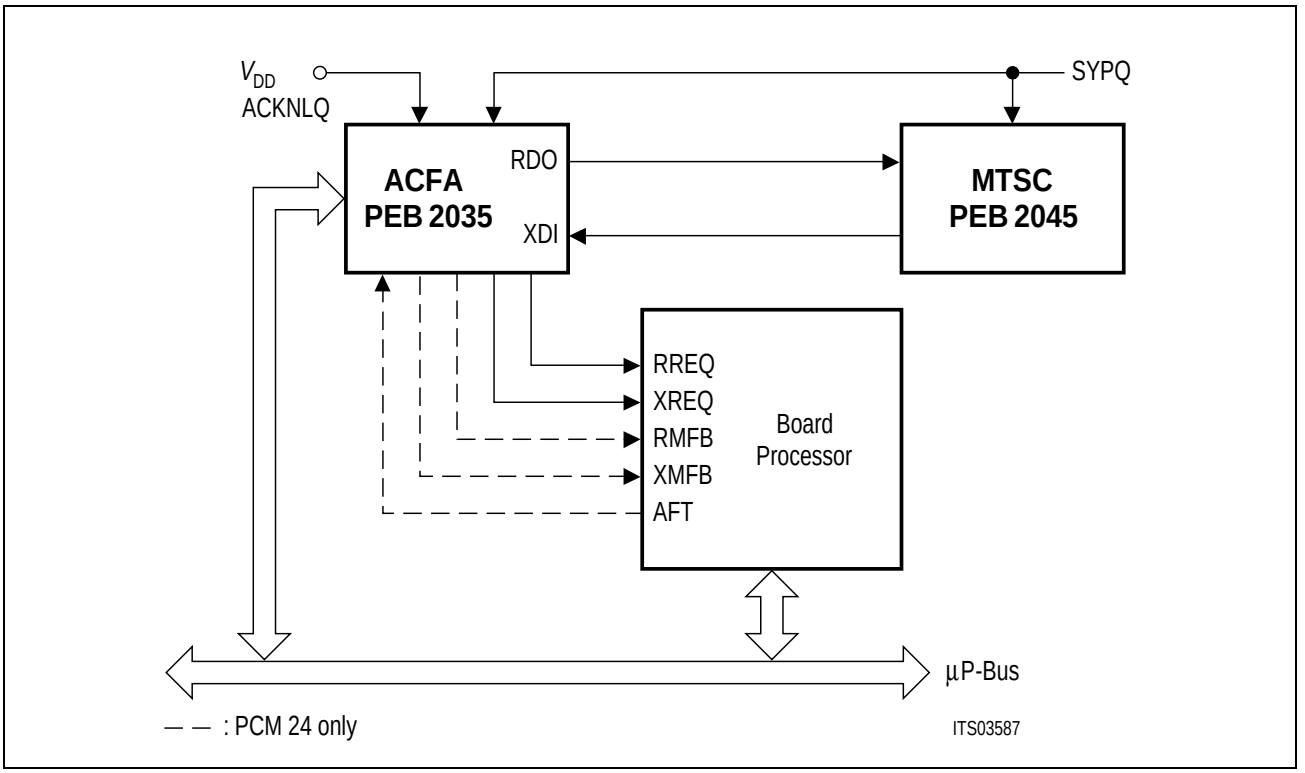


Figure 17
Connection to a Microprocessor for Signaling Applications

Interface to Testing Unit

XTOP	O	Transmit Test Data Out Plus
XTOM	O	Transmit Test Data Out Minus PCM(+) and PCM(–) output signals which may be used for external diagnostic loopback. The output sense is selectable via bit XC0.XTDS.
XRCLK	O	**PCM 30**: as above
RESQ	I	Reset
RCHPY	O	Receive Channel Parity Even/odd parity signal assigned to time-slots on RDO (bit ACR.DLC has to be reset). Its sense is programmed via bit RC0.RPYS.
XCHPY	I	Transmit Channel Parity Even/odd parity signal assigned to time-slots on XDI. This function is enabled via bit XC0.EPY (bits ACR.DLC and ACR.EXMF have to be reset). Its sense is programmed via bit XC0.EPYS.
DFPY	O	**PCM 30**: Doubleframe Parity Even parity signal of the previously received doubleframe.

Interface to Microprocessor

D0-7	I/O	Bidirectional data bus
A0-3	I	Address bus
WRQ	I	Write enable
RDQ	I	Read enable
CEQ	I	Chip enable
COS	I	Carrier Out of Service Initiates transmission of AIS via XDOP, XDOM, and XOID.
AINT	O	Alarm Interrupt If enabled via bit CCR.AINT, this signal may be triggered by any one of the 11 (PCM 30) or 9 (PCM 24) alarm sources configured via register MASK, via bit XC1.MCA, and via bits XSP.MRMB and XSP.MXMB (PCM 30 mode only). Acknowledging is done by writing a '1' to bit LOOP.AIA.
RREQ	O	as above
XREQ	O	as above
RMFB	O	**PCM 24**: as above
XMFB	O	**PCM 24**: as above
AFT	I	**PCM 24**: Additional Function Transmit If bit ACR.EXMF is set, this **input** signal can be used to synchronize the transmitter of the ACFA externally for multiframe begin.

Test Functions

There are three types of monitoring/testing functions:

- Passive tests which do not affect the normal operation of the device (e.g.: parity check)
- Active tests which partly degrade the functionality (e.g.: test loop for a single channel)
- Diagnostics, during which the device is not operational (e.g.: diagnostic loop of an entire trunk).

Alarm Simulation

Alarm simulation does not affect the normal operation of the device, i.e. all channels remain available for transmission. However, possible 'real' alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit CCR.SIM. The following alarms are simulated:

- No signal
- Alarm Indication Signal (AIS)
- Loss of pulse frame
- Remote alarm indication
- Receive slip indication
- Transmit slip indication
- Receive parity error
- Transmit parity error

- Framing error counter
- Code violation counter (HDB3/B8ZS Codes)
- CRC4/6 error counter

Some of the above indications are only simulated if the ACFA is configured in a mode where the alarm is applicable (e.g. no CRC4 error simulation when doubleframe format is enabled).

Controlling the alarm simulation depends on the selected PCM mode:

PCM 30 Mode

Setting of the bit CCR.SIM initiates alarm simulation. Error counting and indication will occurs while this bit is set. After it is reset all simulated error conditions disappear. Alarms like AIS and NOS are cleared automatically. The indications of slips, parity errors and the error counters have to be cleared by setting/resetting corresponding bits of register CCR (CCR.CLR, CCR.CCPY).

PCM 24 Mde

The alarm simulation is controlled by the value of the Alarm Simulation Counter: ASR.SC which is incremented by setting bit: CCR.SIM. Contrary to PCM 30 mode, resetting this bit has no influence on running alarm simulation.

Clearing of alarm indications:

– automatically for NOS, remote alarm, AIS, and loss of synchronization and
– user controlled for slips, parity errors, and error counters via bit CCR.CLR

is only possible at defined counter steps of ASR.SC. For complete simulation (ASR.SC = 0), eight simulation steps are necessary.

Speech Memory Supervision

During normal operation, the receive and transmit paths may be monitored to detect malfunctions by using parity generation/checking and loopback of individual time-slots.

Parity Check

Both the receive and the transmit memories are supervised by a parity bit generation/checking mechanism. A parity bit is generated at the input of the receive (resp. transmit) speech memory and written to the memory along with the eight bit PCM data (in PCM 30 mode the transmit memory is by-passed).

Parity is checked at the memory output and errors are reported via status bits:

- Receive Channel Parity Error: RSR.RPE (PCM 30), ASR.RPE (PCM 24) for the channel selected via register CPY.
- Transmit Channel Parity Error: RSP.XPE (PCM 30), ASR.XPE (PCM 24) for the channel selected via register CPY.
- Global Parity Error: RSP.GPE (PCM 30), MFR.GPE (PCM 24) for all transmit and receive channels.

For the transmit path, the parity bit may optionally be input over pin XCHPY rather than being generated internally (enabled via bit XC0.EPY; input sense selection via bit XC0.EPYS). This parity bit should be fed in simultaneously with bit 8 (LSB) of the corresponding time-slot.

The use of the internal parity generator for the transmit path makes sense only for PCM 24 systems, since for PCM 30 the transmit memory is not operational. An externally generated parity bit (XCHPY) on the contrary, may provide means for monitoring system internal PCM paths for malfunctions, both in PCM 30 and PCM 24 systems.

The parity bit generated at the input of the receive speech memory is output at port RCHPY simultaneously with the corresponding time-slot. The output sense is selectable by bit RC0.RPYS.

Loopback of Time-Slots

Each of the 31 (24) channels may be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one channel at a time selected by register LOOP. In PCM 24 mode, it is possible to enable loop back of ‘pure’ channel data which is input at port XDI, without signaling information supplied at port XSIG (bit LOOP.SLB). This function is permitted in all signaling modes (CCS, CAS-CC and CAS-BR). During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route channel.

For the channel test, sending sequences of test patterns like a 1-kHz check signal should be avoided. Otherwise, an increased occurrence of slips in the tested channel will disturb testing. These slips do not influence the other channels and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

Processor Interface Test

Testing the processor interface will not affect the normal operation of the device. The normally write only control registers may be read in a test mode by setting bit CCR.CRD (except for all acknowledge bits and the PCM 30 S_n-bit stack).

Diagnostic of Receive Speech Memory

The receive speech memory may be tested in the PCM 30 mode by an even parity bit generated over a doubleframe. The doubleframe parity signal is output via pin DFPY.

Diagnostic Loopback

The test outputs XTOP and XTOM give a replica of the normal PCM route outputs and thus enable monitoring of possible malfunctions of the transmission path, even during normal operation. A diagnostic loopback of data may be implemented externally over XTOP and XTOM. During diagnostics, transmission of AIS over XDOP and XDOM (XOID) should be initiated by setting port COS to ‘1’ or setting bit MODE.XAIS to indicate that the PCM route is not available for normal use.In applications with PEB 2235, PEB 2236, IPAT, as the line interface unit for the ACFA, diagnostic loops to remote end and to system internal highway are performed without the need of any additional hardware.

Transparent Mode

The described transparent modes are useful for loopback via the system interface.

PCM 30 Mode

In receive direction, transparency for decoded dual rail data or single rail unipolar data is always achieved if the receiver is in the synchronous state. In asynchronous state the data can be transparently switched through if bit EMOD.DAIS and bit EMOD.RTM are set. However, correct time-slot assignment can not be guaranteed due missing frame alignment.

Transparency in transmit direction can be achieved by activating the time-slot 0 transparent mode (bit XSP.TT0). All internal information of the ACFA (framing, CRC, Sn/Si bit signaling, remote alarm) will be ignored. Only HDB3 data encoding is still provided. For complete transparency the internal signaling stack XSIG has to be disabled.

PCM 24 Mode

Setting bit GCR.TM switches the ACFA in transparent mode:

In receive direction all bits in F-bit position of the incoming multiframe are forewarded to RDO and inserted in the FS/DL time-slot. Bit RDCF (bit 1 of FS/DL time-slot) indicates a DL bit.

In transmit direction bit 8 of the FS/DL time-slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame. For complete transparency the internal signaling stack XSIG has to be disabled and ‘Clear Channels’ have to be defined via registers CCB1 … 3.

Note: For loop back via the system interface (RDO conn. with XDI/XSIG) Channel Translation Mode 0 (MODE.CTM = 0) has to be used to guarantee correct assignment of FS/DL bits to the data of the frame.

5 Operational Description

Reset

The ACFA is forced to the reset state if a low signal is input at port RESQ for a minimum period of 2 ms. During RESET, all output stages are tristated, all internal flip-flops are reset and most of the control registers are initialized with default values.

After RESET, the ACFA is initialized for PCM 30 doubleframe format with register values listed in **table 11**.

Table 11
Initial Values after RESET

Register	Reset Value	Meaning
CCR	00H	Alarm interrupt mode disabled. Double violation detection, no influence on error counting, channel parity alarms, data transmission via port RDO, or synchronization. No alarm simulation. Status register read enabled.
MODE	00H	PCM 30 – doubleframe format with dual rail (RZ) line interface ports, 4 Mbit/s system interface mode, no AIS transmission to remote end. Sn-bit stacks are disabled.
CPY	40H	Channel parity check is active for channel 0.
LOOP	00H	Channel loop back and single frame mode are disabled.
XSW	40H	All bits of the transmitted service word are cleared (bit 2 excl.).
XSP	00H	Spare bit values and additional interrupts are cleared.
XC0	00H	Outputs for transmit dual rail line data and assigned test data are active low, internal signaling stacks and external transmit channel parity are disabled. The transmit clock offset is cleared.
XC1	00H	4096-kHz system clock frequency. The transmit time-slot offset is cleared.
RC0	30H	Even receive channel parity, receive dual rail line data inputs are active low. The receive clock slot offset is cleared. CRC error counter extension is disabled.
RC1	00H	The receive time-slot offset is cleared.
MASK	00H	No interrupt source is enabled.
XSIG	FFH	The transmit signaling stack is cleared. Its values are not readable until the internal signaling mode is enabled.
IDLE	54H	Idle channel code is set to ‘54’ hex.
ICB 1 … 4	00H	Normal operation (no ‘Idle Channel’ selected).
EMOD	00H	No extensions enabled.

If PCM 24 mode is enabled by setting bit MODE.PMOD immediately after RESET goes inactive, the configuration shown in **table 12** is initialized.

Table 12
PCM 24 Mode Configuration if Initialized after RESET

Register	Initiated Value	Meaning
CCR	00H	Alarm interrupt mode disabled, no influence on error counting, channel parity alarms, data transmission via port RDO, or synchronization. No alarm simulation. Status register read is enabled. Type of remote alarm indication via bit 2 = 0 in each speech channel is enabled for the use in F12-format.
MODE	10H	Channel translation mode 0, CCS/CAS-CC signaling support, AMI(ZCS) line code, (CRC6 disabled), dual rail line ports enabled, 4096 kbit/s mode for system internal highway, no AIS towards remote end.
CPY	00H	Channel parity check is active for channel 0. Bank switching is disabled.
LOOP	00H	Channel loop back and loop back of signaling data are disabled.
GCR	40H	Remote alarm indication towards remote end disabled. Non-auto-synchronization mode, F12 multiframing.
XFDL	00H	All FS/DL bits are cleared.
FMR	80H	FS/DL bits are taken from input XDI.
XC0	00H	Outputs for transmit dual rail line data and test data are active low, internal signaling stacks and external transmit channel parity are disabled. The transmit clock-slot offset is cleared.
XC1	00H	4096-kHz system clock frequency. The Transmit time-slot Offset is cleared.
RC0	20H	Even receive channel parity, receive dual rail line data inputs are active low. The receive clock slot offset is cleared. Output FREEZS is enabled. CRC counter extension is disabled.
RC1	00H	The receive time-slot offset is cleared.
MASK	00H	No interrupt source is enabled.
XSIG	FFH	The transmit signaling stack is cleared. Its values are not readable until the internal signaling mode is enabled.
IDLE	FFH	Idle channel code is set to ‘FF’ hex.
ICB 1 … 3	00H	Normal operation (no ‘Idle Channels’ selected).
CCB 1 … 3	00H	Normal operation (no clear channel operation).
EMOD	00H	No extension enabled.
ACR	70H	No extension enabled.

Operational Phase

The ACFA is programmable via a microprocessor interface (eight-bit bidirectional data bus and a four-bit address bus) which enables access to 22 control and 10 status registers in PCM 24 mode and 19 control and 11 status registers in PCM 30 mode.

After RESET, the ACFA is set to PCM 30 mode. Switching to PCM 24 mode is performed by programming the bit MODE.PMODE. In each mode, the ACFA first must be initialized. General guidelines for initialization are described in section Initialization.

The control registers are normally write-only. They can be read by setting bit CCR.CRD. The status registers are read-only and are continuously updated. Normally, the processor periodically reads the status registers to analyze the alarm status and signaling data. For advanced error handling, up to eight alarm sources may trigger the programmable output AINT.

The ACFA generates signals which mark the position of the signaling bits on the system internal highway. To transfer signaling via the microprocessor interface (board processor or DMA controller), specially generated output signals may be used as interrupts or DMA requests.

Initialization

For a correct start up of the Primary Access Interface a set of parameters specific to the system and hardware environment must be programmed after RESET goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in CCITT and DMI recommendations (e.g. Fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 13** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, may be programmed simultaneously with one exception: The **PCM mode** (MODE.PCM) has to be selected **first**.

Table 13
Initialization Parameters

Basic Set Up	PCM 30	PCM 24
AIS to Remote End	port: COS	port: COS
PCM mode	MODE.PMOD	MODE.PMOD
System clock frequency	XC1.SCLK	XC1.SCLK
Specification of line outputs	XC0.XDOS, EMOD.XFB	XC0.XDOS, EMOD.XFB
System interface mode	MODE.IMOD	MODE.IMOD
Channel translation mode		MODE.CTM
Transmit offset counters	XC0.XCO, XC1.XTO	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO	RC0.RCO, RC1.RTO
AIS to system interface	CCR.SAIS, EMOD.DAIS	CCR.SAIS, EMOD.DAIS
Line interface mode	MODE.OPT	MODE.OPT
Sense of line inputs	RC0.RDIS	RC0.RDIS

Operational Set Up	PCM 30	PCM 24
Select framing	MODE.CRC	GCR.FM1, GCR.FM0
Framing additions	(EMOD.DFSN)	MODE.CRC, CCR.SRAF
Synchronization mode	RC1.ASY4, RC1.SWD	GCR.AUTO, RC1.SLC
	MODE.AFR	EMODE.SSP, ACR.EXMF
Signaling mode		MODE.SIGM
General signaling	XSP, XSW	FMR, XFDL, ACR.DLC

Options	PCM 30	PCM 24
Internal signaling stacks	XC0.ISIG, XSIG, EMOD.EDMA	XC0.ISIG, XSIG, EMOD.EDMA
Alarm interrupt mode	MASK, CCR.AINT, XC1.MCA	MASK, CCR.AINT, XC1.MCA
	XSP.MXMB/MRMB	
Testdata output sense	XC0.XTDS	XC0.XTDS
Idle channel code	IDLE	IDLE
Addition for dual rail input	CCR.FULL	
General signaling (Sn-bit stacks)	MODE.ENSN, XSN	
	EMOD.DFSN	
Parity configuration	XC0.EPY, XC0.EPYS,	XC0.EPY, XC0.EPYS,
	RC0.RPYS	RC0.RPYS
Special functions	EMOD.ESEI	GCR.CRCI/AISM, ACR.DLC, RC1.RRAM
Transparent mode	XSP.TT0 / TT0S	GCR.TM
	EMOD.TT0X / RTM	

Features like channel loop back, idle channel activation, clear channel activation (PCM 24 only), channel parity check, extensions for signaling support, alarm simulation, … may be activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

6 Detailed Register Description

PCM 30 Mode

Register Address Arrangement

Table 14
PCM 30 Register Address Arrangement

Address	Read	Write	Comment	
0	RSR	CCR	Receive Status Register	/ Common Control Register
1	FEC	MODE	Framing Error Counter	/ Mode Register
2	CVC	CPY	Code Violation Counter	/ Channel Parity Check
3	CEC	LOOP	CRC Error Counter	/ Channel Loop Back
4	RSW	XSW	Receive Service Word	/ Transmit Service Word
5	RSP	XSP	Receive Spare Bits, Additional Status	/ Transmit Spare Bits
6	ARS	XC0	Additional Receive Status	/ Transmit Control 0
7	RSIG	XC1	Receive Signaling Stack	/ Transmit Control 1
8	SEI	RC0	Sub Multiframe Error Indication	/ Receive Control 0
9	CECX	RC1	CRC Error Counter Extension	/ Receive Control 1
A	–	XSIG	–	/ Transmit Signaling Stack
B	RSN	XSN	Receive Sn-Bit Stack	/ Transmit Sn-Bit Stack
C	–	MASK	–	/ Alarm Interrupt Mask
D	–	IDLE	–	/ Idle Channel Code
E, F	–	–	NO ACCESS ALLOWED	

Bank switching (CPY.SW = 1)

1	FEC	EMOD	Framing Error Counter	/ Extended Mode Register
6	ARS	ICB1	Additional Receive Status	/ Idle Channel Bank 1
7	RSIG	ICB2	Receive Signaling Stack	/ Idle Channel Bank 2
8	SEI	ICB3	Sub Multiframe Error Indication	/ Idle Channel Bank 3
9	CECX	ICB4	CRC Error Counter Extension	/ Idle Channel Bank 4

After ‘RESET’ the ACFA is automatically set to PCM 30 mode. All control registers (except XSN) are initialized to defined values.

Switching to PCM 24 mode is done by setting bit MODE.PMOD to ‘1’. The idle channel code IDLE will be set to ‘FF’. All other control bits will retain their previous values.

The control registers are normally only writeable. In a test mode they may be read by setting bit CCR.CRD (exceptions: bits LOOP.AIA, XSN7 … 0, XFDL.XMAK, XFDL.RMAK).

The status registers are only readable and are updated by the ACFA.

Register Definitions

PCM 30 Control Registers

Common Control Register (WRITE)
Value after RESET: 00H

	7							0	
CCR	AINT	EXTD	CRD	CLR	SAIS	CCPY	FRS	SIM	(00)

AINT … Enable Alarm Interrupt Mode

Setting this bit switches the output DFPY to the alarm interrupt function (AINT). Acknowledging is done by setting bit LOOP.AIA. Programming the mask register MASK and the additional bits XSP.MXMB, XSP.MRMB and XC1.MCA selects the interrupt sources.

EXTD … Extended HDB3 Error Detection

Selects error detection mode.
0 … Only double violations are detected.
1 … Extended code violation detection: 0000 strings are detected additionally. Thereafter, incrementation of Code Violation Counter CVC is first done after receiving an additional four zeros.

CRD … Enable Control Register Read

0 … Normal operation (status register read enabled).
1 … Enables control register read.

CLR … Disable/Clear Error Counters

This bit must be set 1 µs before reading the error counters FEC, CVC, CEC. Clearing the bit will reset these counters and the DMA slip indication (RSP.DSLP). Errors will be ignored while this bit is active.

SAIS … Send AIS Towards System Interface

Send AIS via output RDO towards system interface. This function is not influenced by bit EMOD.DAIS.

CCPY … Clear Channel Parity Alarm Latch

A ‘1’ resets the parity alarm flags: RSR.RPE, RSP.GPE, RSR.XPE.

FRS … Force Resynchronization

A transition from low to high will initiate a resynchronization procedure of the pulse frame and the CRC-multiframe (if enabled via bit MODE.CRC) starting directly after the old framing candidate.

SIM … Alarm Simulation

0 … Normal operation.
1 … Initiates internal error simulation of AIS, no signal, loss of synchronization, slip, parity, framing errors, CRC errors, and code violations. The error counters FEC, CVC, CEC will be incremented.

Mode Register (WRITE)

Value after RESET: 00H

	7							0	
MODE	MFCS	AFR	ENSN	PMOD	CRC	OPT	IMOD	XAIS	(01)

MFCS … Multiframe Force Resynchronization

Only valid if CRC multiframe format is selected.
A transition from low to high will initiate the resynchronization procedure for CRC-multiframe alignment without influencing doubleframe synchronous state. In case, 'Automatic Force Resynchronization' (MODE.AFR) is enabled and multiframe alignment can not be regained a new search of doubleframe (and CRC multiframe) is automatically initiated.

AFR … Automatic Force Resynchronization

Only valid if CRC multiframe format is selected.
If this bit is set, a search of doubleframe alignment is automatically initiated if two multiframe pattern with a distance of n × 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained or command MODE.MFCS has been issued.

ENSN … Enable S_n-Bit Stack

Only applicable if MODE.CRC is set to one.
0 … Normal operation. The S_a-bit information will be taken from bits XSW.XY0 … 4 and written to bits RSW.RY0 … 4.

1 … S_a-bit stack mode. The S_a-bit information will be taken from the stack XSN. In addition, the received information will be written to stack RSN. Transmitting contents of XSN will be disabled if one of time-slot 0 transparent modes is enabled (XSP.TT0, XSP.TT0S, EMOD.TT0X).

PMOD … PCM Mode

0 … PCM 30 mode.
1 … PCM 24 mode.

CRC … Enable CRC Multiframe

0 … Doubleframe format enabled.
1 … and EMOD.DFSN = 0: CRC-multiframe format enabled.
and EMOD.DFSN = 1: Doubleframe format (with internal 16-frame structure) for access to Sn-bit stacks RSN and XSN.

OPT … Enable Optical Interface

0 … RZ dual rail line ports RDIP, RDIM, XDOP, XDOM are enabled.
1 … NRZ line ports ROID, XOID are enabled for connection to fibre optical transmission systems. There is no code violation detection for this unipolar data.

IMOD … System Interface Mode

0 … 4 Mbit/s mode.
1 … 2 Mbit/s mode.

XAIS … Transmit AIS Towards Remote End

Send AIS via ports XDOP, XDOM, XOID towards the remote end. The test data outputs XTOP, XTOM are not affected.

Channel Parity Check (WRITE)

Value after RESET: 40H

	7				0	
CPY	SW	1	DCPY	CPA4 …	CPA0	(02)

SW … Enable Bank Switching

0 … Normal operation. Control register addresses 01, 06 to 09 select registers MODE, XC0, XC1, RC0, and RC1.
1 … Access to Extended Mode Register EMOD and the idle channel registers ICB1, ICB2, ICB3, and ICB4 is enabled.

DCPY … Disable Channel Parity Check

0 … Normal operation.
1 … Disables the channel parity check selected by this register. This bit should be set at least one time-slot before changing the channel address.

CPA4 … CPA0 … Channel Address For Parity Check

CPA = 0 … 31 selects the channel.

Channel Loop Back (WRITE)

Value after RESET: 00H

	7							0	
LOOP	AIA	SFM	DLOP	CLA4				CLA0	(03)

AIA … Alarm Interrupt Acknowledge

(NOT READABLE)
A ‘1’ written to this bit location clears the alarm interrupt signal at port AINT if the alarm interrupt mode is enabled via bit CCR.AINT and register MASK, XSP.MXMB, XSP.MRMB or XC1.MCA. Resetting this bit is not necessary.

SFM … Single Frame Mode

Setting this bit reduces the receive speech memory from two to one frame length. In this case, clocks SCLK and RRCLK have to be phase locked to avoid slip conditions. However, slip detection still works but without any influence on data transmission.

DLOP … Disable Channel Loop Back

0 … Normal operation
1 … Disables the channel loop back selected by this register. This bit should be set at least one time-slot before changing the channel address.

CLA4 … CLA0 … Channel Address For Loop Back

CLA = 1 … 31 selects the channel.
CLA = 0 disables channel loop back.
During looped back the contents of the assigned outgoing channel at ports XDOP, XDOM, XOID is equal to the idle channel code programmed at register IDLE.

Transmit Service Word Pulseframe (WRITE)

Value after RESET: 40H

	7							0	
XSW	XSIS	1	XRA	XY0	XY1	XY2	XY3	XY4	(04)

XSIS … Spare Bit For International Use

First bit of the service word. Only significant in doubleframe format. If not used, this bit should be fixed to '1'. If one of the time-slot 0 transparent modes is enabled (bit XSP.TT0, XSP.TT0S or EMOD.TT0X), bit XSW.XSIS will be ignored.

XRA … Transmit Remote Alarm

0 … Normal operation.
1 … Send remote alarm towards remote end by setting bit 3 of the service word.
If time-slot 0 transparent mode is enabled via bit XSP.TT0, bit XSW.XRA will be ignored.

XY0 … XY4 … Spare Bits For National Use (Y-Bits, S_n-Bits, S_a-Bits)

n These bits are inserted in the service word of every other pulseframe if Sn-bit stack mode is disabled (MODE.ENSN = 0). If not used, they should be fixed to '1'.
If one of the time-slot 0 transparent modes is enabled (bit XSP.TT0, XSP.TT0S or EMOD.TT0X), bits XSW.XY0 … 4 will be ignored.

Transmit Spare Bits (WRITE)

Value after RESET: 00H

	7							0	
XSP	MXMB	MRMB	TT0	TT0S	AXS	XSIF	XS13	XS15	(05)

MXMB … Interrupt Mask: Transmit Multiframe Begin

MRMB … Interrupt Mask: Receive Multiframe Begin

If the alarm interrupt mode is enabled via bit CCR.AINT, these mask bits select transmit and receive multiframe begin as interrupt sources (applicable to doubleframe and CRC multiframe structure):
Mask bit = 0: interrupt source disabled.
Mask bit = 1: interrupt source enabled.
Assigned multiframe status will cause an interrupt signal at port AINT. Acknowledging is done by writing a '1' to the bit LOOP.AIA or with a read/write access to the assigned Sn-bit stack address (refer to bits RSP.XFLG and RSP.RFLG). Triggering a new interrupt by the same source is only possible after this source became inactive.

TT0 … Time-Slot 0 Transparent Mode

0 … Normal operation.
1 … All information of time-slot 0 at port XDI will be inserted in the outgoing pulseframe. All internal information of the ACFA (framing, CRC, S_n/S_i bit signaling, remote alarm) will be ignored. This function is mainly useful for system test applications (test loops).
Priority sequence of transparent modes: XSP.TTO > EMOD.TT0X > XSP.TT0S.

TT0S … Time-Slot 0 Signaling Transparent Mode

0 … Normal operation.
1 … All information of time-slot 0 at port XDI in S_n/S_i -bit position (bit 1, 4 … 8) will be inserted in assigned S_n/S_i -bit positions of the outgoing pulseframe. The internal information of the ACFA (Sn/Si bit information of registers XSW and XSP and S_n-bit stack XSN) will be ignored.
Priority sequence of transparent modes: XSP.TTO > EMOD.TT0X > XSP.TT0S.

AXS … Automatic Transmission of Submultiframe Status

Only applicable to CRC multiframe.
0 … Normal operation.
1 … Information of submultiframe status bits SEI.SI1 and SEI.SI2 will be automatically inserted in S_i -bit positions of the outgoing CRC multiframe (SEI.SI1 $\rightarrow$ S_i -bit of frame 13; SEI.SI2 $\rightarrow$ S_i -bit of frame 15). Contents of XSP.XS13 and XSP.XS15 will be ignored.
If one of the time-slot 0 transparent modes XSP.TT0 or XSP.TT0S is enabled, bit XSP.AXS has no function.

XSIF … Transmit Spare Bit For International Use (FAS Word)

First bit in the FAS word. Only significant in doubleframe format. If not used, this bit should be fixed to ‘1’. If one of the time-slot 0 transparent modes is enabled (bits XSP.TT0, XSP.TT0S or EMOD.TT0X), bit XSP.XSIF will be ignored.

XS13 … Transmit Spare Bit (Frame 13, CRC-Multiframe)

First bit in the service word of frame 13 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to ‘1‘. The information of XSP.XS13 will be shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe (refer to RSP.XFLG).
If automatic transmission of submultiframe status is enabled via bit XSP.AXS, or, if one of the time-slot 0 transparent modes XSP.TT0 or XSP.TT0S is enabled, bit XSP.XS13 will be ignored.

XS15 … Transmit Spare Bit (Frame 15, CRC-Multiframe)

First bit in the service word of frame 15 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to ‘1‘. The information of XSP.XS15 will be shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe (refer to RSP.XFLG).
If automatic transmission of submultiframe status is enabled via bit XSP.AXS, or, if one of the time-slot 0 transparent modes XSP.TT0 or XSP.TT0S is enabled, bit XSP.XS15 will be ignored.

Transmit Control 0 (WRITE)

Value after RESET: 00H

	7						0	
XC0	XDOS	ISIG	EPY	EPYS	XTDS	XCO2	XCO0	(06)

XDOS … Transmit Data Output Sense

0 … Outputs XDOP, XDOM are active low. Output XOID is active high.
1 … Outputs XDOP, XDOM are active high. Output XOID is active low.

ISIG … Enable Internal Signaling Stack

0 … Normal operation. The signaling data are taken from/sent to the system internal PCM highway, time-slot 16 at ports XDI/RDO.
1 … Enables the use of the signaling stacks RSIG and XSIG. Two bytes of received signaling information from time-slot 16 are stored in the stack RSIG, the two bytes of signaling information from the stack XSIG are one after the other inserted in time-slot 16 of the outgoing PCM frame. Access to these stacks is requested by the signals at ports RREQ and XREQ. They may be used either as interrupt or DMA request signals. Acknowledging is done with the end of the first or the beginning of the second read resp. write access to these stacks depending on the value of bit EMOD.EDMA. For I/O-to-memory DMA transfer, the input signal at port ACKNLQ should be used for direct access to the stacks. This eliminates the need for generating the chip enable signal (port CEQ).

EPY … Enable External Transmit Channel Parity Input

0 … Normal operation.
1 … An externally generated channel parity signal will be read via port XCHPY and compared with the internally generated channel parity bit. To avoid difficulties with external parity generation, the parity value for signaling data is generated internally.

EPYS … External Transmit Channel Parity Sense

0 … Even parity.
1 … Odd parity.

XTDS … Transmit Testdata Sense

0 … Outputs XTOP, XTOM active low.
1 … Outputs XTOP, XTOM active high.

XCO2 … XCO0 … Transmit Clock Slot Offset

Initial value loaded into the transmit bit counter at the trigger edge of SCLK when the synchronous pulse at port SYPQ is active (**see figure 6**).

Transmit Control 1 (WRITE)

Value after RESET: 00H

	7						0	
XC1	SCLK	MCA	XTO5				XTO0	(07)

SCLK … Select System Clock

0 … If the system clock at port SCLK is 4096 kHz.
1 … If the system clock at port SCLK is 8192 kHz.

MCA … Mask: CRC Alarm

Only valid if CRC multiframe is selected.
If this bit is set, the occurrence of a CRC error (one per submultiframe maximum) triggers the interrupt port AINT if enabled via CCR.AINT.

XTO5 … XTO0 … Transmit Time-Slot Offset

Initial value loaded into the transmit time-slot counter at the trigger edge of SCLK when the synchronous pulse at port SYPQ is active (**see figure 6**).

Receive Control 0 (WRITE)

Value after RESET: 30H

	7							0	
RC0	ECE	RPYS	1	1	RDIS	RCO2		RCO0	(08)

ECE … Enable CRC Counter Extension

0 … Normal operation. CRC errors are counted at status register CEC (8-bit length) with a maximum value of 255 (‘FF’ hex).
1 … Extended CRC error counting with additional counter stages (bits CECX.CE8 and CECX.CE9, 10 bit counter). Maximum value is 1023 ‘3FF’ hex) which is also valid for interrupt generation if enabled.

RPYS … Receive Parity Sense

0 … Even parity.
1 … Odd parity.

RDIS … Receive Data Input Sense

0 … Inputs RDIP, RDIM are active low, input ROID is active high.
1 … Inputs RDIP, RDIM are active high, input ROID is active low.

RCO2 ... RCO0 ... Receive Clock-Slot Offset

Initial value which is loaded into the receive bit counter at the trigger edge of SCLK when the synchronous pulse at port SYPQ is active (**see figure 5**).

Receive Control 1 (WRITE)

Value after RESET: 00H

	7			0	
RC1	SWD	ASY4	RTO5	RTO0	(09)

SWD ... Service Word Condition Disable

0 ... Standard operation. Three or four consecutive incorrect service words (depending on bit RC1.ASY4) will cause loss of synchronization.
1 ... Errors in service words have no influence when in synchronous state. However, they are used for the resynchronization procedure.

ASY4 ... Select Loss of Sync Condition

0 ... Standard operation. Three consecutive incorrect FAS words or three consecutive incorrect service words will cause loss of synchronization.
1 ... Four consecutive incorrect FAS words or four consecutive incorrect service words will cause loss of synchronization.
The service word condition may be disabled via bit RC1.SWD.

RTO5 ... RTO0 ... Receive Time-Slot Offset

Initial value which is loaded into the receive time-slot counter at the trigger edge of SCLK when the synchronous pulse at port SYPQ is active (**see figure 5**).

Transmit Signaling Stack (WRITE)

Value after RESET: 00H, 00H (not readable if XC0.ISIG = 0)

	7		0	
XSIG	XS7		XS0	(0A)

XS7 … XS0 … Transmit Signaling Data

If the use of the internal signaling registers is enabled via bit XC0.ISIG, the contents of this 2-byte stack will be sent one after the other in time-slot 16 of the outgoing PCM frame. A (DMA/interrupt) request at port XREQ requires loading the stack with two bytes of signaling data. If the ACFA requires new information before a pending request has been answered, the DMA slip indication RSP.DSLP will be set.

Access to this stack is possible
– via a normal write cycle to the chip address location plus stack address (0A Hex), or
– via a direct write access with the signal at port ACKNLQ as access enable in conjunction with a write cycle without the need of generating the chip enable signal at port CEQ. This feature is useful for memory-to-I/O transfer.
If request XREQ is ignored, transmission of the second byte will be repeated until a new information is written to the stack. Although the DMA slip indication RSP.DSLP has been set, function of stack RSIG is unchanged. The function simplifies realization of HDLC procedures via microprocessor interface (idle code transmission etc.).

Transmit S_a- Bit Stack (WRITE)

Value after RESET: undefined

	7		0	
XSN	XSN7		XSN0	(0B)

XSN7 … XSN0 … Transmit S_n-Bit Data

(NOT READABLE)

If the Sn-bit stack mode is enabled by setting bits MODE.CRC = 1 and MODE.ENSN = 1, the

transmit multiframe flag RSP.XFLG requests that five bytes of Sn-bit information be written to this stack. In addition, a transmit multiframe begin interrupt may be generated by setting bits CCR.AINT and XSP.MXMB. Contents of this stack will be sent in the service words of the next outgoing CRC multiframe (or doubleframe) if none of the time-slot 0 transparent modes is enabled. The first byte written to this stack contains the information for the eight XY4-bits per multiframe (bit slot 8 of every service word). XSN7 will be sent out in frame 1, XSN0 in frame 15.
If requests for new information will be ignored, current contents will be repeated.

Alarm Interrupt Mask Register (WRITE)

Value after RESET: 00H

	7							0	
MASK	MLOS	MAIS	MNOS	MRRA	MSLP	MCEC	MFEC	MCVC	(0C)

MLOS … Mask: Loss Of Synchronization
MAIS … Mask: Alarm Indication Signal
MNOS … Mask: No Signal
MRRA … Mask: Receive Remote Alarm
MSLP … Mask: Receive Slip Indication
MCEC … Mask: CRC Error Counter Saturation
MFEC … Mask: Framing Error Counter Saturation
MCVC … Mask: Code Violation Counter Saturation

If the alarm interrupt mode is enabled via bit CCR.AINT this mask register selects the alarm sources:
Mask bit = 0: alarm source disabled.
Mask bit = 1: alarm source enabled.
Assigned alarms will cause an interrupt signal at port AINT. Acknowledging is done by writing a '1' to the bit LOOP.AIA. Triggering a new interrupt by the same source is possible only after this source has been inactive.

Idle Channel Code Register (WRITE)

Value after RESET: 54H

	7							0	
IDLE	IDL7							IDL0	(0D)

IDL7 … IDL0 … Idle Channel Code

If channel loop back is enabled by programming the register LOOP, the contents of the assigned outgoing channel at ports XDOP, XDOM, XOID is set equal to the idle channel code selected by this register.
Additionally, the specified pattern overwrites the contents of all channels selected via the idle channel register bank ICB1 … ICB4.
Its initial value (54 Hex) may be overwritten via the microprocessor interface.

Bank Switching

After setting bit CPY.SW, control register addresses 01, 06 to 09 point to additional control registers.

Extended Mode Register (WRITE)

Only accessible if CPY.SW = 1.
Value after RESET: 00H

	7							0	
EMOD	DFSN	TT0X	RTM	ESEI	ECVE	XFB	EDMA	DAIS	(01)

DFSN … Doubleframe S_a- Bit Stack Mode

No function if MODE.CRC = 0.
If MODE.CRC is set to one, the multiframing structure is determined by

– EMOD.DFSN = 0: CRC-multiframe format
– EMOD.DFSN = 1: Doubleframe format with internal 16-frame structure. This structure is not transparent to the user except status flags RSP.XFLG/RFLG and multiframe begin interrupts (see CCR.AINT, XSP.MXMB/MRMB). This new addition is implemented to enable usage of S_a-bit stacks RSN and XSN (MODE.ENSN) in conjunction with the“ doubleframe format.

TT0X … Time-Slot 0 Extended Signaling Transparent Mode

0 …Normal operation.
1 … All information of time-slot 0 at port XDI in S_a-bit position (bits 4 … 8) will be inserted in assigned S_a bit positions of the outgoing pulseframe. The internal information of the ACFA (S_a-bit information of registers XSW and XSP and S_a-bit stack XSN) will be ignored. Priority sequence of transparent modes: XSP.TTO > EMOD.TT0X > XSP.TT0S.

RTM … Receive Transparent Mode

Setting this bit disconnects control of the internal speech memory from the receiver. The speech memory is now in a ‘free running’ mode without any possibility to actualize the time slot assignment to a probably new frame position in case of re-synchronization of the receiver. This function can be used in conjunction with the ‘disable AIS to system interface’ feature (EMOD.DAIS) to realize undisturbed transparent reception, e.g. for applications such as HDB3 decoder.

ESEI … Enable Submultiframe Error Indication Counter

Only valid if CRC-multiframe format is selected.
If bit ESEI is set, counter CVC (8 or 10 bits) counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. There is no difference in comparison to other counters for reading and resetting this counter and interrupt generation in case of counter

ECVE … Enable Code Violation Counter Extension

0 … Normal operation. Maximum value of counter CVC (8 bit length): 255 (‘FF’ hex).
1 … Additional stages (CECX.CV8 and CECX.CV9) enlarge CVC to a 10 bit counter. Maximum value: 1023 (‘3FF’ hex) which is also valid for interrupt generation if enabled.

XFB … Transmit Full Bauded Mode

0 … Output signals XDOP, XDOM are half bauded (normal operation).
1 … Output signals XDOP, XDOM are full bauded.

EDMA … Extended DMA Mode

0 … DMA request lines RREQ and XREQ are reset at the end of the first read/write access to the assigned stack (rising edge of RDQ/WRQ).
1 … DMA request lines RREQ and XREQ remain active until the beginning of the second read/write access to the assigned stack. RREQ is reset with the falling edge of RDQ.XREQ is reset with the falling edge of ACKNLQ or CEQ and remains reset if a write cycle to stack XSIG follows. Otherwise, it becomes active again until the second access to XSIG is provided.

DAIS … Disable AIS to System Interface

0 … AIS is automatically inserted into the data stream to RDO if ACFA is in asynchronous state.
1 … Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit CCR.SAIS.

Idle Channel Register Bank (WRITE)

Only accessible if CPY.SW = 1.
Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	(06)
ICB2	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16	(07)
ICB3	IC17	IC18	IC19	IC20	IC21	IC22	IC23	IC24	(08)
ICB4	IC25	IC26	IC27	IC28	IC29	IC30	IC31	IC32	(09)

IC1 … IC32 … Idle Channel Selection Bits

These bits define the channels (time-slots) of the outgoing PCM frame to be altered.
Assignments:
IC1 → time-slot 0
IC2 → time-slot 1

IC32 → time-slot 31

0 … Normal operation.
1 … Idle channel mode. The content of the selected time-slot is overwritten by the idle channel code defined via register IDLE.

Note: Although time-slot 0 can be selected via bit IC1, its content is only altered if one of the transparent modes is selected (XSP.TT0, XSP.TT0S or EMOD.TT0X).

PCM 30 Status Registers

Receive Status Register (READ)

	7							0	
RSR	NOS	AIS	LOS	RRA	SLP	RPE	CAL	SDI	(00)

NOS … No Signal Indication

This bit is set when
– 3 or less ones are received in a time interval of 250 µs, or
– a receive route clock pulse (port RRCLK) fails to occur in a time interval of 4 internal SCLK clock cycles (4096 kHz).
The bit will be reset when no alarm condition is detected. The bit will also be set during alarm simulation and reset if CCR.SIM is cleared and no alarm condition exists.

After resynchronization has been regained (RSR.LOS = 0), NOS should be ignored for 250 µs.

AIS … Alarm Indication Signal

This bit is set when two or less zeros in the received bit stream are detected in a time interval of 250 µs. The bit will be reset when no alarm condition is detected.
The bit will also be set during alarm simulation and reset if CCR.SIM is cleared and no alarm condition exists.
After resynchronization has been regained (RSR.LOS = 0), AIS should be ignored for 250 µs.

LOS … Loss Of Synchronization

This bit is set after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (can be disabled). The specification of the loss of sync conditions is done via bits RC1.SWD and RC1.ASY4. After loss of synchronization, the frame aligner will resynchronize automatically. The following conditions have to be detected to regain synchronous state:
– the presence of the correct FAS word in frame n
– the presence of the correct service word (bit 2 = 1) in frame n + 1
– for a second time the presence of a correct FAS word in frame n + 2
The bit is cleared when synchronization has been regained (directly after the second correct FAS word of the procedure described above has been received).
If the CRC-multiframe structure is enabled by setting bit MODE.CRC, multiframe alignment is assumed to be lost if pulseframe synchronization has been lost. The resynchronization procedure for multiframe alignment starts after the bit RSR.LOS has been cleared. Multiframe alignment has been regained if two consecutive CRC-multiframes have been received without a framing error (refer to RSR.CAL).
The bit will be set during alarm simulation and reset if CCR.SIM is cleared and no alarm condition exists.
In case no signal alarm (RSR.NOS) has been triggered by loss of route clock condition, RSR.LOS will be set, too. It will be reset if ACFA stays at synchronous state and the ‘No Signal’ alarm disappears.

RRA … Receive Remote Alarm

Set if bit 3 of the received service word is set. RSR.RRA will be cleared when no alarm is detected. The bit RSW.RRA has the same function.
Both bits will be set during alarm simulation and reset if CCR.AINT is cleared.

SLP … Receive Slip Indication

Toggles when the difference between the receive route clock RRCLK and the system clock SCLK caused a received frame to be repeated or discarded.
This bit will toggle only once during alarm simulation.

RPE … Receive Parity Error

Set when a parity error occurs in the received channel selected by register CPY. It is cleared by setting bit CCR.CCPY.
The bit will be set during alarm simulation and must be cleared by setting bit CCR.CCPY.

CAL … CRC4 Alarm

Not used in doubleframe format (MODE.CRC = 0 or MODE.CRC = 1 **and** EMOD.DFSN = 1). In this case, set to logical '1'.
In CRC-multiframe mode (MODE.CRC = 1 **and** EMOD.DFSN = 0), this bit is set
– if force resynchronization is initiated by setting bit CCR.FRS, or
– if multiframe force resynchronization is initiated by setting bit MODE.MFCS, or
– if pulseframe alignment has been lost (RSR.LOS).
It is reset if two CRC-multiframes have been received at an interval of n × 2 ms (n = 1, 2, 3 …) without a framing error.

SDI … Slip Direction Indication

This bit is actualized if the receive slip indication (RSR.SLP) toggles:
0 … Negative slip: flags that the frequency of Receive Route Clock RRCLK is greater than the frequency of internal system clock → a frame will be skipped.
1 … Positive slip: flags that the frequency of receive route clock is less than the frequency of internal system clock → a frame will be repeated.

Framing Error Counter (READ)

	7						0	
FEC	FE7						FE0	(01)

FE7 … FE0 … Framing Errors

This 8-bit counter will be incremented when a FAS word has been received with an error. Framing errors will not be counted during asynchronous state. A counter overflow will be inhibited. During alarm simulation, the counter is incremented every 250 µs up to its saturation. Disabling the counter is done by setting bit CCR.CLR; clearing is done by resetting it.

Code Violation Counter (READ)

	7						0	
CVC	CV7						CV0	(02)

CV7 ... CV0 ... Code Violations

The function of this counter depends on bit EMOD.ESEI:

ESEI = 0: No function if optical interface mode has been enabled.
If the dual rail input mode is selected (bit MODE.OPT = 0), the 8-bit counter will be incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit CCR.EXTD. A counter overflow will be inhibited. During alarm simulation, the counter is incremented every four bits received up to its saturation. Disabling the counter is done by setting bit CCR.CLR; clearing is done by resetting it.

As extension to this 8-bit counter, two stages (CECX.CV8, CECX.CV9) may be added to get a 10-bit counter with a maximum value of 1023 (3FF hex). This counter mode is enabled by setting bit EMOD.ECVE. All other features are the same as for 8-bit counting.

ESEI = 1: If doubleframe format is selected, CVC has no function. If CRC-multiframe mode is enabled, CVC now works as submultiframe error indication counter (8 or 10 bits) which counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. There is no difference in comparison to other counters for reading and resetting this counter and interrupt generation in case of counter overflow.

CRC Error Counter (READ)

	7		0	
CEC	CE7		CE0	(03)

CE7 ... CE0 ... CRC Errors

– No function if doubleframe format is selected.

– In CRC-multiframe mode, the 8-bit counter will be incremented when a CRC-submultiframe has been received with a CRC error. CRC errors will not be counted during asynchronous state. A counter overflow will be inhibited.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation. Disabling the counter is done by setting the bit CCR.CLR and clearing is done by resetting it.

As extension to this 8-bit counter, two stages (CECX.CE8, CECX.CE9) may be added to get a 10-bit counter with a maximum value of 1023 (3FF hex). This counter mode is enabled by setting bit RC0.ECE. All other features are the same as for 8-bit counting.

Receive Service Word Pulseframe (READ)

	7							0	
RSW	RSIS	1	RRA	RYO	RY1	RY2	RY3	RY4	(04)

RSIS … Receive Spare Bit for International Use

First bit of the received service word. It is fixed to one if CRC-multiframe mode is enabled.

RRA … Receive Remote Alarm

Equivalent to bit RSR.RRA.

RY0 … RY4 … Receive Spare Bits for National Use (Y-Bits, Sn-Bits, Sa-Bits)

Receive Spare Bits/Additional Status (READ)

	7							0	
RSP	XFLG	RFLG	DSLP	GPE	XPE	RSIF	RS13	RS15	(05)

XFLG … Transmit Multiframe Flag

No function if standard doubleframe format is enabled (MODE.CRC = 0, ref. to EMOD.DFSN). If MODE.CRC is set to one, this bit is set at the beginning of every transmitted CRC-multiframe (or every eighth transmitted doubleframe). It is cleared
– with the first write access to the stack XSN, or
– automatically with beginning of frame 15 of every outgoing CRC multiframe (this is valid only if EMOD.DFSN = 0). In that case, a write access to the stack and to Si bits should be avoided. The data written to the stack XSN and to S_i -bits XSP.XS13 and XSP.XS15 is shifted into internal transmission buffers with the beginning of every CRC-multiframe (or every eighth doubleframe). RSP.XFLG should be monitored continuously at time intervals less than 2 ms (1.5 ms recommended) for correct Sn-/Si-bit insertion. If the stack is not updated, the previous information will be transmitted.

RFLG … Receive Multiframe Flag

No function if standard doubleframe format is enabled (MODE.CRC = 0, ref. to EMOD.DFSN). If MODE.CRC is set to one, this bit is set in (multiframe) synchronous state at the beginning of every received CRC multiframe (or every eighth received doubleframe). It is cleared
– with the first read access to the stack RSN, or
– automatically with beginning of frame 15 of every received CRC multiframe (this is valid only if EMOD.DFSN = 0). In that case, a read access to the stack and to Si bits should be avoided. Stack RSN and Si bits RSP.RS13 and RSP.RS15 will be updated with beginning of every CRC multiframe (or every eighth doubleframe). RSP.RFLG should be monitored continuously at time intervals less than 2 ms (1.5 ms recommended) to receive correct Sn/Si-bit information.

DSLP … DMA Request Slip

If the use of the signaling stacks RSIG and XSIG is enabled by setting bit XC0.ISIG, this flag is set if access to one of these stacks (2 bytes) is not completed before a new assigned request occurs. The flag is cleared by setting bit CCR.CLR.

GPE … Global Parity Error

Set by a parity error in any transmit or receive channel. Cleared by bit CCR.CCPY.
The bit will be set during alarm simulation.

XPE … Transmit Parity Error

If channel parity check is enabled by programming register CPY this bit is set after a transmit channel parity error occurs in the selected channel. This flag is meaningful only when the external transmit channel parity input XCHPY is used (enabled by setting bit XC0.EPY). The flag is set during alarm simulation.

RSIF … Receive Spare Bit for International Use (FAS Word)

First bit in FAS-word. Used only in doubleframe format, otherwise fixed to ‘1’.

RS13 … Receive Spare Bit (Frame 13, CRC Multiframe)

First bit in service word of frame 13. Significant only in CRC-multiframe format, otherwise fixed to ‘0’. This bit is updated with beginning of every received CRC multiframe (refer to RSP.RFLG and XSP.MRMB).

RS15 … Receive Spare Bit (Frame 15, CRC Multiframe)

First bit in service word of frame 15. Significant only in CRC-multiframe format, otherwise fixed to ‘0’. This bit is updated with beginning of every received CRC multiframe (refer to RSP.RFLG and XSP.MRMB).

Additional Receive Status

	7							0	
ASR	1	ERL	1	1	1	1	1	1	(06)

ERL … Error On Receive Line

Only valid if optical interface mode is disabled.
The flag is set while signals at ports RDIP and RDIM are both active.

Receive Signaling Stack (READ)

	7							0	
RSIG	RS7							RS0	(07)

RS7 … RS0 … Receive Signaling Data

If the use of the internal signaling register is enabled via bit XC0.ISIG two bytes of sequentially received signaling data (time-slot 16 of the received PCM frame) will be stored in this stack. A (DMA or interrupt) request at port RREQ requires that the stack must be read twice. Access to this stack is possible
– via a normal read cycle to the chip address location plus stack address (07 Hex), or
– via a direct read access with the signal at port ACKNLQ as access enable in conjunction with a read cycle without the need of generating the chip enable signal at port CEQ. This feature is useful for I/O-to-memory DMA transfer.

Submultiframe Error Indication

	7							0	
SEI	1	1	1	1	1	1	SI1	SI2	(08)

SI1 … SI2 … Submultiframe Error Indication 1, 2

Not valid if doubleframe format is enabled. In this case, both bits are set to logical ‘1’.

When using CRC-multiframe format these bits are set to

0 … if multiframe alignment has been lost, or
if the last multiframe has been received with CRC error(s). SI1 flags a CRC error in last sub-multiframe 1, SI2 flags a CRC error in last sub-multiframe 2.

1 …If at multiframe synchronous state last assigned sub-multiframe has been received without a CRC error.

Both flags will be actualized with beginning of every received CRC multiframe.

If automatic transmission of sub-multiframe status is enabled by setting bit XSP.AXS, above status information will be inserted automatically in S_i -bit position of every outgoing CRC multiframe (under the condition that time-slot 0 transparent modes are both disabled): SI1 $\rightarrow$ S_i -bit of frame 13, SI2 $\rightarrow$ S_i -bit of frame 15.

CRC Error Counter Extension

	7							0	
CECX	1	1	CV9	CV8	1	1	CE9	CE8	(09)

CV8 … CV9 … Code Violation Counter Extension

Additional bits which increase CVC to a 10-bit counter. These bits are activated by setting control bit EMOD.ECVE. For detailed information, refer to description of status register CVC.

CE8 … CE9 … CRC Error Counter Extension

Additional bits which increase CEC to a 10-bit counter. These bits are activated by setting control bit RC0.ECE. For detailed information on CRC counting, refer to description of status register CEC.

Receive Sn-Bit Stack (READ)

	7							0	
RSN	RSN7							RSN0	(0B)

RSN7 … RSN0 … Receive Sn-Bit Data (Y-Bits)

If the Sn-bit stack mode is enabled by setting bits MODE.CRC = 1 and MODE.ENSN = 1, the receive multiframe flag RSP.RFLG requests reading five bytes of Sn-bit information from this stack. In addition, a receive multiframe begin interrupt may be generated by setting bits CCR.AINT and XSP.MRMB.
Contents of the stack are updated with the service word information of the previously received CRC multiframe (or previously received eight doubleframes). The first byte read from this stack contains the information of the eight RY4-bits per multiframe (bit slot 8 of every service word). RSN7 is received in frame 1, RSN0 in frame 15.

PCM 24 Mode

Register Address Arrangement

Table 15
PCM 24 Register Address Arrangement

Address	Read	Write	Comment	
0	RSR	CCR	Receive Status Register	/ Common Control Register
1	FEC	MODE	Framing Error Counter	/ Mode Register
2	CVC	CPY	Code Violation Counter	/ Channel Parity Check
3	CEC	LOOP	CRC Error Counter	/ Channel Loop Back
4	ASR	GCR	Additional Status Register	/ General Configuration Register
5	MSR	XFDL	Multiframe Status Register	/ Transmit Spare Bits
6	FSR	XC0	Framing Status Register	/ Transmit Control 0
7	RSIG	XC1	Receive Signaling Stack	/ Transmit Control 1
8	RFDL	RC0	Receive FS/DL Data	/ Receive Control 0
9	CECX	RC1	CRC Error Counter Extension	/ Receive Control 1
A	–	XSIG	–	/ Transmit Signaling Stack
B	–	FMR	–	/ FS/DL Mask Register
C	–	MASK	–	/ Alarm Interrupt Mask
D	–	IDLE	–	/ Idle Channel Code
E,F	–	–	NO ACCESS ALLOWED	

Bank switching (CPY, SW = 1, CPY.BSEL = 0)

6	FSR	CCB1	Framing Status Register	/ Clear Channel Bank 1
7	RSIG	CCB2	Receive Signaling Stack	/ Clear Channel Bank 2
8	RFDL	CCB3	Receive FS/DL Data	/ Clear Channel Bank 3
9	CECX	ACR	CRC Error Counter Extension	/ Additional Control Register
1	FEC	EMOD	Framing Error Counter	/ Extended Mode Register
6	FSR	ICB1	Framing Status Register	/ Idle Channel Bank 1
7	RSIG	ICB2	Receive Signaling Stack	/ Idle Channel Bank 2
8	RFDL	ICB3	Receive FS/DL Data	/ Idle Channel Bank 3
9	CECX	–	CRC Error Counter Extension	–

The Control registers are normally only writeable. In a test mode they may be read by setting bit CCR.CRD (exceptions: bits LOOP.AIA, XFDL.XMAK, XFDL.RMAK).
The status registers are only readable and are updated by the ACFA.

6.1 Register Definitions

PCM 24 Control Registers

Common Control Register (WRITE)

	7							0	
CCR	AINT	FRS	CRD	CLR	SAIS	SRAF	EXLS	SIM	(00)

AINT … Enable Alarm Interrupt Mode

Setting this bit switches the output: FREEZS to the alarm interrupt function (AINT). Acknowledging is done by setting the bit LOOP.AIA. Programming the mask register MASK and the additional bit XC1.MCA selects the interrupt sources.

FRS … Force Resynchronization

A transition from low to high will force the frame aligner to execute a resynchronization of the pulse frame. In the asynchronous state, a new frame position is assumed at the next candidate if there is one. Otherwise, a new frame search with the meaning of a general reset is started. In the synchronous state this bit will have the same meaning as bit CCR.EXLS.

CRD ... Enable Control Register Read

0 ... Normal operation (status register read enabled).
1 ... Enables control register read.

CLR ... Clear Error Latches

This bit has to be set 1 µs before reading the error counters FEC, CVC, or CEC. Errors occuring during setting and resetting of this bit will be ignored. The error indications RSR.SLPP, RSR.SLPN, ASR.RPE, ASR.XPE, ASR.XSLP, MFR.DSLP, and MFR.GPE are also cleared when CLR is reset.

SAIS ... Send AIS Towards System Interface

Send AIS via output RDO towards system interface. This function is not influenced by bit EMOD.DAIS.

SRAF ... Select Remote Alarm Format for F12 and ESF Format

0 ... F12: bit2 = 0 in every channel. ESF: pattern ‘1111 1111 0000 0000..‘ in data link channel.
1 ... F12: FS bit of frame 12. ESF: bit2 = 0 in every channel

EXLS ... External Loss Of Frame

With a low to high transition a new frame search will be started. This has the meaning of a general reset of the internal frame alignment unit. Synchronous state is reached only if there is one definite framing candidate. In the case of multiple candidates, the setting of the bit CCR.FRS forces the receiver to lock onto the next available framing position.

SIM ... Alarm Simulation

Setting/resetting this bit initiates internal error simulation of: AIS, no signal, loss of synchronization, slip, parity, framing errors, CRC errors, code violations. The error counters FEC, CVC, CEC will be incremented.

The selection of simulated alarms is done via the error simulation counter: ASR.SC which will be incremented with each setting of bit CCR.SIM. For complete checking of the alarm indications eight simulation steps are necessary (ASR.SC = 0 after a complete simulation).

Mode Register (WRITE)

	7							0	
MODE	CTM	SIGM	CODE	PMOD	CRC	OPT	IMOD	XAIS	(01)

CTM ... Select Channel Translation Mode

0 ... Channel translation mode 0
1 ... Channel translation mode 1

SIGM ... Select Signaling Mode

0 ... CCS/CAS-CC mode
1 ... CAS-BR mode
For selection of clear channels refer to bit CPY.SWTCH and Clear Channel Banks CCB1 ... CCB3.

CODE ... Select Line Code

0 ... AMI coding with Zero Code Suppression (ZCS, B7-Stuffing)
For selection of clear channels refer to bit CPY.SWTCH and Clear Channel Banks CCB1 ... CCB3.
1 ... B8ZS coding

PMOD ... PCM Mode

0 ... PCM 30 mode.
1 ... PCM 24 mode.

CRC ... Enable CRC6

This bit is only significant when using the ESF format.
0 ... CRC check/generation disabled. For transmit direction, all CRC bit positions are set to ‘1’ .
1 ... CRC check/generation enabled.

OPT ... Enable Optical Interface

0 ... RZ dual rail line ports RDIP, RDIM, XDOP, and XDOM are enabled. Bit MODE.CODE selects the line code.
1 ... Ports RDIP, XDOP are switched to NRZ line ports for connection to fibre optical transmission systems. There is no code violation detection for this unipolar data.

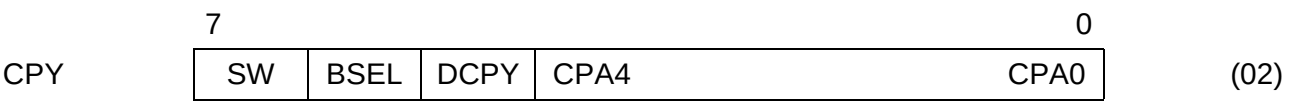
IMOD ... System Interface Mode

0 ... 4 Mbit/s mode
1 ... 2 Mbit/s mode

XAIS ... Transmit AIS Towards Remote End

Send AIS via ports: XDOP, XDOM towards the remote end. The test data outputs XTOP, XTOM are not affected.

Channel Parity Check (WRITE)



SW ... Enable Bank Switching

0 ... Normal operation. Control register addresses 01, 06 to 09 select register MODE, XC0, XC1, RC0, and RC1.
1 ... Access to additional control registers selected via bit CPY.BSEL is enabled (bank switching).

BSEL ... Bank Select

0 ... If bit CPY.SW is set, control register addresses 06 to 09 select the clear channel registers CCB1, CCB2, CCB3 and register ACR.
1 ... If bit CPY.SW is set, control register addresses 01, 06 to 09 select registers EMOD and the idle channel registers ICB1, ICB2, ICB3. Address 09 is reserved for future extensions.

DCPY ... Disable Channel Parity Check

0 ... Normal operation.
1 ... Disables the channel parity check selected by this register. This bit should be set at least one time-slot before changing the channel address.

CPA4 ... CPA0 ... Channel Address For Parity Check

CPA = 0 ... 24 selects the channel.

Channel Loop Back (WRITE)

	7				0	
LOOP	AIA	SLB	DLOP	CLA4 ... CLA0		(03)

AIA ... Alarm Interrupt Acknowledge

(NOT READABLE)
A ‘1’ written to this bit location clears the alarm interrupt signal at port AINT if the alarm interrupt mode is enabled via bit CCR.AINT and register MASK or XC1.MCA.
Resetting this bit is not necessary.

SLB ... Enable Signaling Loop Back

If channel loop back is enabled by programming register LOOP
0 ... loop back of signaling data is suppressed, e.g. a ‘clear’ channel without bitrobbing data is looped back.
1 ... channel data and signaling data will be looped back.

DLOP ... Disable Channel Loop Back

0 ... Normal operation.
1 ... Disables the channel loop back selected by this register. This bit should be set at least one time-slot before changing the channel address.

CLA4 ... CLA0 ... Channel Address For Loop Back

CLA = 1 ... 24 selects the channel.
CLA = 0 disables channel loop back.
During loop back, the contents of the associated outgoing channel at ports XDOP, XDOM is equal to the idle channel code programmed in register IDLE.

General Configuration Register (WRITE)

	7							0	
GCR	AIS3	1	XRA	CRCI	TM	AUTO	FM1	FM0	(04)

AIS3 ... Select AIS Condition

0 ... AIS is indicated (RSR.AIS) when two or less zeros in the received bit stream are detected in a time interval of 12 frames (F4, F12, F72) or 24 frames (ESF).

1 ... AIS detection is only enabled when ACFA is in asynchronous state. The alarm is indicated (RSR.AIS) when
– three or less zeros within a time interval of 12 frames (F4, F12, F72), or
– five or less zeros within a time interval of 24 frames (ESF)
are detected in the received bit stream.

XRA ... Transmit Remote Alarm

If high remote alarm is sent via PCM route. Clearing the bit will remove the remote alarm pattern. Remote alarm indication depends on the multiframe structure as follows:

F4: bit2 = 0 in every speech channel
F12: – CCR.SRAF = 0: bit2 = 0 in every speech channel
– CCR.SRAF = 1: FS-bit of frame 12 is forced to ‘1’
ESF: – CCR.SRAF = 0: pattern ‘1111 1111 0000 0000...’ in data link channel
– CCR.SRAF = 1: bit2 = 0 in every speech channel
F72: bit2 = 0 in every speech channel

CRCI ... CRC6 Inversion

If set, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe.

TM ... Transparent Mode

Setting this bit enables the transparent mode:
– In transmit direction bit 8 of every FS/DL time-slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame. Internal framing generation, insertion of CRC and DL data is disabled.
– In receive direction the framing bit is also forwarded to RDO and inserted in the FS/DL time slot. Bit RDCF (bit 1 of FS/DL time-slot) indicates a DL bit.

Note: For loop back via the system interface (RDO connected with XDI/XSIG) channel translation mode 0 (MODE.CTM = 0) has to be used to guarantee correct assignment of FS/DL bits to the data of the frame.

AUTO ... Enable Auto Resynchronization

0 ... The receiver will not resynchronize automatically. Starting a new synchronization procedure is possible via the bits: CCR.EXLS or CCR.FRS.
1 ... Auto-resynchronization is enabled.

FM1 ... FM0 ... Select Frame Mode

FM = 0: 12-frame multiframe format (F12, D3/4)
FM = 1: 4-frame multiframe format (F4)
FM = 2: 24-frame multiframe format (ESF)
FM = 3: 72-frame multiframe format (F72, remote switch mode)

Transmit FS/DL Data (WRITE)

	7			0	
XFDL	XMAK	RMAK	XFD5	XFD0	(05)

XMAK ... XMFB Interrupt Acknowledge (NOT READABLE)

A ‘1’ will reset the valid marker pulse at the port XMFB (normal length: two frames). This bit is useful for interrupt applications if access to FS/DL-bits is done via the microprocessor interface. Resetting the bit is not necessary.

RMAK ... RMFB Interrupt Acknowledge

(NOT READABLE)
A ‘1’ will reset the valid marker pulse at the port RMFB (normal length: two frames). This bit is useful for interrupt applications if access to FS/DL-bits is done via the microprocessor interface. Resetting the bit is not necessary.

XFD5 ... XFD0 ... Transmit FS/DL Data

Only significant for F4, ESF and F72 format.
XFD5: DL bit of frame 11 (23),FS bit of frame n + 12
XFD4: DL bit of frame 9 (21),FS bit of frame n + 10
XFD3: DL bit of frame 7 (19),FS bit of frame n + 8
XFD2: DL bit of frame 5 (17),FS bit of frame n + 6
XFD1: DL bit of frame 3 (15),FS bit of frame n + 4
XFD0: DL bit of frame 1 (13),FS bit of frame n + 2

ESF and F4 format: n = 0
F72 format: n = 24, 36, 48, 60

The microprocessor should update this register every 12 frames after request signal XMFB goes active. Otherwise, the previous contents are sent out. The relationship to the multiframe structure is given by the bits MFR.XMB and MFR.XRS. The bit-frame allocation in F4 format is not definite. In F72 format, transmission of data link information is stopped

when FS framing bits are sent in the DL channel. Deactivation of port XMFB is done by setting bit XFDL.XMAK.

The data is taken immediately before the marker XMFB occurs so that the processor has almost 12 frames to write the register.

Transmit Control 0 (WRITE)

	7						0	
XC0	XDOS	ISIG	EPY	EPYS	XTDS	XCO2	XCO0	(06)

XDOS ... Transmit Data Output Sense

0 ... Outputs XDOP, XDOM are active low.
1 ... Outputs XDOP, XDOM are active high.

ISIG ... Enable Internal Signaling Stack

0 ... Normal operation. The signaling data are taken from/sent to the system internal PCM highway at ports XDI, XSIG, RDO.
1 ... Enables the use of the signaling stacks RSIG and XSIG. Three bytes of received signaling information are stored in the stack RSIG. The three bytes of signaling information from the stack XSIG are inserted one after the other in the outgoing PCM frame. Access to three stacks is requested by the signals at ports RREQ and XREQ. They may be used as interrupt or DMA request signals. Acknowledging is done with the end of the first or the beginning of the third read resp. write access to these stacks depending on the value of bit EMOD.EDMA. For I/O-to-memory DMA transfer the input signal at port ACKNLQ should be used for direct access to the stacks without the need of generating the chip enable signal (port CEQ).
The location of the signaling data in the PCM data stream depends on the signaling mode (MODE.SIGM), the channel translation mode (MODE.CTM) and the CCS marker location (FMR.SM24).

EPY ... Enable External Transmit Channel Parity Input

0 ... Normal operation.
1 ... An externally generated channel parity signal will be read at port XCHPY and compared with
the internally generated channel parity bit. To avoid difficulties with external parity generation, the internal parity checker will take the signaling data inputs into account.

EPYS ... External Transmit Channel Parity Sense

0 ... Even parity.
1 ... Odd parity.

XTDS ... Transmit Test Data Sense

0 ... Outputs XTOP, XTOM are active low.
1 ... Outputs XTOP, XTOM are active high.

XCO2 ... XCO0 ... Transmit Clock-Slot Offset

Initial value loaded into the transmit bit counter at the trigger edge of SCLK when the synchronous pulse at port SYPQ is active (**see figure 6**).

Transmit Control 1 (WRITE)

	7						0	
XC1	SCLK	MCA	XTO5				XTO0	(07)

SCLK ... Select System Clock

0 ... If the system clock at port SCLK is 4096 kHz.
1 ... If the system clock at port SCLK is 8192 kHz.

MCA ... Mask: CRC Alarm

Only valid if extended multiframe is selected.
If this bit is set, the occurrence of a CRC error (one per multiframe maximum) triggers the interrupt port AINT if enabled via CCR.AINT.

XTO5 ... XTO0...Transmit Time-slot Offset

Initial value loaded into the transmit time-slot counter at the trigger edge of SCLK when the synchronous pulse at port SYPQ is active (**see figure 6**).
A write access to this address resets the transmit speech memory to its basic starting position. Therefore, updating the value should only be done when the ACFA is initialized or when a transmit slip indicates a defective clock system.

Receive Control 0 (WRITE)

	7						0	
RC0	ECE	RPYS	1	DFRZ	RDIS	RCO2	RCO0	(08)

ECE ... Enable CRC Counter Extension

0 ... Normal operation. CRC errors are counted at status register CEC (8 bit length) with a maximum value of 255 (‘FF’ hex).
1 ... Extended CRC error counting with additional counter stages (bits CECX.CE8 and CECX.CE9, 10 bit counter). Maximum value is 1023 (‘3FF’ hex) which is also valid for interrupt generation if enabled.

RPYS ... Receive Parity Sense

0 ... Even parity.
1 ... Odd parity.

DFRZ ... Disable Freeze Signal

If high the synchronization status signal at port FREEZS is disabled.

RDIS ... Receive Data Input Sense

0 ... Inputs: RDIP, RDIM active low.
1 ... Inputs: RDIP, RDIM active high.

RCO2 ... RCO0 ... Receive Clock-Slot Offset

Initial value loaded into the receive bit counter at the trigger edge of SCLK when the synchronous pulse at port SYPQ is active (**see figure 5**).

Receive Control 1 (WRITE)

	7			0	
RC1	SLC	RRAM	RTO5	RTO0	(09)

SLC ... Select Loss of Sync Conditions

Loss of synchronization (RSR.LOS or opt. FSR.MLOS) is declared if
SLC = 0 : 2 out of 4
SLC = 1 : 2 out of 5
framing bits are incorrect. It depends on the selected multiframe format and optionally on bit EMOD.SSP which framing bits are observed:

F4: FT bits → RSR.LOS
F12, F72: SSP = 0: FT bits → RSR.LOS: FS bits → RSR.LOS and FSR.MLOS
SSP = 1: FT → RSR.LOS
FS → FSR.MLOS
ESF: ESF framing bits → RSR.LOS

RRAM ... Receive Remote Alarm Mode

The conditions for remote alarm (RSR.RRA) detection can be selected via this bit to allow detection even in the presence of BER 10**-3:

RRAM = 0
Detection
F4: bit2 = 0 in every speech channel per frame.
F12: – CCR.SRAF = 0: bit2 = 0 in every speech channel per frame.
– CCR.SRAF = 1: S-bit of frame 12 is forced to ‘1’
ESF: – CCR.SRAF = 0: pattern ‘1111 1111 0000 0000 ...’ in data link channel
– CCR.SRAF = 1: bit2 = 0 in every speech channel

F72: bit2 = 0 in every speech channel per frame.

Release

The alarm will be reset when above conditions are no longer detected.

RRAM = 1

Detection

F4: bit2 = 0 in 255 consecutive speech channels.

F12: – CCR.SRAF = 0: bit 2 = 0 in 255 consecutive speech channels.
– CCR.SRAF = 1: S-bit of frame 12 is forced to ‘ 1’

ESF: – CCR.SRAF = 0: pattern ‘ 1111 1111 0000 0000 ...’ in data link channel
– CCR.SRAF = 1: bit 2 = 0 in 255 consecutive speech channels

F72: bit 2 = 0 in 255 consecutive speech channels.

Release

Depending on the selected multiframe format the alarm will be reset when ACFA does not detect

– the ‘bit 2 = 0’ condition for three consecutive pulseframes (all formats if selected),
– the ‘FS bit’ condition for three consecutive multiframes (F12),
– the ‘DL pattern’ for three times in a row (ESF).

RTO5 ... RTO0 ... Receive Time-Slot Offset

Initial value loaded into the receive time-slot counter at the trigger edge of SCLK when the synchronous pulse at port SYPQ is active (**see figure 5**).

Transmit Signaling Stack (WRITE)

	7		0	
XSIG	XS7		XS0	(0A)

XS7 ... XS0 ... Transmit Signaling Data

If the use of the internal signaling register is enabled via bit XC0.ISIG, the contents of this 3-byte stack will be sent one after the other in the outgoing PCM frame. A (DMA or interrupt) request at port XREQ requires loading the stack with three bytes of signaling data. Access to this stack is possible
– via a normal write cycle to the chip address location plus stack address (0A Hex), or
– via a direct write access with the signal at port ACKNLQ as access enable in a write cycle without the need of generating the chip enable signal at port CEQ. This feature is useful for memory to I/O DMA transfer.
In CCS or CAS-CC, mode the contents of this stack are sent in the signaling channels 17 or 24 (depending on MODE.CTM and FMR.SM24). The MSB of the first byte written to the stack is sent out first.

In CAS-BR mode, the contents are shifted out in the corresponding bit locations to the remote end:

XS7: transmit channel 1, 9, 17
XS6: transmit channel 2, 10, 18
XS5: transmit channel 3, 11, 19
XS4: transmit channel 4, 12, 20
XS3: transmit channel 5, 13, 21
XS2: transmit channel 6, 14, 22
XS1: transmit channel 7, 15, 23
XS0: transmit channel 8, 16, 24

If request XREQ is ignored, transmission of the third byte will be repeated until a new information is written to the stack. Although the DMA slip indication RSP.DSLP has been set, function of stack RSIG is unchanged. The function simplifies realization of HDLC procedures via microprocessor interface (idle code transmission etc.).

FS/DL Mask Register (WRITE)

	7							0	
FMR	1	SM24	FM5					FM0	(0B)

SM24 ... Shift CCS Marker

If CCS/CAS-CC mode (MODE.SIGM = 0) and channel translation mode 1 (MODE.CTM = 1) are enabled:

0 ... output signals RSIGM and XSIGM mark channel 24,
1 ... output signals RSIGM and XSIGM mark channel 17.

FM5 ... FM0 ... FS/DL Mask Bits

Only significant in F4, ESF and F72 format.
These bits enable a mixed insertion of the corresponding FS/DL bits of register XFDL and the information from the system internal highway at port XDI:

0 ... the assigned data is taken from port XDI,
1 ... the assigned data is taken from the register XFDL.

Alarm Interrupt Mask Register (WRITE)

	7							0	
MASK	MLOS	MAIS	MNOS	MRRA	MSLP	MCEC	MFEC	MCVC	(0C)

MLOS ... Mask: Loss Of Synchronization
MAIS ... Mask: Alarm Indication Signal
MNOS ... Mask: No Signal
MRRA ... Mask: Receive Remote Alarm
MSLP ... Mask: Receive Slip Indication
MCEC ... Mask: CRC Error Counter Overflow
MFEC ... Mask: Framing Error Counter Overflow
MCVC ... Mask: Code Violation Counter Overflow

If the alarm interrupt mode is enabled via bit CCR.AINT this mask register selects the alarm sources:
Mask bit = 0: alarm source disabled.
Mask bit = 1: alarm source enabled.
Selected alarms cause an interrupt signal at port AINT. Acknowledging is done by writing a '1' to the bit LOOP.AIA. Triggering a new interrupt by the same source is possible only after this source has been inactive.

Idle Channel Code Register (WRITE)

	7							0	
IDLE	IDL7							IDL0	(0D)

IDL7 ... IDL0 ... Idle Channel Code

If channel loop back is enabled by programming the register LOOP, the contents of the assigned outgoing channel at ports XDOP, XDOM is set equal to the idle channel code selected by this register.
Additionally, the specified pattern overwrites the contents of all channels of the outgoing PCM frame selected via the idle channel register bank ICB1 ... ICB3.
Its initial value (FF Hex after switching to PCM 24 mode) may be overwritten via the microprocessor interface.

Bank Switching

After setting bit CPY.SW control register addresses 01, 06 to 09 select additional control registers in dependance of bit CPY.BSEL.

Clear Channel Register Bank (WRITE)

Only accessible if CPY.SW = 1 and CPY.BSEL = 0
Value after RESET: 00H, 00H, 00H

	7							0	
CCB1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	(06)
CCB2	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	(07)
CCB3	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	(08)

CH1 ... CH24 ... Channel Selection bits

0 ... Normal operation. Bit robbing information and Zero Code Suppression (ZCS, B7 stuffing) may change contents of the selected speech/data channel if assigned modes are enabled via bits MODE.SIGM and MODE.CODE.

1 ... Clear channel mode. Contents of selected speech/data channel will not be overwritten by bit robbing and ZCS information. Transmission of channel assigned signaling and control of pulse density is applied by the user.

Additional Control Register (WRITE)

Only accessible if CPY.SW = 1 and CPY.BSEL = 0
Value after RESET: 70H

	7							0	
ACR	0(*)	1(*)	1(*)	1(*)	EXMF	SLM	DLC	MFBS	(09)

(*) These bits are reserved for future extensions. When programming register ACR they have to be set to '0' for correct operation.
Note: Read back value for the high nibble: '7' H.

EXMF ... External Multiframe Synchronization

If set, the transmitter of the ACFA can be synchronized externally for multiframe begin via port XCHPY/AFT (bit EXMF has higher priority than bit DLC). Refer to description of port XCHPY/AFT for detailed information.

SLM ... Slip Limit

In channel translation mode 0 the maximum permissible wander amplitude can be selected:

0 ... 126 UI peak-to-peak

1 ... 142 UI peak-to-peak

DLC ... Enable DL Clock

If set, ports RCHPY/AFR and XCHPY/AFT provide signals which mark the DL-bit position within the data stream at RDO and XDI. For XCHPY/AFT, bit EXMF has higher priority than bit DLC.

MFBS ... Enable pure Multiframe Begin Signals

Only valid if ESF or F72 format is selected.
If set, signals RMFB and XMFB indicate only the multiframe begin. Additional pulses (every 12 frames) are disabled.

Extended Mode Register (WRITE)

Only accessible if CPY.SW = 1 and CPY.BSEL = 1.

	7							0	
EMOD	0	0	0	SSP	ECVE	XFB	EDMA	DAIS	(01)

SSP ... Select Sync/Resync Procedure

Only valid if F12 or F72 format is selected:

0 ... Specified number of errors in both FT framing and FS framing lead to loss of sync (RSR.LOS is set). In the case of FS bit framing errors, bit FSR.MLOS is set additionally. A complete new synchronization procedure is initiated to regain pulseframe alignment and then multiframe alignment.
1 ... Specified number of errors in FT framing has the sames effect as above. Specified number of errors in FS framing only initiates a new search for multiframe alignment without influencing pulseframe synchronous state (FSR.MLOS is set).

ECVE ... Enable Code Violation Counter Extension

0 ... Normal operation. Code violations are counted at status register CVC (8 bit length) with a maximum value of 255 (‘FF’ hex).
1 ... Extended code violation counting with additional counter stages (bits CECX.CV8 and CECX.CV9, 10 bit counter). Maximum value is 1023 (‘3FF’ hex) which is also valid for interrupt generation if enabled.

XFB ... Transmit Full Bauded Mode

0 ... Output signals XDOP, XDOM are half bauded (normal operation).
1 ... Output signals XDOP, XDOM are full bauded.

EDMA ... Extended DMA Mode

0 ... DMA request lines RREQ and XREQ are reset at the end of the first read/write access to the assigned stack (rising edge of RDQ/WRQ)
1 ... DMA request lines RREQ and XREQ remain active until the beginning of the third read/write access to the assigned stack. RREQ is reset with the falling edge of RDQ.XREQ is reset with the falling edge of ACKNLQ or CEQ and remains reset if a write cycle to stack XSIG follows. Otherwise, it becomes active again until the third access to XSIG is provided.

DAIS ... Disable AIS to System Interface

0 ... AIS is automatically inserted into the data stream to RDO if ACFA is in asynchronous state.
1 ... Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit CCR.SAIS.

Idle Channel Register Bank (WRITE)

Only accessible if CPY.SW = 1 and CPY.BSEL = 1.
Value after RESET: 00H, 00H, 00H, 00H

	7							0	
ICB1	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	(06)
ICB2	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16	(07)
ICB3	IC17	IC18	IC19	IC20	IC21	IC22	IC23	IC24	(08)
ICB4				(reserved)					(09)

IC1 ... IC24 ... Idle Channel Selection Bits

These bits define the channels of the outgoing PCM frame to be altered.
0 ... Normal operation.
1 ... Idle channel mode. The content of the selected channel is overwritten by the idle channel code defined via register IDLE.

PCM 24 Status Registers

Receive Status Register (READ)

	7							0	
RSR	NOS	AIS	LOS	RRA	SLPP	SLPN	1	FSRF	(00)

NOS ... No Signal Indication

This bit is set when
– 31 or more consecutive zero bits are detected, or
– a receive route clock pulse (port RRCLK) fails to occur in a time interval of 4 internal SCLK clock cycles (4096 kHz). The flag stays active for at least one multiframe. It will be reset with the beginning of the next following multiframe if no alarm condition is detected.

The bit will be set during alarm simulation and reset if ASR.SC = 0, 3, 4, 7 and no alarm condition exists.

AIS ... Alarm Indication Signal

This bit is set when the conditions defined via bit GCR.AIS3 are detected. The flag stays active for at least one multiframe. It will be reset with the beginning of the next following multiframe if no alarm condition is detected.
The bit will be set during alarm simulation and reset if ASR.SC = 0, 3, 4, 7 and no alarm condition exists.

LOS ... Loss Of Synchronization

The flag is set if pulseframe synchronization has been lost. The conditions are specified via bit RC1.SLC.
The flag is cleared when synchronization has been regained.

RRA ... Receive Remote Alarm

The flag is set after detecting remote alarm. Conditions for setting/resetting are defined by bit RC1.RRAM.
The bit will be set during alarm simulation and reset if ASR.SC = 0, 3, 4, 7 and no alarm condition exists.

SLPP ... Receive Slip Indication Positive

Set after a slip caused a received frame to be repeated. The bit indicates that the receive route clock frequency is low relative to the internal clock. The bit will be cleared by bit CCR.CLR. It will be set during alarm simulation.

SLPN ... Receive Slip Indication Negative

Set after a slip caused a received frame to be discarded. The bit indicates that the receive route clock frequency is high relative to the internal clock. The bit will be cleared by bit CCR.CLR. It will be set during alarm simulation.

FSRF ... Frame Search Restart Flag

Toggles when no framing candidate (pulseframing or multiframing) is found and a new frame search is started.

Framing Error Counter (READ)

FE7 ... FE0 ... Framing Errors

This 8-bit counter will be incremented when incorrect FT and FS bits in F4, F12 and F72 format or incorrect FAS bits in ESF format are received. A counter overflow will be inhibited. During alarm simulation, the counter will be incremented twice. Disabling the counter is done by setting the bit CCR.CLR. Clearing is done by resetting it.

Code Violation Counter (READ)

CV7 ... CV0 ... Code Violations

No function if optical interface mode has been enabled.
If the dual rail input mode is selected (bit MODE.OPT = 0), the 8-bit counter will be incremented by detecting violations in the B8ZS mode (MODE.CODE = 1) which are not due to zero substitution. If simple AMI coding is enabled (MODE.CODE = 0) all bipolar violations are counted. A counter overflow will be inhibited.
During alarm simulation, the counter will be incremented continuously with every second received bit up to its saturation. Disabling the counter is done by setting bit CCR.CLR; clearing is done by resetting it.
As extension to this 8-bit counter, two stages (CECX.CV8, CECX.CV9) may be added to get a 10 bit counter with a maximum value of 1023 (3FF hex). This counter mode is enabled by setting bit EMOD.ECVE. All other features are the same as for 8-bit counting.

CRC Error Counter (READ)

	7							0	
CEC	CE7							CE0	(03)

CE7 ... CE0 ... CRC Errors

- No function if CRC6 procedure or ESF format are disabled (MODE.CRC = 0 or GSR.FM = 2).
- If ESF format and CRC6 procedure are enabled, the 8-bit counter will be incremented when a multiframe with a CRC error has been received. A counter overflow will be inhibited. During alarm simulation the counter will be incremented once per multiframe up to its saturation. Disabling the counter is done by setting the bit CCR.CLR, and clearing is done by resetting it.
  As extension to this 8-bit counter, two stages (CECX.CE8, CECX.CE9) may be added to get a 10-bit counter with a maximum value of 1023 (3FF hex). This counter mode is enabled by setting bit RC0.ECE. All other features are the same as for 8-bit counting.

Additional Status Register (READ)

	7							0	
ASR	SC2		SC0	FRES	1	RPE	XPE	XSLP	(04)

SC2 ... SC0 ... Error Simulation Counter

This three-bit counter is incremented by setting bit CCR.SIM. The state of the counter determines the function to be tested:
For complete checking of the alarm indications, eight simulation steps are necessary (ASR.SC = 0 after a complete simulation).

Tested alarms SC2 ... SCO =	0	1	2	3	4	5	6	7
LOS	.	.	X	.	.	.	X.	
RRA (bit2 = 0)	.	X	.	.	.	.	..	
RRA (S-bit fr. 12)	.	.	X	.	.	.	..	
RRA (DL-pattern)	.	.	.	.	.	.	X .	
NOS (= 31 zeros)	.	X	X	.	.	X	.	.
NOS (clock check)	.	.	.	.	.	.	X	.
AIS	.	X	X	.	.	X	X	.
FEC	.	.	X	.	.	.	X	.
CVC	.	X	X	.	.	X	.	.
CEC	.	X	X	.	.	X	X	.
RPE	.	.	.	.	.	X	X	.
XPE	.	X	X	.	.	.	.	.
GPE	.	X	X	.	.	X	X	.
SLPP	.	X	.	.	.	.	.	.
SLPN	.	.	.	.	.	X	.	.
XSLP	.	X	X	.	.	X	X	.

Some of these alarm indications are simulated only if the ACFA is configured in the appropriate mode. At simulation steps 0, 3, 4, and 7, pending status flags are reset automatically and clearing of the error counters is enabled. Incrementing the simulation counter should not be done at time intervals shorter than 1.5 ms (F4, F12, F72) or 3 ms (ESF). Otherwise, reactions of initiated simulations may occur at later steps.

FRES ... Freeze Signaling Status

Synchronization status signal which informs the CAS-processor that current signaling should be frozen. Set by:
- one or more framing bit errors in a multiframe
- loss of synchronization
- receive slip

Cleared after receiving a correct multiframe in the synchronous state.

RPE ... Receive Parity Error

Set after a receive parity error occurs in the channel selected by register CPY. Cleared by setting bit CCR.CLR.
The bit will be set during alarm simulation and must be cleared by setting bit CCR.CLR.

XPE ... Transmit Parity Error

Set after a transmit parity error occurs in the channel selected by register CPY. Cleared by setting bit CCR.CLR.
The bit will be set during alarm simulation and must be cleared by setting bit CCR.CLR.

XSLP ... Transmit Slip Indication

A one in this bit position indicates that there is an error in the host clock system. If the wander of the transmit route clock (XRCLK), which normally has to be phase locked to a common submultiple of the system clock (SCLK) such as 8 kHz, is too great, data transmission errors will occur. In that case, the transmit speech memory has to be reset to its start position by writing the initial value to the transmit time-slot counter XC1.XTO. ASR.XSLP will be reset by bit CCR.CLR.

Multiframe Status Register (READ)

	7							0	
MFR	1	1	DSLP	GPE	RRS	RMB	XRS	XMB	(05)

DSLP ... DMA Request Slip

If the use of the signaling stacks RSIG and XSIG is enabled by setting bit XC0.ISIG, this flag is set if access to one of these stacks (3 bytes) is not completed before a new assigned request occurs. The flag is cleared by setting bit CCR.CLR.

GPE ... Global Parity Error

Set by a parity error in any transmit or receive channel. Cleared by bit CCR.CLR.
The bit will be set during alarm simulation.

RRS ... Receive Remote Switch Flag

This flag signals that register RFDL contents the first six bits of the D channel of a received F72 multiframe. It is set when port RMFB goes active with the beginning of frame 37 and reset when port RMFB returns to zero.

RMB ... Receive Multiframe Begin Flag

Set when port RMFB goes active at the beginning of a received multiframe and reset when port RMFB returns to zero.

XRS ... Transmit Remote Switch Flag

Set when port XMFB goes active at the beginning of the D channel of a transmitted F72 multiframe and reset when port XMFB returns to zero.

XMB ... Transmit Multiframe Begin Flag

Set when port XMFB goes active at the beginning of a transmitted multiframe and reset when port XMFB returns to zero.

Framing Status Register (READ)

	7							0	
FSR	MLOS	ERL	FEH5					FEH0	(06)

MLOS ... Loss Of Multiframe Signal

Set in F12 or F72 format when 2 out of 4- (or 5) multiframe alignment patterns are incorrect. Cleared after multiframe synchronization has been regained.

ERL ... Error On Receive Line

Only valid if optical interface mode is disabled.
The flag is set while signals at ports RDIP and RDIM are both active.

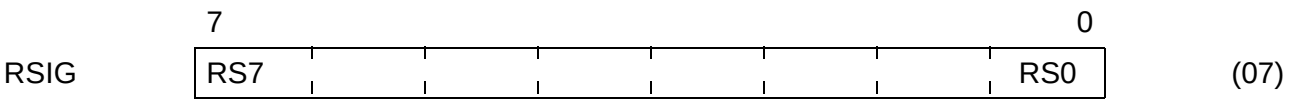
FEH5 ... FEH0 ... F-Bit Error History

The bits are set if errors occur in the corresponding framing bit locations. They will be updated once per superframe (ESF format) or every six frames (other framing formats). Organization:

ESF	others
FEH5: FAS (24)	FT (6 or 12)
FEH4: FAS (20)	FT (5 or 11)
FEH3: FAS (16)	FT (4 or 10)
FEH2: FAS (12)	FT (3 or 9)
FEH1: FAS (8)	FT (2 or 8)
FEH0: FAS (4)	FT (1 or 7)

Note: All error history bits corresponding to FS bits substituted by data link information are fixed to‘0’.

Receive Signaling Stack (READ)



RS7 ... RS0 ... Receive Signaling Data

If the use of the internal signaling register is enabled via bit XC0.ISIG three bytes of received signaling data will be stored in this stack. A DMA or interrupt request at port RREQ requires reading the stack three times. Access to this stack is possible
– via a normal read cycle to the chip address location plus stack address (07 Hex), or
– via a direct read access with the signal at port ACKNLQ as access enable in a read cycle without the need of generating the chip enable signal at port CEQ. This feature is useful for I/O to memory DMA transfer.
In CCS or CAS-CC mode three bytes of signaling data of channels 17 or 24 (depending on MODE.CTM and FMR.SM24) are stored in this stack. The MSB of the first byte read from the stack is received first.
In CAS-BR mode every eighth bit per channel of the signaling frame is stored:
RS7: receive channel 1, 9, 17
RS6: receive channel 2, 10, 18
RS5: receive channel 3, 11, 19
RS4: receive channel 4, 12, 20
RS3: receive channel 5, 13, 21
RS2: receive channel 6, 14, 22
RS1: receive channel 7, 15, 23
RS0: receive channel 8, 16, 24

Receive FS/DL Data (READ)

	7							0	
RFDL	1	1	RFD5					RFD0	(08)

RFD7 ... RFD0 ... Receive FS/DL Bits

Only significant in F4, ESF and F72 format.
RFD5: DL bit of frame 11 (23), FS bit of frame n + 12
RFD4: DL bit of frame 9 (21), FS bit of frame n + 10
RFD3: DL bit of frame 7 (19), FS bit of frame n + 8
RFD2: DL bit of frame 5 (17), FS bit of frame n + 6
RFD1: DL bit of frame 3 (15), FS bit of frame n + 4
RFD0: DL bit of frame 1 (13), FS bit of frame n + 2

ESF format F4 format: n = 0
F72 format: n = 24, 36, 48, 60

The microprocessor should read this register within 12 frames after request signal RMFB goes active. The relationship to the multiframe structure is given by the bits MFR.RMB and MFR.RRS. The bit-frame allocation in F4 format is not definite. Deactivation of port RMFB is done by setting bit XFDL.RMAK.

CRC Error Counter Extension

	7							0	
CECX	1	1	CV9	CV8	1	1	CE9	CE8	(09)

CV8 ... CV9 ... Code Violation Counter Extension

Additional bits which increase CVC to a 10 bit counter. These bits are activated by setting control bit EMOD.ECVE. For detailed information, refer to description of status register CVC.

CE8 ... CE9 ... CRC Error Counter Extension

Additional bits which increase CEC to a 10 bit counter. These bits are activated by setting control bit RC0.ECE. For detailed information on CRC counting, refer to description of status register CEC.

7 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	℃
Storage temperature	T_{stg}	– 65 to 125	℃
Voltage on any pin with respect to ground	V_S	– 0.4 V to V_{DD} + 0.4 V	V

DC Characteristics

T_A = 0 to 70 ℃; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	– 0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} + 0.4	V	
L-output voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA
Power supply current	I_{CC}		18	mA	V_{DD} = 5 V Inputs at 0 V/V_{DD}, no output loads
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

T_A = 25 ℃; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}	5	10	pF
Output capacitance	C_{OUT}	10	20	pF
I/O	C_{IO}	8	15	pF

AC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

Inputs are driven to 2.4 V for a logical ‘1’ and to 0.4 V for a logical ‘0’. Timing measurements are made at 2.0 V for a logical ‘1’ and at 0.8 V for a logical ‘0’.

The AC testing input/output waveforms are shown in **figure 18**.

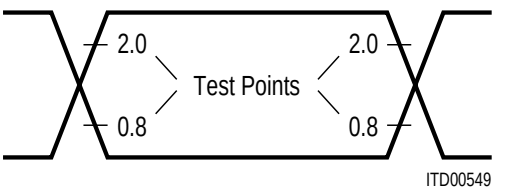


Figure 18
Input/Output Waveform for AC Tests

Output load: 150 pF load capacitance in connection with resistive loads for I_{OL} = 2 mA and I_{OH} = – 100 µA.

Rise/fall times: 20 ns max.

µP Interface Timing

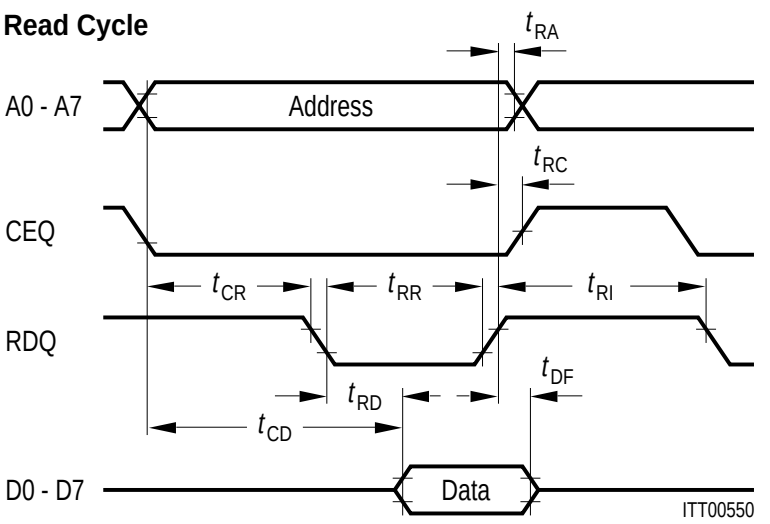


Figure 19
µP Read Timing

µP Read Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
CEQ and ADDRESS valid to DATA valid	t_{CD}		110	ns
CEQ and ADDRESS stable before RDQ	t_{CR}	0		ns
RDQ to DATA valid	t_{RD}		90	ns
RDQ pulse width	t_{RR}	100		ns
DATA float after RDQ	t_{DF}	10	30	ns
CEQ hold after RDQ	t_{RC}	0		ns
ADDRESS hold after RDQ	t_{RA}	0		ns
RDQ control interval	t_{RI}	70		ns

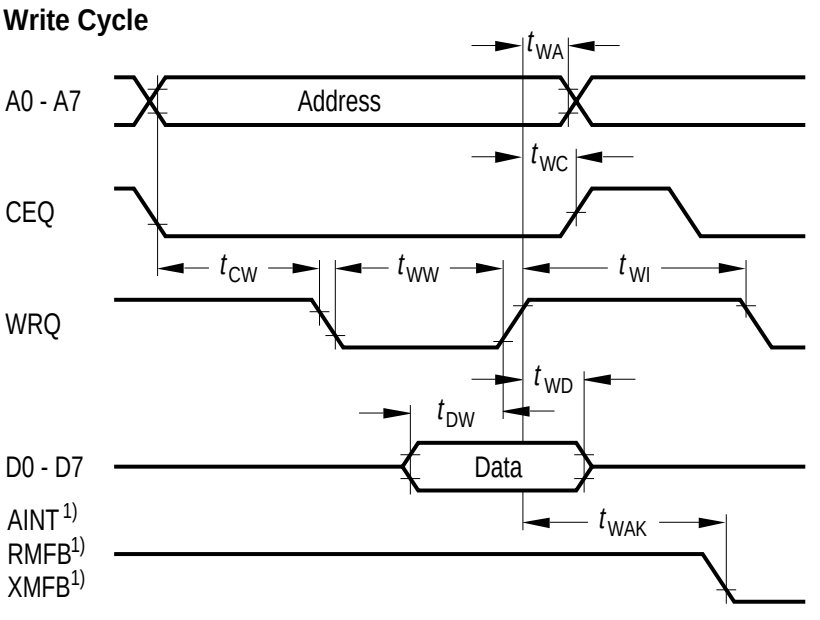


Figure 20
µP Write Timing

µP Write Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
CEQ and ADDRESS valid to WRQ valid	t_{CW}	20		ns
DATA setup before end of write	t_{DW}	35		ns
DATA hold after WRQ	t_{WD}	10		ns
WRQ pulse width	t_{WW}	70		ns
CEQ hold after WRQ	t_{WC}	10		ns
ADDRESS hold after WRQ	t_{WA}	10		ns
WRQ control interval	t_{WI}	70		ns
Interrupt acknowledge delay	t_{WAK}		$2 * t_{CP4} + 60$ $2 * t_{CP8} + 80$	ns

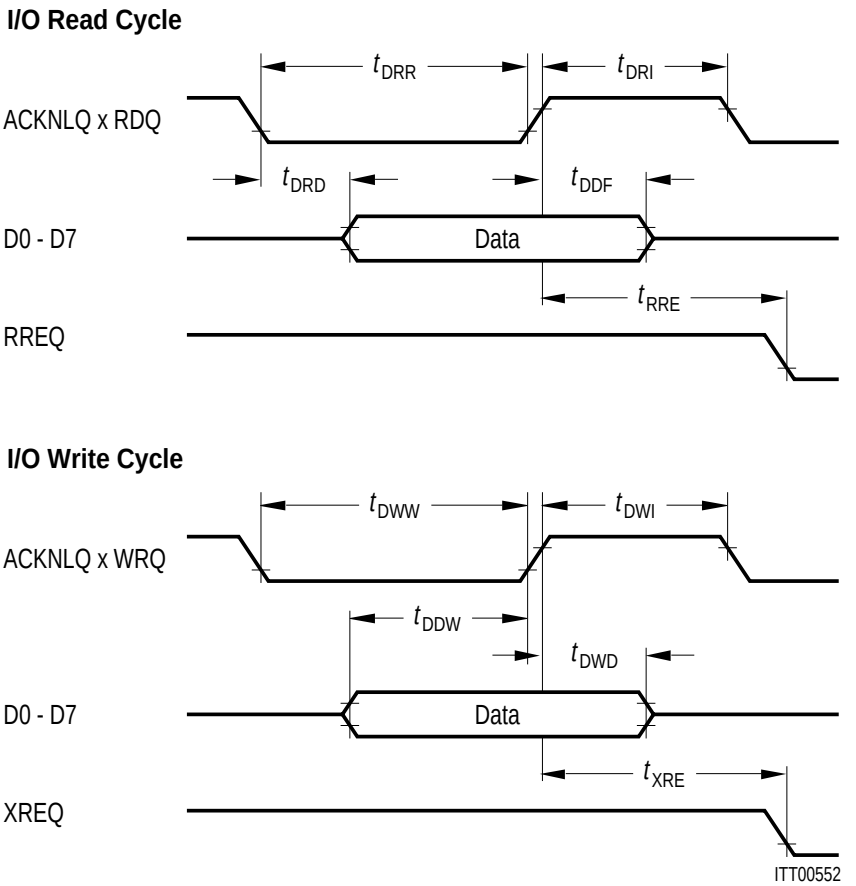
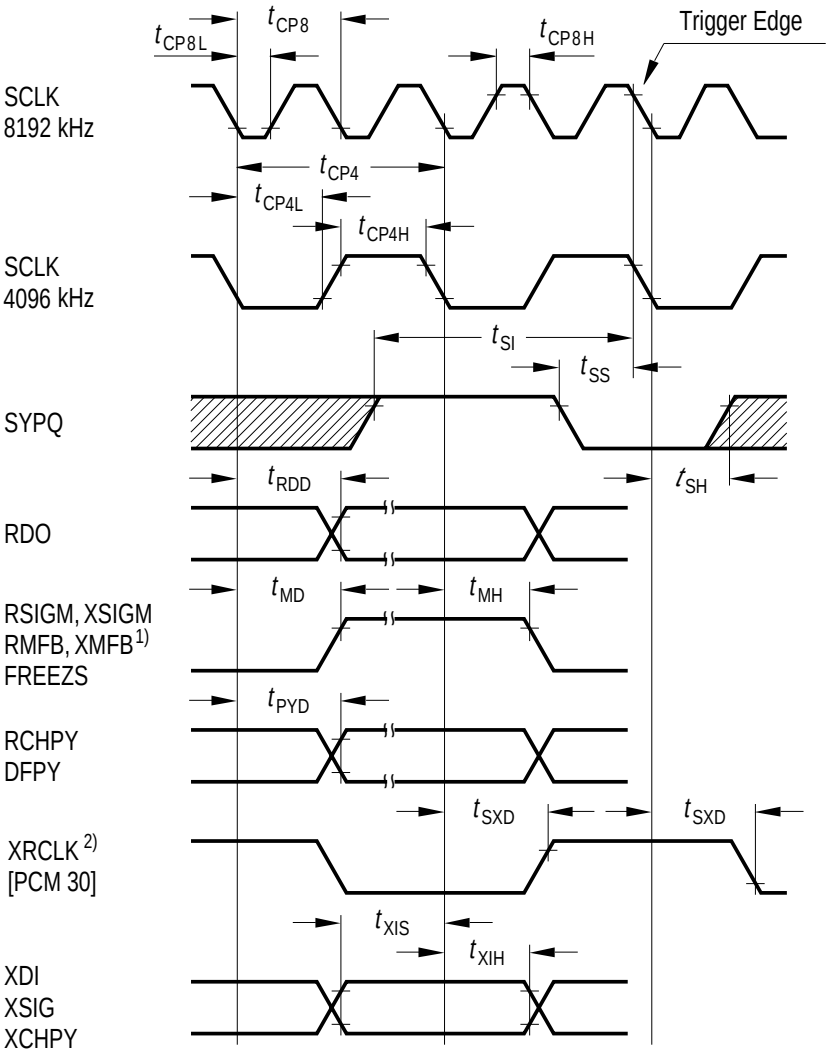


Figure 21
DMA Timing

DMA Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RDQ to DATA valid	t_{DRD}		90	ns
DATA float after RDQ	t_{DDF}	10	30	ns
RDQ pulse width	t_{DRR}	100		ns
RDQ control interval	t_{DRI}	70		ns
RREQ reset after RDQ	t_{RRE}		120	ns
DATA setup before end of write	t_{DDW}	35		ns
DATA hold after WRQ	t_{DWD}	10		ns
WRQ pulse width	t_{DWW}	70		ns
WRQ control interval	t_{DWI}	70		ns
XREQ reset after WRQ	t_{XRE}		120	ns

Serial Interface Timing



1) If not reset via µP interface

2) For even values of XCO.XCO, otherwise inverted

ITT00553

Figure 22
System Interface Timing

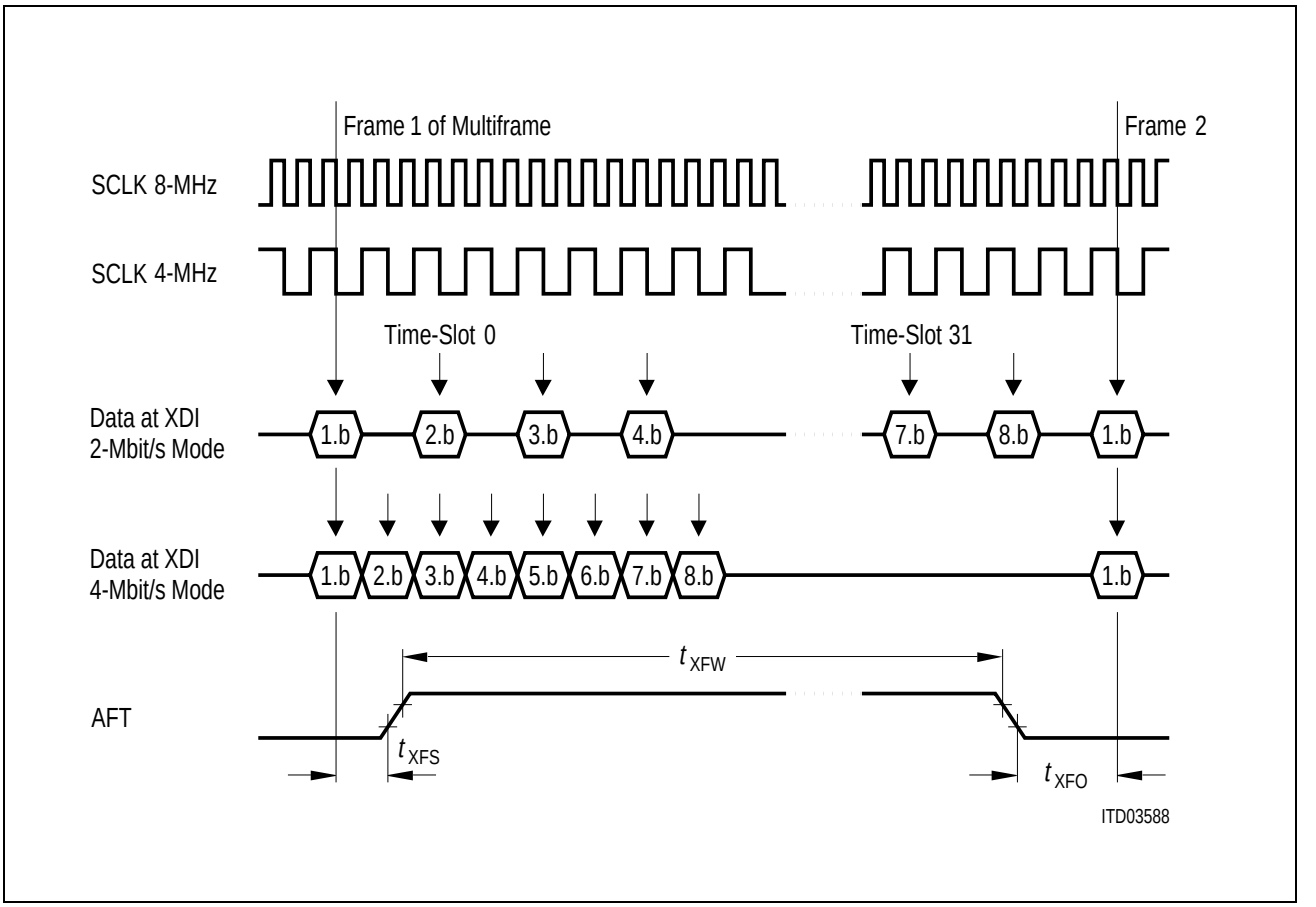


Figure 22a
Timing for Signal AFT (External Transmit Multiframe Synchronization)

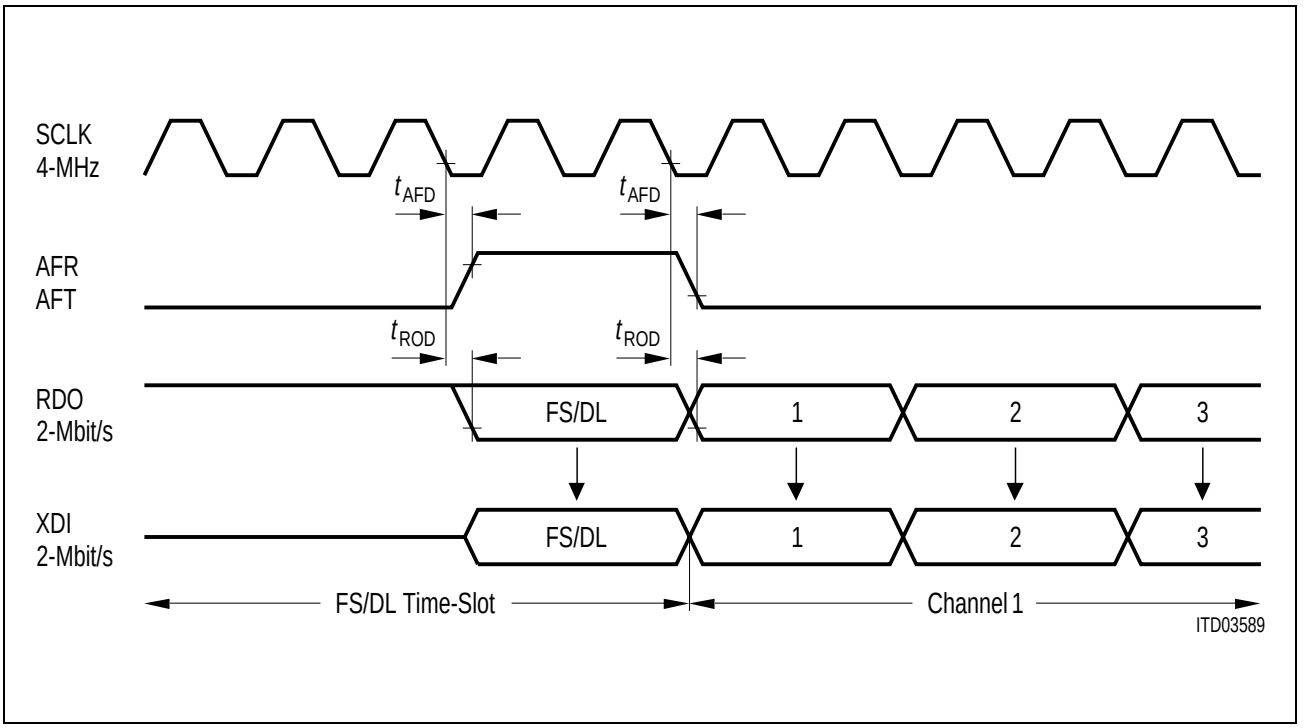


Figure 22b
Timing for Signals AFT/AFR (DL Clock) in Case of 2-Mbit/s System Interface Mode

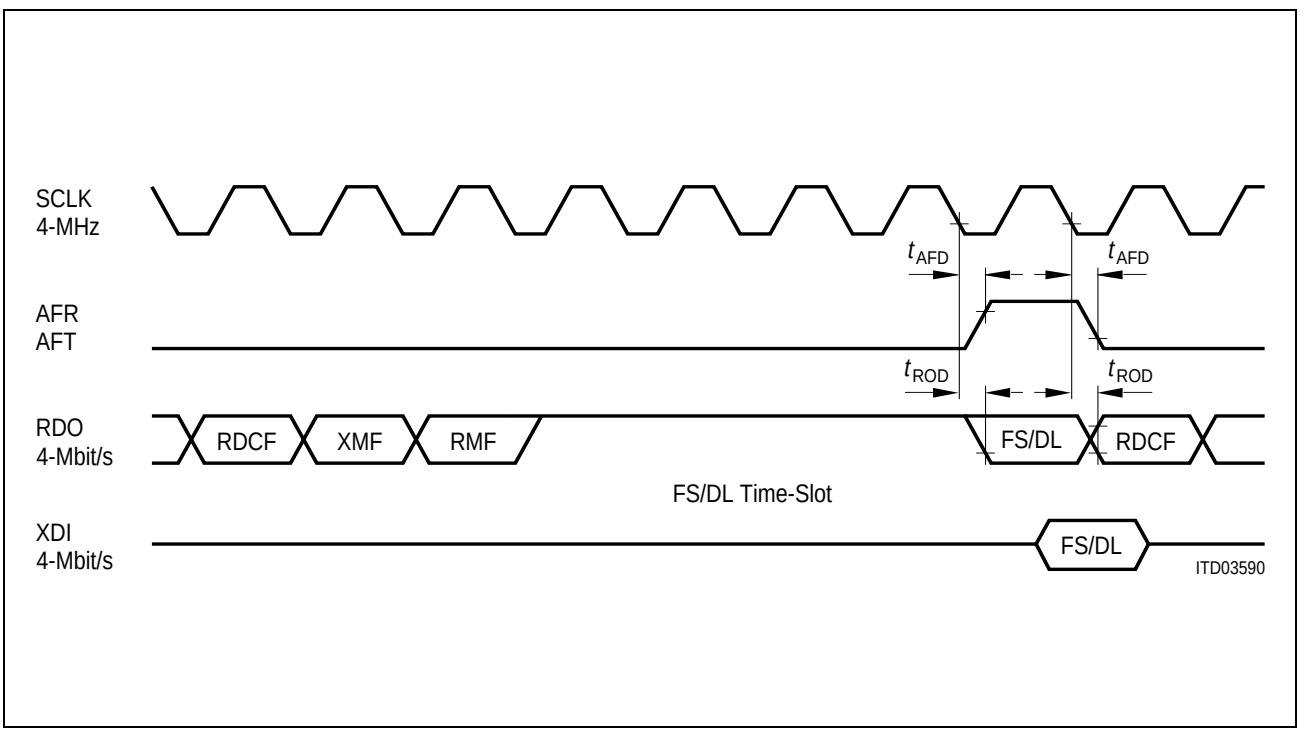
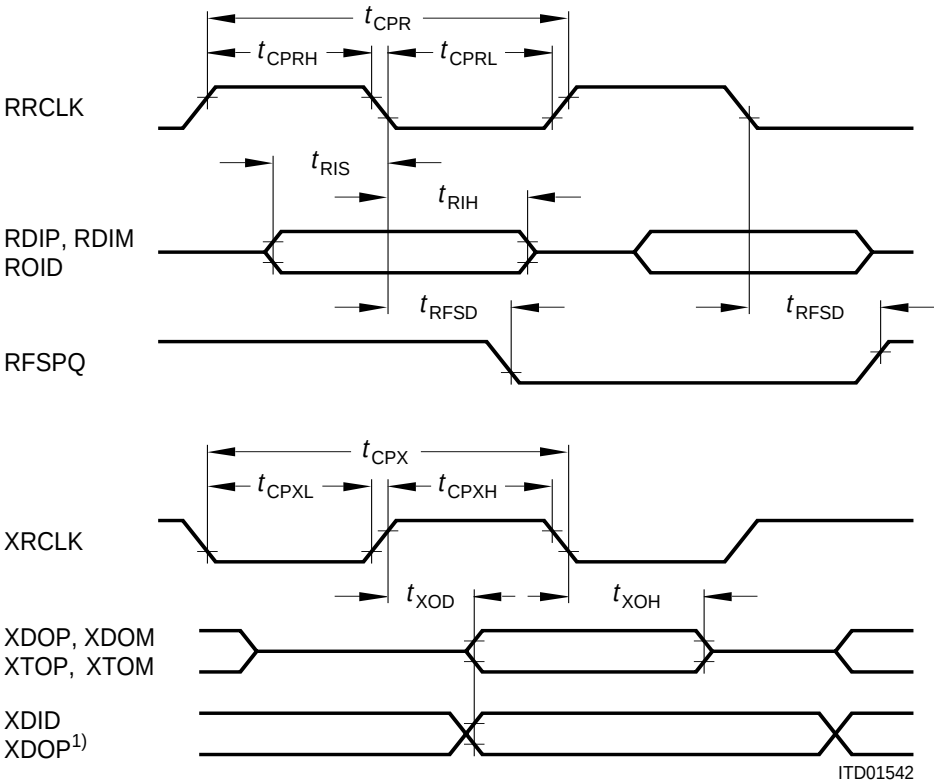


Figure 22c
Timing for Signals AFT/AFR (DL Clock) in Case of 4-Mbit/s System Interface Mode

System Interface Timing

Parameter	Symbol	Limit Values				Unit
		4096 kHz SCLK		8192 kHz SCLK		
		min.	max.	min.	max.	
SCLK period 8 MHz	t_{CP8}			typ. 122		ns
SCLK period 8 MHz low	t_{CP8L}			40		ns
SCLK period 8 MHz high	t_{CP8H}			40		ns
SCLK period 4 MHz	t_{CP4}	typ. 244				ns
SCLK period 4 MHz low	t_{CP4L}	50				ns
SCLK period 4 MHz high	t_{CP4H}	50				ns
SYPQ setup time	t_{SS}	40	t_{CP4} – 30	t_{CP8} – 40	t_{CP8} + 40	ns
SYPQ hold time	t_{SH}	40		40		ns
SYPQ inactive setup	t_{SI}	t_{CP4} + 30		2∗ t_{CP8}+ 30		ns
RDO propagation delay	t_{ROD}		90		110	ns
Marker propagation delay	t_{MS}		110		130	ns
Marker hold	t_{MH}		110		130	ns
Parity propagation delay	t_{PYD}		100		120	ns
XRCLK to SCLK delay	t_{SXD}		110		130	ns
Transmit data setup	t_{XIS}	30		30		ns
Transmit data hold	t_{XIH}	30		30		ns
AFT setup time	t_{XFS}	0		0		ns
AFT inactive setup time	t_{XFO}	2 ∗ t_{TCP4}		4 ∗ t_{TCP8}		ns
AFT pulse width	t_{XFW}	t_{CP4}		2 ∗ t_{CP8}		ns
AFT/AFR delay time	t_{AFD}	30*	90	30*	100	ns

* Test conditions: 0 °C, C_L = 50 pF



1) PCM24, Optical Interface Mode

Figure 23
Line Interface Timing

Line Interface Timing

Parameter	Symbol	Limit Values				Unit
		PCM 30		PCM 24		
		min.	max.	min.	max.	
RRCLK clock period	t_{CPR}	typ. 488		typ. 648		ns
RRCLK clock period low	t_{CPRL}	100		100		ns
RRCLK clock period high	t_{CPRH}	100		100		ns
Receive data setup	t_{RIS}	30		30		ns
Receive data hold	t_{RIH}	30		30		ns
RFSPQ propagation delay	t_{RFSD}		130		130	ns
XRCLK clock period	t_{CPX}	$2 \times t_{CP4}$ $4 \times t_{CP8}$		typ. 648		ns
XRCLK clock period low	t_{CPXL}			100		ns
XRCLK clock period high	t_{CPXH}			100		ns
Transmit data output delay	t_{XOD}		50		90	ns
Transmit data output hold	t_{XOH}	0*	50	20*	90	ns

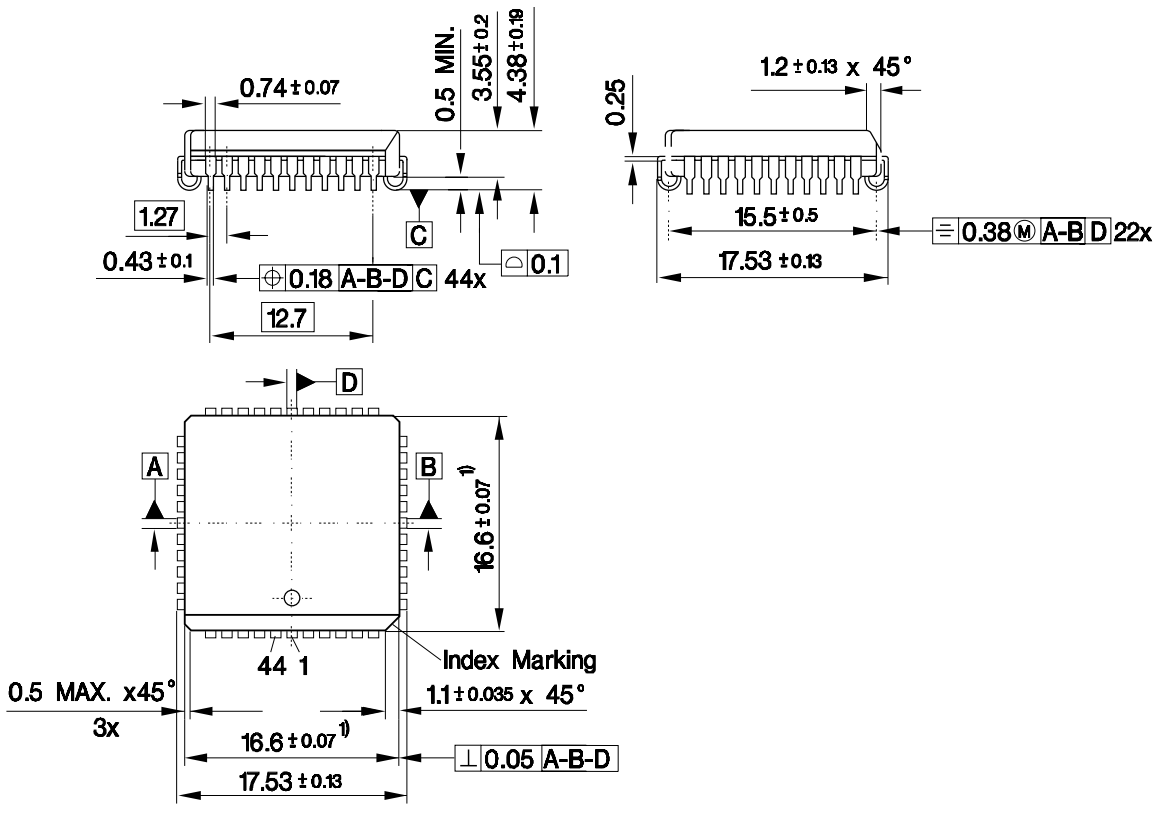
Reset Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RESQ low	t_{REL}	2000		ns

* Test conditions: 0 °C, C_L = 50 pF

8 Package Outlines

Plastic Package P-LCC-44
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

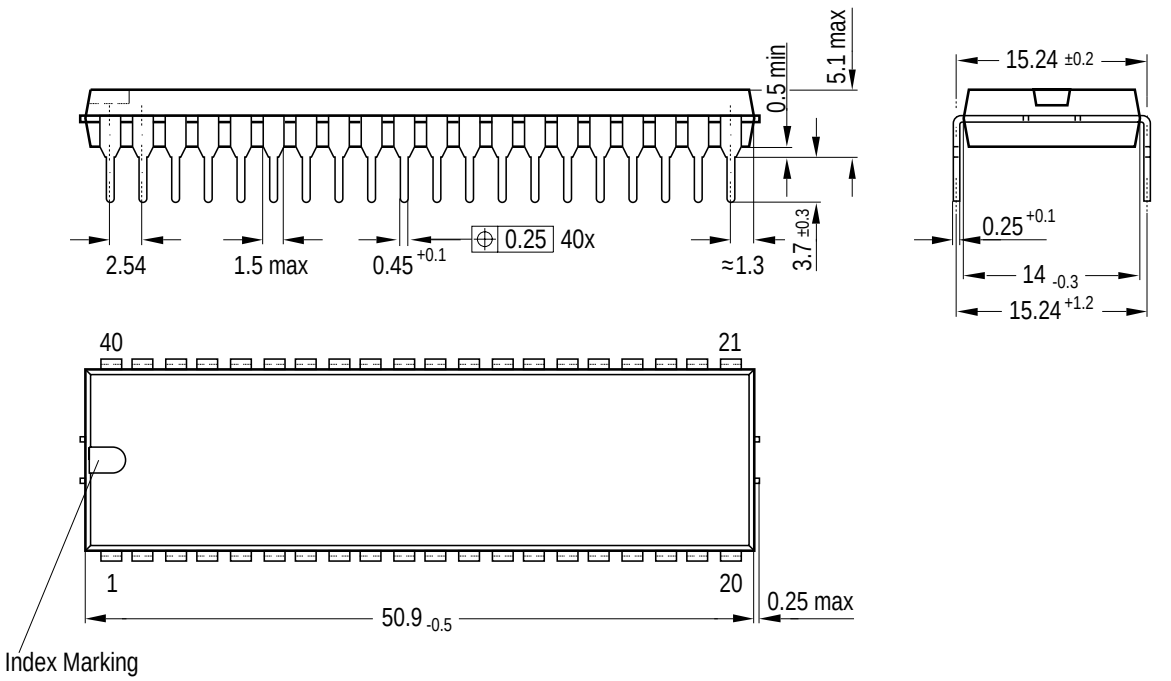
GPM05247

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-DIP-40
(Plastic Dual In-line Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

9 Annex

Additional Features of ACFA, Version 4

Additions to PCM 30 mode

- **CRC Alarm Interrupt**
  As an extension of the alarm interrupt capabilities, the occurrence of a CRC error can be defined as interrupt source (XC1.MCA) for triggering interrupt port AINT.

- **Idle Code Insertion**
  In transmit direction, the contents of selectable channels (time-slots) can be overwritten by the pattern defined via register IDLE. The selection of 'idle channels' is done by programming the four-byte register bank ICB1 ... ICB4 (enabled via CPY.SW).

- **Selectable Conditions for Loss of Synchronization**
  Asynchronous state is reached either after three or after four consecutive incorrect FAS/service words (bit RC1.ASY4). Additionally, the service word condition can be disabled (bit RC1.SWCD).

- **Multiframe Force Resynchronization**
  A search for a new multiframe alignment can be initiated via bit MODE.MFCS without influence on doubleframe synchronous state.

- **Automatic Force Resynchronization**
  A search for doubleframe alignment is automatically initiated if two multiframe pattern with a distance of n $\times$ 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained (bit MODE.AFR).

- **Submultiframe Error Indication Counter**
  If programmed via bit EMOD.ESEI, counter CVC (8 or 10 bits) counts zeros in Si-bit position of frame 13 and 15 of every received CRC multiframe. This counter option gives information about the outgoing transmit PCM line if the Si bits are used by the remote end for submultiframe error indication.

- **Code Violation Counter Extension**
  The counter CVC can be switched to 10-bit length via bit EMOD.ECVE (status bits CECX.CV8 and CECX.CV9). This is useful for extended submultiframe error indication counting.

- **Full Bauded Mode**
  Output pins XDOP, XDOM can be switched to full bauded mode via bit EMOD.XFB.

- **Extended DMA Mode**
  DMA request lines RREQ, XREQ remain active until the second read/write access to the assigned stack is provided (bit EMOD.EDMA).

- **Disable AIS to System Interface**
  Automatic transmission of AIS to system internal highway (RDO) during asynchronous state can be disabled via bit EMOD.DAIS. However, it remains programmable via bit CCR.SAIS.

- **Time-Slot 0 Extended Signaling Transparent Mode**
  Enabled via EMOD.TT0X this new mode provides transparency in transmit direction only for Sn bits.

- **Doubleframe Format with Support of Sn-Bit Stacks**
  As extension to standard doubleframe format the internal 5-byte Sn-bit stacks RSN and XSN can be used (refer to EMOD.DFSN).

- **Corrections**: generation of signal XREQ and read-back option of XSP.XS13, XSP.XS15.

Additions to PCM 24 mode

- **CRC Alarm Interrupt**
  As an extension of the alarm interrupt capabilities, the occurrence of a CRC error can be defined as interrupt source (XC1.MCA) for triggering interrupt port AINT.

- **CRC6 Inversion**
  If enabled via bit GCR.CRCI, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe.

- **Idle Code Insertion**
  In transmit direction, the contents of selectable channel can be overwritten by the pattern defined via register IDLE. The selection of 'idle channels' is done by programming the three-byte register bank ICB1 ... ICB3 (enabled via CPY.SW and CPY.BSEL).

- **Selectable Conditions for Loss of Synchronization**
  Selection is provided via bit RC1.SLC between '2 errors out of 4' or '2 errors out of 5' FT/FS bits.

- **Selectable Sync/Resync Procedure for F12 and F72 Format**
  FT and FS bit conditions, i.e. pulse frame alignment and multiframe alignment can be handled separately if programmed via bit EMOD.SSP.

- **Multiframe Begin Signal**
  Signals RMFB and XMFB indicate only the multiframe begin. Additional pulses (every 12 frames) are disabled via bit ACR.MFBS.

- **4-kHz DL Clock**
  If programmed via bit ACR.DLC, ports RCHPY and XCHPY provide signals which mark the DL-bit position within the data stream at RDO and XDI.

- **AIS Indication**
  The AIS indication algorithm is changed to detect AIS even in the presence of BER 10**-3 (bit GCR.AISM).

- **Remote Alarm Indication**
  Algorithms are changed to detect remote alarm even in the presence of BER 10**-3 (bit RC1.RRAM).

- **Transparent Mode**
  Setting bit GCR.TM switches the ACFA in transparent mode:
  – In transmit direction bit 8 of the FS/DL time-slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame.
  – In receive direction the framing bit is also forwarded to RDO and inserted in the FS/DL time-slot. Bit RDCF (bit 1 of FS/DL time-slot) indicates a DL bit.

- **External Multiframe Synchronization**
  The transmitter of the ACFA can be synchronized externally for multiframe begin (port XCHPY, bit ACR.EXMF). This feature is required if the bit-robbed signals are routed through the switching network and are inserted in transmit direction via the system interface.
- **Wander Compensation**
  In receive direction and channel translation mode 0 the ACFA compensates wander with the maximum wander amplitude of 142 UI peak to peak if enabled via bit ACR.SLM.
- **Code Violation Counter Extension**
  The counter CVC can be switched to 10-bit length via bit EMOD.ECVE (status bits CECX.CV8 and CECX.CV9).
- **Full Bauded Mode**
  Output pins XDOP, XDOM can be switched to full bauded mode via bit EMOD.XFB.
- **Extended DMA Mode**
  DMA request lines RREQ, XREQ remain active until the third read/write access to the assigned stack is provided (bit EMOD.EDMA).
- **Disable AIS to System Interface**
  Automatic transmission of AIS to system internal highway (RDO) during asynchronous state can be disabled via bit EMOD.DAIS. However, it remains programmable via bit CCR.SAIS.
- **Corrections**: generation of signal XREQ.

Important Remarks

- Unused control bits have to be programmed with a logical ‘0’, although they are set to logical ‘1’ when reading the assigned registers.
- In contrast to the Preliminary Delta Sheet 03.90. status bits CECX.CV8 and CECX.CV9 occupy bit positions 4 and 5 of register CECX.