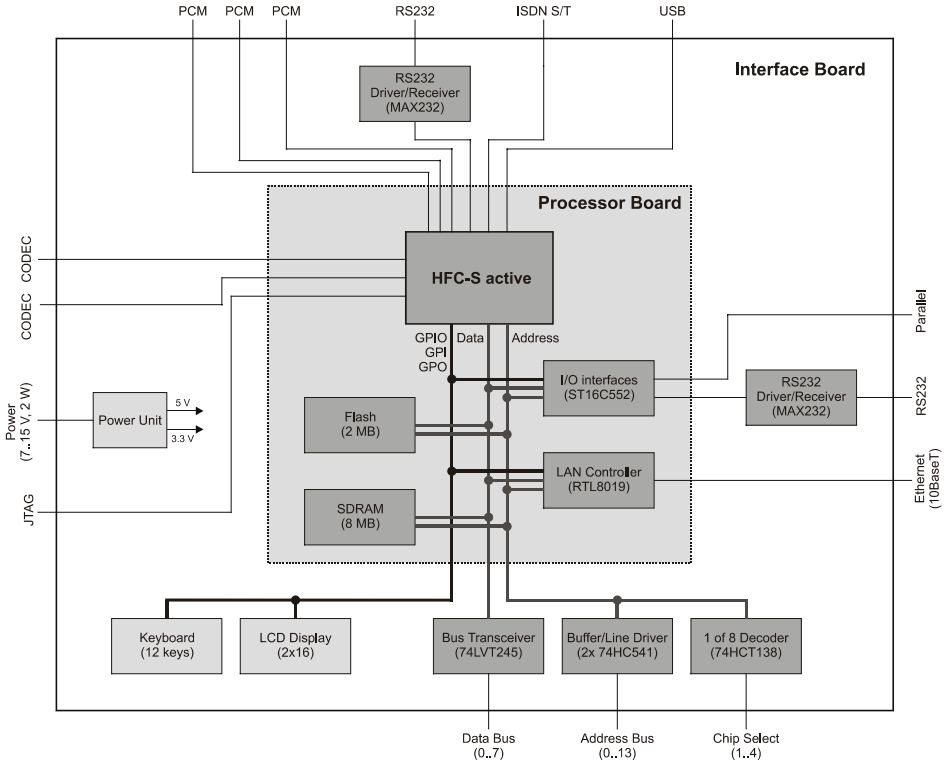
Product Brief HFC-S active Evaluation Kit

HFC-S active Evaluation Kit

The ISDN Processor Demo Board

Block Diagram of Evaluation Board HFC-S active



Introduction

Evaluation Board HFC-S active

The Evaluation Kit of the „HFC-S active“ is the perfect testing environment for ISDN hardware projects like ISDN PABX, ISDN POTS terminal adapters or ISDN telephones with data port. The board consists of a Processor Modul with the „HFC-S active“ which is mounted on top of an Interface PCB. The interfaces of the Evaluation Board include ISDN S/T, UART, USB, PCM, two CODECs and Ethernet among others. The interface board contains keyboard, display and buzzer for evaluation purposes. A JTAG cable for the Evaluation Board is also available as optional extra.

The Evaluation Kit contains a µC-Linux which was ported to the „HFC-S active“, including the ISDN protocol software of the ISDN4Linux developers group. An additional Ethernet chip is implemented in the evaluation system in order to enable an easy communication over TCP/IP. As the Evaluation Board is capable of booting from LAN, the firmware development process can be accelerated significantly.

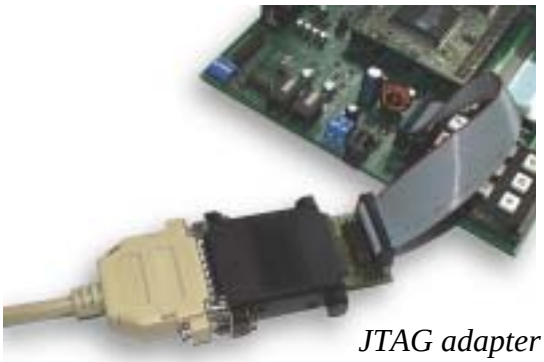
The source code of all protocol stacks in the Evaluation Kit is available as source code. It even can be used for commercial ISDN developments without license fees under the regulations of GPL (GNU Public License). Therefore the Evaluation Kit is not only an excellent test environment for the ISDN processor „HFC-S active“, but can also function as a basis for product development with short time-to-market.

The HFC-S active Evaluation Kit can be ordered directly from Cologne Chip at the cost price of 400,- USD, the additional JTAG adapter at the cost price of 50,- USD.

Product Brief HFC-S active Evaluation Kit

Contents of Evaluation Kit

- ❑ Processor Modul with HFC-S active
- ❑ Interface PCB
- ❑ Telephone handset
- ❑ Power supply unit
- ❑ Software/Instruction CD-ROM
- ❑ JTAG adapter (optional extra)



JTAG adapter

Technical Overview of Evaluation Kit

Hardware

- ❑ Interfaces of HFC-S active:
  ISDN S/T, UART, USB (1.1), 3 PCM, 2 CODECs, PWM (all accessible on the Evaluation Board)
- ❑ Additional interfaces of the Evaluation Board:
  Ethernet 10BaseT (Realtek RTL8019), RS232 and RS485 with FIFO and all signals, 14 bit address bus, 8 bit data bus, 4 free chip select signals, parallel port, JTAG
- ❑ Peripheral components:
  keyboard matrix (3x4 keys), LCD (2x16 characters), piezzo buzzer, 4 DIP switches, GPIOs, 2 LEDs, reset button, JTAG adapter (optional extra)
- ❑ Flash: 2 MB
- ❑ Memory: 8 MB SDRAM

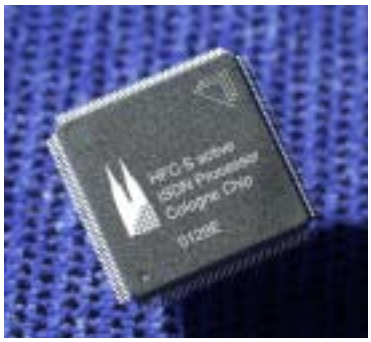
Software

- ❑ Operating system: µC-Linux, kernel version 2.0.39, ARM7 port adopted to the HFC-S active
- ❑ GNU C compiler (GCC) as cross compiler for ARM7 TDMI™ processor, version 2.95.3
- ❑ Boot loader (binary only) for bootp/tftp support (remote booting via LAN)
- ❑ Driver for LCD and keyboard
- ❑ Telephone application as demo software
- ❑ Protocol stacks:
  All ISDN protocols of the ISDN4Linux package and an Ethernet protocol stack are enclosed as source code and may be used under the terms of GPL.

Note:
Memory resources can be minimized according to target application!

Contact

In case of any questions, please contact us directly. Our Sales and Support Team is glad to assist!



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