XHFC Series Evaluation Kit

XHFC-2SU Evaluation Board
Revision 1

Hardware Description

January 2016

Contents

1 Overview

XHFC-2SU is a single-chip ISDN transceiver with integrated HDLC controllers for two ISDN S/T or U_{pN} / U_{p0} [1] Basic Rate Interfaces. Similar microchips with four ISDN ports or with one ISDN port are also available within the XHFC microchip series.

This document describes the XHFC-2SU Evaluation Board revision 1 which is part of the XHFC Series Evaluation Kit.

Up to two line interfaces can be used with this evaluation board. Different line interface subassemblies are available and must be piggypacked onto the XHFC-2SU Evaluation Board.

The XHFC-2SU Evaluation Board is made of the following functional parts:

- the XHFC-2SU microchip,
- two sockets to mount a line interface subassembly each,
- a socket for a power feeding module (optional)
- a connector to the host processor system
- a PCM interface connector.

The schematic is shown in Figures 3 and 4 from page 7.

The printed cicuit board consists of 4 layers. Signal traces are assigned to the outer layers while the inner layers are used for ground and power planes. Views of the board design are shown in Figures 5 to 7 from page 10.

Please refer to the data sheet [1] for detailed information on the XHFC-2SU microchip.

Software is not included in the XHFC Series Evaluation Kit. Please contact the Cologne Chip support team for a demo layer 1 driver, register header files, Linux drivers or further software support.

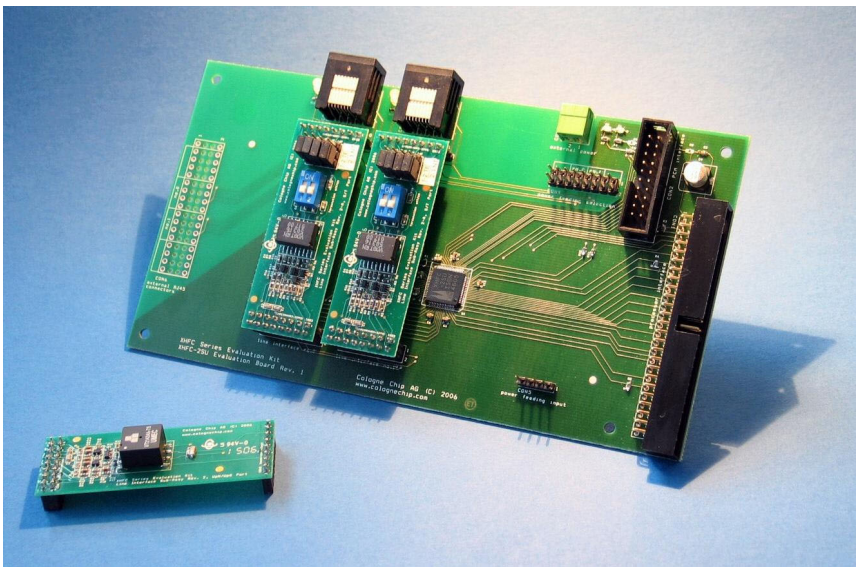


Figure 1: *XHFC-2SU Evaluation Board with two subassemblies for S/T line interface mounted and an additional subassembly for U_{pN} / U_{p0} line interface beside*

[1] U_{pN} / U_{p0} in the following referred to as U_p.

2 Evaluation board description

2.1 Line interfaces

The XHFC-2SU Evaluation Board has two board sockets CON7 / CON8 and CON10 / CON11 to piggyback line interface modules.

Several line interface subassemblies can be used with the XHFC Series Evaluation Kit:

- Line Interface Subassembly for S/T Port (universal circuitry for TE mode and NT mode) [2]
- Line Interface Subassembly for S/T Port (reduced circuitry for NT mode only) [3]
- Line Interface Subassembly for S/T Port with software configuration (TE / NT mode selection, line termination and power feeding enable / disable) [4]
- Line Interface Subassembly for U_{pN} / U_{p0} Port [5]
- Line Interface Subassembly for combined ST/U_p Port (same circuitry can be used for either S/T or U_{pN} / U_{p0} mode selected by coding plug) [6]
- Line Interface Subassembly for combined ST/U_p Port (same circuitry can be used for either S/T or U_{pN} / U_{p0} mode detected automatically) [7]

For every XHFC Series Evaluation Kit order, the Cologne Chip team asserts a set of subassemblies according to the specific project requirements.

Two RJ45 jacks for the line interfaces are mounted on the XHFC-2SU Evaluation Board.

An optional connector to pass the line interface signals to an external system in replacement for the RJ45 jacks is provided as well.

2.2 Power feeding

Every line interface can have power feeding capability. Power feeding is an option for bus-powered terminal devices, e.g. phones, and must not be enabled for terminals in TE mode.

Two different operation modes can be used as described in the following.

External power feeding source

The external power source has to be connected to CON3. The typical voltage range is 34 V . . 42 V.

Jumpers on CON4 are used to enable power feeding of every line interface individually as shown in table 1. Two jumpers are required for every line interface. Without jumpers inserted, the power source is not connected to a line interface.

CON5 is not used in this operation mode.

Using the power feeding module on board socket CON4 / CON5 (optional)

An optional power feeding module can be piggybacked onto the board socket CON4 / CON5. It generates 38 V from 12 V input voltage connected to CON3.

Table 1: *Power feeding jumper settings on CON4*

Line interface	Jumper repuired on CON4 pins for P+	Jumper repuired on CON4 pins for P-
no. 0	10 – 12	9 – 11
no. 1	6 – 8	5 – 7

The power feeding module houses jumpers to power-up every line interface individually. Two jumpers are required for every line interface. Without jumpers inserted, the power source is not connected to a line interface.

2.3 General purpose I/O signals

Every board socket which is not used for a line interface, offers eight general purpose I/O (GPIO) signals. From these, six GPIO signals are available as second pin function of XHFC-2SU.

Two further GPIO signals GPn_0 and GPn_1 (n = 0 . . 1) are provided for service bits on the line interface subassemblies and are unreserved when the subassembly is not mounted on the board socket. As some line interface subassemblies do not use their GPIO signals, these can be used for other purposes optionally. Please refer to the subassembly documentations [2, 5].

Table 2: *GPIO signals GPn_0 and GPn_1*

GPIO	Signal source	Signal target
GPIO0_0	XHFC-2SU pin 36 (GPIO0)	line interface no. 0, connector CON7.5
GPIO0_1	XHFC-2SU pin 35 (GPIO1)	line interface no. 0, connector CON7.7
GPIO1_0	XHFC-2SU pin 28 (GPIO2)	line interface no. 1, connector CON10.5
GPIO1_1	XHFC-2SU pin 27 (GPIO3)	line interface no. 1, connector CON10.7

2.4 PCM interface

The PCM interface and several additional signals are wired to CON2. The connection to an external PCM bus and to synchronization signals can be configured with 0 Ω resistors R9 . . 12 which are optionally populated or omitted due to the application needs.

Furthermore, F1_0 and F1_1 signals or their second pin functions GPIO2 and GPIO3 of XHFC-2SU can be used for three different tasks on the XHFC-2SU Evaluation Board:

1. Two LEDs D1 and D2 can report status information on GPIO2 and GPIO3 outputs.
2. F1_0 and F1_1 can be wired to CON2 with R9 and R10 populated. These signals can be used for external CODECs connected to the PCM bus, e.g.
3. GPIO2 and GPIO3 are optionally used from the line interface subassembly connected to the board socket CON10 / CON11.

2.5 Host processor interface

The host processor has to be connected to CON1. As all XHFC-2SU pins of the microprocessor interface are wired to CON1, all processor modes can be used with the XHFC-2SU Evaluation Board:

- Serial processor interface (SPI)
- Parallel processor interface in Motorola mode (8 bit, multiplexed)
- Parallel processor interface in Motorola mode (8 bit, non-multiplexed)
- Parallel processor interface in Siemens / Intel mode (8 bit, multiplexed)
- Parallel processor interface in Siemens / Intel mode (8 bit, non-multiplexed)

Figure 2 shows how to interconnect the XHFC-2SU Evaluation Board to an SPI system. CON100 has to be connected to CON1 of the XHFC-2SU Evaluation Board. Please note, that all signal names at CON100 are changed to SPI pin names of the XHFC-2SU. Pins 21, 23 and 39 of CON100 must not be connected. All other open pins (1, 2, 6, even numbers 10 . . 46, 49) are attached to ground or power supply of the XHFC-2SU Evaluation Board.

For interconnection of the XHFC-2SU Evaluation Board to a parallel processor system, please refer to the data sheet schematics [1].

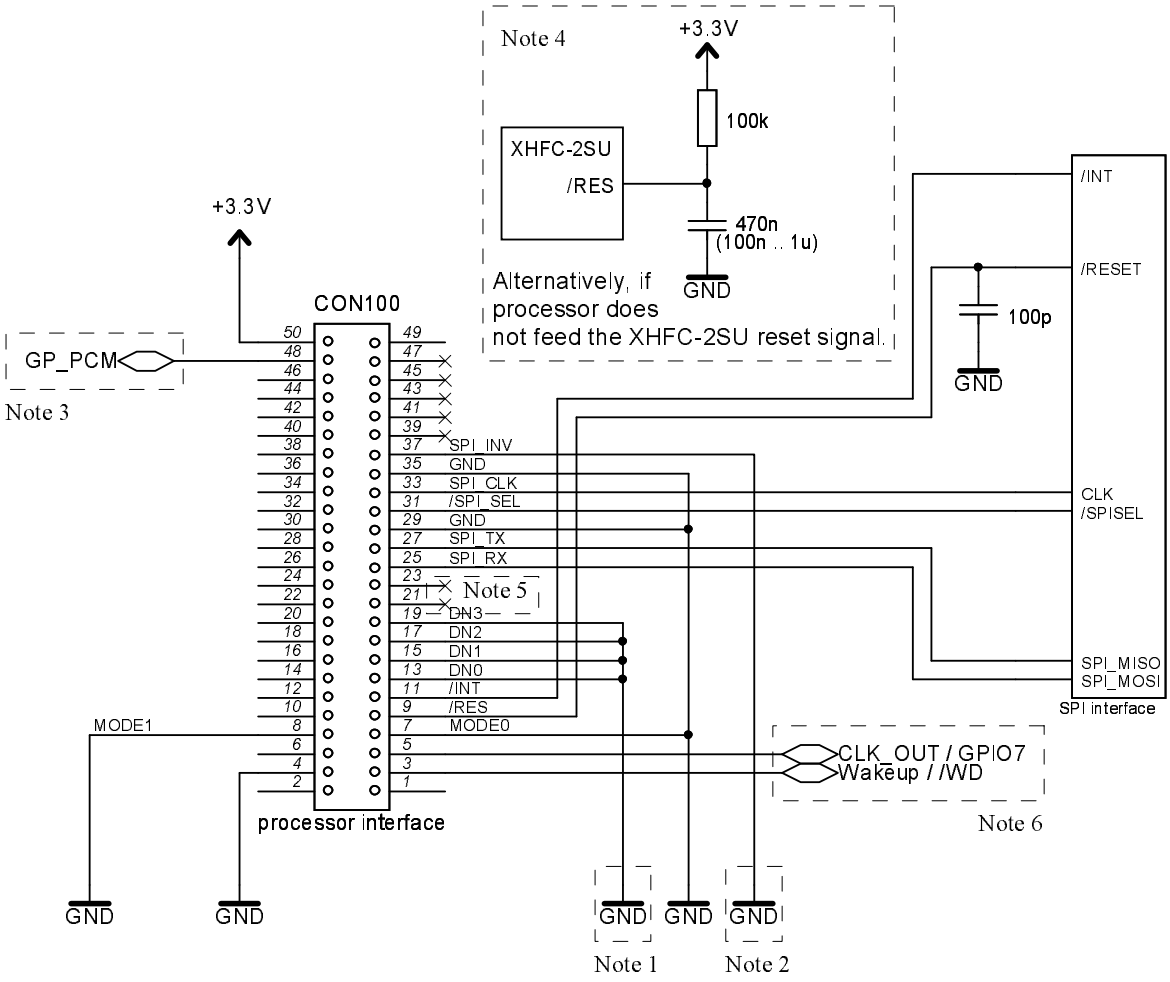
Please note !

Please note, that pins 35 and 29 of CON100 must be connected to ground in SPI mode. These pins have a different function in parallel processor mode. Thus, ground connection via any GND pin (4, 6 or even numbers 10 . . 46) is required as well.

Pins 23, 21 and 39 of CON100 are NC in SPI mode and must not be connected. They are only used in parallel processor mode.

2.6 Power supply

The XHFC-2SU Evaluation Board requires 3.3 V stabilized supply voltage on CON1 pins 1, 2, 49 and 50. System ground must be connected to CON1 pins 4, 6 and others (please refer to the schematic on page 7).



Note 1:

DN0 .. 3 are used to select an SPI device number. Any number in the range 0 .. 15 is allowed and '0000' is shown here.

Note 2:

SPI_INV can optionally be used to invert the SPI clock. It should either be connected to ground or power supply.

Note 3:

GP_PCM can optionally be used to offer a GPIO signal to the PCM connector of the XHFC Series Evaluation Kit. It can be left open if not used.

Note 4:

The reset pin /RES of XHFC-2SU should never be left open. See data sheet for detailed reset information.

Note 5:

XHFC-2SU pins 6 and 7 (CON1 pins 21 and 23) should be connected to ground in SPI mode to avoid floating inputs.

However, the SPI connection of the eval board leaves them open to avoid short circuit if XHFC-2SU is in parallel processor mode during start-up procedure.

Note 6:

These signals can optionally be used. When not used, they should be configured to output characteristic and can be left open in this case.

Important note:

DN0 .. 3 can only be connected to VDD or GND when MODE0 and MODE1 pins are fixed to GND. Otherwise serial resistors must be inserted because DN0 ..3 might be outputs during reset.

Figure 2: *XHFC-2SU Evaluation Board interconnection to an SPI system*

3 Evaluation board schematic

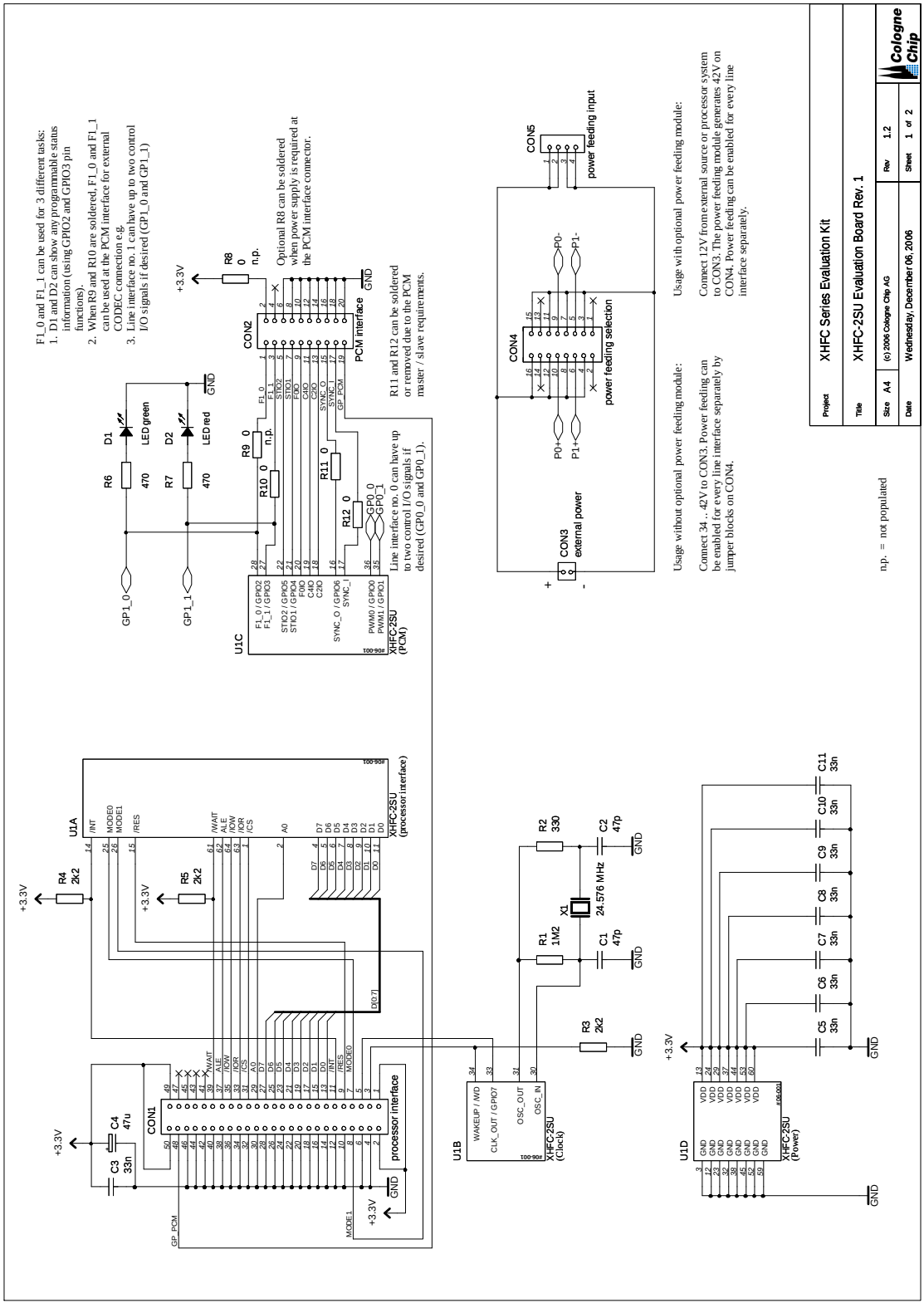


Figure 3: *XHFC-2SU Evaluation Board schematic (page 1 of 2)*

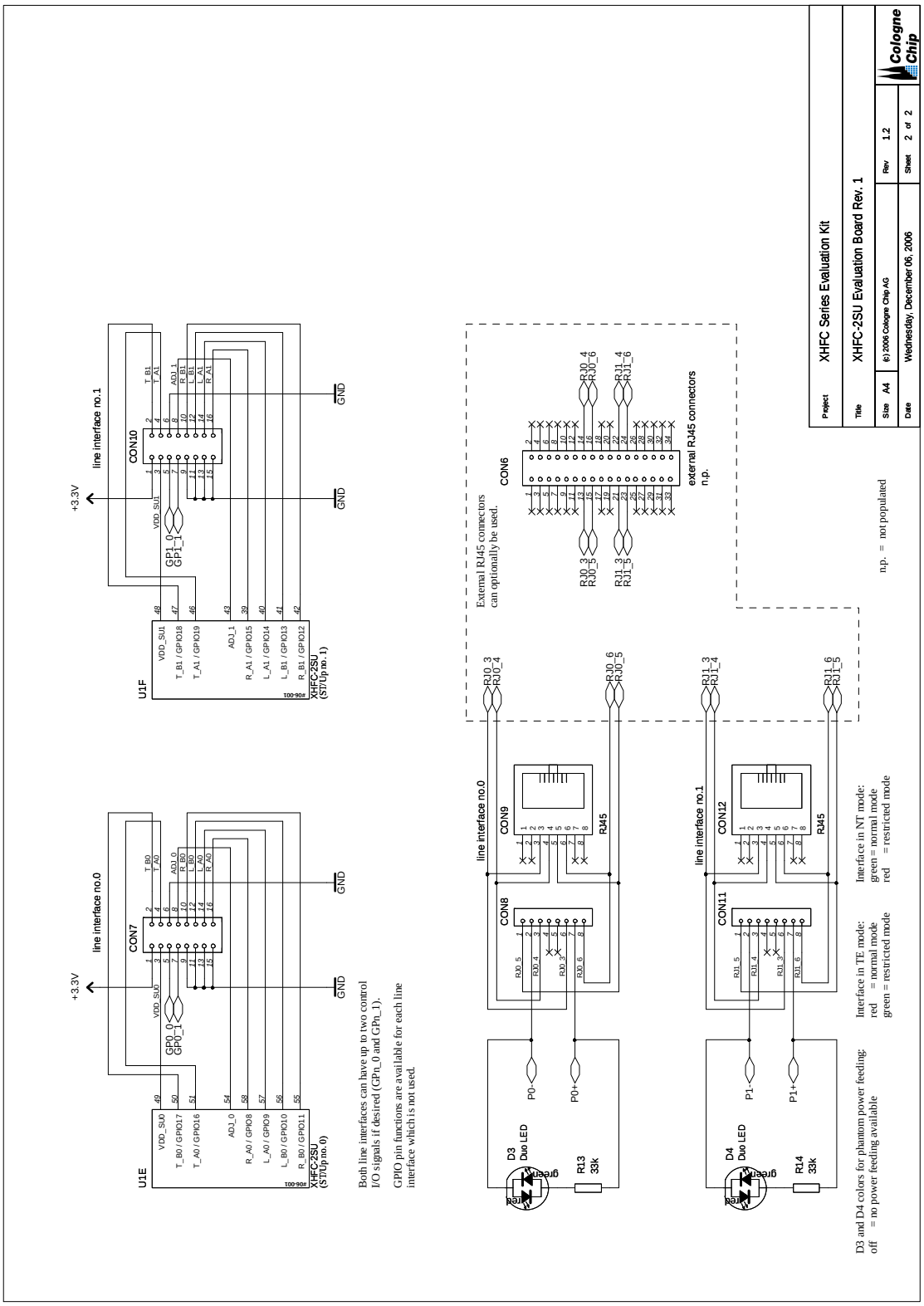


Figure 4: *XHFC-2SU Evaluation Board schematic (page 2 of 2)*

Bill of Materials: **XHFC Series Evaluation Kit**

XHFC-2SU Evaluation Board Rev. 1

Revision: 1.2, generated on Wednesday, December 06, 2006 by Cologne Chip AG

(n.p. = not populated)

Resistors (12..14 pcs.)

R1	1M	
R2	330	
R3,R4,R5	2k2	
R6,R7	470	
R8,R9	0	n.p.
R10,R11,R12	0	
R13,R14	33k	

Capacitors (11 pcs.)

C1,C2	47p
C3,C5,C6,C7,C8,C9,C10,C11	33n
C4	47u

Diodes (4 pcs.)

D1	LED green
D2	LED red
D3,D4	Duo LED

Integrated Circuits (ICs) (1 pc.)

U1	XHFC-2SU

Connectors (11..12 pcs.)

CON1	Box header 2x25, angled	
CON2	Box header 2x10	
CON3	STL1550-2-G35-H	
CON4,CON7,CON10	Pin header 2x8	
CON5	Pin header 1x4	
CON6	Female header 2x17, dual entry type	n.p.
CON8,CON11	Pin header 1x8	
CON9,CON12	RJ45	

Oscillators (1 pc.)

X1	24.576 MHz

Total:

12 x Resistors
11 x Capacitors
4 x Diodes
1 x Integrated Circuits (ICs)
11 x Connectors
1 x Oscillators

40 total
+ 3 not populated

4 Evaluation board layout

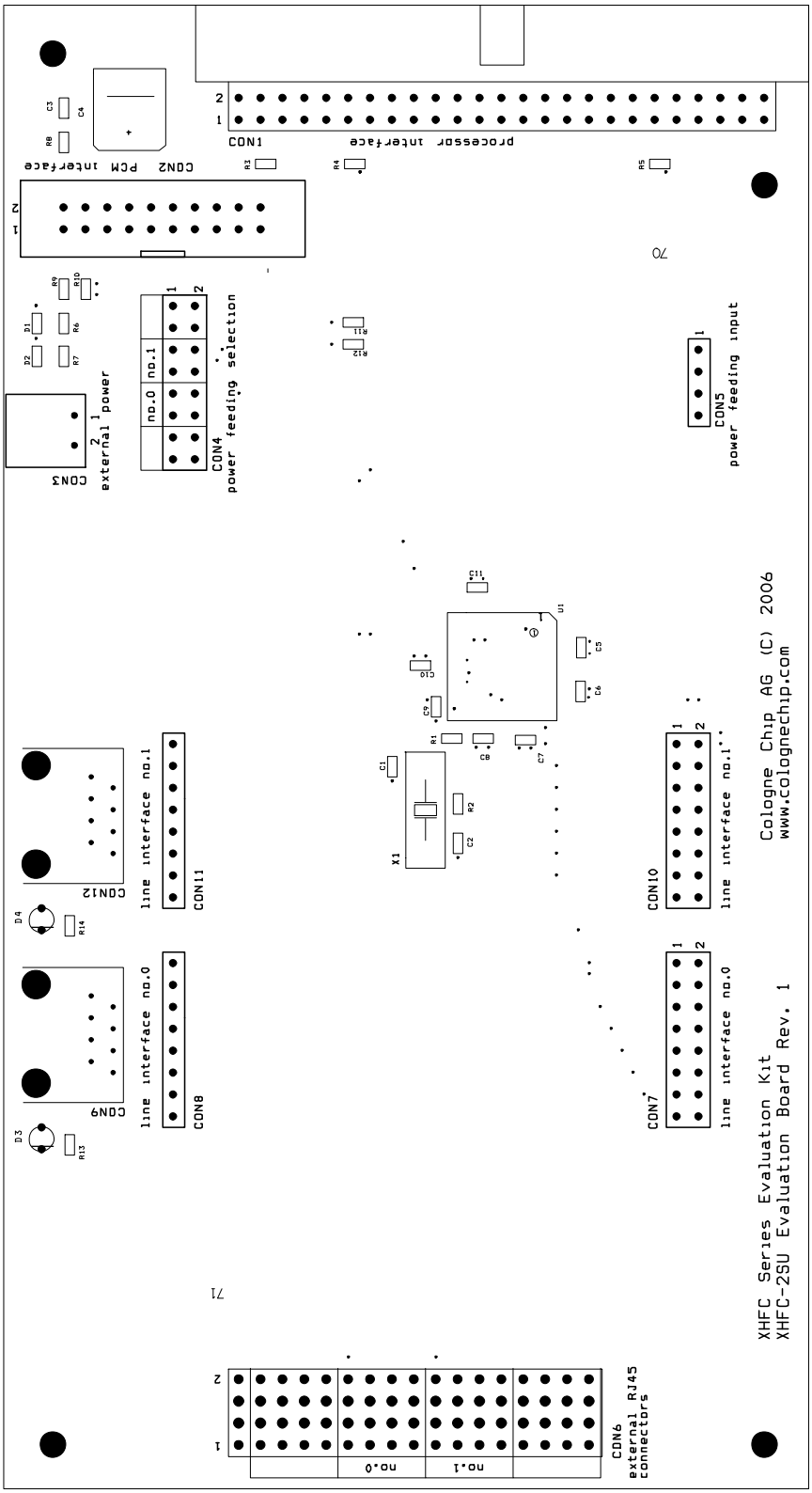


Figure 5: *XHFC-2SU Evaluation Board board (top side inscription)*

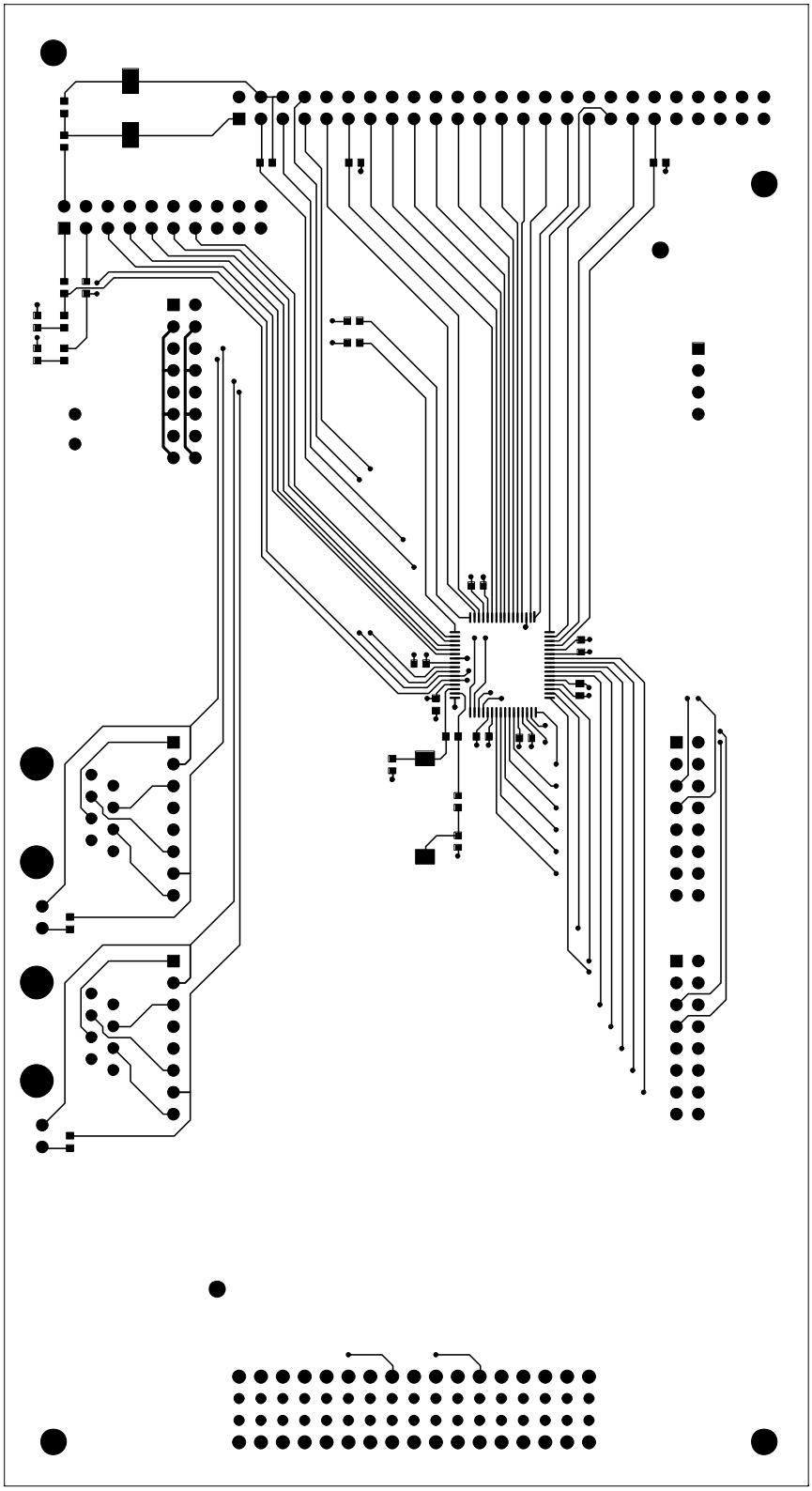


Figure 6: *XHFC-2SU Evaluation Board board (top side traces)*

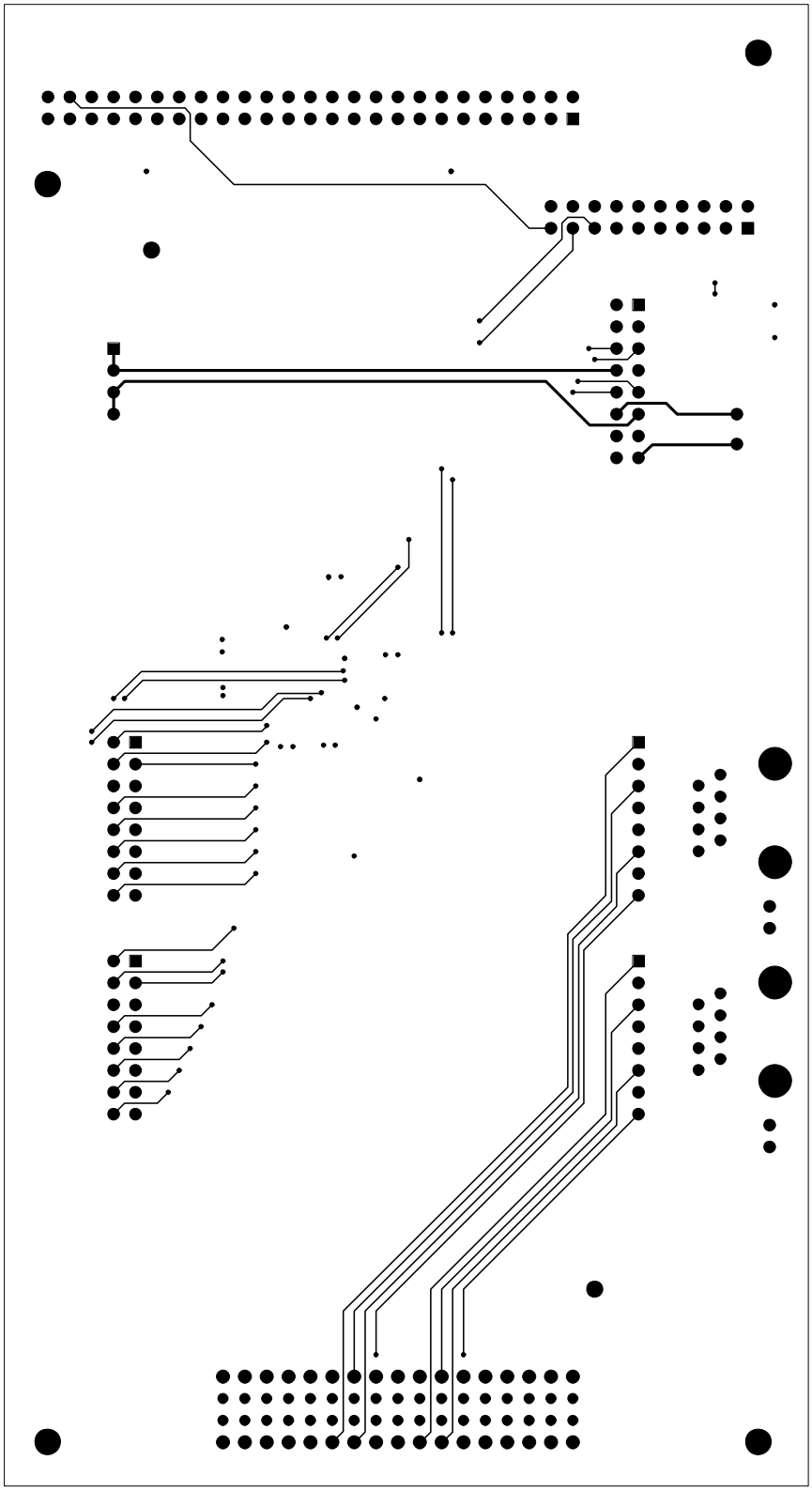


Figure 7: *XHFC-2SU Evaluation Board board (bottom side traces)*

References

[1] Cologne Chip AG. *XHFC-2SU, Extended ISDN HDLC FIFO controller with two Universal ISDN Ports (data sheet)*, June 2012.

[2] Cologne Chip AG. *XHFC Series Evaluation Kit. Line Interface Subassembly Rev. 2, S/T Port*, January 2007.

[3] Cologne Chip AG. *XHFC Series Evaluation Kit. S/T Port Line Interface Subassembly (for NT Mode only) Rev. 2*, January 2007.

[4] Cologne Chip AG. *XHFC Series Evaluation Kit. S/T Port Line Interface Subassembly with Software Configuration Rev. 1*, January 2007.

[5] Cologne Chip AG. *XHFC Series Evaluation Kit. Line Interface Subassembly Rev. 2, U_{pN} / U_{p0} Port*, January 2016.

[6] Cologne Chip AG. *XHFC Series Evaluation Kit. ST / Up Port Line Interface Subassembly with Coding Plug Rev. 1*, January 2007.

[7] Cologne Chip AG. *XHFC Series Evaluation Kit. ST /Up Port Line Interface Subassembly with Automatic Detection Rev. 2*, April 2009.

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