RF Agile Transceiver

ADI Confidential

AD9365

FEATURES

- RF transceiver with integrated 12-bit DACs and ADCs
- Band: 200 MHz to 2.3 GHz
- Supports TDD and FDD operation
- Tunable channel BW: <200 kHz to 10 MHz
- 3 band receiver: 3 differential or 6 single-ended inputs
- Superior receiver sensitivity with a noise figure < 2.5 dB
- RX gain control
  - Real-time monitor and control signals for manual gain
  - Independent automatic gain control (AGC)
- 2 band differential output transmitter
- Highly linear broadband transmitter
  - TX EVM: ≤−34 dB
  - TX noise: ≤−157 dBm/Hz noise floor
  - TX monitor: ≥66 dB dynamic range with 1 dB accuracy
- Integrated fractional-N synthesizers
  - 2.5 Hz maximum local oscillator (LO) step size
- No TX or RX SAW filters required
- CMOS digital interface

APPLICATIONS

- 3G femtocell base stations
- Smart grid power meter transceivers

FUNCTIONAL BLOCK DIAGRAM

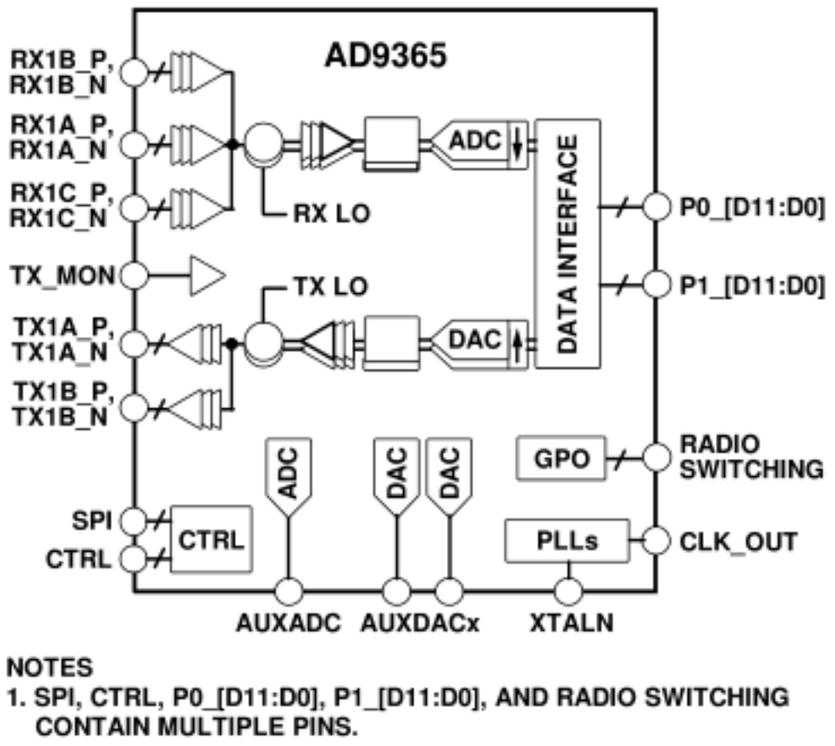

Figure 1.

GENERAL DESCRIPTION

The AD9365 is a high performance, highly integrated RF Agile Transceiver™ designed for use in 3G base station applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The AD9365 operates in the 200 MHz to 2.3 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from <200 kHz to 10 MHz are supported.

The direct conversion receiver has state-of-the-art noise figure and linearity. The receive (RX) subsystem includes independent automatic gain control (AGC), dc offset correction, quadrature correction, and digital filtering, thereby eliminating the need for these functions in the digital baseband. The AD9365 also has flexible manual gain modes that can be externally controlled. Two high dynamic range ADCs digitize the received I and Q signals and pass them through configurable decimation filters and 128-tap FIR filters to produce a 12-bit output signal at the appropriate sample rate.

The transmitter uses a direct conversion architecture that achieves high modulation accuracy with ultralow noise. This transmitter design produces a best-in-class TX EVM of <−34 dB, allowing significant system margin for the external power amplifier (PA) selection. The on-board transmit (TX) power monitor can be used as a power detector, enabling highly accurate TX power measurements.

The fully integrated phase-locked loops (PLLs) provide low power fractional-N frequency synthesis for all receive and transmit channels. All VCO and loop filter components are integrated.

The core of the AD9365 can be powered directly from a 1.3 V regulator. The IC is controlled via a standard 4-wire serial port and three real-time I/O control pins. Comprehensive power-down modes are included to minimize power consumption in normal use. The AD9365 is packaged in a 10 mm × 10 mm, 144-ball chip scale package ball grid array (CSP_BGA).

Rev. Sp0
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REVISION HISTORY

1/12—Revision Sp0: Initial Version

SPECIFICATIONS

VDD_GPO = 3.3 V, VDD_INTERFACE = 1.8 V, all other VDDx pins = 1.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
RECEIVERS, GENERAL						
Center Frequency		200		2300	MHz	
Gain						
Minimum			0		dB	
Maximum			74.5		dB	At 800 MHz
			73.0		dB	At 2300 MHz, RX1A
			72.0		dB	At 2300 MHz, RX1B, RX1C
Gain Step			1		dB	
Received Signal Strength Indicator	RSSI					
Range			100		dB	
Accuracy			±2		dB	
RECEIVERS, 800 MHz						
Noise Figure	NF		2		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		−18		dBm	Maximum RX gain
Second-Order Input Intermodulation Intercept Point	IIP2		40		dBm	Maximum RX gain
Local Oscillator (LO) Leakage			−122		dBm	At RX front-end input
Quadrature Gain Error			0.2		%	
Quadrature Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			−34		dB	19.2 MHz reference clock
Input S11			−10		dB	
RECEIVERS, 2.3 GHz						
Noise Figure	NF		3		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		−14		dBm	Maximum RX gain
Second-Order Input Intermodulation Intercept Point	IIP2		45		dBm	Maximum RX gain
Local Oscillator (LO) Leakage			−110		dBm	At RX front-end input
Quadrature Gain Error			0.2		%	
Quadrature Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			−34		dB	40 MHz reference clock
Input S11			−10		dB	
TRANSMITTERS, GENERAL						
Center Frequency		650		2300	MHz	
Power Control Range			90		dB	
Power Control Resolution			0.25		dB	
TRANSMITTERS, 800 MHz						
Output S22			−10		dB	
Maximum Output Power			8		dBm	1 MHz tone into 50 Ω load
Modulation Accuracy (EVM)			−34		dB	19.2 MHz reference clock
Third-Order Output Intermodulation Intercept Point	OIP3		23		dBm	
Carrier Leakage			−50		dBc	0 dB attenuation
			−32		dBc	40 dB attenuation
Noise Floor			−157		dBm/Hz	90 MHz offset

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
TRANSMITTERS, 2.3 GHz						
Output S22			−10		dB	
Maximum Output Power			7.5		dBm	1 MHz tone into 50 Ω load
Modulation Accuracy (EVM)			−34		dB	40 MHz reference clock
Third-Order Output Intermodulation Intercept Point	OIP3		19		dBm	
Carrier Leakage			−50		dBc	0 dB attenuation
			−32		dBc	40 dB attenuation
Noise Floor			−156		dBm/Hz	90 MHz offset
TX MONITOR INPUT (TX_MON)						
Maximum Input Level			4		dBm	
Dynamic Range			66		dB	
Accuracy			1		dB	
LO SYNTHESIZER						
LO Frequency Step			1.2		Hz	2.3 GHz, 40 MHz reference clock
Integrated Phase Noise						100 Hz to 100 MHz
800 MHz			0.36		° rms	30.72 MHz reference clock (doubled internally for RF synthesizer)
2.3 GHz			0.37		° rms	40 MHz reference clock
REFERENCE CLOCK (REF_CLK)						REF_CLK is the input to the XTALN pin
Input Frequency Range		10		80	MHz	External oscillator
Input Signal Level			1.3		V p-p	AC-coupled external oscillator
AUXILIARY ADC						
Resolution			12		Bits	
Input Voltage						
Minimum			0.05		V	
Maximum			VDDA1P3_BB – 0.05		V	
AUXILIARY DAC						
Resolution			10		Bits	
Output Voltage						
Minimum			0.5		V	
Maximum			VDD_GPO – 0.3		V	
Output Current			10		mA	
DIGITAL SPECIFICATIONS (CMOS)						
Logic Inputs						
Input Voltage High		VDD_INTERFACE × 0.8		VDD_INTERFACE	V	
Input Voltage Low		0		VDD_INTERFACE × 0.2	V	
Input Current High		−10		+10	µA	
Input Current Low		−10		+10	µA	
Logic Outputs						
Output Voltage High		VDD_INTERFACE × 0.8			V	
Output Voltage Low				VDD_INTERFACE × 0.2	V	
GENERAL-PURPOSE OUTPUTS						
Output Voltage High		VDD_GPO × 0.8			V	
Output Voltage Low				VDD_GPO × 0.2	V	
Output Current			10		mA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
SPI TIMING						VDD_INTERFACE = 1.8 V
SPI_CLK						
Period	t_{CP}	20			ns	
Pulse Width	t_{MP}	9			ns	
SPI_ENB Setup to First SPI_CLK Rising Edge	t_{SC}	1			ns	
Last SPI_CLK Falling Edge to SPI_ENB Hold	t_{HC}	0			ns	
SPI_DI						
Data Input Setup to SPI_CLK	t_S	2			ns	
Data Input Hold to SPI_CLK	t_H	1			ns	
SPI_CLK Rising Edge to Output Data Delay						
4-Wire Mode	t_{CO}	3		8	ns	
3-Wire Mode	t_{CO}	3		8	ns	
Bus Turnaround Time, Read	t_{HZM}	t_H		t_{CO} (max)	ns	After BBP drives the last address bit
	t_{HZS}	0		t_{CO} (max)	ns	After AD9365 drives the last data bit
DIGITAL DATA TIMING (CMOS), VDD_INTERFACE = 1.8 V						
DATA_CLK Clock Period	t_{CP}	16.276			ns	61.44 MHz
DATA_CLK and FB_CLK Pulse Width	t_{MP}	45% of t_{CP}		55% of t_{CP}	ns	
TX Data						TX_FRAME, P0_D, and P1_D
Setup to FB_CLK	t_{STX}	1			ns	
Hold to FB_CLK	t_{HTX}	0			ns	
DATA_CLK to Data Bus Output Delay	t_{DDRX}	0		1.5	ns	
DATA_CLK to RX_FRAME Delay	t_{DDDV}	0		1.0	ns	
ENABLE Pulse Width	t_{ENPW}	t_{CP}			ns	
TXNRX Pulse Width	$t_{TXNRXPW}$	t_{CP}			ns	FDD independent ENSM mode
TXNRX Setup to ENABLE	$t_{TXNRXSU}$	0			ns	TDD ENSM mode
Bus Turnaround Time						TDD mode
Before RX	t_{RPRE}	$2 \times t_{CP}$			ns	
After RX	t_{RPST}	$2 \times t_{CP}$			ns	
Capacitive Load			3		pF	
Capacitive Input			3		pF	
DIGITAL DATA TIMING (CMOS), VDD_INTERFACE = 2.5 V						
DATA_CLK Clock Period	t_{CP}	16.276			ns	61.44 MHz
DATA_CLK and FB_CLK Pulse Width	t_{MP}	45% of t_{CP}		55% of t_{CP}	ns	
TX Data						TX_FRAME, P0_D, and P1_D
Setup to FB_CLK	t_{STX}	1			ns	
Hold to FB_CLK	t_{HTX}	0			ns	
DATA_CLK to Data Bus Output Delay	t_{DDRX}	0		1.2	ns	
DATA_CLK to RX_FRAME Delay	t_{DDDV}	0		1.0	ns	
ENABLE Pulse Width	t_{ENPW}	t_{CP}			ns	
TXNRX Pulse Width	$t_{TXNRXPW}$	t_{CP}			ns	FDD independent ENSM mode
TXNRX Setup to ENABLE	$t_{TXNRXSU}$	0			ns	TDD ENSM mode

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
Bus Turnaround Time						TDD mode
Before RX	t_{RPRE}	$2 \times t_{CP}$			ns	
After RX	t_{RPST}	$2 \times t_{CP}$			ns	
Capacitive Load			3		pF	
Capacitive Input			3		pF	
SUPPLY CHARACTERISTICS						
1.3 V Main Supply		1.267	1.3	1.33	V	
VDD_INTERFACE Supply		1.2		2.5	V	
VDD_GPO Supply		1.3	3.3		V	When unused, must be set to 1.3 V

CURRENT CONSUMPTION SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
VDD_GPO		50		µA	No load
VDD_INTERFACE					
VDD_INTERFACE = 1.2 V					
Sleep Mode		45		µA	Power applied, device disabled
10 MHz BW, Single Port, DDR		2.9		mA	30.72 MHz data clock
10 MHz BW, Dual Port, DDR		2.7		mA	15.36 MHz data clock
VDD_INTERFACE = 1.8 V					
Sleep Mode		84		µA	Power applied, device disabled
10 MHz BW, Single Port, DDR		4.5		mA	30.72 MHz data clock
10 MHz BW, Dual Port, DDR		4.1		mA	15.36 MHz data clock
VDD_INTERFACE = 2.5 V					
Sleep Mode		150		µA	Power applied, device disabled
10 MHz BW, Single Port, DDR		6.5		mA	30.72 MHz data clock
10 MHz BW, Dual Port, DDR		6.0		mA	15.36 MHz data clock
VDDD1P3_DIG AND VDDAx (ALL OTHER SUPPLIES)					Combination of all 1.3 V supply current
Sleep Mode		180		µA	Power applied, device disabled
TDD Mode, 800 MHz, RX					
5 MHz BW		180		mA	Continuous RX
10 MHz BW		210		mA	Continuous RX
TDD Mode, 800 MHz, TX					
5 MHz BW					
7 dBm		340		mA	Continuous TX
−27 dBm		190		mA	Continuous TX
10 MHz BW					
7 dBm		360		mA	Continuous TX
−27 dBm		220		mA	Continuous TX
TDD Mode, 2300 MHz, RX					
5 MHz BW		175		mA	Continuous RX
10 MHz BW		200		mA	Continuous RX
TDD Mode, 2300 MHz, TX					
5 MHz BW					
7 dBm		350		mA	Continuous TX
−27 dBm		160		mA	Continuous TX
10 MHz BW					
7 dBm		380		mA	Continuous TX
−27 dBm		220		mA	Continuous TX
FDD Mode, 800 MHz					
5 MHz BW					
7 dBm		490		mA	
−27 dBm		345		mA	
10 MHz BW					
7 dBm		540		mA	
−27 dBm		395		mA	
FDD Mode, 2300 MHz					
5 MHz BW					
7 dBm		500		mA	
−27 dBm		350		mA	
10 MHz BW					
7 dBm		540		mA	
−27 dBm		390		mA	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDDx to VSSx	−0.3 V to +1.4 V
VDD_INTERFACE to VSSx	−0.3 V to +3.0 V
VDD_GPO to VSSx	−0.3 V to +3.9 V
Logic Inputs and Outputs to VSSx	−0.3 V to VDD_INTERFACE
Input Current to Any Pin Except Supplies	±10 mA
RF Inputs (Peak Power)	2.5 dBm
TX Monitor Input Power (Peak Power)	9 dBm
Package Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Maximum Junction Temperature (T_{JMAX})	110°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

REFLOW PROFILE

The AD9365 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
144-Ball CSP_BGA	0	32.3	9.6	20.2	0.27	°C/W
	1.0	29.6			0.43	°C/W
	2.5	27.8			0.57	°C/W

[1] Per JEDEC JESD51-7, plus JEDEC JESD51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSSA	VSSA	NC	VSSA	TX_MON	VSSA	VDDA1P3_ RX_TX	VDDA1P3_ RX_TX	VDDA1P3_ RX_TX	VDDA1P3_ RX_TX	VDDA1P1_ TX_VCO	VSSA
B	VSSA	VSSA	AUXDAC1	GPO_3	GPO_2	GPO_1	GPO_0	VDD_GPO	VDDA1P3_ TX_LO	VDDA1P3_ TX_VCO_ LDO	TX_VCO_ LDO_OUT	VSSA
C	VSSA	VSSA	AUXDAC2	TEST/ ENABLE	CTRL_IN0	CTRL_IN1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
D	VSSA	VDDA1P3_ RX_RF	VDDA1P3_ RX_TX	NC	VSSA	CTRL_IN2	P0_D9	P0_D7	P0_D5	P0_D3	P0_D1	VSSD
E	VSSA	VDDA1P3_ RX_LO	VDDA1P3_ TX_LO_ BUFFER	NC	NC	NC	P0_D11	P0_D8	P0_D6	P0_D4	P0_D2	P0_D0
F	VSSA	VDDA1P3_ RX_VCO_ LDO	VSSA	CTRL_OUT2	CTRL_OUT1	CTRL_OUT0	VSSD	P0_D10	VSSD	FB_CLK	VSSD	VDDD1P3_ DIG
G	VSSA	RX_VCO_ LDO_OUT	VDDA1P1_ RX_VCO	NC	EN_AGC	ENABLE	VSSA	RX_ FRAME	TX_ FRAME	VSSA	DATA_ CLK	VSSD
H	RX1B_P	VSSA	VSSA	TXNRX	SYNC_IN	VSSA	VSSD	P1_D11	VSSA	VSSD	VSSA	VDD_ INTERFACE
J	RX1B_N	VSSA	VDDA1P3_ RX_SYNTH	SPI_DI	SPI_CLK	CLK_OUT	P1_D10	P1_D9	P1_D7	P1_D5	P1_D3	P1_D1
K	RX1C_P	VSSA	VDDA1P3_ TX_SYNTH	VDDA1P3_ BB	RESETB	SPI_ENB	P1_D8	P1_D6	P1_D4	P1_D2	P1_D0	VSSD
L	RX1C_N	VSSA	VSSA	RBIAS	AUXADC	SPI_DO	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
M	RX1A_P	RX1A_N	NC	VSSA	VSSA	VSSA	TX1A_P	TX1A_N	TX1B_P	TX1B_N	NC	XTALN

ANALOG I/O
DIGITAL I/O
NO CONNECT
DC POWER
GROUND

10492-002

Figure 2. Pin Configuration, Top View

Table 5. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic	Description
A5	I	TX_MON	Transmit Channel Power Monitor Input. If this pin is unused, tie it to ground.
A7, A8, A9, A10, D3	I	VDDA1P3_RX_TX	1.3 V Supply Input.
A11	I	VDDA1P1_TX_VCO	Transmit VCO Supply Input. Connect to B11.
B3	O	AUXDAC1	Auxiliary DAC 1 Output.
B4, B5, B6, B7	O	GPO_3 to GPO_0	3.3 V Capable General-Purpose Outputs.
B8	I	VDD_GPO	2.5 V to 3.3 V Supply Input for the AUXDAC and General-Purpose Output Pins. When the VDD_GPO supply is not used, this supply must be set to 1.3 V.
B9	I	VDDA1P3_TX_LO	Transmit LO 1.3 V Supply Input.
B10	I	VDDA1P3_TX_VCO_LDO	Transmit VCO LDO 1.3 V Supply Input. Connect to B9.
B11	O	TX_VCO_LDO_OUT	Transmit VCO LDO Output. Connect to A11 and to a 1 µF bypass capacitor in series with a 1 Ω resistor to ground.
C3	O	AUXDAC2	Auxiliary DAC 2 Output.
C4	I	TEST/ENABLE	Test Input. Ground this pin for normal operation.
C5, C6, D6	I	CTRL_IN0 to CTRL_IN2	Control Inputs. Used for manual RX gain and TX attenuation control.
D2	I	VDDA1P3_RX_RF	Receiver 1.3 V Supply Input. Connect to D3.
D7	I/O	P0_D9	Digital Data Port P0_D9. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
D8	I/O	P0_D7	Digital Data Port P0_D7. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
D9	I/O	P0_D5	Digital Data Port P0_D5. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
D10	I/O	P0_D3	Digital Data Port P0_D3. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
D11	I/O	P0_D1	Digital Data Port P0_D1. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
E2	I	VDDA1P3_RX_LO	Receive LO 1.3 V Supply Input.
E3	I	VDDA1P3_TX_LO_BUFFER	1.3 V Supply Input.
E7	I/O	P0_D11	Digital Data Port P0_D11. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
E8	I/O	P0_D8	Digital Data Port P0_D8. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.

Pin No.	Type[1]	Mnemonic	Description
E9	I/O	P0_D6	Digital Data Port P0_D6. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
E10	I/O	P0_D4	Digital Data Port P0_D4. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
E11	I/O	P0_D2	Digital Data Port P0_D2. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
E12	I/O	P0_D0	Digital Data Port P0_D0. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
F2	I	VDDA1P3_RX_VCO_LDO	Receive VCO LDO 1.3 V Supply Input. Connect to E2.
F4, F5, F6	O	CTRL_OUT2 to CTRL_OUT0	Control Outputs. These pins are multipurpose outputs that have programmable functionality.
F8	I/O	P0_D10	Digital Data Port P0_D10. Part of the 12-bit bidirectional parallel CMOS level Data Port 0.
F10	I	FB_CLK	Feedback Clock. This pin receives the FB_CLK signal that clocks in TX data.
F12	I	VDDD1P3_DIG	1.3 V Digital Supply Input.
G2	O	RX_VCO_LDO_OUT	Receive VCO LDO Output. Connect to G3 and to a 1 µF bypass capacitor in series with a 1 Ω resistor to ground.
G3	I	VDDA1P1_RX_VCO	Receive VCO Supply Input. Connect to G2.
G5	I	EN_AGC	Manual Control Input for Automatic Gain Control (AGC).
G6	I	ENABLE	Control Input. This pin moves the device through various operational states.
G8	O	RX_FRAME	Receive Digital Data Framing Output Signal. This pin transmits the RX_FRAME signal that indicates when the RX output data is valid.
G9	I	TX_FRAME	Transmit Digital Data Framing Input Signal. This pin receives the TX_FRAME signal that indicates when the TX data is valid.
G11	O	DATA_CLK	Receive Data Clock Output. This pin transmits the DATA_CLK signal that is used by the BBP to clock RX data.
H1, J1	I	RX1B_P, RX1B_N	Receive Channel 1 Differential Input B. Alternatively, each pin can be used as a single-ended input. Unused pins must be tied to ground.
H4	I	TXNRX	Enable State Machine Control Signal. This pin controls the data port bus direction. Logic low selects the RX direction; logic high selects the TX direction.
H5	I	SYNC_IN	Input to Synchronize Digital Clocks Between Multiple AD9365 Devices. If this pin is unused, leave it unconnected.
H8	I/O	P1_D11	Digital Data Port P1_D11. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
H12	I	VDD_INTERFACE	1.2 V to 2.5 V Supply Input for Digital I/O Pins.
J3	I	VDDA1P3_RX_SYNTH	1.3 V Supply Input.
J4	I	SPI_DI	SPI Serial Data Input.
J5	I	SPI_CLK	SPI Clock Input.
J6	O	CLK_OUT	Clock Output. This pin can be configured as either a buffered version of the external input clock or a divided-down version of the internal ADC_CLK.
J7	I/O	P1_D10	Digital Data Port P1_D10. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
J8	I/O	P1_D9	Digital Data Port P1_D9. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
J9	I/O	P1_D7	Digital Data Port P1_D7. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
J10	I/O	P1_D5	Digital Data Port P1_D5. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
J11	I/O	P1_D3	Digital Data Port P1_D3. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
J12	I/O	P1_D1	Digital Data Port P1_D1. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
K1, L1	I	RX1C_P, RX1C_N	Receive Channel 1 Differential Input C. Alternatively, each pin can be used as a single-ended input. Unused pins must be tied to ground.
K3	I	VDDA1P3_TX_SYNTH	1.3 V Supply Input.
K4	I	VDDA1P3_BB	1.3 V Supply Input.
K5	I	RESETB	Asynchronous Reset Input. Logic low resets the device.
K6	I	SPI_ENB	SPI Enable Input. Set this pin to logic low to enable the SPI bus.
K7	I/O	P1_D8	Digital Data Port P1_D8. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
K8	I/O	P1_D6	Digital Data Port P1_D6. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
K9	I/O	P1_D4	Digital Data Port P1_D4. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
K10	I/O	P1_D2	Digital Data Port P1_D2. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
K11	I/O	P1_D0	Digital Data Port P1_D0. Part of the 12-bit bidirectional parallel CMOS level Data Port 1.
L4	I	RBIAS	Bias Input Reference. Connect this pin through a 14.3 kΩ (1% tolerance) resistor to ground.
L5	I	AUXADC	Auxiliary ADC Input. If this pin is unused, tie it to ground.
L6	O	SPI_DO	SPI Serial Data Output in 4-Wire Mode, High-Z in 3-Wire Mode.

Pin No.	Type[1]	Mnemonic	Description
M1, M2	I	RX1A_P, RX1A_N	Receive Channel 1 Differential Input A. Alternatively, each pin can be used as a single-ended input. Unused pins must be tied to ground.
M7, M8	O	TX1A_P, TX1A_N	Transmit Channel 1 Differential Output A. Unused pins must be tied to 1.3 V.
M9, M10	O	TX1B_P, TX1B_N	Transmit Channel 1 Differential Output B. Unused pins must be tied to 1.3 V.
M12	I	XTALN	External Clock Input. Connect the clock source to this pin.
D12, F7, F9, F11, G12, H7, H10, K12	I	VSSD	Digital Ground. Tie these pins directly to the VSSA analog ground on the PCB (one ground plane).
A1, A2, A4, A6, A12, B1, B2, B12, C1, C2, C7, C8, C9, C10, C11, C12, D1, D5, E1, F1, F3, G1, G7, G10, H2, H3, H6, H9, H11, J2, K2, L2, L3, L7, L8, L9, L10, L11, L12, M4, M5, M6	I	VSSA	Analog Ground. Tie these pins directly to the VSSD digital ground on the PCB (one ground plane).
A3, D4, E4, E5, E6, G4, M3, M11	NC	NC	No Connect. Do not connect to these pins.

[1] I is input, O is output, I/O is input/output, NC is not connected.

TYPICAL PERFORMANCE CHARACTERISTICS

800 MHZ FREQUENCY BAND

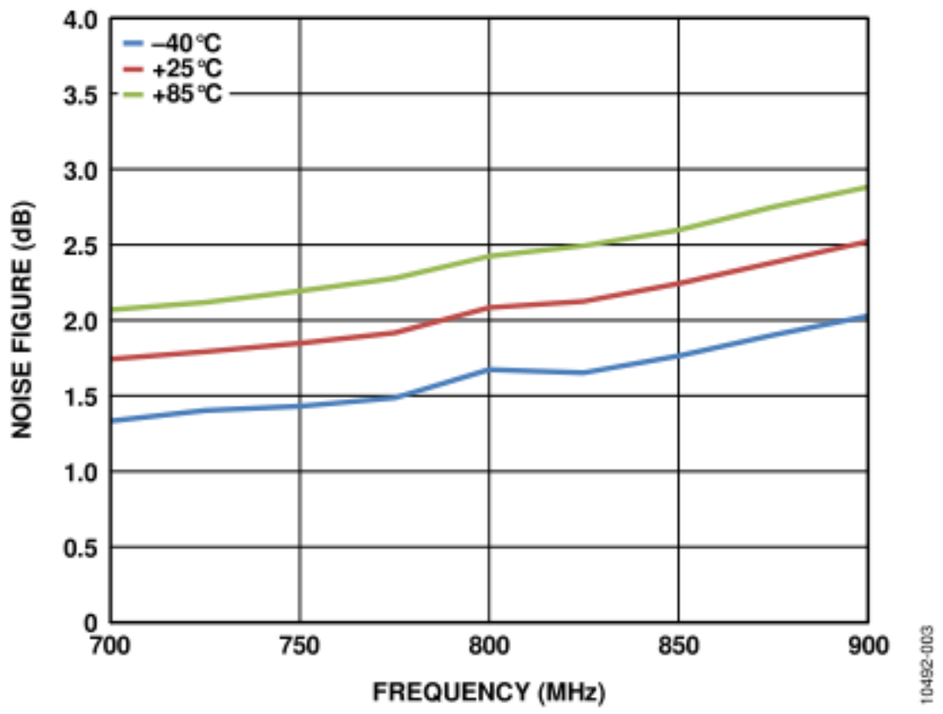


Figure 3. RX Noise Figure vs. RF Frequency

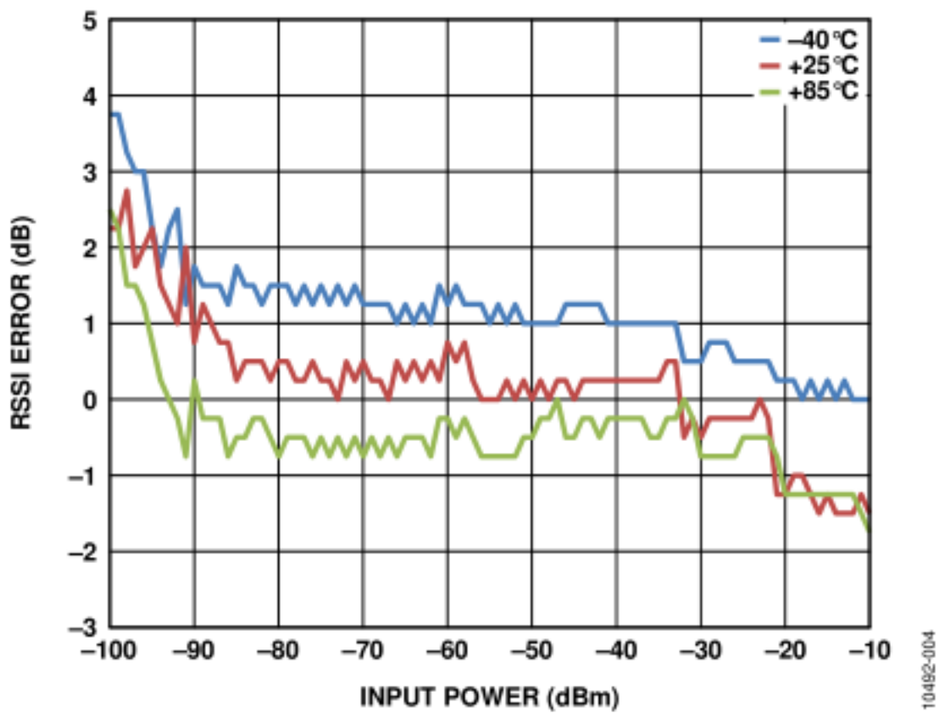


Figure 4. RSSI Error vs. Input Power, LTE 10 MHz Modulation (Referenced to −50 dBm Input Power at 800 MHz)

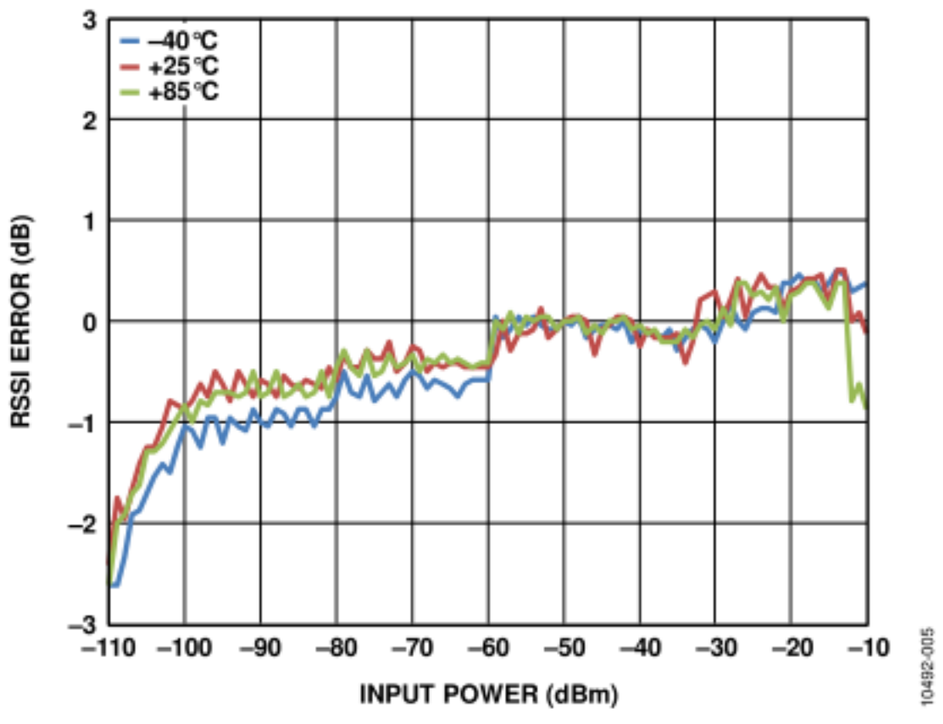


Figure 5. RSSI Error vs. Input Power, EDGE Modulation (Referenced to −50 dBm Input Power at 800 MHz)

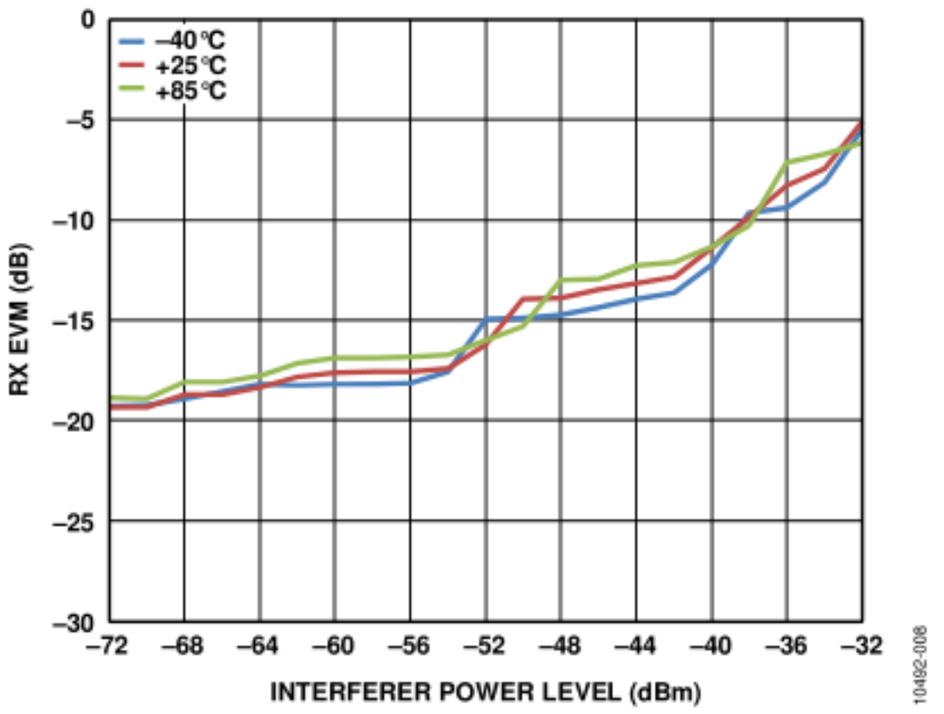


Figure 6. RX EVM vs. Interferer Power, LTE 10 MHz Signal of Interest with P_{IN} = −82 dBm, 5 MHz OFDM Blocker at 7.5 MHz Offset

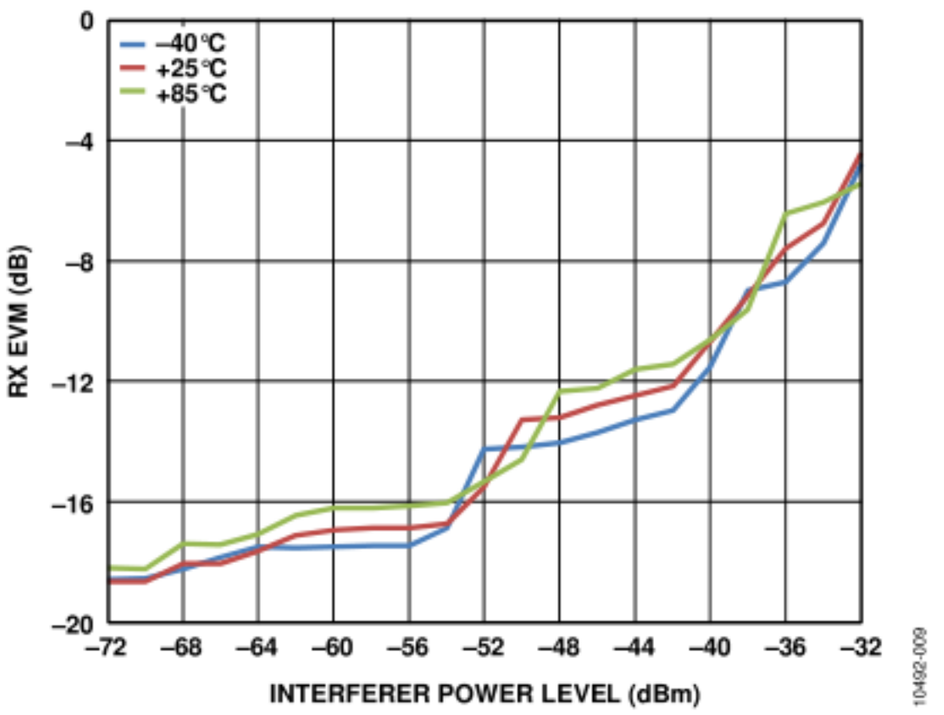


Figure 7. RX EVM vs. Interferer Power, LTE 10 MHz Signal of Interest with P_{IN} = −90 dBm, 5 MHz OFDM Blocker at 17.5 MHz Offset

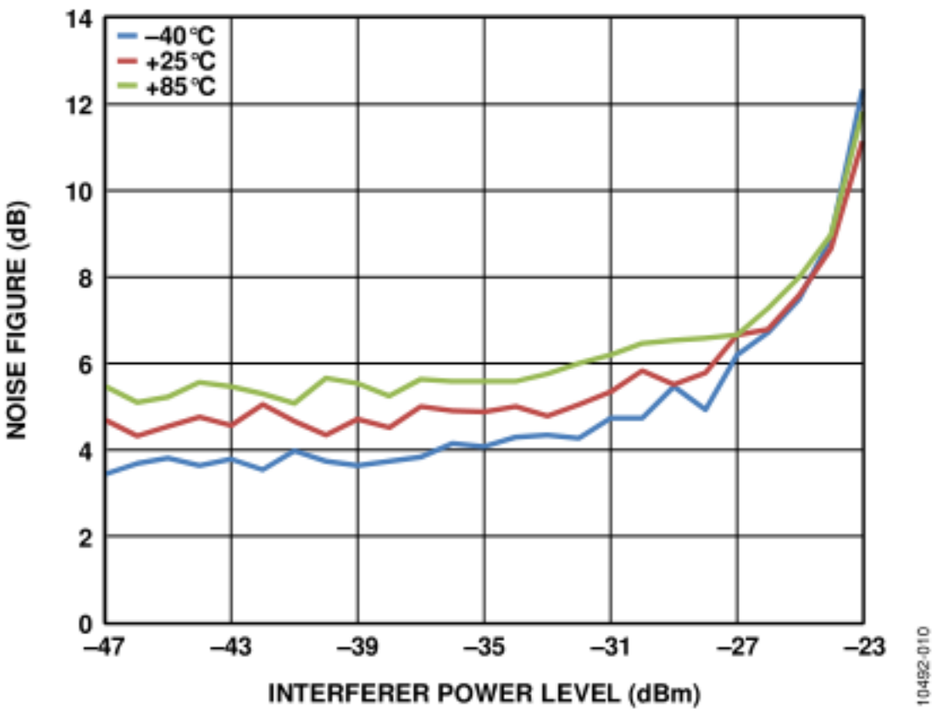


Figure 8. RX Noise Figure vs. Interferer Power, EDGE Signal of Interest with P_{IN} = −90 dBm, CW Blocker at 3 MHz Offset, Gain Index = 64

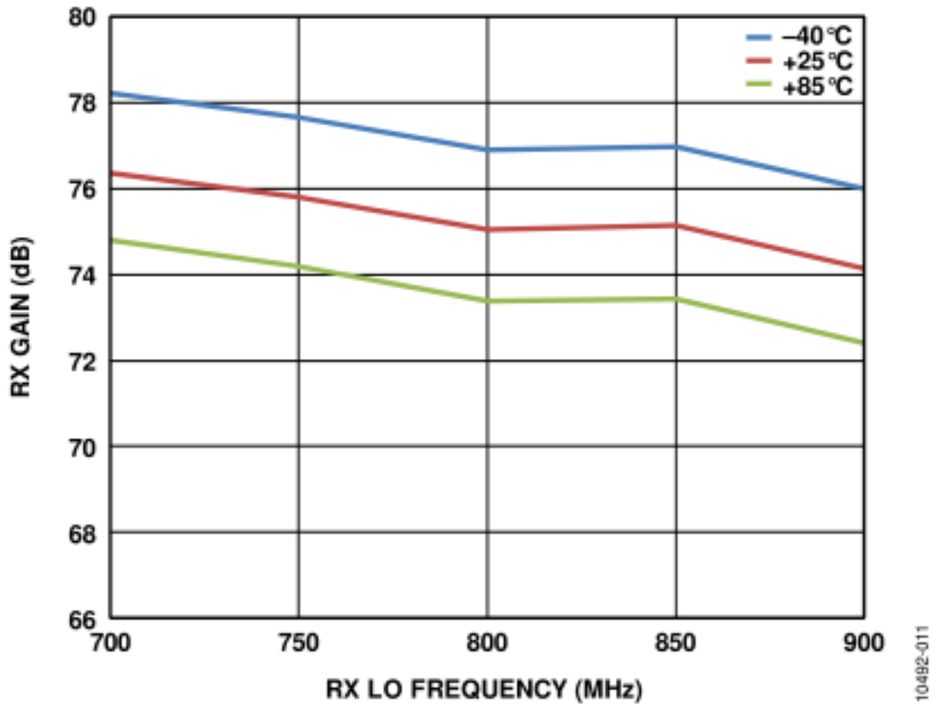


Figure 9. RX Gain vs. Frequency, Gain Index = 76 (Maximum Setting)

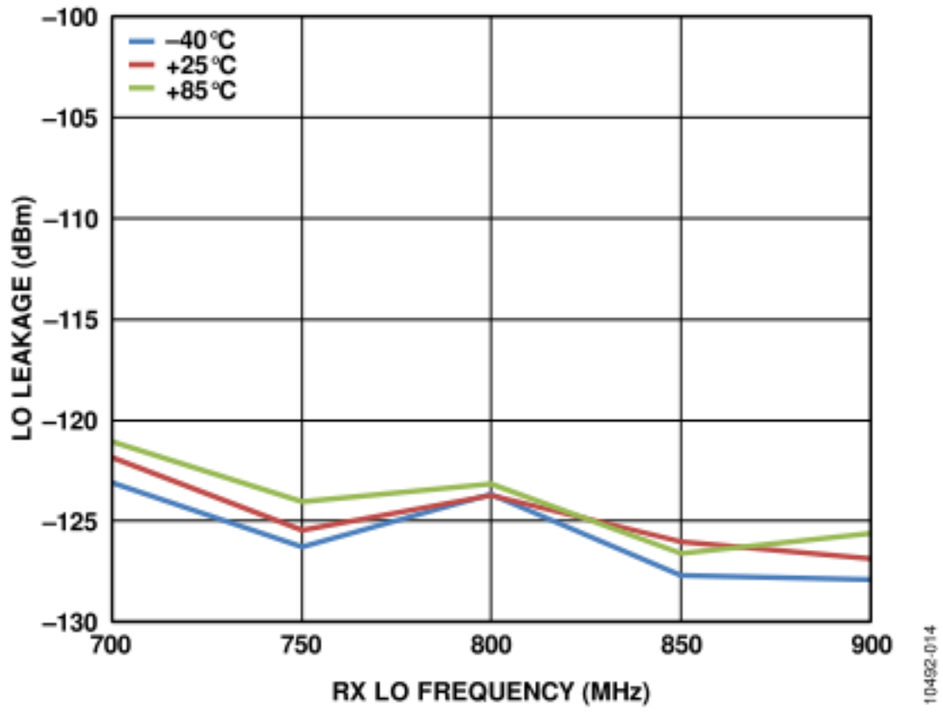


Figure 12. RX Local Oscillator (LO) Leakage vs. Frequency

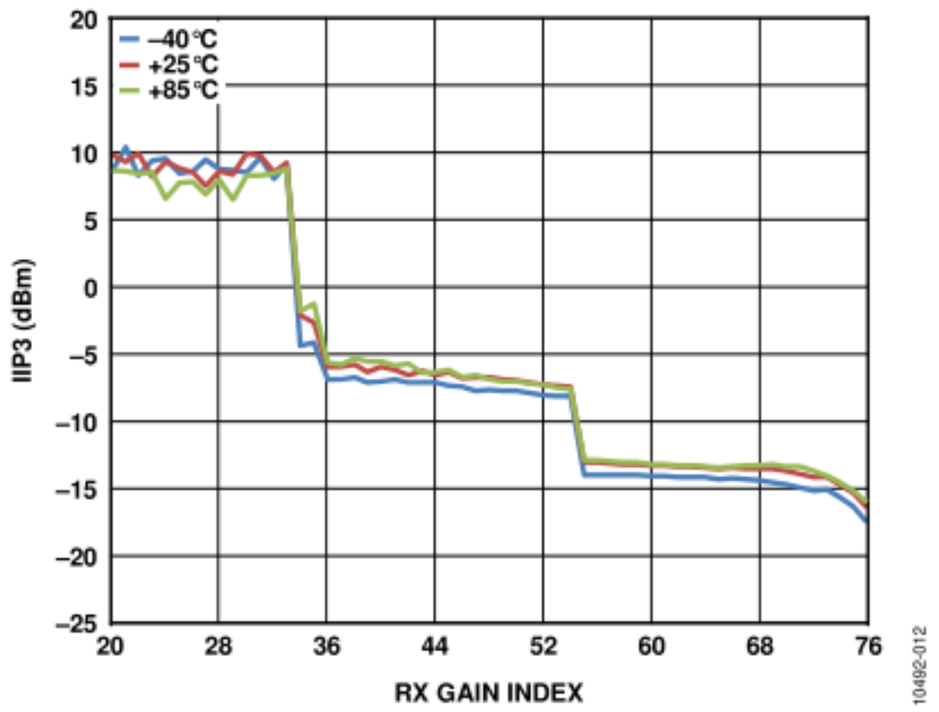


Figure 10. Third-Order Input Intercept Point (IIP3) vs. RX Gain Index, f1 = 1.45 MHz, f2 = 2.89 MHz, GSM Mode

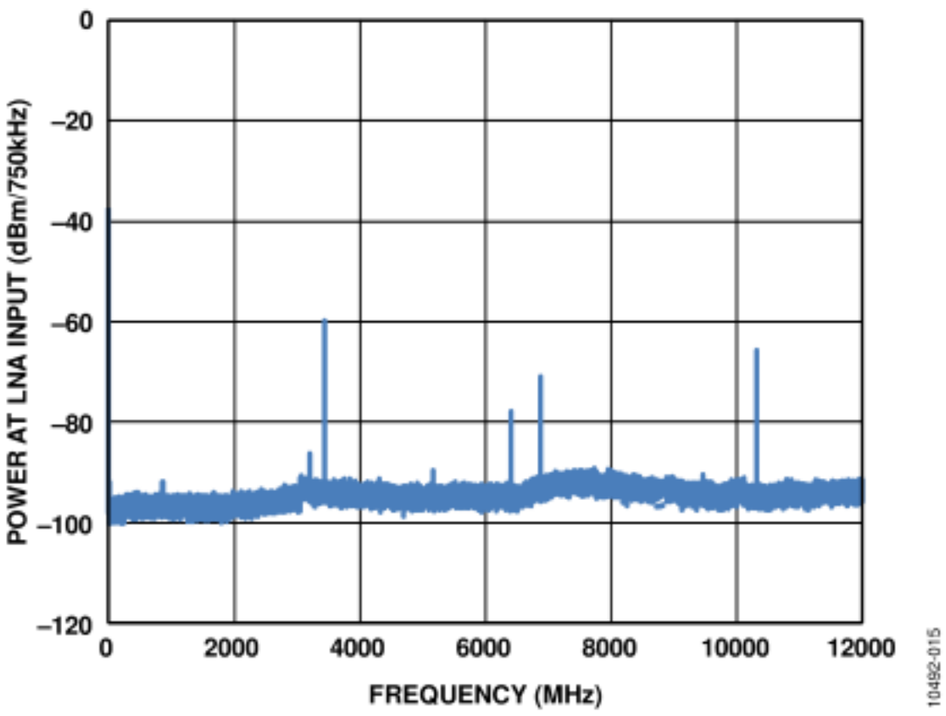


Figure 13. RX Emission at LNA Input, DC to 12 GHz, f_{LO_RX} = 800 MHz, LTE 10 MHz, f_{LO_TX} = 860 MHz

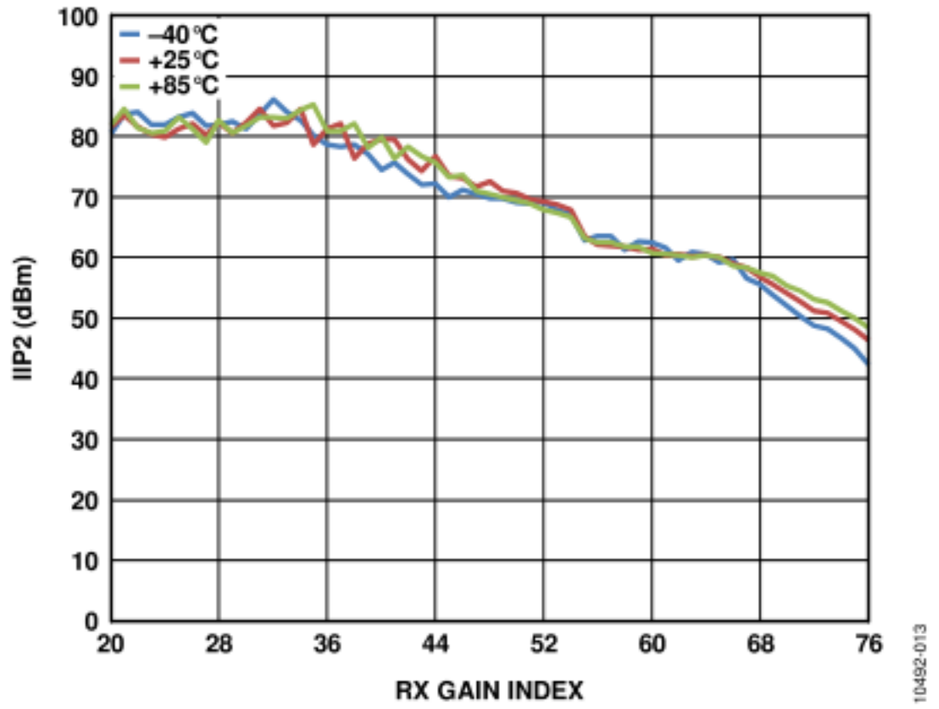


Figure 11. Second-Order Input Intercept Point (IIP2) vs. RX Gain Index, f1 = 2.00 MHz, f2 = 2.01 MHz, GSM Mode

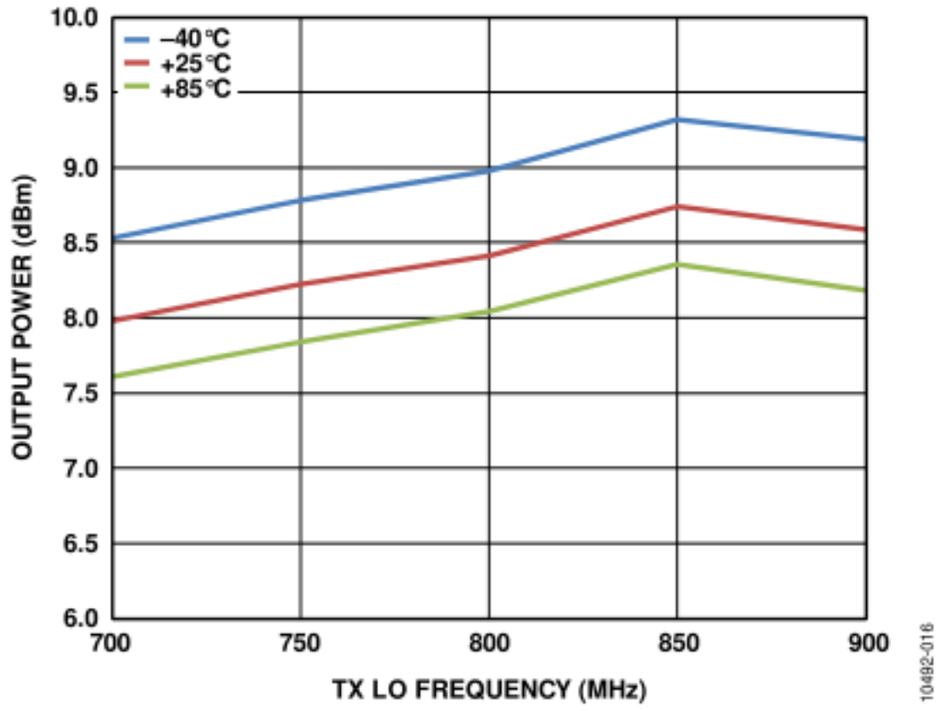


Figure 14. TX Output Power vs. Frequency, Attenuation Setting = 0 dB, Single Tone Output

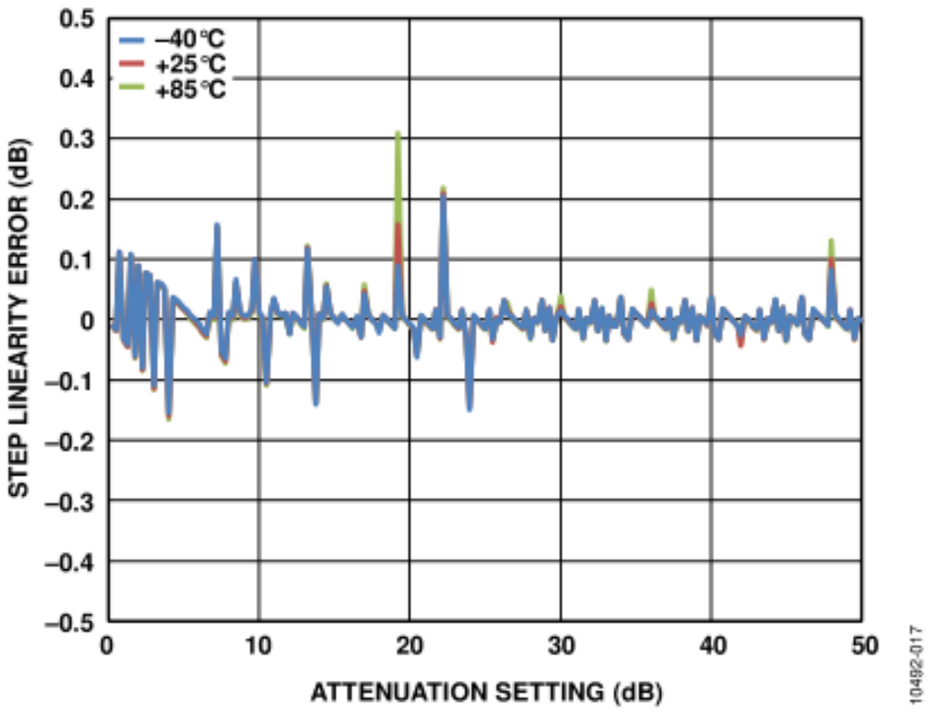


Figure 15. TX Power Control Linearity Error vs. Attenuation Setting

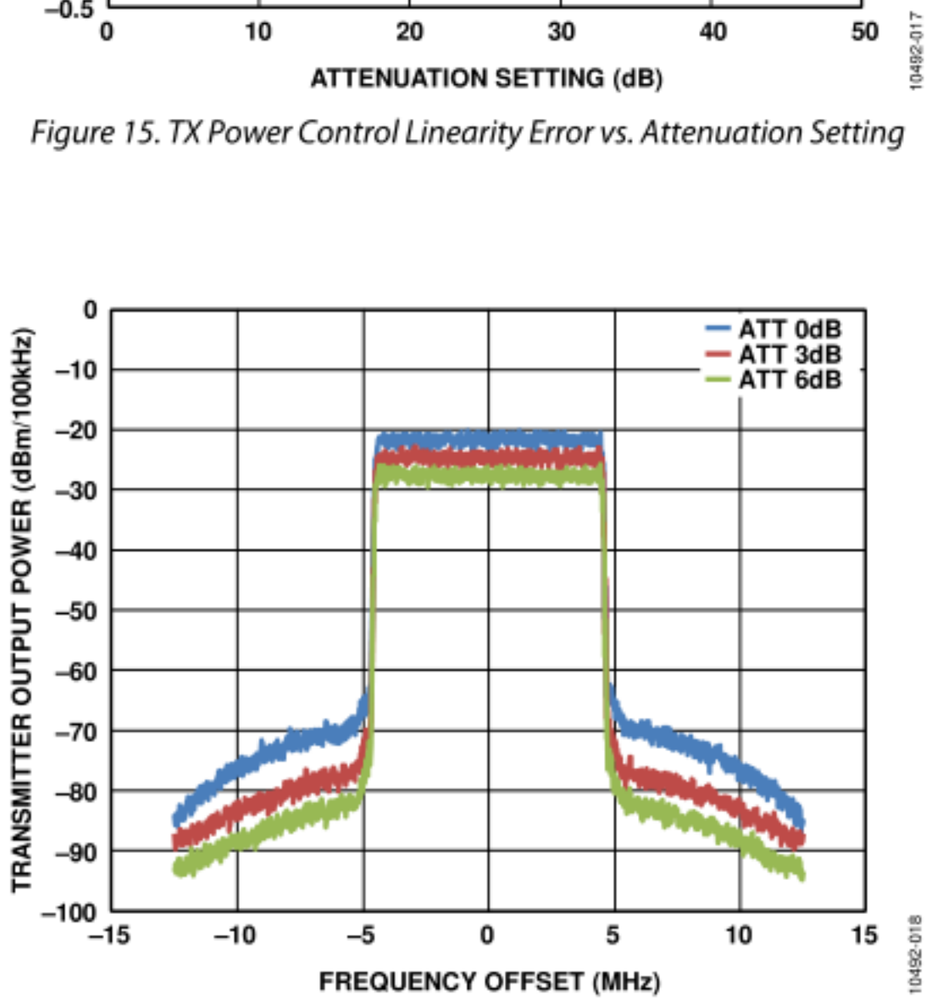


Figure 16. TX Spectrum vs. Frequency Offset from Carrier Frequency, f_{LO_TX} = 800 MHz, LTE 10 MHz Downlink (Digital Attenuation Variations Shown)

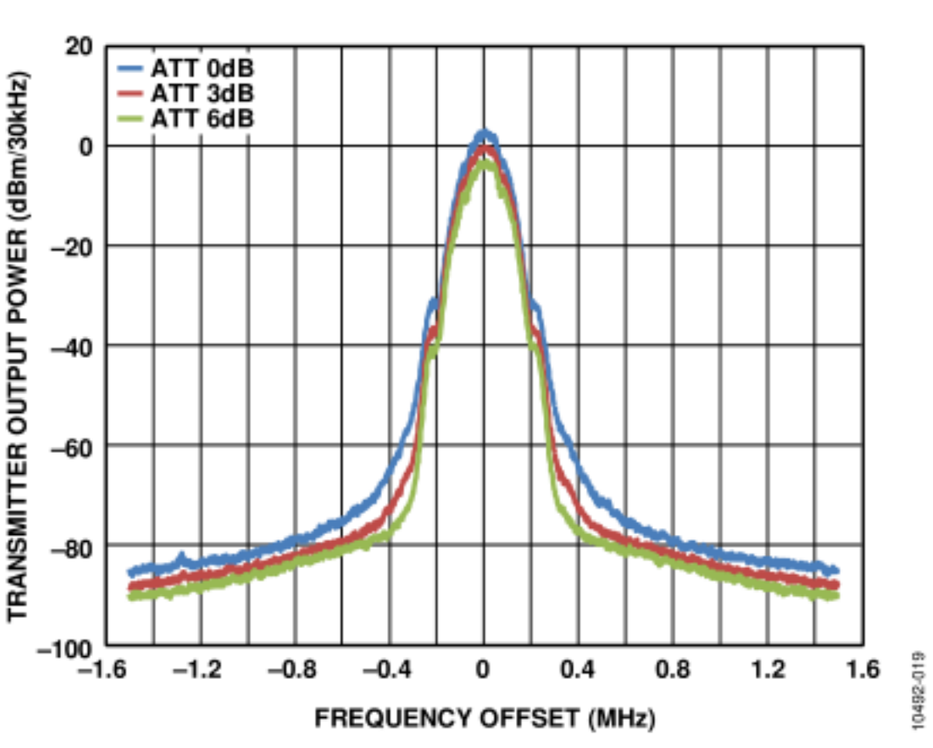


Figure 17. TX Spectrum vs. Frequency Offset from Carrier Frequency, f_{LO_TX} = 800 MHz, GSM Downlink (Digital Attenuation Variations Shown), 3 MHz Range

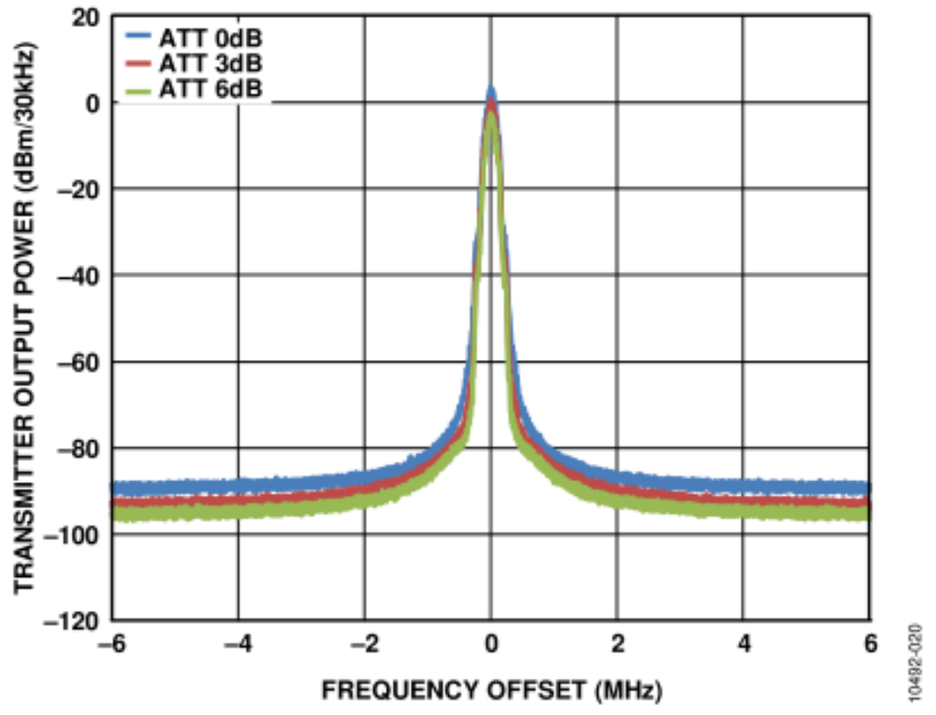


Figure 18. TX Spectrum vs. Frequency Offset from Carrier Frequency, f_{LO_TX} = 800 MHz, GSM Downlink (Digital Attenuation Variations Shown), 12 MHz Range

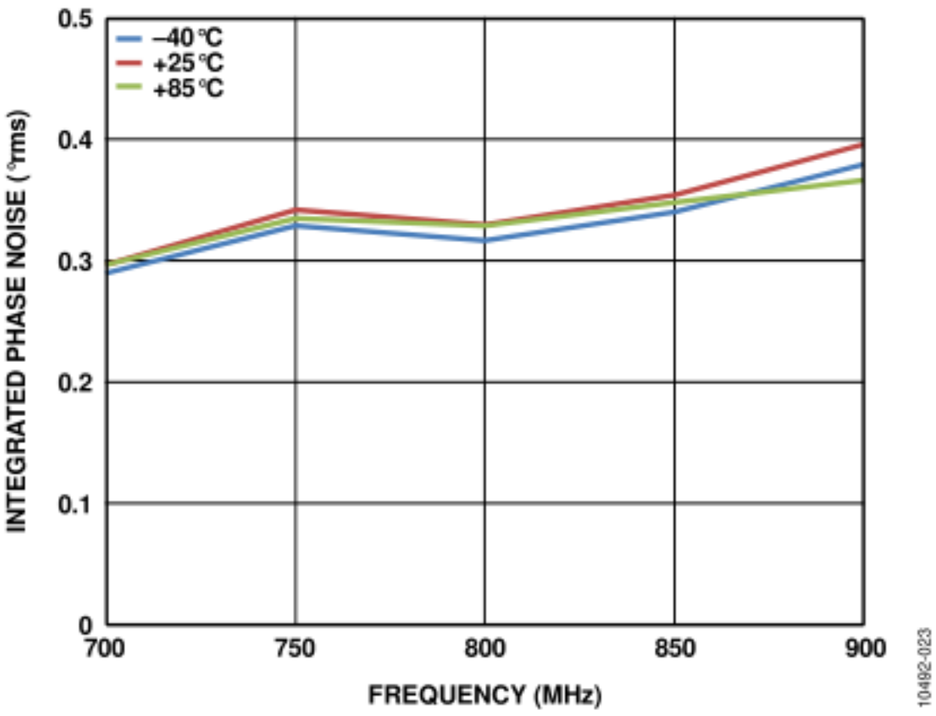


Figure 19. Integrated TX LO Phase Noise vs. Frequency, 19.2 MHz REF_CLK

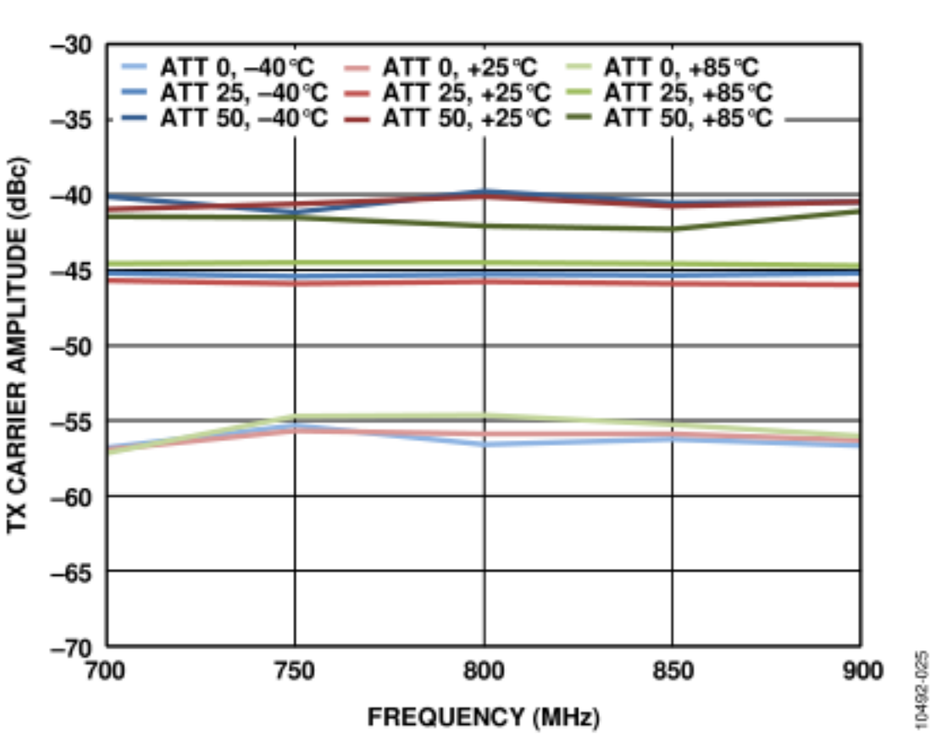


Figure 20. TX Carrier Rejection vs. Frequency

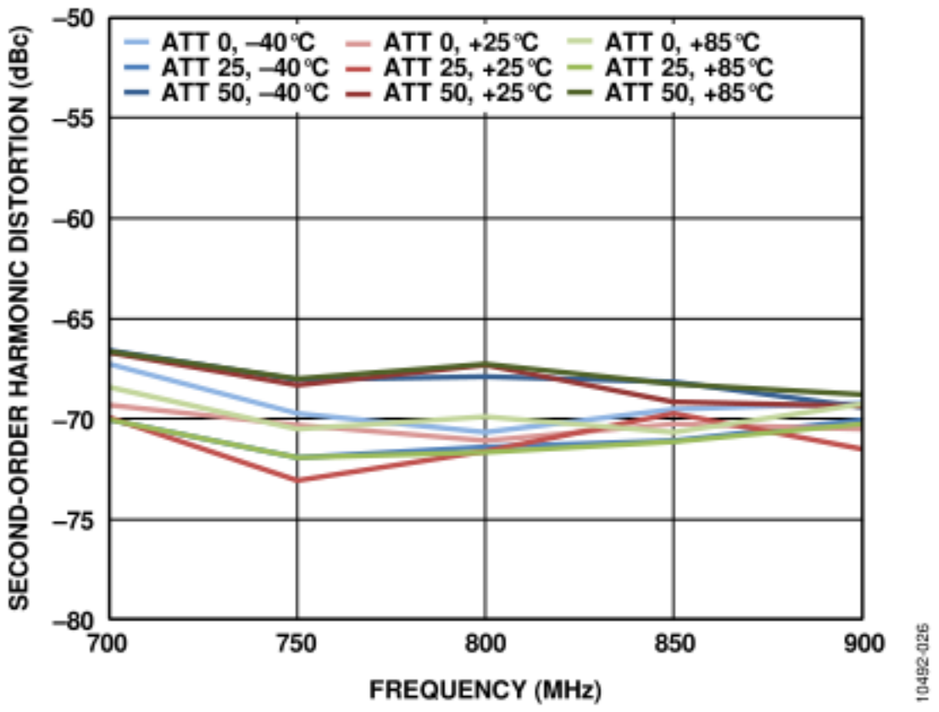


Figure 21. TX Second-Order Harmonic Distortion (HD2) vs. Frequency

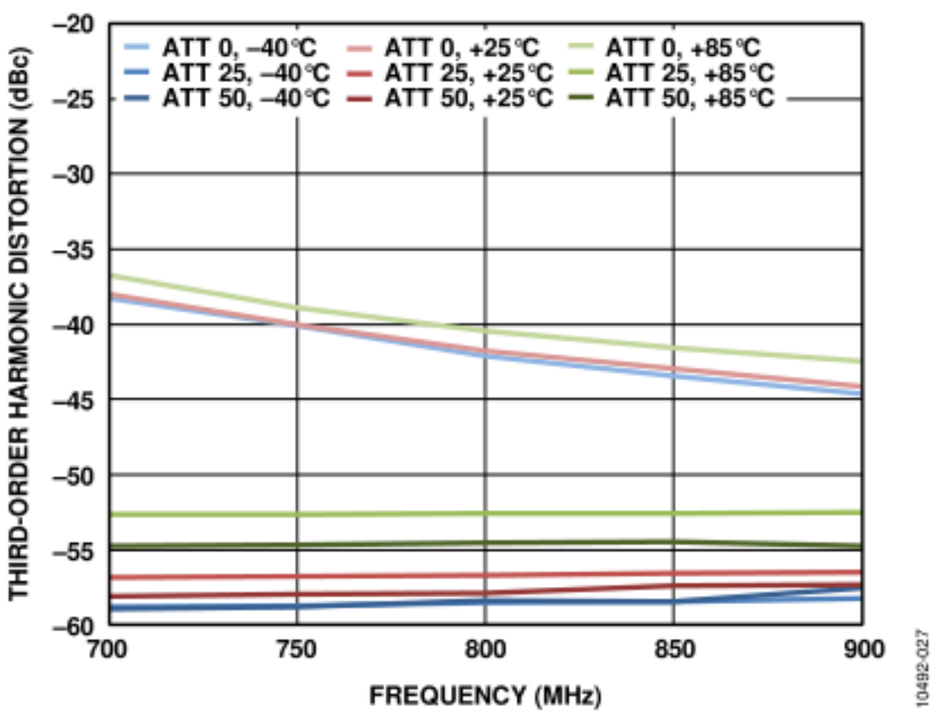


Figure 22. TX Third-Order Harmonic Distortion (HD3) vs. Frequency

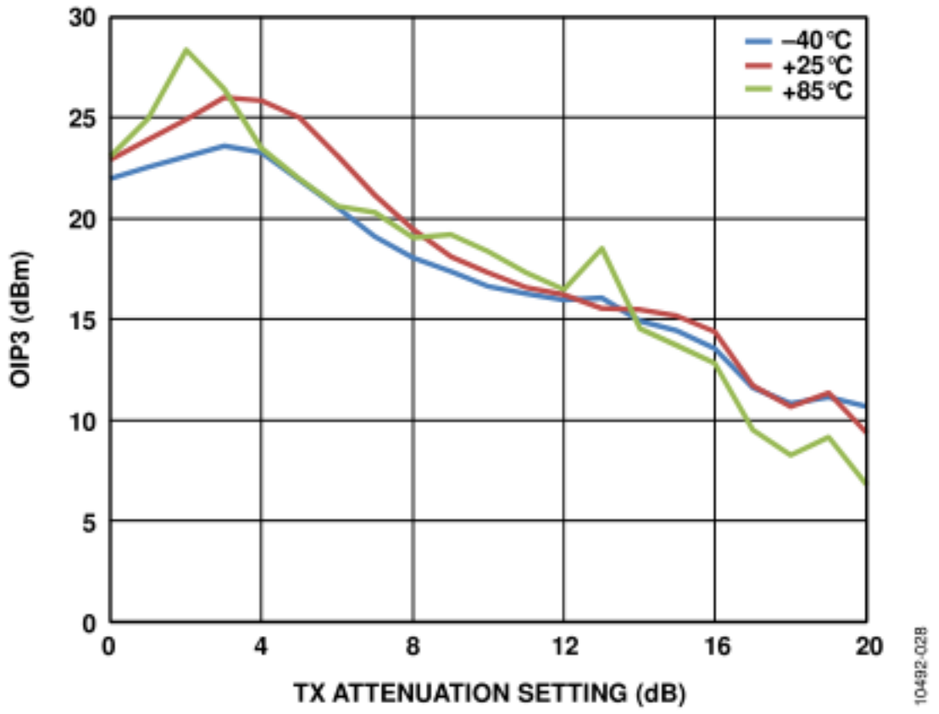


Figure 23. TX Third-Order Output Intercept Point (OIP3) vs. Attenuation Setting

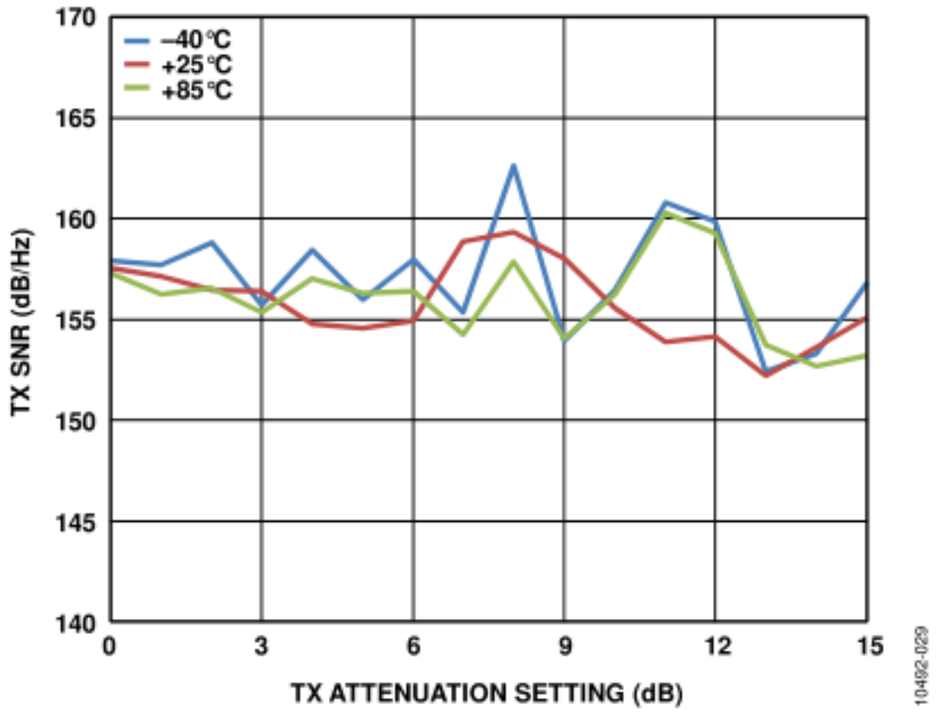


Figure 24. TX Signal-to-Noise Ratio (SNR) vs. Attenuation Setting, LTE 10 MHz Signal of Interest with Noise Measured at 90 MHz Offset

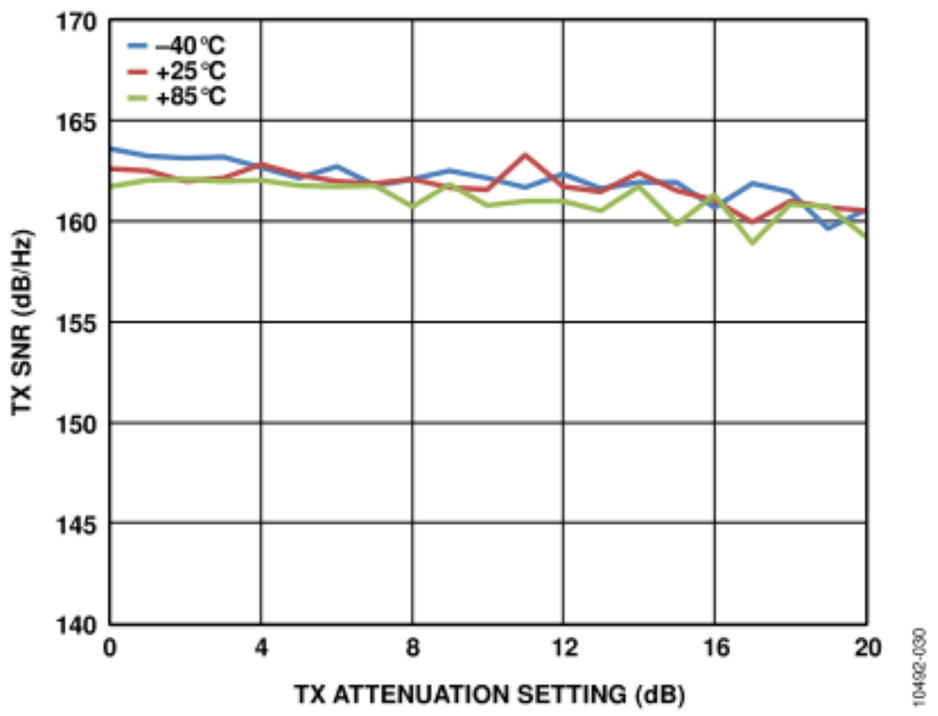


Figure 25. TX Signal-to-Noise Ratio (SNR) vs. Attenuation Setting, GSM Signal of Interest with Noise Measured at 20 MHz Offset

Figure 26. TX Single Sideband (SSB) Rejection vs. Frequency, 1.5375 MHz Offset

2.3 GHZ FREQUENCY BAND

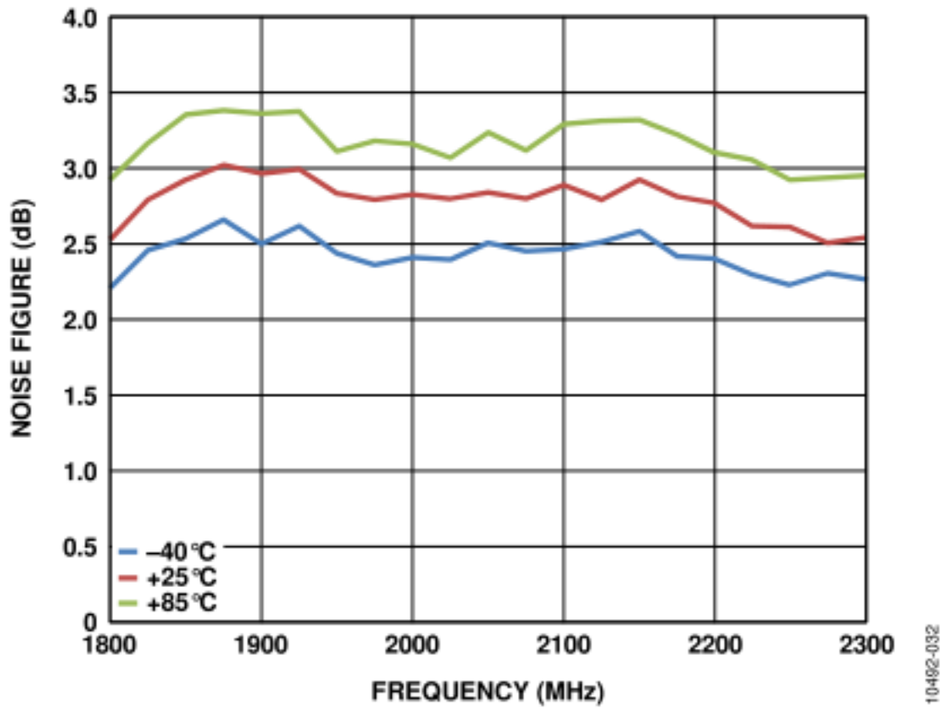


Figure 27. RX Noise Figure vs. RF Frequency

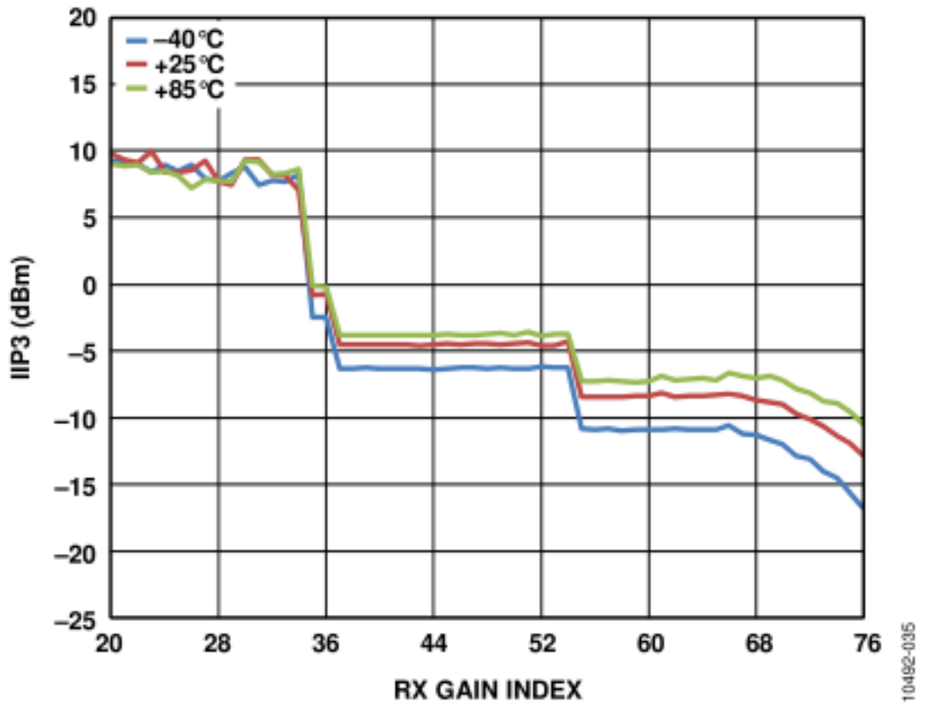


Figure 30. Third-Order Input Intercept Point (IIP3) vs. RX Gain Index, f1 = 30 MHz, f2 = 61 MHz

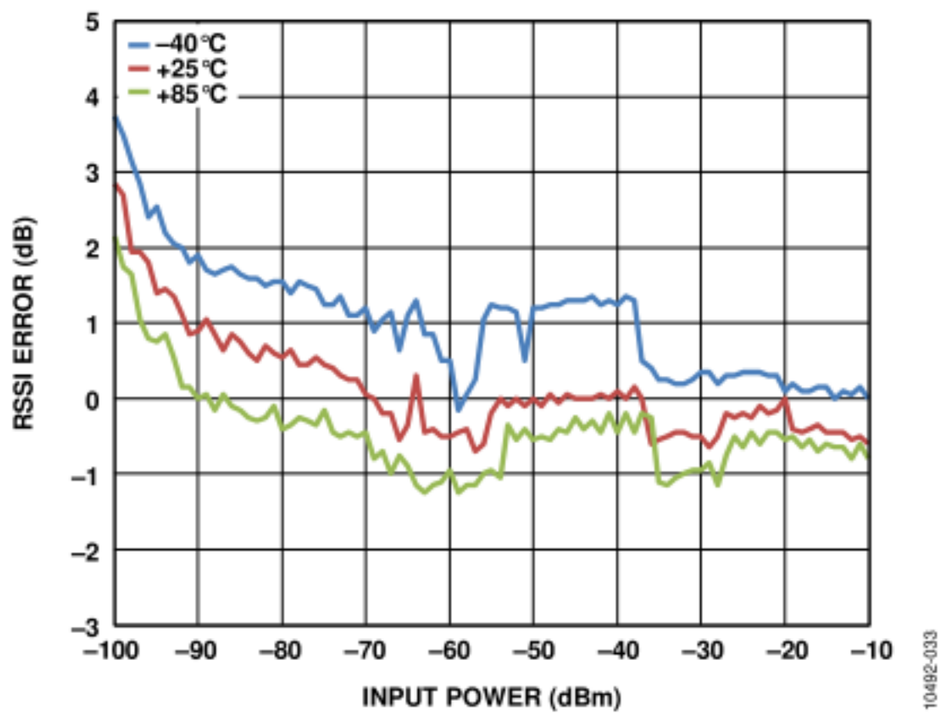


Figure 28. RSSI Error vs. Input Power (Referenced to −50 dBm Input Power at 2.3 GHz)

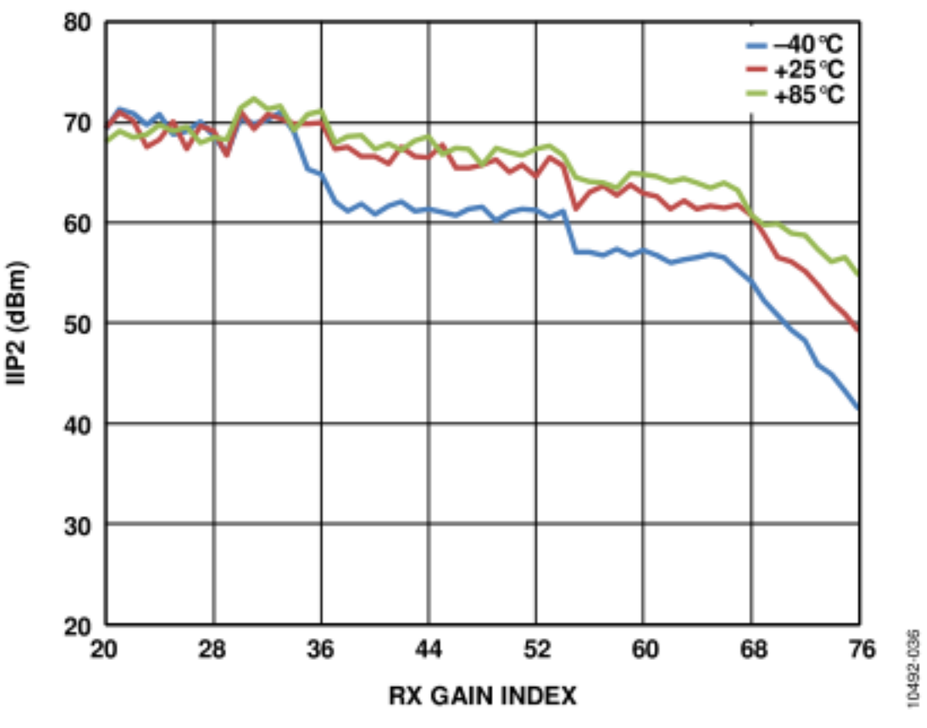


Figure 31. Second-Order Input Intercept Point (IIP2) vs. RX Gain Index, f1 = 60 MHz, f2 = 61 MHz

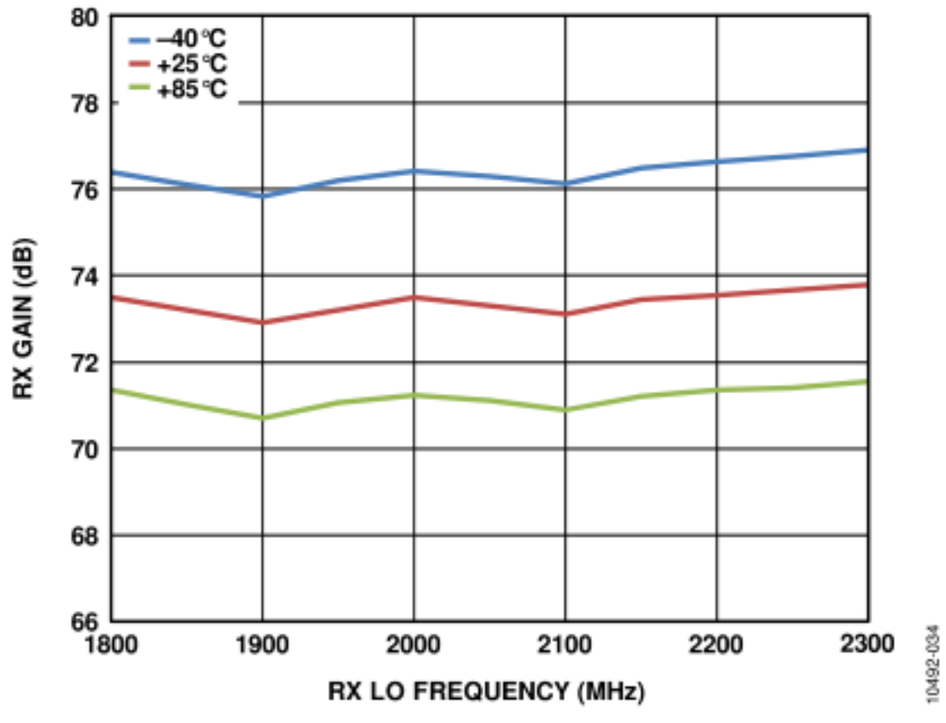


Figure 29. RX Gain vs. Frequency, Gain Index = 76 (Maximum Setting)

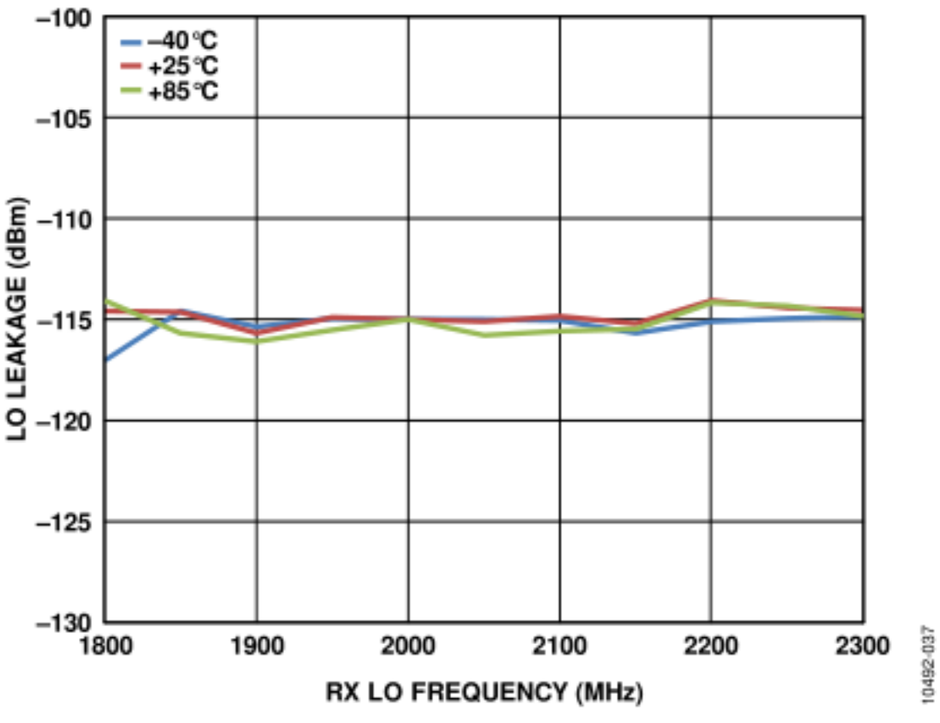


Figure 32. RX Local Oscillator (LO) Leakage vs. Frequency

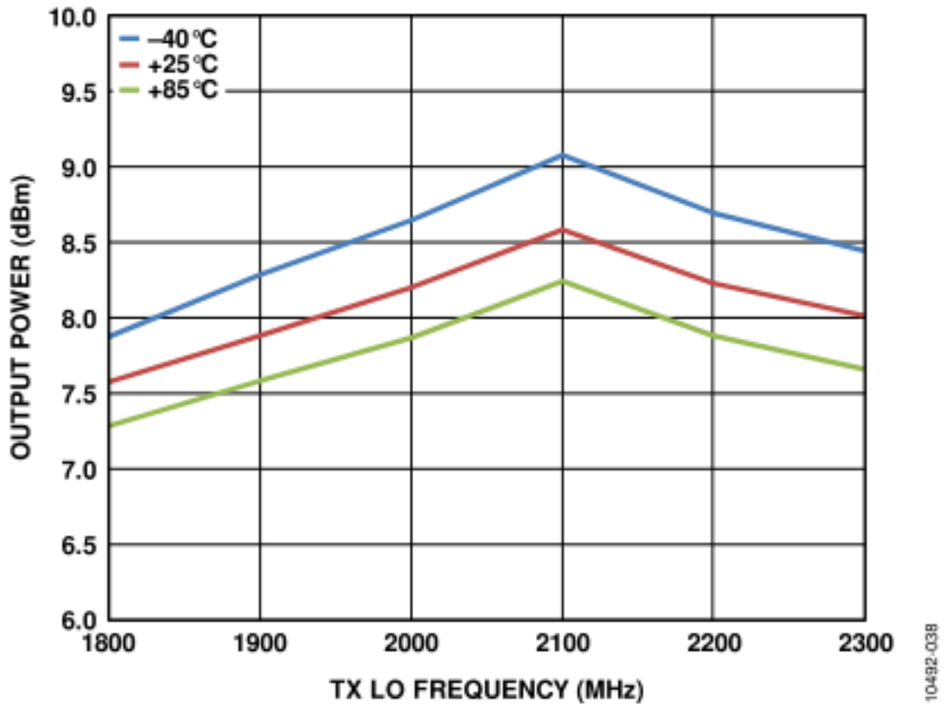


Figure 33. TX Output Power vs. Frequency, Attenuation Setting = 0 dB, Single Tone Output

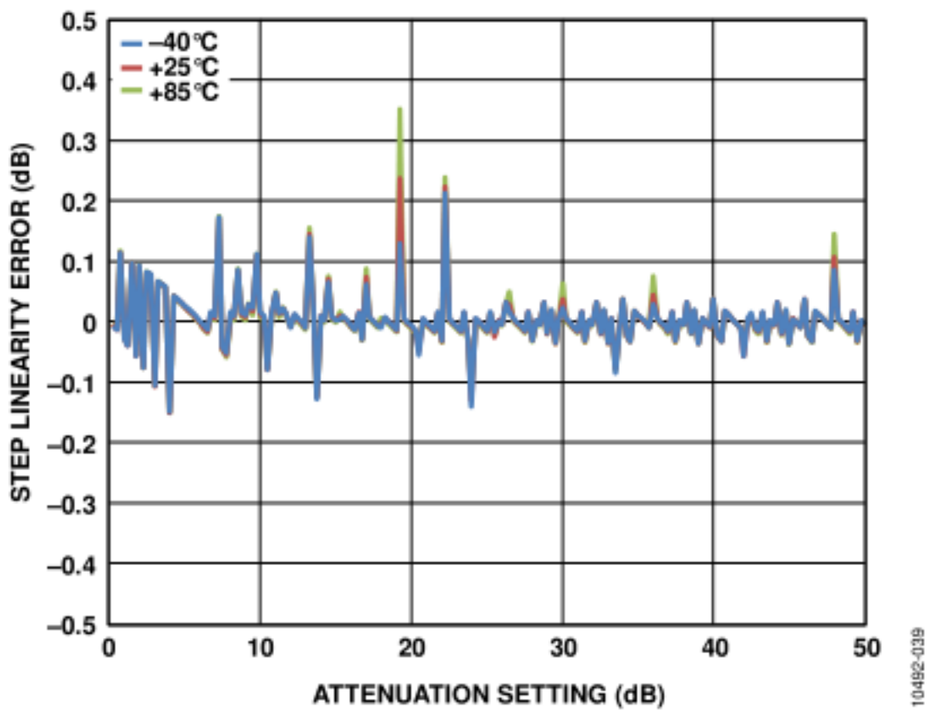


Figure 34. TX Power Control Linearity Error vs. Attenuation Setting

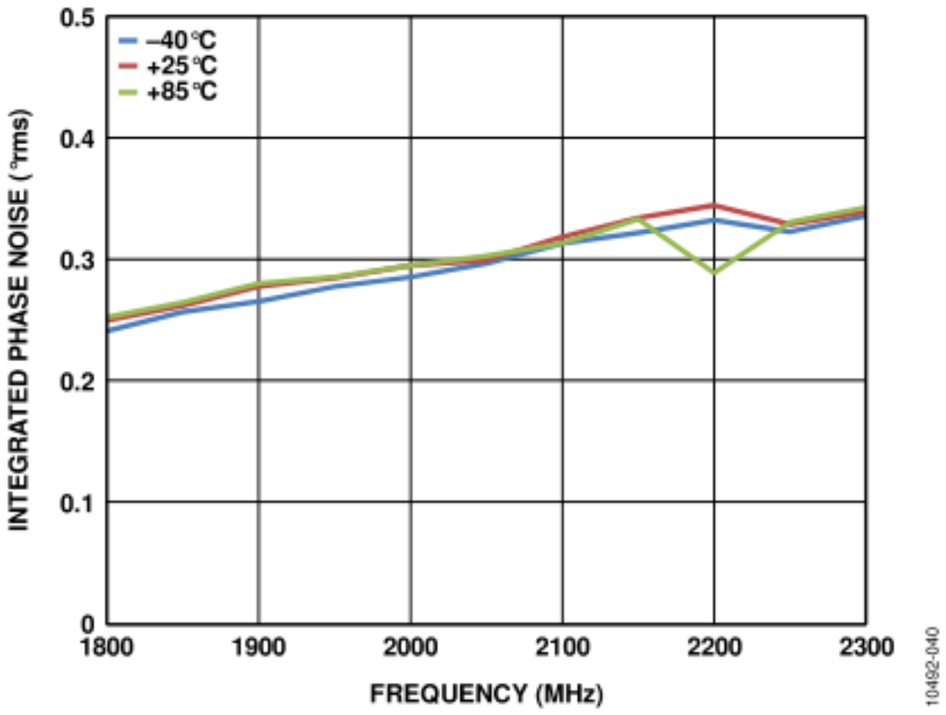


Figure 35. Integrated TX LO Phase Noise vs. Frequency, 40 MHz REF_CLK

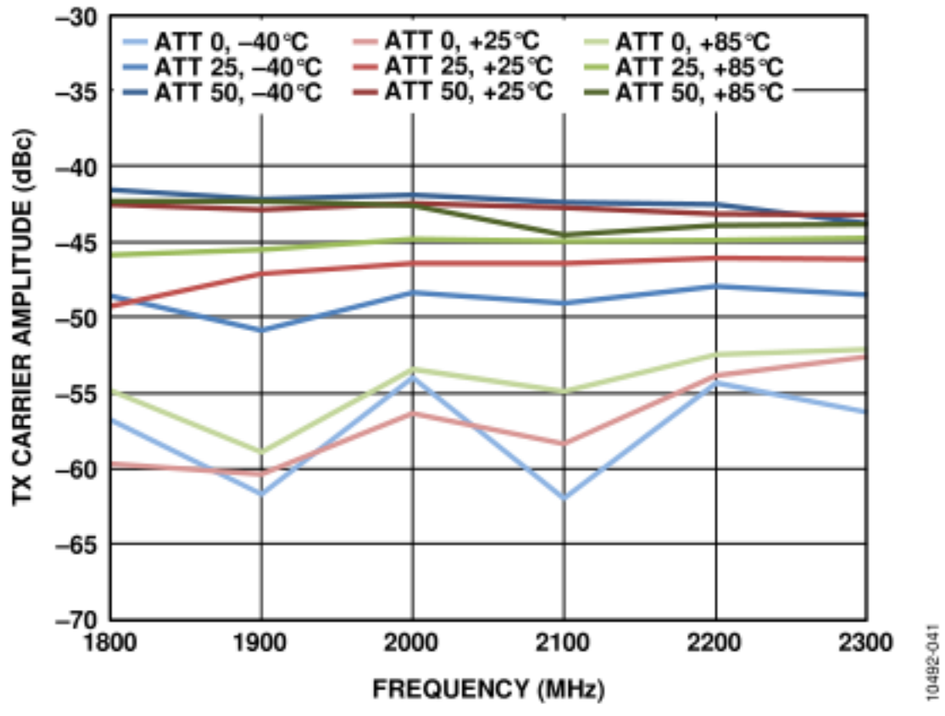


Figure 36. TX Carrier Rejection vs. Frequency

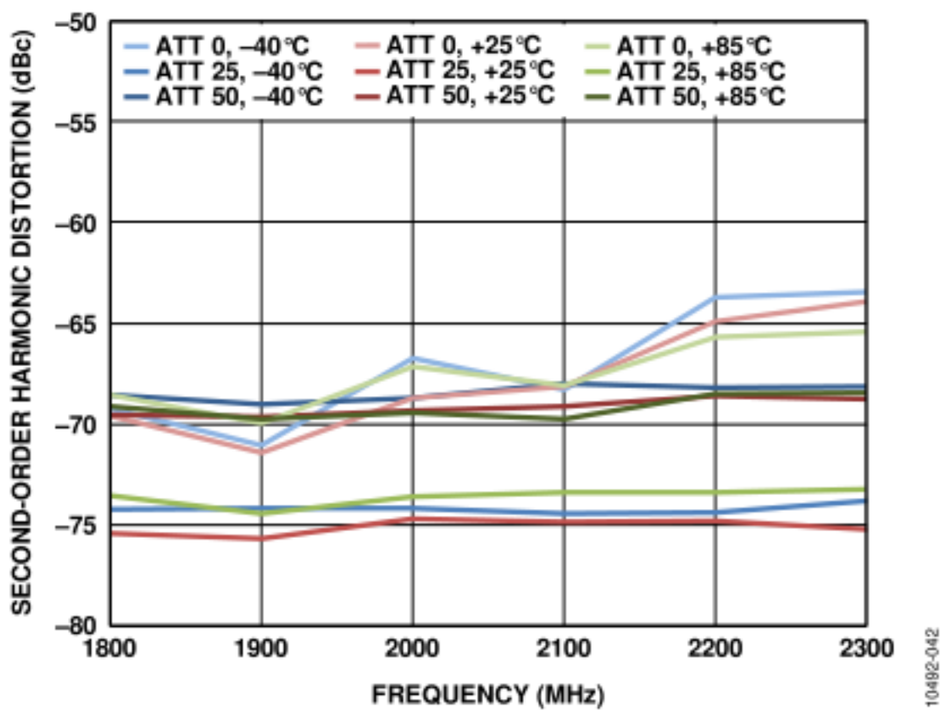


Figure 37. TX Second-Order Harmonic Distortion (HD2) vs. Frequency

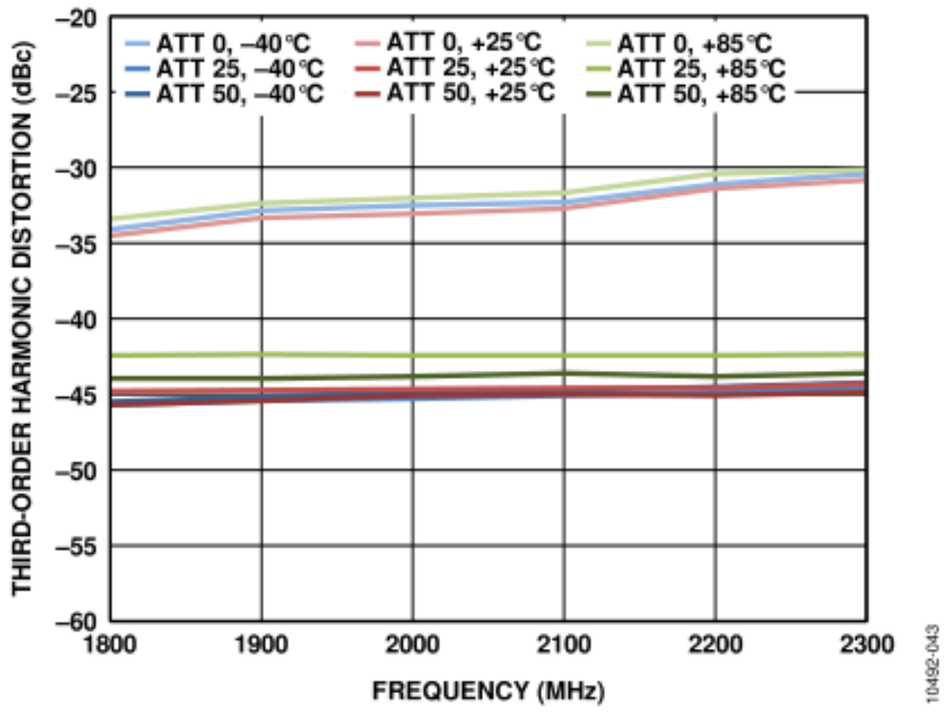


Figure 38. TX Third-Order Harmonic Distortion (HD3) vs. Frequency

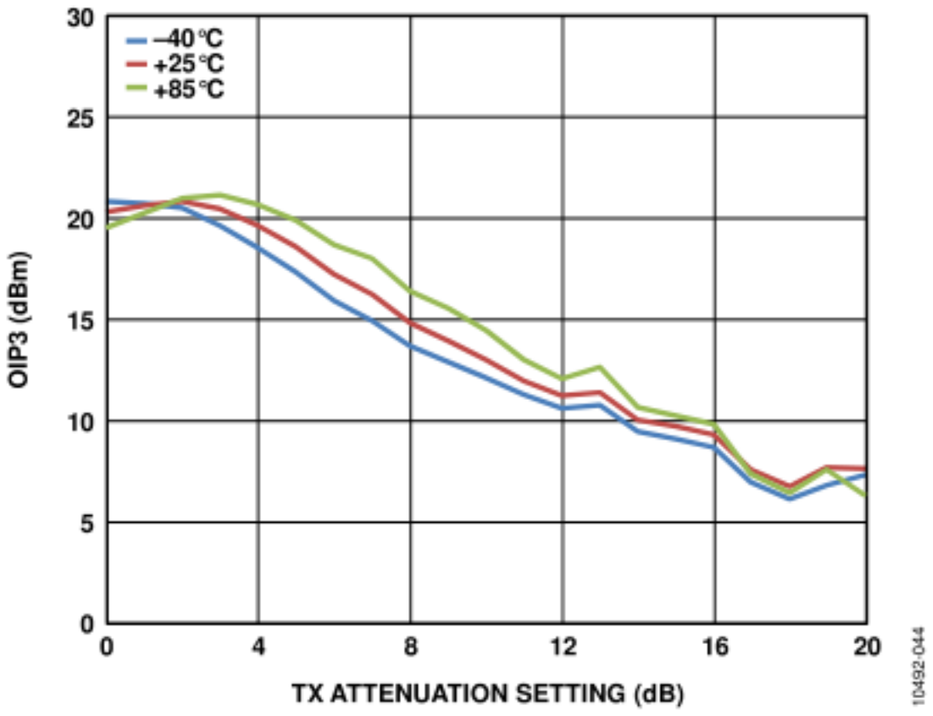


Figure 39. TX Third-Order Output Intercept Point (OIP3) vs. Attenuation Setting

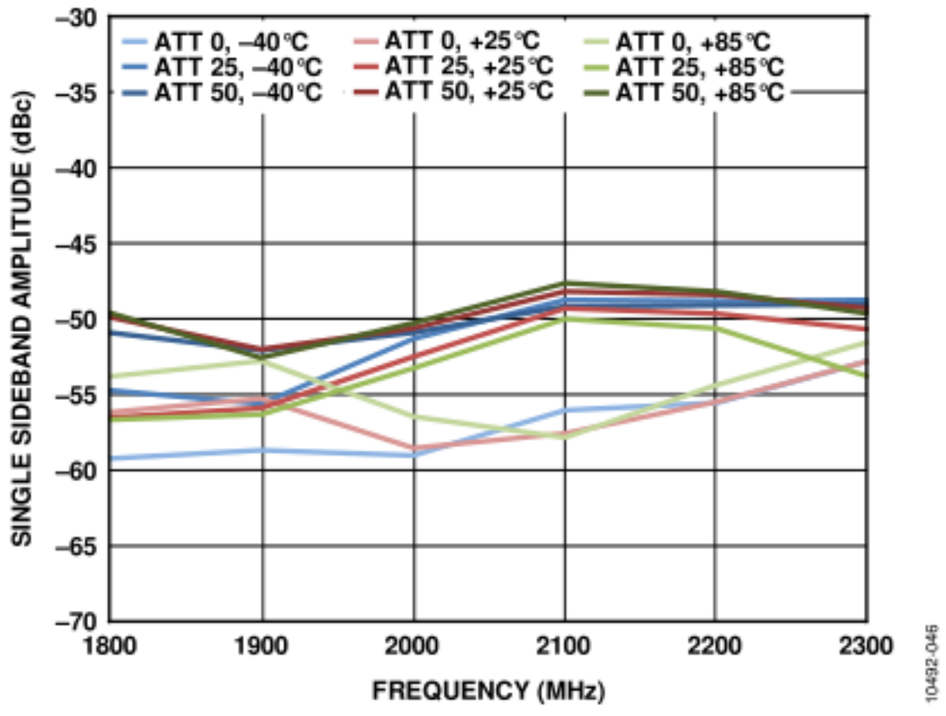


Figure 41. TX Single Sideband (SSB) Rejection vs. Frequency, 3.075 MHz Offset

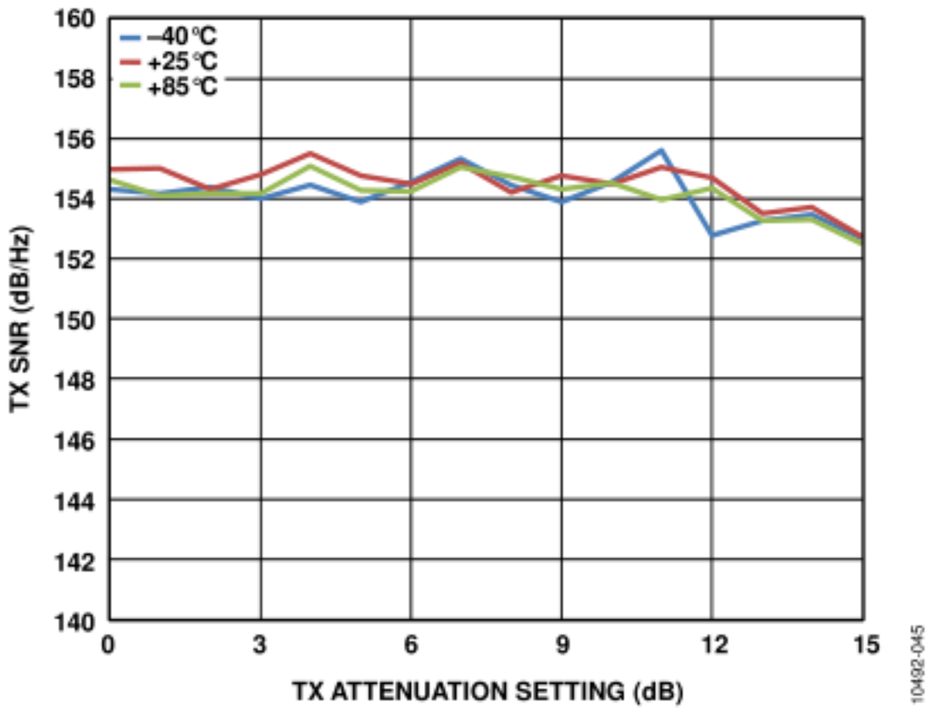


Figure 40. TX Signal-to-Noise Ratio (SNR) vs. Attenuation Setting, LTE 10 MHz Signal of Interest with Noise Measured at 90 MHz Offset

THEORY OF OPERATION

GENERAL

The AD9365 is a highly integrated radio frequency (RF) transceiver capable of being configured for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide all transceiver functions in a single device. Programmability allows this broadband transceiver to be adapted for use with multiple communication standards, including frequency division duplex (FDD) and time division duplex (TDD) systems. This programmability also allows the device to interface to various baseband processors (BBPs) using a single 12-bit parallel data port or dual 12-bit parallel data ports.

The AD9365 also provides self-calibration and automatic gain control (AGC) systems to maintain a high performance level under varying temperatures and input signal conditions. In addition, the device includes several test modes that allow system designers to insert test tones and create internal loopback modes to debug their designs during prototyping and optimize their radio configuration for a specific application.

RECEIVER

The receiver section contains all blocks necessary to receive RF signals and convert them to digital data that is usable by a BBP. It has three inputs that can be multiplexed to the signal chain, making the AD9365 suitable for use in multiband systems with multiple antenna inputs. The receiver is a direct conversion system that contains a low noise amplifier (LNA), followed by matched in-phase (I) and quadrature (Q) amplifiers, mixers, and band shaping filters that downconvert received signals to baseband for digitization. External LNAs can also be interfaced to the device, allowing designers the flexibility to customize the receiver front end for their specific application.

Gain control is achieved by following a preprogrammed gain index map that distributes gain among the blocks for optimal performance at each level. This can be achieved by enabling the internal AGC in either fast or slow mode or by using manual gain control, allowing the BBP to make the gain adjustments as needed. Additionally, the receiver provides independent RSSI measurement capability, dc offset tracking, and all circuitry necessary for self-calibration.

The receiver includes 12-bit, sigma-delta (Σ-Δ) ADCs and adjustable sample rates that produce data streams from the received signals. The digitized signals can be conditioned further by a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block can also be adjusted by changing decimation factors to produce the desired output data rate.

TRANSMITTER

The transmitter section consists of two differential output stages that can be multiplexed to the transmit channel. The transmit channel provides all digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system. The digital data received from the BBP passes through a fully programmable 128-tap FIR filter with interpolation options. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each 12-bit DAC has an adjustable sampling rate. Both the I and Q channels are fed to the RF block for upconversion.

When converted to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts and fed to the upconversion mixers. At this point, the I and Q signals are recombined and modulated on the carrier frequency for transmission to the output stage. The combined signal also passes through analog filters that provide additional band shaping; the signal is then transmitted to the output amplifier. The transmit channel provides a wide attenuation adjustment range with fine granularity to help designers optimize signal-to-noise ratio (SNR).

Self-calibration circuitry is built into the transmit channel to provide automatic real-time adjustment. The transmitter block also provides a TX monitor that routes the transmitter output back through an unused receiver channel to the BBP for signal monitoring. The TX monitor is available in both FDD mode and TDD mode.

CLOCK INPUT OPTIONS

The AD9365 uses an external oscillator or clock distribution device (such as the AD9548) to provide a reference clock to the XTALN pin. The clock frequency can vary between 10 MHz and 80 MHz. This reference clock is used to supply the synthesizer blocks that generate all data clocks, sample clocks, and local oscillators inside the device.

SYNTHESIZERS

RF PLLs

The AD9365 contains two identical synthesizers to generate the required LO signals for the RF signal paths—one for the receiver and one for the transmitter. Phase-locked loop (PLL) synthesizers are fractional-N designs that incorporate completely integrated voltage controlled oscillators (VCOs) and loop filters. In TDD mode, the synthesizers turn on and off as appropriate for the RX and TX frames. In FDD mode, the TX PLL and the RX PLL can be activated at the same time. These PLLs require no external components.

BB PLL

The AD9365 also contains a baseband PLL (BB PLL) synthesizer that is used to generate all baseband related clock signals. These signals include the ADC and DAC sampling clocks, the DATA_CLK signal (see the Digital Data Interface section), and all data framing signals. The BB PLL is programmed from 700 MHz to 1400 MHz based on the data rate and sample rate requirements of the system.

DIGITAL DATA INTERFACE

The AD9365 data interface uses parallel data ports (P0 and P1) to transfer data between the device and the BBP. The data ports consist of single-ended, CMOS format, 12-bit buses. Each bus can be configured in multiple arrangements to match system requirements for data ordering and data port connections. These configurations include single port data bus, dual port data bus, single data rate, and double data rate.

Bus transfers are controlled using simple hardware handshake signaling. The two ports can be operated in either bidirectional (TDD) mode or in full duplex (FDD) mode, where half the bits are used for transmitting data and half are used for receiving data. The interface can also be configured to use only one of the data ports for applications that do not require high data rates and require fewer interface pins.

DATA_CLK Signal

The AD9365 supplies the DATA_CLK signal that the BBP uses when receiving the data. The DATA_CLK can be set to a rate that provides single data rate (SDR) timing, where data is sampled on each rising clock edge, or it can be set to provide double data rate (DDR) timing, where data is captured on both rising and falling clock edges. SDR or DDR timing applies to operation using either a single port or both ports.

FB_CLK Signal

For transmit data, the interface uses the FB_CLK signal as the timing reference. FB_CLK allows source synchronous timing with rising edge capture for burst control signals and either rising edge capture (SDR mode) or both edge capture (DDR mode) for transmit signal bursts. The FB_CLK signal must have the same frequency and duty cycle as DATA_CLK.

RX_FRAME Signal

The device generates an RX_FRAME output signal whenever the receiver outputs valid data. This signal has two modes: level mode (RX_FRAME stays high as long as the data is valid) and pulse mode (RX_FRAME pulses with a 50% duty cycle). Similarly, the BBP must provide a TX_FRAME signal that indicates the beginning of a valid data transmission with a rising edge. Like RX_FRAME, this signal can stay high throughout the burst or it can be pulsed with a 50% duty cycle.

ENABLE STATE MACHINE

The AD9365 transceiver includes an enable state machine (ENSM) that allows real-time control over the current state of the device. The device can be placed in several different states during normal operation, including

- Wait—power save, synthesizers disabled
- Sleep—wait with all clocks and the BB PLL disabled
- TX—TX signal chain enabled
- RX—RX signal chain enabled
- FDD—TX and RX signal chains enabled
- Alert—synthesizers enabled

The ENSM has two control modes: SPI control and pin control.

SPI Control Mode

In SPI control mode, the ENSM is controlled asynchronously by writing to SPI registers to advance the current state to the next state. SPI control is considered asynchronous to the DATA_CLK because the SPI_CLK can be derived from a different clock reference and can still function properly. The SPI control ENSM method is recommended when real-time control of the synthesizers is not necessary. SPI control can be used for real-time control as long as the BBP can perform timed SPI writes accurately.

Pin Control Mode

In pin control mode, the enable function of the ENABLE pin and the TXNRX pin allow real-time control of the current state. The ENSM allows TDD or FDD operation, depending on the configuration of the corresponding SPI register. The ENABLE and TXNRX pin control mode is recommended if the BBP has extra control outputs that can be controlled in real time, allowing a simple 2-wire interface to control the state of the device. To advance the current state of the ENSM to the next state, the enable function of the ENABLE pin can be driven by either a pulse (edge detected internally) or a level.

When a pulse is used, it must have a minimum pulse width of one FB_CLK cycle. In level mode, the ENABLE and TXNRX pins are also edge detected by the AD9365 and must meet the same minimum pulse width requirement of one FB_CLK cycle.

In FDD mode, the ENABLE and TXNRX pins can be remapped to serve as real-time RX and TX data transfer control signals. In this mode, the enable function of the ENABLE pin assumes the RXON function (controls when the RX path is enabled and disabled), and the TXNRX pin assumes the TXON function (controls when the TX path is enabled and disabled). In this mode, the ENSM must be controlled by SPI writes while the ENABLE and TXNRX pins control all data flow.

SPI INTERFACE

The AD9365 uses a serial peripheral interface (SPI) to communicate with the BBP. This interface can be configured as a 4-wire interface with dedicated receive and transmit ports, or it can be configured as a 3-wire interface with a bidirectional data communication port. This bus allows the BBP to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first six bits are used to set the bus direction and number of bytes to transfer. The next 10 bits set the address where data is to be written. The final eight bits are the data to be transferred to the specified register address (MSB to LSB). The AD9365 also supports an LSB-first format that allows the commands to be written in LSB to MSB format. In this mode, the register addresses are incremented for multi-byte writes.

Read commands follow a similar format, with the exception that the first 16 bits are transferred on the SPI_DI pin and the final eight bits are read from the AD9365, either on the SPI_DO pin in 4-wire mode or on the SPI_DI pin in 3-wire mode.

CONTROL PINS

Control Outputs (CTRL_OUT2 to CTRL_OUT0)

The AD9365 provides three simultaneous real-time output signals for use as interrupts to the BBP. These outputs can be configured to output a number of internal settings and measurements that the BBP can use when monitoring transceiver performance in different situations. The control output pointer register selects the information that is output to these pins, and the control output enable register determines which signals are activated for monitoring by the BBP. Signals used for manual gain mode, calibration flags, state machine states, and the ADC output are among the outputs that can be monitored on these pins.

Control Inputs (CTRL_IN2 to CTRL_IN0)

The AD9365 provides three edge detected control input pins. In manual gain mode, the BBP can use these pins to change the gain table index in real time. In transmit mode, the BBP can use two of the pins to change the transmit gain in real time.

GPO PINS (GPO_3 TO GPO_0)

The AD9365 provides four, 3.3 V capable general-purpose logic output pins: GPO_3, GPO_2, GPO_1, and GPO_0. These pins can be used to control other peripheral devices such as regulators and switches via the AD9365 SPI bus, or they can function as slaves for the internal AD9365 state machine.

AUXILIARY CONVERTERS

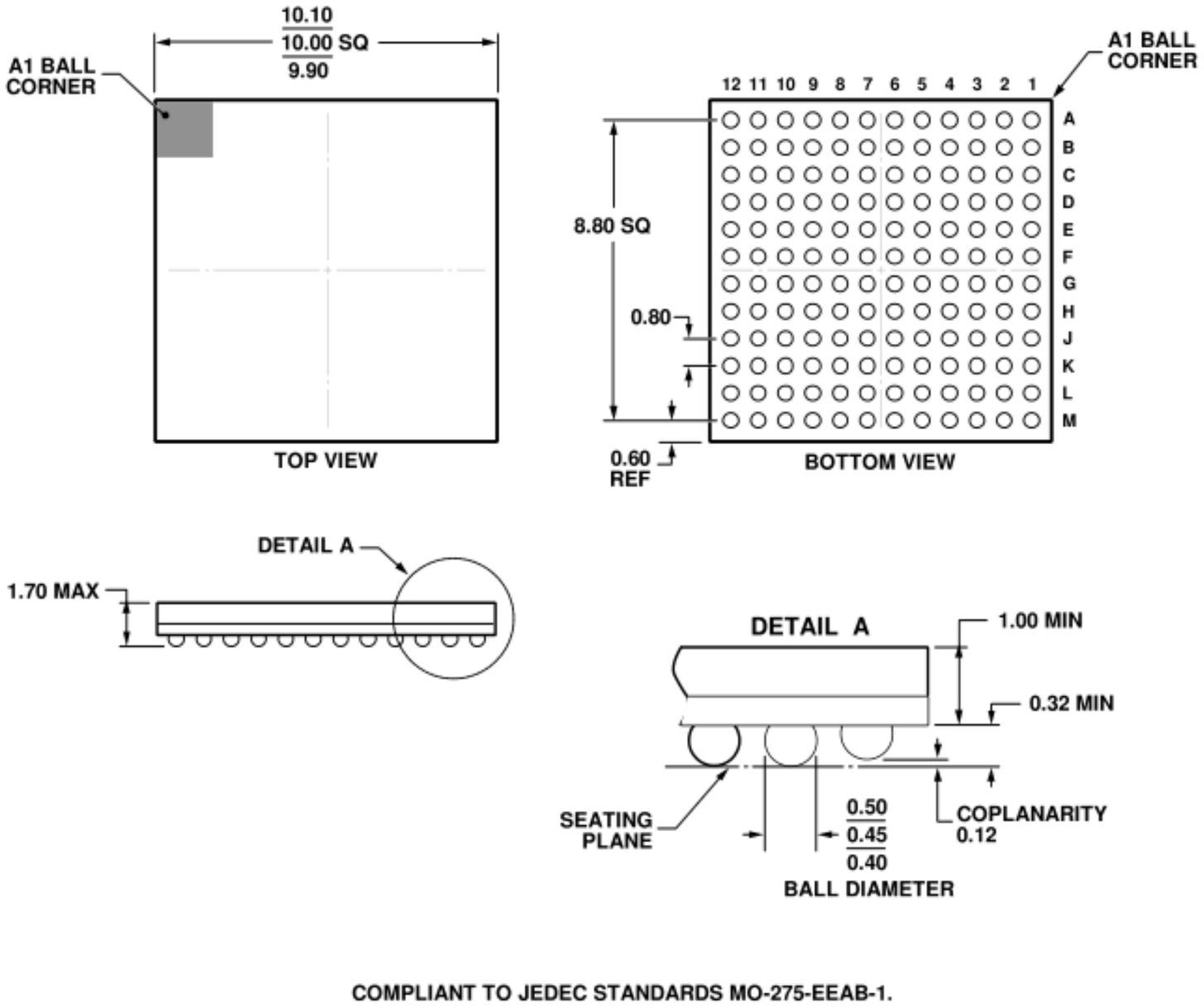
AUXADC

The AD9365 contains an auxiliary ADC that can be used to monitor system functions such as temperature or power output. The converter is 12 bits wide and has an input range of 0 V to the VDDA1P3_BB supply voltage. When enabled, the ADC is free running. SPI reads provide the last value latched at the ADC output. A multiplexer in front of the ADC allows the user to select between the AUXADC input pin and a built-in temperature sensor.

AUXDAC1 and AUXDAC2

The AD9365 contains two identical auxiliary DACs that can provide power amplifier (PA) bias or other system functionality. The auxiliary DACs are 10 bits wide, have an output voltage range of 0.5 V to VDD_GPO – 0.3 V and a current drive of 10 mA, and can be directly controlled by the internal enable state machine.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-EEAB-1.

Figure 42. 144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-144-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9365BBCZ	–40°C to +85°C	144-Ball CSP_BGA	BC-144-7
AD9365BBCZ-REEL	–40°C to +85°C	144-Ball CSP_BGA	BC-144-7
AD9365/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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