

Silicon-Based Technology

Very High Speed and Low Power Memory

SB61L256A

32,768 x 8-Bits

STATIC CMOS RAM

PRELIMINARY

Description:

The SB61L256A series products are 32,768-words by 8-bits static RAMs fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the SB61L256A series products exhibit very high-speed performance with single +5-volt power supply while requiring very low power and no clock or refreshing to operate. The SB61L256A is packed in a standard 28-pin 300mil SOJ/PDIP.

Features:

- 32,768-word x 8-bit organization
- Single +5-volt power supply
- Fully static operation — no clock or refreshing required
- LVTTL-compatible inputs and outputs
- Common I/O capability
- Low power consumption
 - Active: 180/160/140 mA (Max.)
 - Standby: 5 mA
- Very high speed access: 8/10/12 ns (Max.)
- 28-pin plastic 300 mil SOJ/PDIP package
- Output Enable (\overline{OE}) available for very fast access

Ordering Information:

Part Number	Package	Word Organization	Access Time ns(Max.)	Supply Voltage (Typ.)	Supply Current mA (Max.)	
					Operating	Standby
SB61L256A-8	28-Pin Plastic SOJ/DIP (300 mil)	32Kx 8 bits	8	5V± 5%	180	5
SB61L256A-10			10		160	
SB61L256A-12			12		140	

The information in this document is subject to change without notice



Silicon-Based Technology Corporation

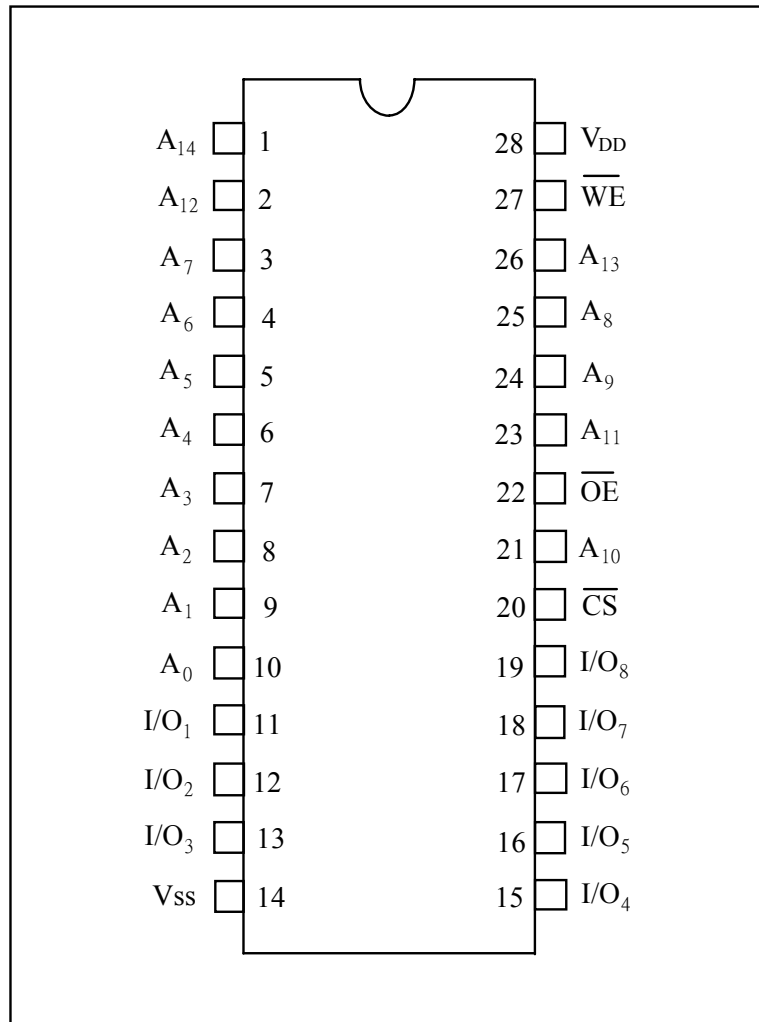
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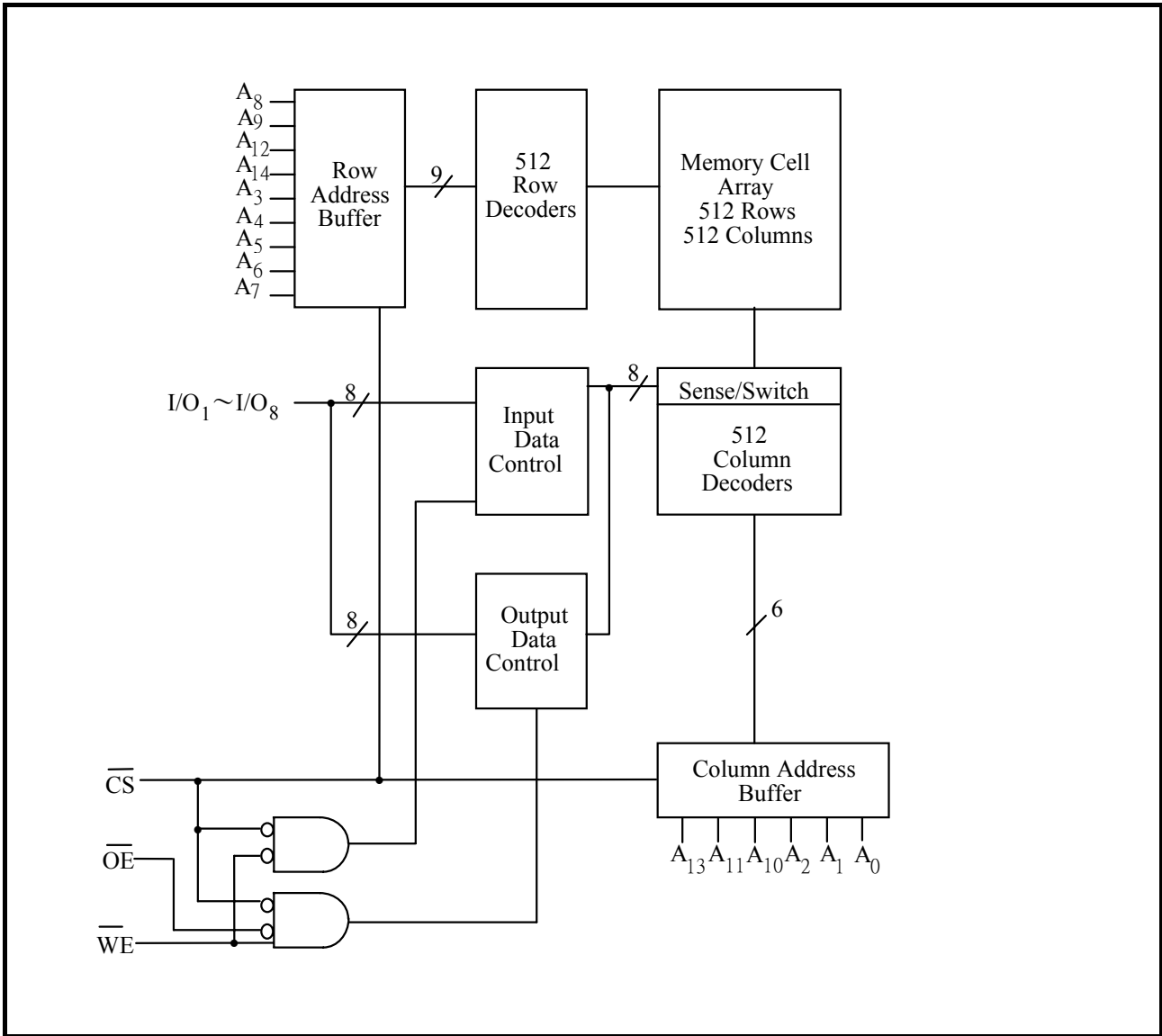
Pin Configuration: 28-Pin 300 mil SOJ



Symbols	Functions
$A_0 \sim A_{14}$	Address Inputs
$I/O_1 \sim I/O_8$	Data Inputs/Outputs
\overline{CS}	Chip Select Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power Supply
V_{SS}	Ground



Block Diagram:



Truth Table:

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O ₁ ~I/O ₈	V _{DD} Current
H	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
L	H	H	Output Disable	High Z	I _{DD}
L	L	H	Read	Data Out	I _{DD}
L	X	L	Write	Data In	I _{DD}



DC Characteristics:

Absolute Maximum Ratings

Parameters	Rating	Unit
Supply Voltage to V _{SS}	-0.5 to +7.0	V
Input/Output to V _{SS}	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Operating Characteristics:

(V_{DD} = 5V ± 5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameters	Symbols	Test Conditions	Min.	Typ.	Max.	Unit	
Input Low Voltage	V _{IL}	-	-0.3	-	+0.8	V	
Input High Voltage	V _{IH}	-	+2.6	-	V _{DD} +0.5	V	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA	
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , \overline{CS} = V _{IH} or \overline{OE} = V _{IH} or \overline{WE} = V _{IL}	-10	-	+10	μA	
Output Low Voltage	V _{OL}	I _{OL} = +8.0mA	-	-	+0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	+2.8	-	-	V	
Operating Power	I _{DD}	\overline{CS} = V _{IL} , I/O = 0 mA Cycle = MIN, Duty = 100%	8	-	-	180	mA
Supply Current			10	-	-	160	mA
			12	-	-	140	mA
Standby Power	I _{SB}	\overline{CS} = V _{IH} , Cycle = MIN Duty = 100%	-	-	15	mA	
Supply Current	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	5	mA	

Note: Typical characteristics are measured at V_{DD} = 5V, T_a = 25°C



AC Characteristics:

Capacitances

($V_{DD} = 5V$, $T_a = 25^\circ C$, $f = 1\text{ MHz}$)

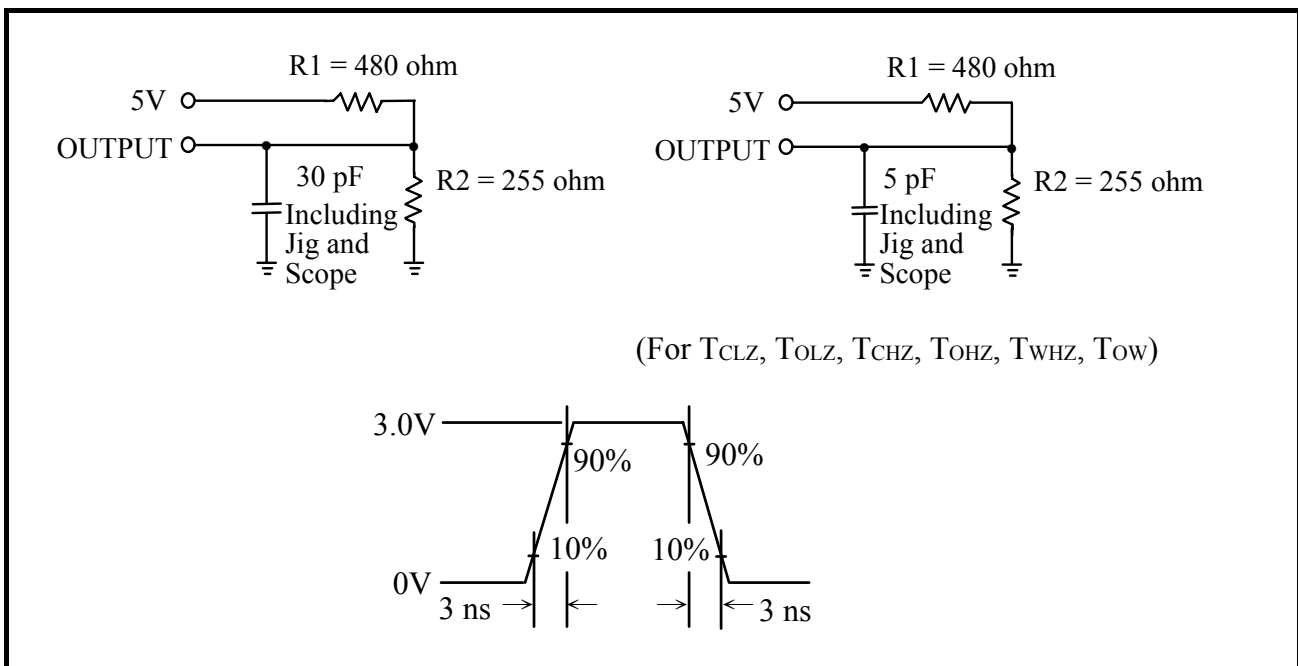
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0V$	8	pF

Note: These parameters are sampled but not 100% tested.

AC Test Conditions

Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 30\text{ pF}$, $I_{OH}/I_{OL} = -4\text{ mA}/8\text{ mA}$

AC Test Loads and Waveforms





AC Performances:

($V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0$ to $70^\circ C$)

(1) Read Cycle

Parameters	Symbols	SB61L256A-8		SB61L256A-10		SB61L256A-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T _{RC}	8	-	10	-	12	-	ns
Address Access Time	T _{AA}	-	8	-	10	-	12	ns
Chip Select Access Time	T _{ACS}	-	8	-	10	-	12	ns
Output Enable to Output Valid	T _{AOE}	-	5	-	6	-	7	ns
Chip Selection to Output in Low Z	T _{CLZ} *	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	T _{OLZ} *	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	T _{CHZ} *	-	4	-	5	-	6	ns
Output Disable to Output in High Z	T _{OHZ} *	-	4	-	5	-	6	ns
Output Hold from Address Change	T _{OH}	3	-	3	-	3	-	ns

*These parameters are sampled but not 100% tested

(2) Write Cycle

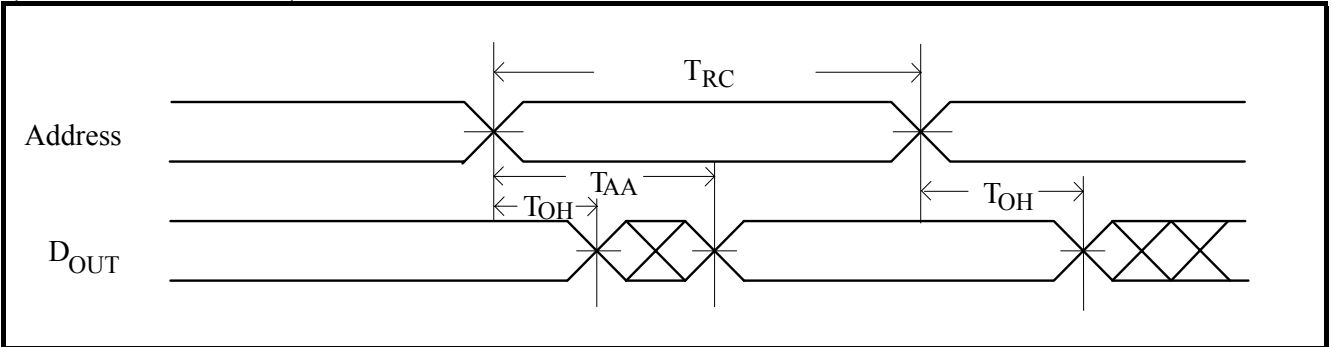
Parameters	Symbols	SB61L256A-8		SB61L256A-10		SB61L256A-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T _{WC}	8	-	10	-	12	-	ns
Chip Selection to End of Write	T _{CW}	6	-	8	-	10	-	ns
Address Valid to End of Write	T _{AW}	6	-	8	-	10	-	ns
Address Setup Time	T _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	T _{WP}	6	-	8	-	10	-	ns
Write Recovery Time	T _{WR}	0	-	0	-	0	-	ns
Data Valid to End of Write	T _{DW}	4	-	6	-	8	-	ns
Data Hold from End of Write	T _{DH}	0	-	0	-	0	-	ns
Write to Output in High Z	T _{WHZ} *	-	4	-	5	-	6	ns
Output Disable to Output in High Z	T _{OHZ} *	-	4	-	5	-	6	ns
Output Active from End of Write	T _{OW}	0	-	0	-	0	-	ns

* These parameters are sampled but not 100% tested

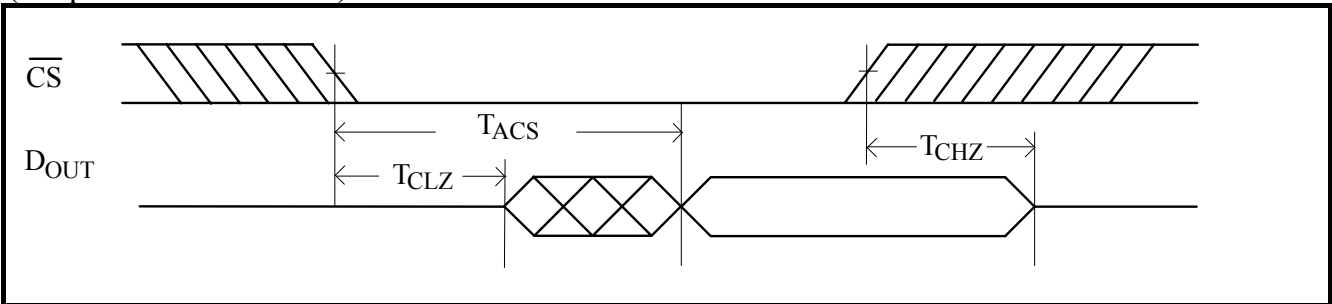


Timing Waveforms

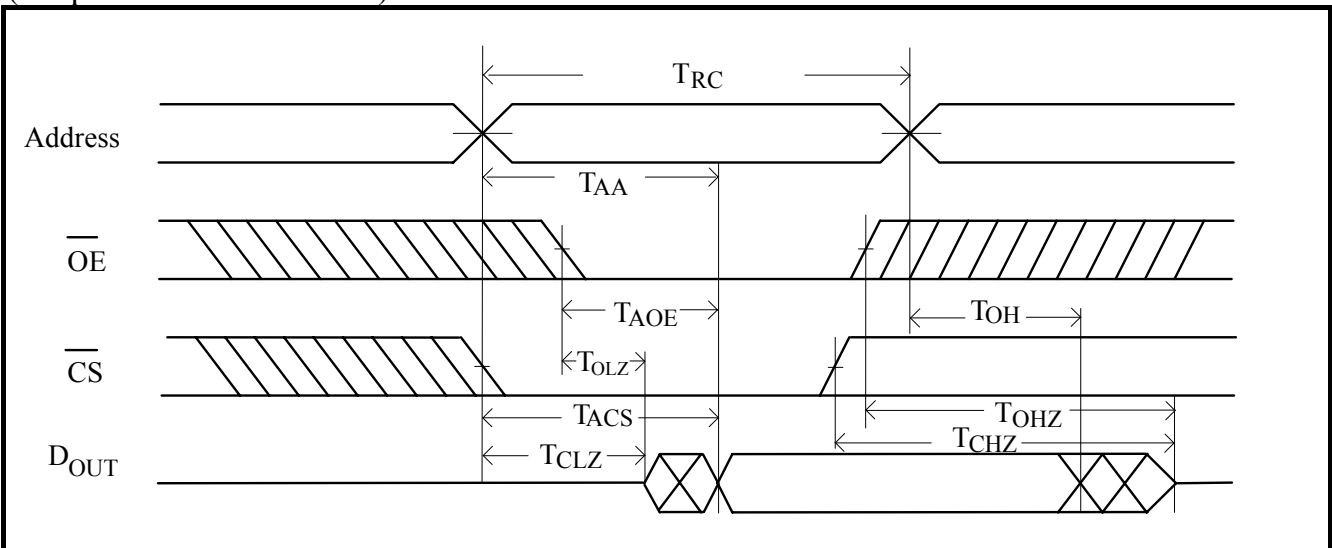
Read Cycle 1 (Address Controlled)



Read Cycle 2 (Chip Select Controlled)

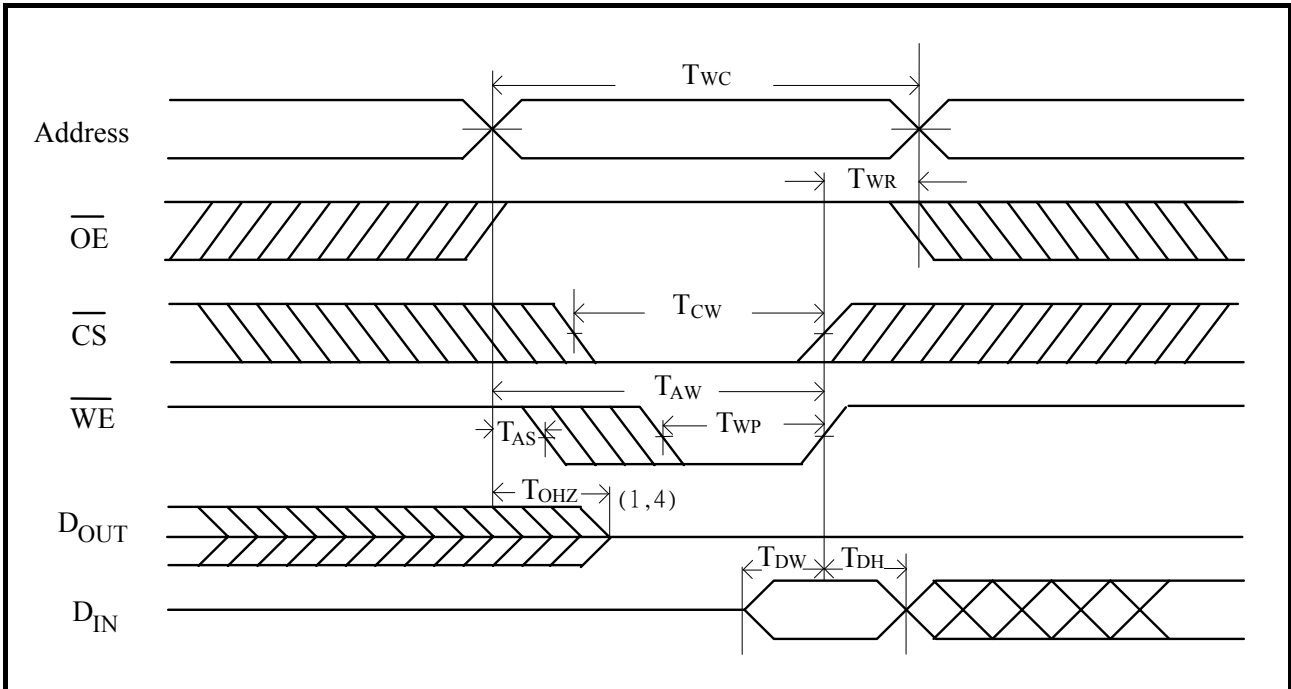


Read Cycle 3 (Output Enable Controlled)

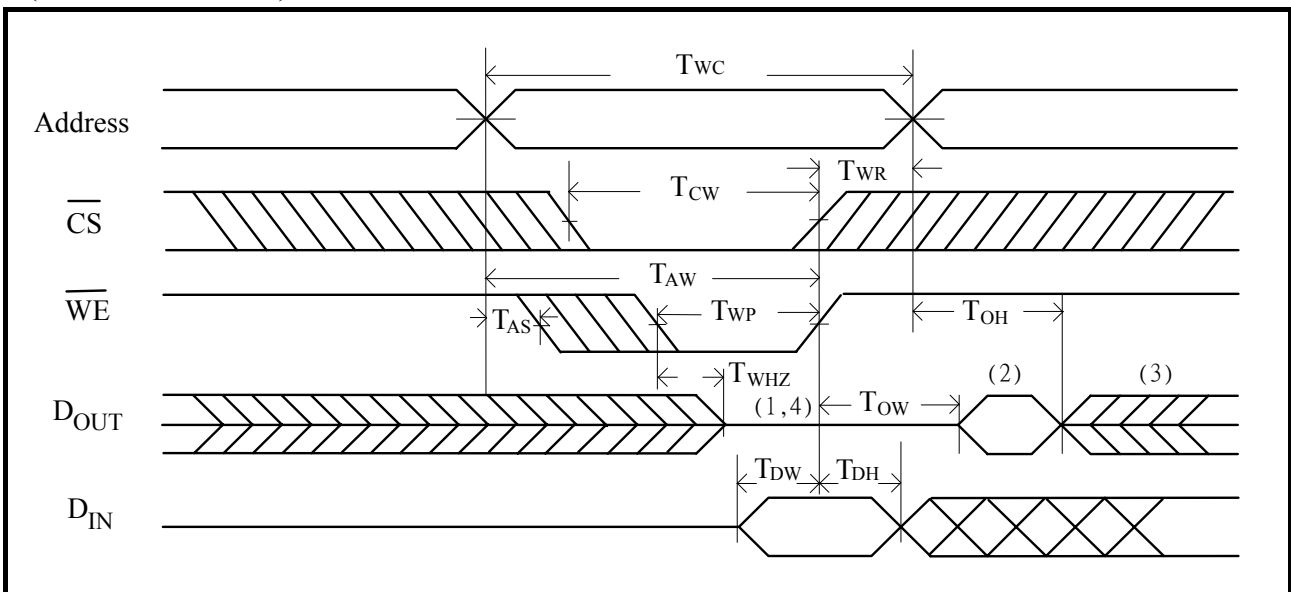




Write Cycle 1
(\overline{OE} Clock)



Write Cycle 2
($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$. This parameter is guaranteed but not 100% tested.



SB61L256A

Preliminary