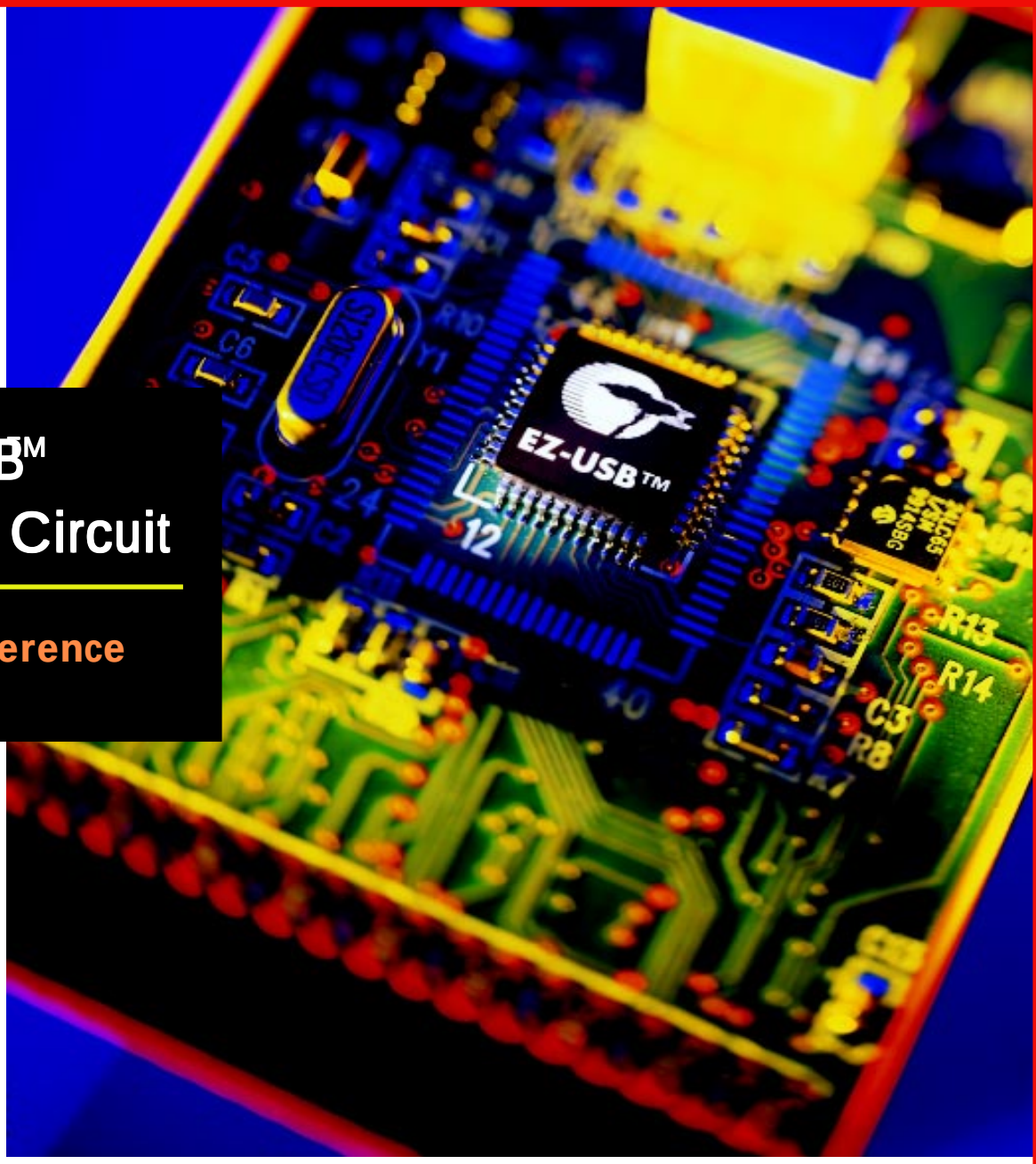
The EZ-USB™ Integrated Circuit

Technical Reference



CYPRESS

The EZ-USB Technical Reference Manual

Development Kit — Getting Started

Documentation for the EZ-USB™ Xcelerator™ Development it. Includes an overview of the kit, descriptions of kit components with installation instructions, and details about the development board.

Technical Reference

Documentation of the EZ-USB controller. Includes details about the CPU, memory, input/output, ReNumeration™, bulk transfers, endpoint zero, isochronous transfers, interrupts, resets, power management, registers, AC/DC parameters, and packages.

Appendices

Documentation for the 8051 enhanced core. Includes an introduction, an architectural overview, and a hardware description.

Registers

EZ-USB register maps.

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EZ-USB
Technical Reference Manual

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1 Introducing EZ-USB

1.1 Introduction

Like a well designed automobile or appliance, a USB peripheral's outward simplicity hides internal complexity. There's a lot going on "under the hood" of a USB device, which gives the user a new level of convenience. For example:

- A USB device can be plugged in anytime, even when the PC is turned on.
- When the PC detects that a USB device has been plugged in, it automatically interrogates the device to learn its capabilities and requirements. From this information, the PC automatically loads the device's driver into the operating system. When the device is unplugged, the operating system automatically logs it off and unloads its driver.
- USB devices do not use DIP switches, jumpers, or configuration programs. There is never an IRQ, DMA, MEMORY, or IO conflict with a USB device.
- USB expansion hubs make the bus available to dozens of devices.
- USB is fast enough for printers, CD-quality audio, and scanners.

USB is defined in the *Universal Serial Bus Specification Version 1.1* (**http://usb.org**), a 268-page document that describes all aspects of a USB device in elaborate detail. This EZ-USB Technical Reference Manual describes the EZ-USB chip along with USB topics that should provide help in understanding the Specification.

The Cypress Semiconductor EZ-USB is a compact integrated circuit that provides a highly integrated solution for a USB peripheral device. Three key EZ-USB features are:

- The EZ-USB family provides a *soft* (RAM-based) solution that allows unlimited configuration and upgrades.
- The EZ-USB family delivers full USB throughput. Designs that use EZ-USB are not limited by number of endpoints, buffer sizes, or transfer speeds.
- The EZ-USB family does much of the USB housekeeping in the EZ-USB core, simplifying code and accelerating the USB learning curve.

This chapter introduces some key USB concepts and terminology that should make reading the rest of this Technical Reference Manual easier.

1.2 EZ-USB Block Diagrams

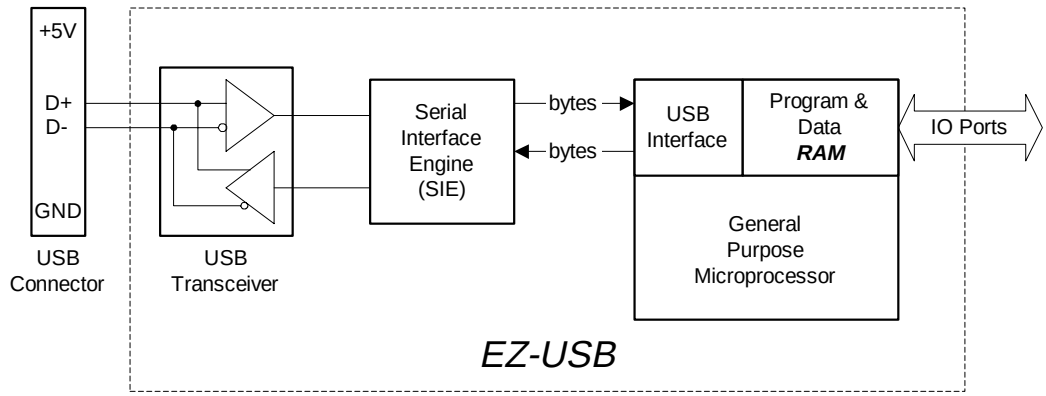


Figure 1-1. AN2131S (44 pin) Simplified Block Diagram

The Cypress Semiconductor EZ-USB chip packs the intelligence required by a USB peripheral interface into a compact integrated circuit. As Figure 1-1 illustrates, an integrated USB transceiver connects to the USB bus pins D+ and D-. A Serial Interface Engine (SIE) decodes and encodes the serial data and performs error correction, bit stuffing, and other signaling-level details required by USB, and ultimately transfers data bytes to and from the USB interface.

The internal microprocessor is enhanced 8051 with fast execution time and added features. It uses internal RAM for program and data storage, making the EZ-USB family a *soft* solution. The USB host downloads 8051 program code and device personality into RAM over the USB bus, and then the EZ-USB chip re-connects as the custom device as defined by the loaded code.

The EZ-USB family uses an enhanced SIE/USB interface (called the “USB Core”) which has the intelligence to function as a full USB device even before the 8051. The enhanced core simplifies 8051 code by implementing much of the USB protocol itself.

EZ-USB chips operate at 3.3V. This simplifies the design of bus-powered USB devices, since the 5V power available in the USB connector (which the USB specification allows to be as low as 4.4V) can drive a 3.3V regulator to deliver clean isolated power to the EZ-USB chip.

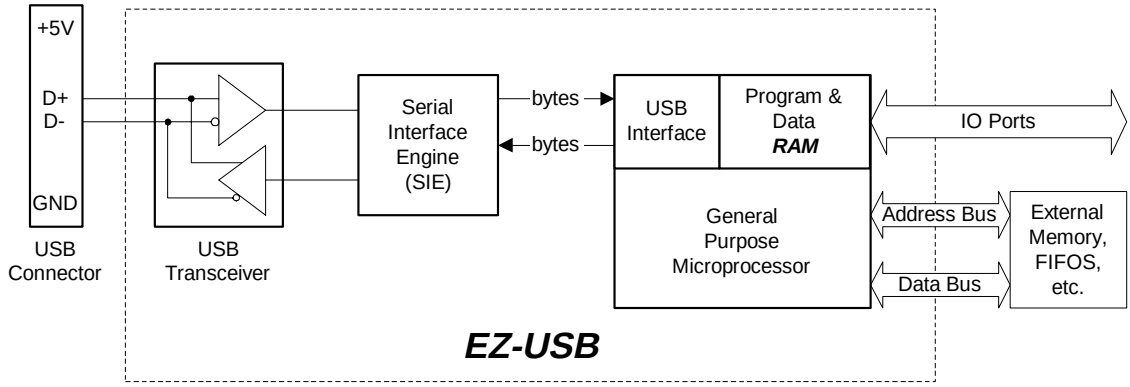


Figure 1-2. AN2131Q (80 pin) Simplified Block Diagram

Figure 1-2 illustrates the An2131Q, an 80-pin version of the EZ-USB family. In addition to the 24 IO pins, it contains a 16-bit address bus and an 8-bit data bus for external memory expansion.

A special *fast transfer* mode moves data directly between external logic and internal USB FIFOs. The fast transfer mode, along with abundant endpoint resources, allows the EZ-USB family to support transfer bandwidths beyond the maximum required by the *Universal Serial Bus Specification Version 1.1*.

1.3 The USB Specification

The *Universal Serial Bus Specification Version 1.1* is available on the Internet at **http://usb.org**. Published in January 1998, the specification is the work of a founding committee of seven industry heavyweights: Compaq, DEC, IBM, Intel, Microsoft, NEC, and Northern Telecom. This impressive list of implementers secures USB as the low to medium speed PC connection method of the future.

A glance at the USB Specification makes it immediately apparent that USB is not nearly as simple as the customary serial or parallel port. The specification uses new terms like "endpoint," isochronous," and "enumeration," and finds new uses for old terms like "configuration," "interface," and "interrupt." Woven into the USB fabric is a software abstraction model that deals with things such as "pipes." The specification also contains detail about the connector types and wire colors.

1.4 Tokens and PIDs

In this manual, you will read statements like, “When the host sends an IN token...” or “The device responds with an ACK.” What do these terms mean? A USB transaction consists of data packets identified by special codes called Packet IDs or PIDs. A PID signifies what kind of packet is being transmitted. There are four PID types, as shown in Table 1-1.

Table 1-1. USB PIDs

PID Type	PID Name
Token Data	IN, OUT, SOF, SETUP, DATA0, DATA1
Handshake	ACK, NAK, STALL
Special	PRE

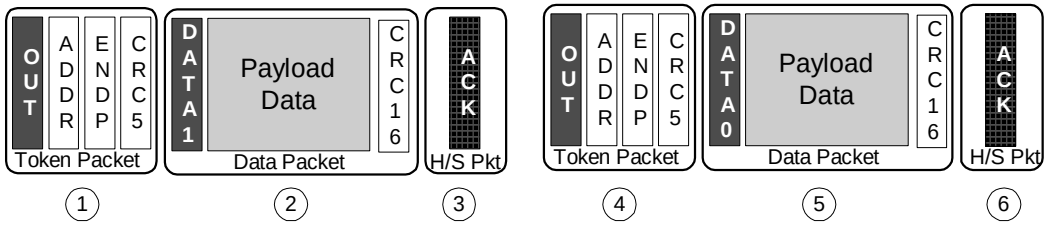


Figure 1-3. USB Packets

Figure 1-3 illustrates a USB transfer. Packet j is an OUT token, indicated by the OUT PID. The OUT token signifies that data from the host is about to be transmitted over the bus. Packet !k contains data, as indicated by the DATA1 PID. Packet l is a handshake packet, sent by the device using the ACK (acknowledge) PID to signify to the host that the device received the data error-free.

Continuing with Figure 1-3, a second transaction begins with another OUT token m, followed by more data n, this time using the DATA0 PID. Finally, the device again indicates success by transmitting the ACK PID in a handshake packet o.

Why two DATA PIDs, DATA0 and DATA1? It’s because the USB architects took error correction very seriously. As mentioned previously, the ACK handshake is a signal to the host that the peripheral received data without error (the CRC portion of the packet is used to detect errors). But what if a handshake packet itself is garbled in transmission? To detect this, each side, host and device maintains a *data toggle* bit, which is toggled between data packet transfers. The state of this internal toggle bit is compared with the

PID that arrives with the data, either DATA0 or DATA1. When sending data, the host or device sends alternating DATA0-DATA1 PIDs. By comparing the Data PID with the state of the internal toggle bit, the host or device can detect a corrupted handshake packet.

SETUP tokens are unique to CONTROL transfers. They preface eight bytes of data from which the peripheral decodes host Device Requests.

SOF tokens occur once per millisecond, denoting a USB *frame*.

There are three handshake PIDs: ACK, NAK, and STALL.

- ACK means "success;" the data was received error-free.
- NAK means "busy, try again." It's tempting to assume that NAK means "error," but it doesn't. A USB device indicates an error by *not responding*.
- STALL means that something unforeseen went wrong (probably as a result of miscommunication or lack of cooperation between the software and firmware writers). A device sends the STALL handshake to indicate that it doesn't understand a device request, that something went wrong on the peripheral end, or that the host tried to access a resource that isn't there. It's like "halt," but better, because USB provides a way to recover from a stall.

A PRE (Preamble) PID precedes a low-speed (1.5 Mbps) USB transmission. The EZ-USB family supports high-speed (12 Mbps) USB transfers only, so it ignores PRE packets and the subsequent low-speed transfer.

1.5 Host is Master

This is a fundamental USB concept. There is exactly one master in a USB system: the host computer. *USB devices respond to host requests*. USB devices cannot send information between themselves, as they could if USB were a peer-to-peer topology.

Actually, there is one case where a USB device can initiate signaling without prompting from the host. After being put into a low-power suspend mode by the host, a device can signal a remote wakeup. But that's the only way to "yank the host's chain." Everything else happens because the host makes device requests and the device responds to them.

There's an excellent reason for this host-centric model. The USB architects were keenly mindful of cost, and the best way to make low-cost peripherals is to put most of the smarts

into the host side, the PC. If USB had been defined as peer-to-peer, every USB device would have required more intelligence, raising cost.

Here are two important consequences of the “host is master” concept:

1.5.1 Receiving Data from the Host

To send data to a USB peripheral, the host issues an OUT token followed by the data. If the peripheral has space for the data, and accepts it without error, it returns an ACK to the host. If it is busy, it instead sends a NAK. If it finds an error, it sends nothing back. For the latter two cases, the host re-sends the data at a later time.

1.5.2 Sending Data to the Host

A USB device never spontaneously sends data to the host. Nevertheless, in the EZ-USB chip, there’s nothing to stop the 8051 from loading data for the host into an endpoint buffer (Section 1.13, "EZ-USB Endpoints") and *arming* it for transfer. But the data will sit in the buffer *until the host sends an IN token to that particular endpoint*. If the host never sends the IN token, the data sits there indefinitely.

1.6 USB Direction

Once you accept that the host is the bus master, it’s easy to remember USB direction: OUT means from the host to the device, and IN means from the device to the host. EZ-USB nomenclature uses this naming convention. For example, an endpoint that sends data to the host is an IN endpoint. This can be confusing at first, because the 8051 *sends* data by loading an IN endpoint buffer, but keeping in mind that an 8051 *out* is IN to the host, it makes sense.

1.7 Frame

The USB host provides a time base to all USB devices by transmitting a SOF (Start Of Frame) packet every millisecond. The SOF packet includes an incrementing, 11-bit frame count. The 8051 can read this frame count from two EZ-USB registers. SOF-time has significance for isochronous endpoints; it’s the time that the *ping-ponging* buffers switch places. The EZ-USB core provides the 8051 with an SOF interrupt request for servicing isochronous endpoint data.

1.8 EZ-USB Transfer Types

USB defines four transfer types. These match the requirements of different data types delivered over the bus. (Section 1.13, "EZ-USB Endpoints" explains how the EZ-USB family supports the four transfer types.)

1.8.1 Bulk Transfers

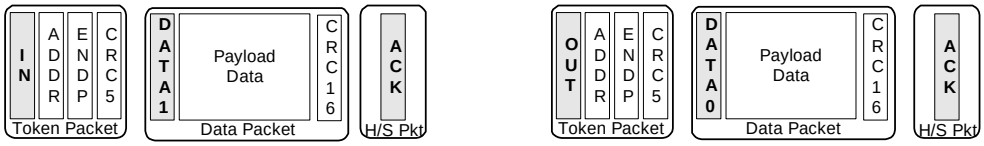


Figure 1-4. Two Bulk Transfers, IN and OUT

Bulk data is *bursty*, traveling in packets of 8, 16, 32, or 64 bytes. Bulk data has guaranteed accuracy, due to an automatic re-try mechanism for erroneous data. The host schedules bulk packets when there is available bus time. Bulk transfers are typically used for printer, scanner, or modem data. Bulk data has built-in flow control provided by handshake packets.

1.8.2 Interrupt Transfers

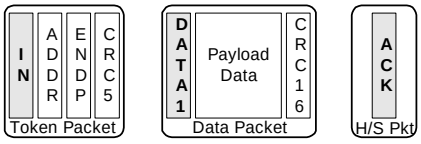


Figure 1-5. An Interrupt Transfer

Interrupt data is like bulk data, but exists only for IN endpoints in the “Universal Serial Bus Specification Version 1.1.” Interrupt data can have packet sizes of 1-64 bytes. Interrupt endpoints have an associated polling interval that ensures that they will be *pinged* (will receive an IN token) by the host on a regular basis.

1.8.3 Isochronous Transfers

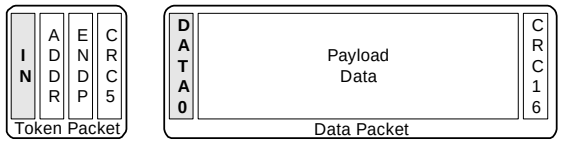


Figure 1-6. An Isochronous Transfer

Isochronous data is time-critical and used for *streaming* data like audio and video. Time of delivery is the most important requirement for isochronous data. In every USB frame, a certain amount of USB bandwidth is allocated to isochronous transfers. To lighten the overhead, isochronous transfers have no handshake (ACK/NAK/STALL), and no retries. Error detection is limited to a 16-bit CRC. Isochronous transfers do not use the data toggle mechanism; isochronous data uses only the DATA0 PID.

1.8.4 Control Transfers

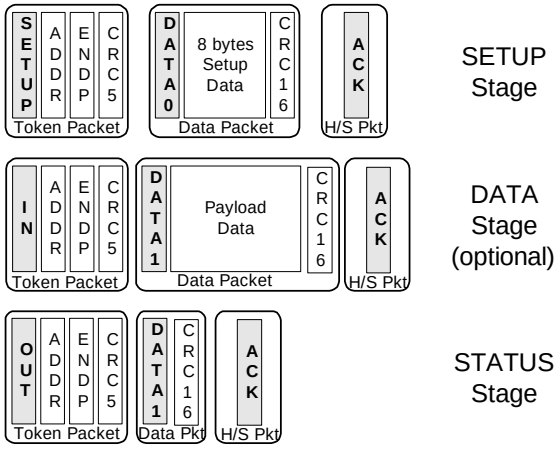


Figure 1-7. A Control Transfer

Control transfers are used to configure and send commands to a device. Being *mission critical*, they employ the most extensive error checking USB offers. Control transfers are delivered on a *best effort* basis by the host (*best effort* is defined by a six-step process in the *Universal Serial Bus Specification Version 1.1, "Section 5.5.4"*). The host reserves a part of each USB frame time for Control transfers.

Control transfers consist of two or three stages. The SETUP stage contains eight bytes of USB CONTROL data. An optional DATA stage contains more data, if required. The STATUS (or *handshake*) stage allows the device to indicate successful completion of a control operation.

1.9 Enumeration

Your computer is ON. You plug in a USB device, and the Windows™ cursor switches to an hourglass, and then back to a cursor. And magically, your device is connected and its Windows™ driver is loaded! Anyone who has installed a sound card into a PC and had to configure countless jumpers, drivers, and IO/Interrupt/DMA settings knows that a USB connection can be like a miracle. We've all *heard* about Plug and Play, but USB delivers the real thing.

How does all this happen automatically? Inside every USB device is a table of 'descriptors' that are the sum total of the device's requirements and capabilities. When you plug into USB, the host goes through a 'sign-on' sequence:

1. The host sends a "Get_Descriptor/Device" request to address zero (devices must respond to address zero when first attached).

2. The device dutifully responds to this request by sending ID data back to the host telling what it is.

3. The host sends the device a "Set_Address" request, which gives it a unique address to distinguish it from the other devices connected to the bus.

4. The host sends more "Get_Descriptor" requests, asking more device information. from this, it learns everything else about the device, like how many endpoints the device has, its power requirements, what bus bandwidth it requires, and what driver to load.

This sign-on process is called *Enumeration*.

1.10 The USB Core

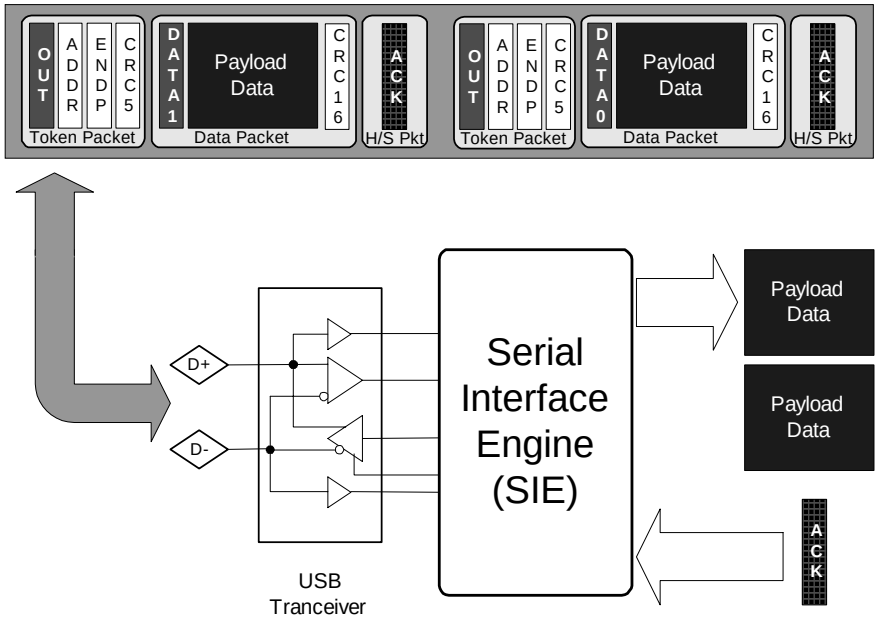


Figure 1-8. What the SIE Does

Every USB device has a Serial Interface Engine (SIE). The SIE connects to the USB data lines D+ and D-, and delivers bytes to and from the USB device. Figure 1-8 illustrates a USB bulk transfer, with time moving from left to right. The SIE decodes the packet PIDs, performs error checking on the data using the transmitted CRC bits, and delivers payload data to the USB device. If the SIE encounters an error in the data, it automatically indicates *no response* instead of supplying a handshake PID. This instructs the host to retransmit the data at a later time.

Bulk transfers such as the one illustrated in Figure 1-8 are *asynchronous*, meaning that they include a flow control mechanism using ACK and NAK handshake PIDs. The SIE indicates *busy* to the host by sending a NAK handshake packet. When the peripheral device has successfully transferred the data, it commands the SIE to send an ACK handshake packet, indicating success.

To send data to the host, the SIE accepts bytes and control signals from the USB device, formats it for USB transfer, and sends it over the two-wire USB. Because the USB uses a self-clocking data format (NRZI), the SIE also inserts bits at appropriate places in the bit stream to guarantee a certain number of transitions in the serial data. This is called “bit stuffing,” and is transparently handled by the SIE.

One of the most important features of the EZ-USB family is that it is *soft*. Instead of requiring ROM or other fixed memory, it contains internal program/data RAM that is downloaded over the USB itself to give the device its unique personality. This make modifications, specification revisions, and updates a snap.

The EZ-USB family can connect as a USB device and download code into internal RAM, all while its internal 8051 is held in RESET. This is done by an enhanced SIE, which does all of the work shown in Figure 1-8, and more. It contains additional logic to perform a full enumeration, using an internal table of descriptors. It also responds to a vendor specific "Firmware Download" device request to load its internal RAM. An added bonus is that the added SIE functionality is also made available to the 8051. This saves 8051 code and processing time.

Throughout this manual, the SIE and its enhancements are referred to as the "USB Core."

1.11 EZ-USB Microprocessor

The EZ-USB microprocessor is an enhanced 8051 core. Use of an 8051 compatible processor makes extensive software support tools immediately available to the EZ-USB designer. This enhanced 8051 core, described in Chapter 2, "EZ-USB CPU" and Appendices A-C, has the following features:

- 4-clock cycle, as compared to the 12-clock cycle of a standard 8051, giving a 3X speed improvement.
- Dual data pointers for faster memory-to-memory transfers.
- Two UARTs.
- Three counter-timers.
- An expanded interrupt system.
- 24-MHz clock.
- 256 bytes of internal register RAM.
- Standard 8051 instruction set—if you know the 8051, you know EZ-USB

The enhanced 8051 core uses on-chip RAM as program and data memory, giving EZ-USB its *soft* feature. Chapter 3, "EZ-USB Memory" describes the various memory options.

The 8051 communicates with the SIE using a set of registers, which occupy the top of the on-chip RAM address space. These registers are grouped and described by function in individual chapters of this reference manual, and summarized in register order in Chapter 12, "EZ-USB Registers."

The EZ-USB 8051 has two duties. First, it participates in the protocol defined in the *Universal Serial Bus Specification Version 1.1, "Chapter 9, USB Device Framework."* Thanks to EZ-USB enhancements to the SIE and USB interface, the 8051 firmware associated with USB overhead is simplified, leaving code space and bandwidth available for the 8051's primary duty, to help implement your device. On the device side, abundant input/output resources are available, including IO ports, UARTs, and an I^2C bus master controller. These resources are described in Chapter 4, "EZ-USB Input/Output."

1.12 ReNumeration™

Because it is *soft*, the EZ-USB chip can take on the identities of multiple distinct USB devices. The first device downloads your 8051 firmware and USB descriptor tables over the USB cable when the peripheral device is plugged in. Once downloaded, another device comes on as a totally different USB peripheral as defined by the downloaded information. This two-step process, called ReNumeration™, happens instantly when the device is plugged in, with no hint that the initial load step has occurred.

Chapter 5, "EZ-USB Enumeration and ReNumeration‘" describes this feature in detail, along with other EZ-USB boot (startup) modes.

1.13 EZ-USB Endpoints

The *Universal Serial Bus Specification Version 1.1* defines an endpoint as a source or sink of data. Since USB is a serial bus, a device endpoint is actually a FIFO which sequentially empties/fills with USB bytes. The host selects a device endpoint by sending a 4-bit address and one direction bit. Therefore, USB can uniquely address 32 endpoints, IN0 through IN15 and OUT0 through OUT15.

From the EZ-USB point of view, an endpoint is a buffer full of bytes received or to be transmitted over the bus. The 8051 reads endpoint data from an OUT buffer, and writes endpoint data for transmission over USB to an IN buffer.

Four USB endpoint types are defined as: Bulk, Control, Interrupt, and Isochronous.

1.13.1 EZ-USB Bulk Endpoints

Bulk endpoints are unidirectional—one endpoint address per direction. Therefore endpoint 2-IN is addressed differently than endpoint 2-OUT. Bulk endpoints use maximum packet sizes (and therefore buffer sizes) of 8, 16, 32, or 64 bytes. EZ-USB provides fourteen bulk endpoints, divided into seven IN endpoints (endpoint 1-IN through 7-IN), and seven OUT endpoints (endpoint 1-OUT through 7-OUT). Each of the fourteen endpoints has a 64-byte buffer.

Bulk data is available to the 8051 in RAM form, or as FIFO data using a special EZ-USB *Autopointer* (Chapter 6, "EZ-USB Bulk Transfers").

1.13.2 EZ-USB Control Endpoint Zero

Control endpoints transfer mission-critical control information to and from the USB device. The *Universal Serial Bus Specification Version 1.1* requires every USB device to have a default CONTROL endpoint, endpoint zero. Device enumeration, the process that the host initiates when the device is first plugged in, is conducted over endpoint zero. The host sends all USB requests over endpoint zero.

Control endpoints are bi-directional; if you have an endpoint 0 IN CONTROL endpoint, you automatically have an endpoint 0 OUT endpoint. Control endpoints alone accept SETUP PIDs.

A CONTROL transfer consists of a two or three stage sequence:

- SETUP
- DATA (If needed)
- HANDSHAKE

Eight bytes of data in the SETUP portion of the CONTROL transfer have special USB significance, as defined in the *Universal Serial Bus Specification Version 1.1, "Chapter 9."* A USB device must respond properly to the requests described in this chapter to pass USB compliance testing (usually referred to as the USB "Chapter Nine Test").

Endpoint zero is the only CONTROL endpoint in the EZ-USB chip. The 8051 responds to device requests issued by the host over endpoint zero. The EZ-USB core is significantly enhanced to simplify the 8051 code required to service these requests. Chapter 7, "EZ-USB Endpoint Zero" provides a detailed roadmap for writing USB Chapter 9 compliant 8051 code.

1.13.3 EZ-USB Interrupt Endpoints

Interrupt endpoints are almost identical to bulk endpoints. Fourteen EZ-USB endpoints (EP1-EP7, IN, and OUT) may be used as interrupt endpoints. Interrupt endpoints have maximum packet sizes up to 64, and contain a “polling interval” byte in their descriptor to tell the host how often to service them. The 8051 transfers data over interrupt endpoints in exactly the same way as for bulk endpoints. Interrupt endpoints are described in Chapter 6, "EZ-USB Bulk Transfers."

1.13.4 EZ-USB Isochronous Endpoints

Isochronous endpoints deliver high bandwidth, time critical data over USB. Isochronous endpoints are used to stream data to devices such as audio DACs, and from devices such as cameras and scanners. Time of delivery is the most critical requirement, and isochronous endpoints are tailored to this requirement. Once a device has been granted an isochronous bandwidth slot by the host, it is guaranteed to be able to send or receive its data every frame.

EZ-USB contains 16 isochronous endpoints, numbered 8-15 (8IN-15IN, and 8OUT-15OUT). 1,024 bytes of FIFO memory are available to the 16 endpoints, and may be FIFO memory to provide double-buffering. Using double buffering, the 8051 reads OUT data from isochronous endpoint FIFOs containing data from the previous frame while the host writes current frame data into the other buffer. Similarly, the 8051 loads IN data into isochronous endpoint FIFOs that will be transmitted over USB during the next frame while the host reads current frame data from the other buffer. At every SOF the USB FIFOs and 8051 FIFOs switch, or *ping-pong*.

Isochronous transfers are described in Chapter 8, "EZ-USB Isochronous Transfers."

1.14 Fast Transfer Modes

The following versions of the EZ-USB have a fast transfer mode: AN2125SC, AN2126SC, AN2135SC, AN2136SC, and AN2131QC, that is, those versions that have a data bus (see Table 1-2). The fast transfer mode minimizes the transfer time from EZ-USB core also supplies external FIFO read and write strobes to synchronize the transfers.

Using the fast transfer mode, the 8051 transfers a byte of data between an internal FIFO and the external bus using a single 8051 MOVX instruction, which takes two cycles or 333 ns. Both Isochronous and Bulk endpoints can use this fast transfer mode.

1.15 Interrupts

The EZ-USB enhanced 8051 adds seven interrupt sources to the standard 8051 interrupt system. Three of the added interrupts are used internally, and the others are available on device pins. INT2 is used for all USB interrupts. INT3 is used by the I^2C interface. A third interrupt is used for remote wakeup indication.

The EZ-USB core automatically supplies jump vectors (Autovectors) for its USB interrupts to save the 8051 from having to test bits to determine the source of the interrupt. Each BULK/CONTROL/INTERRUPT endpoint has its own vector, so when an endpoint requires service, the proper interrupt service routine is automatically invoked. The 8051 services all isochronous endpoints in response to a SOF (Start Of Frame) interrupt request. Chapter 9, "EZ-USB Interrupts" describes the EZ-USB interrupt system.

1.16 Reset and Power Management

The EZ-USB chip contains four resets:

- Power-On-Reset (POR)
- USB bus reset
- 8051 reset
- USB Disconnect/Re-connect

The functions of the various EZ-USB resets are described in Chapter 10, "EZ-USB Resets."

A USB peripheral may be put into a low power state when the host signals a *suspend* operation. The *Universal Serial Bus Specification Version 1.1* states that a bus powered device cannot draw more than 500 *u*A of current from the Vcc wire while in suspend. The EZ-USB chip contains logic to turn off its internal oscillator and enter a *sleep* state. A special interrupt, triggered by a wakeup pin or wakeup signaling on the USB bus, starts the oscillator and interrupts the 8051 to resume operation.

Low power operation is described in Chapter 11, "EZ-USB Power Management."

1.17 EZ-USB Product Family

The EZ-USB family is available in various pinouts to serve different system requirements and costs. Table 1-2 shows the feature set for each member of the EZ-USB Series 2100 Family.

Table 1-2. EZ-USB Series 2100 Family

Part Number	RAM Size	Key Features					Package	Max UART (Async) Speed (Kbaud)	Power Saving Option	IBN/ STOP
		ISO Support	Endpoints	Data Bus or Port B	I/O Rate Bytes/s Max	Prog I/Os				
AN2121S	4KB	Y	32	Port B	600K	16	S = 44 PQFP	115.2	N	N
AN2122S	4KB	N	13	Port B	600K	16	S = 44 PQFP	230.4	N	Y
AN2122T	4KB	N	13	Port B	600K	19	T = 48 TQFP	230.4	Y	Y
AN2125S	4KB	Y	32	Data Bus	2M	8	S = 44 PQFP	115.2	N	N
AN2126S	4KB	N	13	Data Bus	2M	8	S = 44 PQFP	230.4	N	Y
AN2126T	4KB	N	13	Data Bus	2M	11	T = 48 TQFP	230.4	Y	Y
AN2131Q	8KB	Y	32	Both	2M	24	Q = 80 PQFP	115.2	N	N
AN2131S	8KB	Y	32	Port B	600K	16	S = 44 PQFP	115.2	N	N
AN2135S	8KB	Y	32	Data Bus	2M	8	S = 44 PQFP	115.2	N	N
AN2136S	8KB	N	16	Data Bus	2M	8	S = 44 PQFP	115.2	N	N

1.18 Summary of AN2122, AN2126 Features

This section summarizes the features of the AN2122 and AN2126 packages. These features are not available in the other packages of the EZ-USB family.

Power Saving Option

To reduce power, the 8051 processor can be run at half speed. When the CPU12MHZ pin is tied high, the 8051 processor core runs at 12 MHz. When tied low, the 8051 runs at the normal 24 MHz. The logic state of this pin should never be changed while the 8051 is running.

230 Kbaud UART Operation

Two control bits in a register, UART230, allow 230-Kbaud operation by UART0 and UART1 (see Section 12.8, "230-Kbaud UART Operation - AN2122, AN2126").

48-pin Variants

There are two 48-pin devices:

AN2122T
AN2126T

The four extra pins are used as follows:

- PA7, PA6, and PA0 are GPIO pins. This makes five of the eight PORTA pins available (all except PA1-PA3).
- CPU12MHZ - This input controls the speed of the 8051:
  - tied high 12 MHz
  - tied low 24 MHz

Bulk Endpoints

The AN2122 and AN2126 have a reduced set of thirteen bulk endpoints (see Section 6.1, "Introduction").

Interrupts

The AN2122 and AN2126 contain two interrupts not present in the other AN21xx family members.

- An IBN (In-Bulk NAK) interrupt request activates when an IN packet is NAKd by the SIE because the 8051 has not loaded the buffer (and byte count register) for an IN endpoint. This is useful for applications that need to know when the host is *pinging* an IN endpoint (see Section 9.13, "In Bulk NAK Interrupt - (AN2122/ AN2126 only)").
- An I^2C interrupt source is added to the I^2C interrupt (INT3), indicating that transmission of a STOP bit is complete (see Section 9.14, "I^2C STOP Complete Interrupt - (AN2122/AN2126 only)").

1.19 Revision ID

The Revision ID for each part is shown in Table 1.2. The revision value is reported in the internal DID (Device ID), which is the value read by the host during enumeration if no EEPROM is connected to the I^2C bus. This value also appears in the CPUCS register bits.

1.20 Pin Descriptions

Figures 1-9 through 1-13 are pin descriptions by package type. Table 1-3 describes the pins by pin function.

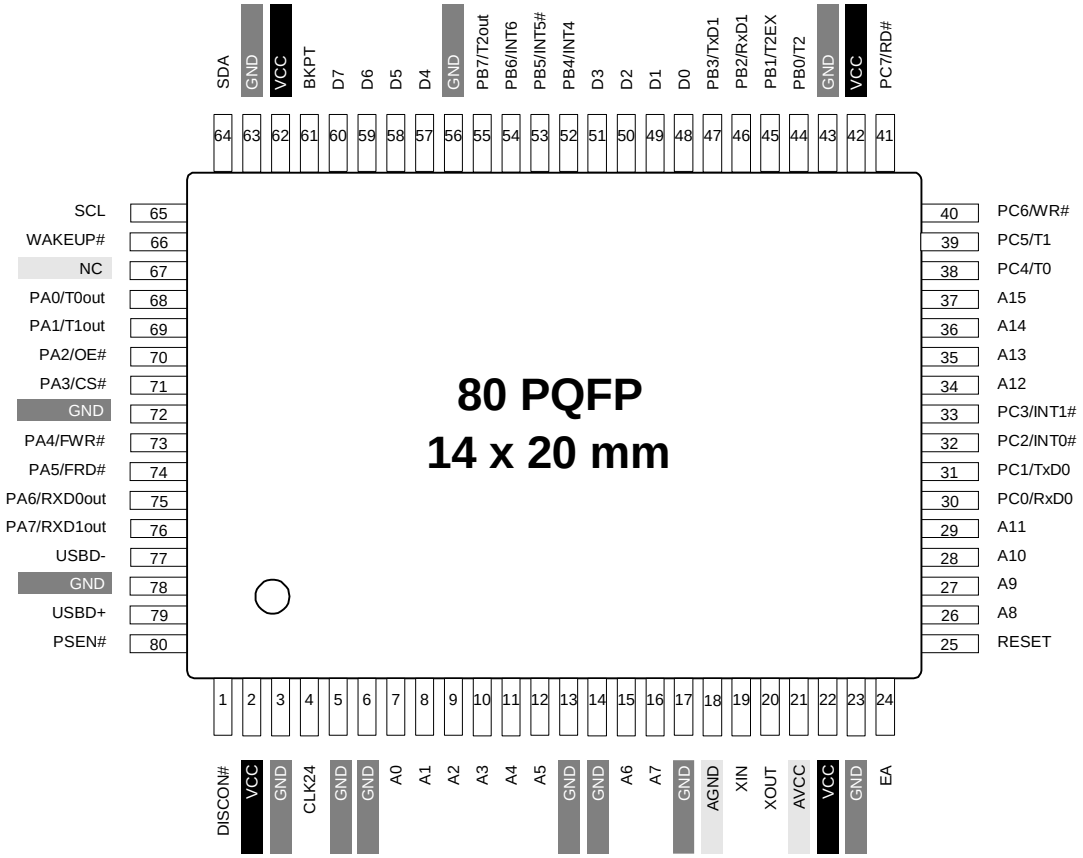


Figure 1-9. 80-pin PQFP Package (AN2131Q)

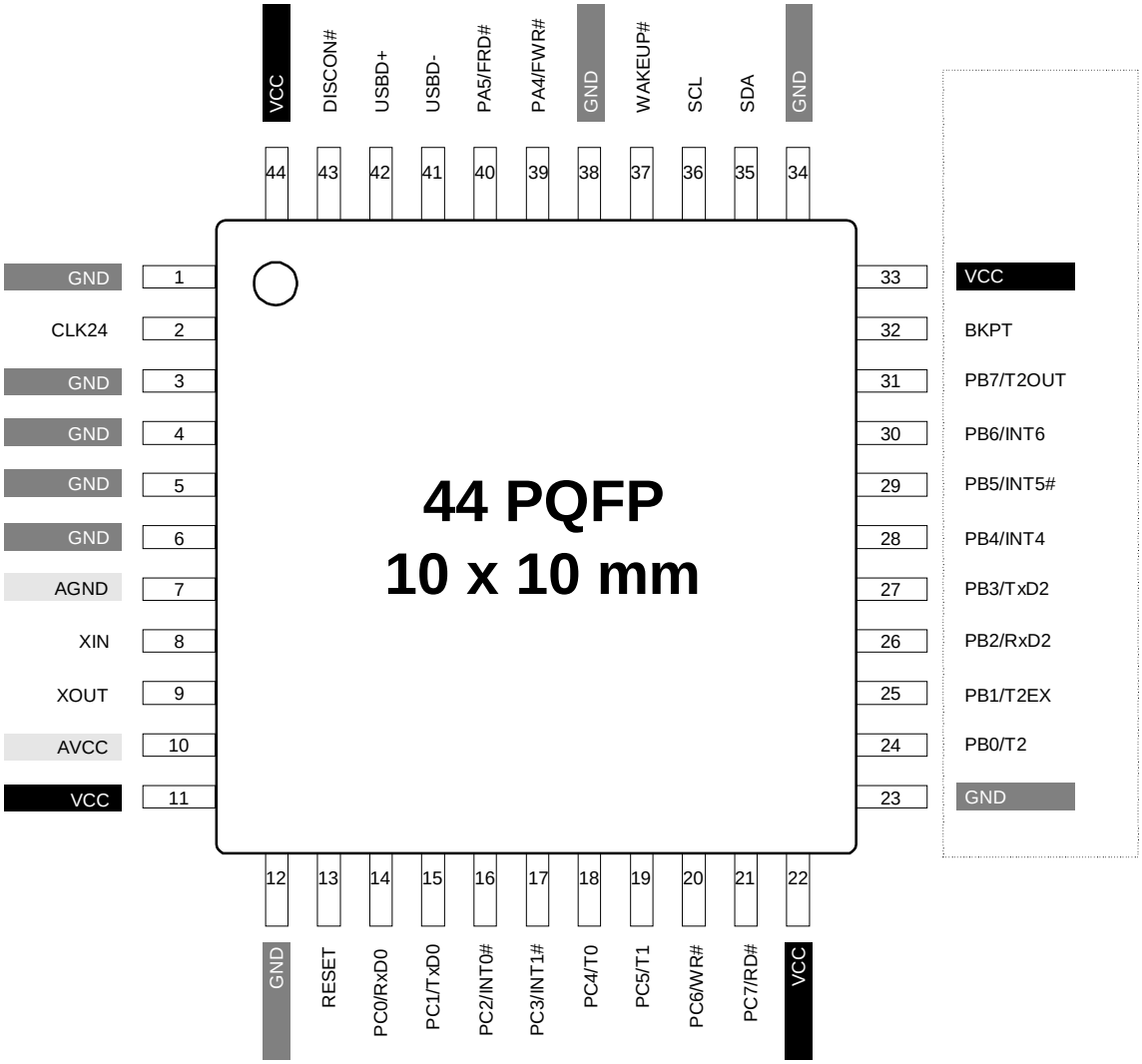


Figure 1-10. 44-pin PQFP Package with Port B (AN2121S, AN2122S, and AN2131S)

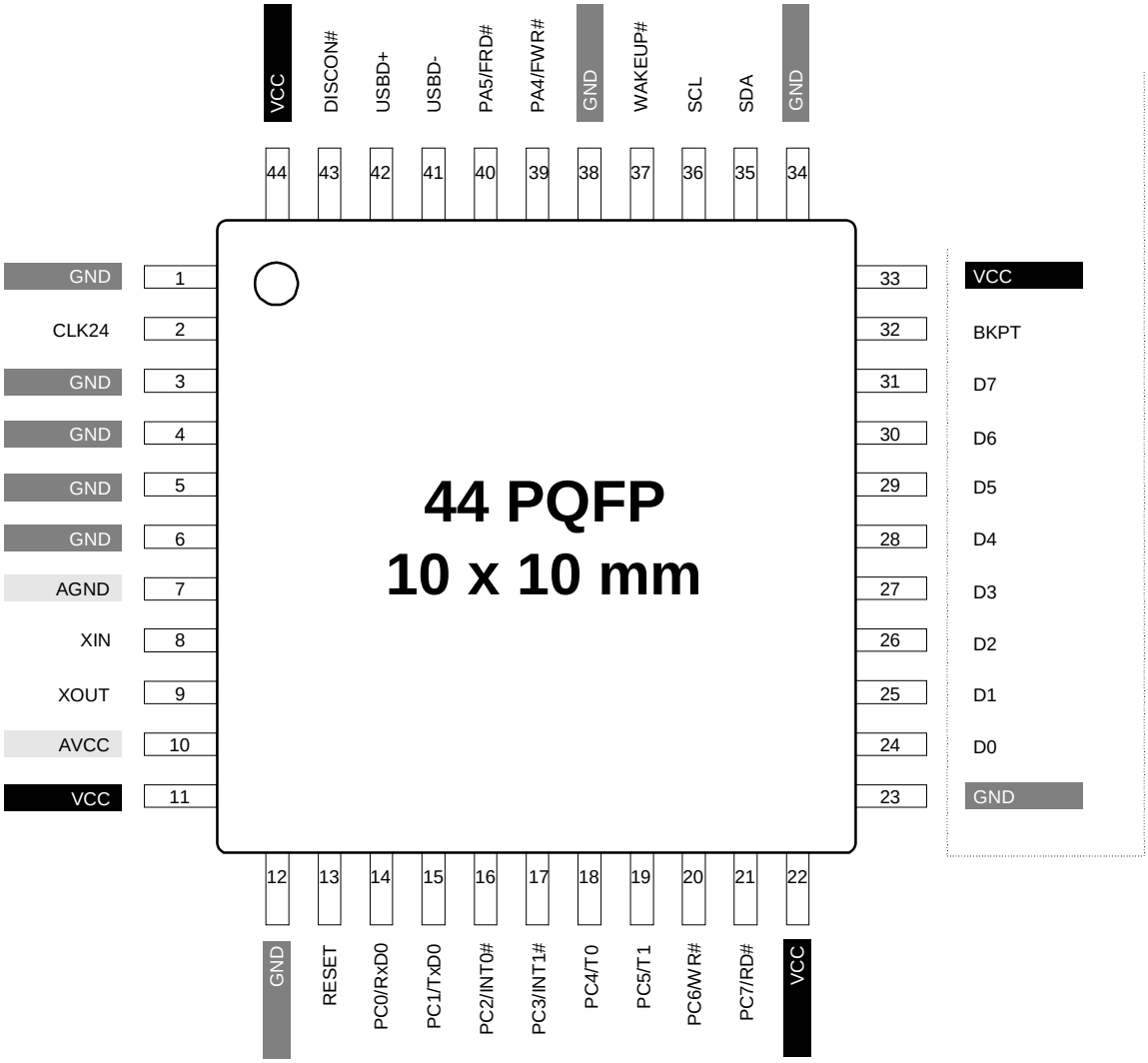


Figure 1-11. 44-pin Package with Data Bus (AN2125S, AN2126S, AN2135S, and AN2136)

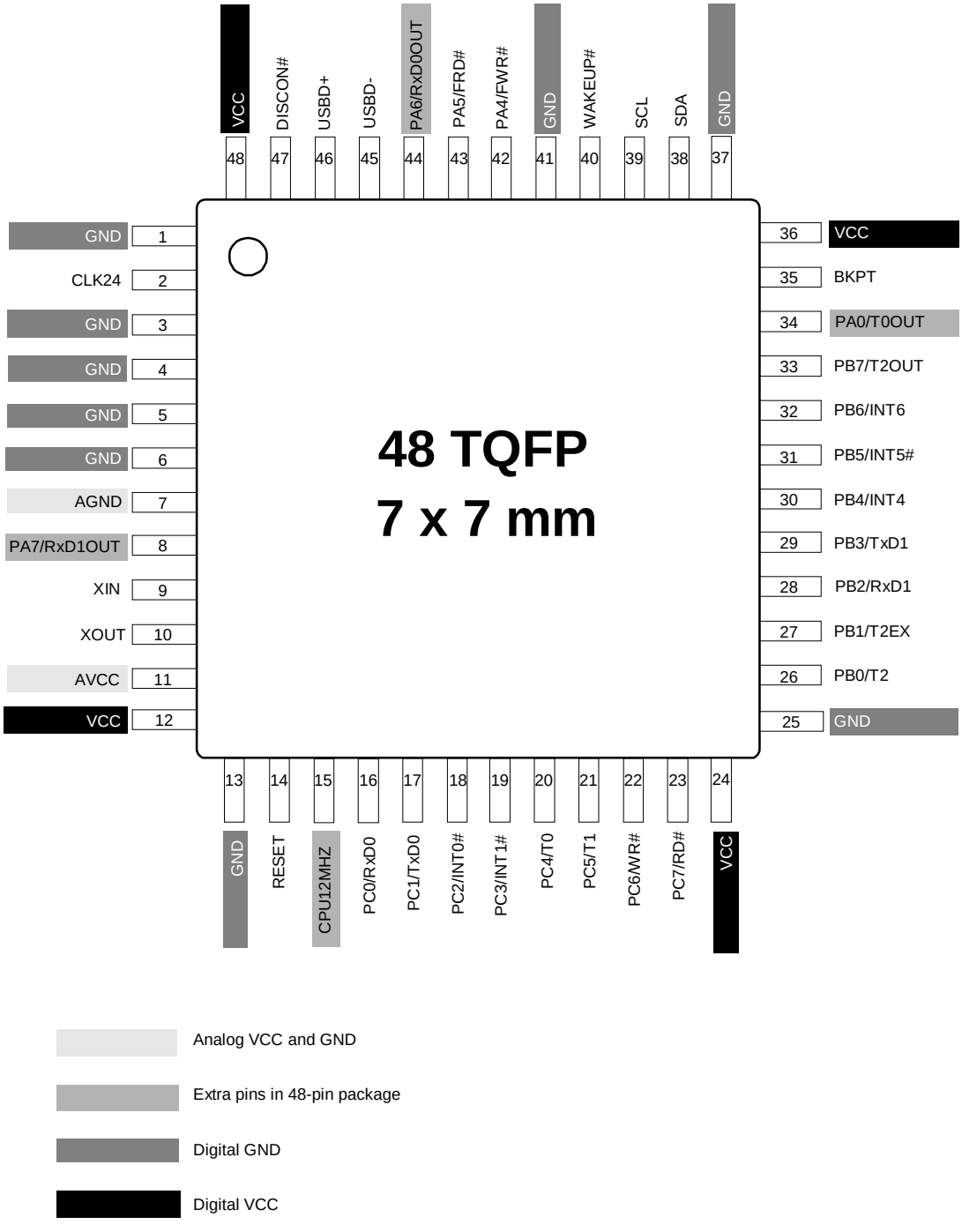


Figure 1-12. 48-pin TQFP Package (AN2122T)

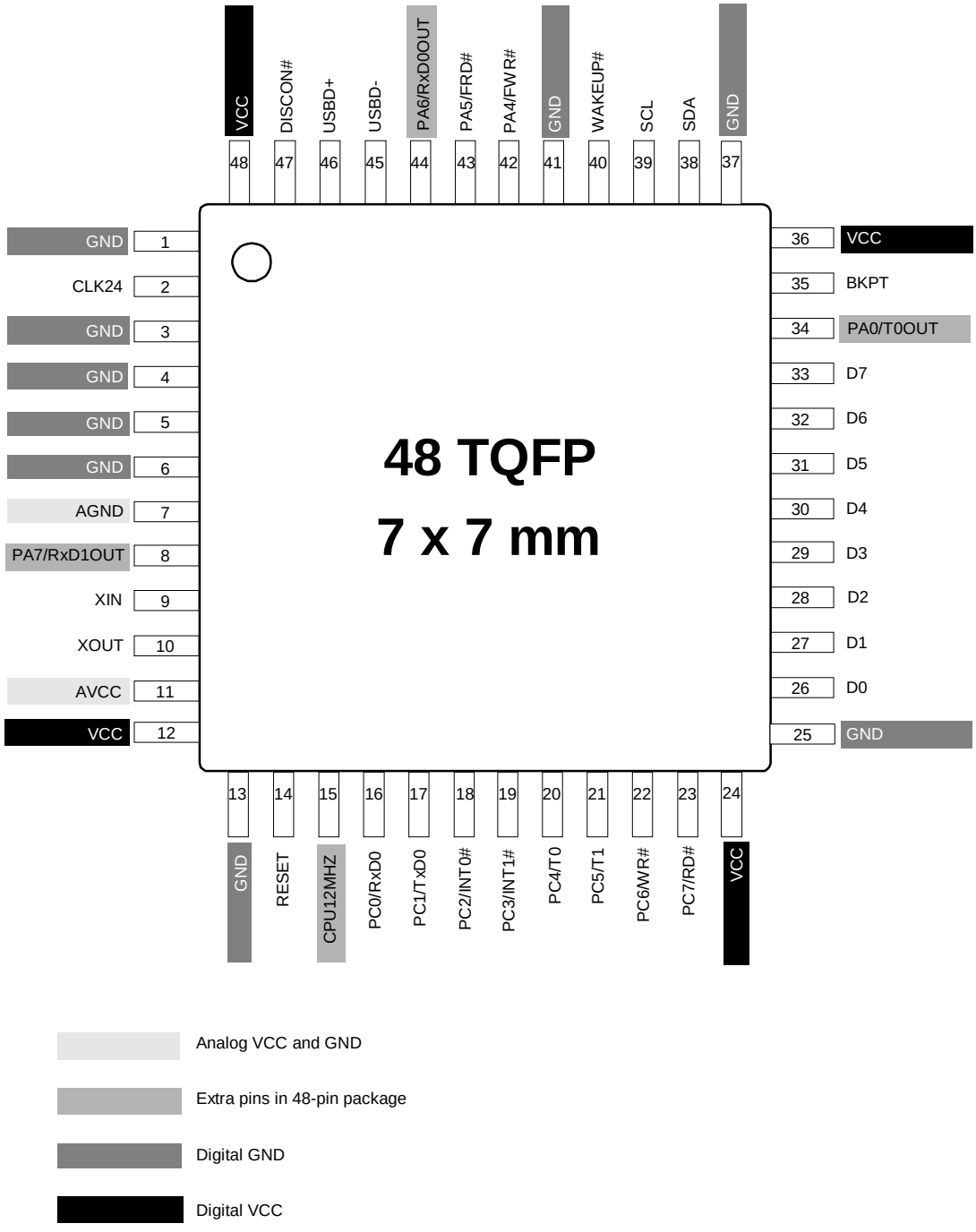


Figure 1-13. 48-pin TQFP Package (AN2126T)

Table 1-3. EZ-USB Series 2100 Pinouts by Pin Function

2131Q	2121S 2122S 2131S	2125S 2126S 2135S 2136S	2122T	2126T	Name	Type	Default	Description
21	10	10	11	11	AVCC	Power	N/A	**Analog Vcc**. This signal provides power to the analog section of the chip.
18	7	7	7	7	AGND	Power	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
1	43	43	47	47	DISCON#	Output	HI	**Disconnect**. This pin is controlled by two bits, DISCOE and DISCON. When DISCOE=0, the pin floats. When DISCOE=1, it drives. When DISCOE=1, the driven logic level is the inverse of the DISCON bit.
77	41	41	45	45	USBD	I/O/Z	Z	**USB D- signal**. Connect to the USB D- signal through a 24-ohm resistor.
79	42	42	46	46	USBD	I/O/Z	Z	**USB D+ signal**. Connect to the USB D+ pin through a 24-ohm resistor.
7-12, 15, 16, 26-29, 34-37	N/A	N/A	N/A	N/A	A0-A5, A6, A7, A8-A11, A12-A15	Output	0x0000	**8051 Address bus**. This bus is driven at all times. When the 8051 is addressing internal RAM it reflects the internal address.
48-51, 57-60	N/A	24-27, 28-31	N/A	26-29, 30-33	D0-D3, D4-D7	I/O/Z	Z	**8051 Data bus**. This bi-directional bus is high-impedance when inactive, input for bus reads, and output for bus writes. The data bus is also used to transfer data directly to and from internal EZ-USB FIFOs under control of the FRD# and FWR# strobes. D0-D7 are active only for external bus accesses, and are driven low in suspend.
80	N/A	N/A	N/A	N/A	PSEN#	Output	H	**Program Store Enable**. This active-low signal indicates a code fetch from external memory. It is active for program memory fetches above 0x1B40 when the EA pin is LO, or above 0x0000 when the EA pin is HI.
61	32	32	35	35	BKPT	Output	0	**Breakpoint**. This pin goes active (high) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the USBBAV register (BPEN=1). If the BPPULSE bit in the USBBAV register is HI, this signal pulses high for eight 24-MHz clocks. If the BPPULSE bit is LO, the signal remains high until the 8051 clears the BREAK bit (by writing 1 to it) in the USBBAV register.
25	13	13	14	14	RESET	Input	N/A	**Active High Reset**. Resets the 8051 and the USB SIE. This pin is normally tied to ground through a 10K-ohm resistor and to Vcc through a 1 µF capacitor.

Table 1-3. EZ-USB Series 2100 Pinouts by Pin Function

2131Q	2121S 2122S 2131S	2125S 2126S 2135S 2136S	2122T	2126T	Name	Type	Default	Description
24	N/A	N/A	N/A	N/A	EA	Input	N/A	**External Access**. If this signal is active (high), the 8051 fetches code from external memory instead of the internal program RAM. If EA=0, the 8051 fetches code from external memory starting at 0x1B40 (AN2131).
19	8	8	9	9	XIN	Input	N/A	**Crystal Input**. Connect this signal to a 12-MHz series resonant, fundamental mode crystal and 22-33-pF capacitor to GND. This pin may also be driven by a 12-MHz clock.
20	9	9	10	10	XOUT	Output	N/A	**Crystal Output.** Connect this signal to a 12-MHz series resonant, fundamental mode crystal and 22-33-pF capacitor to GND. If XIN is driven by a 12-MHz clock, this pin should not be connected.
68	N/A	N/A	34	34	PA0 or T0OUT	I/O	I (PA0)	Multiplexed pin whose function is selected by the T0OUT bit of the PORTACFG register. If T0OUT=0, the pin is the bi-directional I/O port bit PA0. If T0OUT=1, the pin is the active-high T0OUT signal from 8051 Timer/Counter0. T0OUT outputs a high level for one CLK24 clock cycle when Timer0 overflows. If Timer0 is operated in mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
69	N/A	N/A	N/A	N/A	PA1 or T1OUT	I/O	I (PA1)	Multiplexed pin whose function is selected by the T1OUT bit of the PORTACFG register. If T1OUT=0, the pin is the bi-directional I/O port bit PA1. If T1OUT=1, the pin is the active-high T1OUT signal from 8051 Timer-counter1 T1OUT outputs a high level for one CLK24 clock cycle when Timer1 overflows. If Timer1 is operated in mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.
70	N/A	N/A	N/A	N/A	PA2 or OE#	I/O	I (PA2)	Multiplexed pin whose function is selected by the OE bit of the PORTACFG register. If OE=0, the pin is the bi-directional I/O port pin PA2. If OE=1, the pin is an active-low output enable for external memory. If the OE# pin is used, it should be externally pulled up to Vcc to ensure that the write strobe is inactive (high) at power-on.

Table 1-3. EZ-USB Series 2100 Pinouts by Pin Function

2131Q	2121S 2122S 2131S	2125S 2126S 2135S 2136S	2122T	2126T	Name	Type	Default	Description
71	N/A	N/A	N/A	N/A	PA3 or CS#	I/O	I (PA3)	Multiplexed pin whose function is selected by the CS bit of the PORTACFG register. If CS=0, the pin is the bi-directional I/O port pin PA3. If CS=1, the pin is an active-low chip select for external memory. If the CS# pin is used, it should be externally pulled up to Vcc to ensure that the write strobe is inactive (high) at power-on.
73	39	39	N/A	N/A	PA4 or FWR#	I/O	I (PA4)	Multiplexed pin whose function is selected by the FWR (Fast Write) bit of the PORTAFCG register. If FWR=0, the pin is the bi-directional I/O port pin PA4. If FWR=1, the pin is the write strobe for an external FIFO. If the FWR# pin is used, it should be externally pulled up to Vcc to ensure that the write strobe is inactive (high) at power-on.
74	40	40	N/A	N/A	PA5 or FRD#	I/O	I (PA5)	Multiplexed pin whose function is selected by the FRD (Fast Read) bit of the PORTAFCG register. If FRD=0, the pin is the bi-directional I/O port pin PA5. If FRD=1, the pin is the read strobe for an external FIFO. If the FRD# pin is used, it should be externally pulled up to Vcc to ensure that the write strobe is inactive (high) at power-on.
75	N/A	N/A	44	44	PA6 or RXD0OUT	I/O	I (PA6)	Multiplexed pin whose function is selected by the RXD0OUT bit of the PORTAFCG register. If RXD0OUT=0 (default), the pin is the bi-directional I/O port bit PA6. If RXD0OUT=1, the pin is the active-high RXD0OUT signal from 8051 UART0. If RXD0OUT is selected and UART0 is in mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise, it is a 1.
76	N/A	N/A	8	8	PA7 OR RXD1OUT	I/O	I (PA7)	Multiplexed pin whose function is selected by the RXD1OUT bit of the PORTAFCG register. If RXD1OUT=0 (default), the pin is the bi-directional I/O port bit PA7. If RXD1OUT=1, the pin is the active-high RXD1OUT signal from 8051 UART1. When RXD1OUT is selected and UART1 is in mode 0, this pin provides the output data for UaRT1 only when it is in sync mode. In modes 1, 2, and 3, this pin is a 1.

Table 1-3. EZ-USB Series 2100 Pinouts by Pin Function

2131Q	2121S 2122S 2131S	2125S 2126S 2135S 2136S	2122T	2126T	Name	Type	Default	Description
44	24	N/A	26	N/A	PB0 or T2	I/O	I (PB0)	Multiplexed pin whose function is selected by the T2 bit of the PORTBFCG register. If T2=0, the pin is the bi-directional I/O port bit PB0. If T2=1, the pin is the active-high T2 signal from 8051 Timer2, which provides the input to Timer2 when C/T2=1. When C/T2=0, Timer2 does not use this pin.
45	25	N/A	27	N/A	PB1 or T2EX	I/O	I (PB1)	Multiplexed pin whose function is selected by the T2EX bit of the PORTBCFG register. If T2EX=0, the pin is the bi-directional I/O port bit PB1. If T2EX=1, the pin is the active-high T2EX signal from 8051 Timer2.
46	26	N/A	28	N/A	PB2 or RXD1	I/O	I (P{B2)	Multiplexed pin whose function is selected by the RXD1 bit of the PORTBCFG register. If RXD1=0, the pin is the bi-directional I/O port bit PB2. If RXD1=1, the pin is the active-high RXD1 input signal for 8051 UART1, which provides data to the UART in all modes.
47	27	N/A	29	N/A	PB3 or TXD1	I/O	I (PB3)	Multiplexed pin whose function is selected by the TXD1 bit of the PORTBCFG register. If TXD1=0, the pin is the bi-directional I/O port bit PB3. If TXD1=1, the pin is the active-high TXD1 output pin for 8051 UART1 which provides the output clock in sync mode and the output data in async mode.
52	28	N/A	30	N/A	PB4 or INT4	I/O	I (PB4)	Multiplexed pin whose function is selected by the INT4 bit of the PORTBCFG register. If INT4=0, the pin is the bi-directional I/O port bit PB4. If INT4=1, the pin is the 8051 INT4 interrupt request signal. The INT4 pin is edge-sensitive, active high.
53	29	N/A	31	N/A	PB5 or INT5#	I/O	I (PB5)	Multiplexed pin whose function is selected by the INT5 bit of the PORTBCFG register. If INT5=0, the pin is the bi-directional I/O port bit PB5. If INT5=1, the pin is the INT5# interrupt register signal. The INT5# pin is edge-sensitive, active low.
54	30	N/A	32	N/A	PB6 or INT6	I/O	I (PB6)	Multiplexed pin whose function is selected by the INT6 bit of the PORTBCFG register. If INT6=0, the pin is the bi-directional I/O port bit PB6. If INT6=1, the pin is the INT6 interrupt request signal. The INT6 pin is edge-sensitive, active high.

Table 1-3. EZ-USB Series 2100 Pinouts by Pin Function

2131Q	2121S 2122S 2131S	2125S 2126S 2135S 2136S	2122T	2126T	Name	Type	Default	Description
55	31	N/A	33	N/A	PB7 or T2OUT	I/O	I (PB7)	Multiplexed pin whose function is selected by the T2OUT bit of the PORTBCFG register. If T2OUT=0, the pin is the bi-directional I/O port bit PB7. If T2OUT=1, the pin is the active-high T2OUT signal from 8051 Timer2. T2OUT is active (high) for one clock cycle when Timer/Counter 2 overflows.
30	14	14	16	16	PC0 or RXD0	I/O	I (PC0)	Multiplexed pin whose function is selected by the RXD0 bit of the PORTCCFG register. If RXD0=0, the pin is the bi-directional I/O port bit PC0. If RXD0=1, the pin is the active-high RXD0 from 8051 UART0, which provides data to the UART in all modes.
31	15	15	17	17	PC1 or TXD0	I/O	I (PC1)	Multiplexed pin whose function is selected by the TXD0 bit of the PORTCCFG register. If TXD0=0, the pin is the bi-directional I/O port bit PC1. If TXD0=1, the pin is the active-high TXD0 signal for 8051 UART0, which provides the output clock in sync mode, and the output data in async mode.
32	16	16	18	18	PC2 or INT0#	I/O	I (PC2)	Multiplexed pin whose function is selected by the INT0 bit of the PORTCCFG register. If INT0=0, the pin is the bi-directional I/O port bit PC2. If INT0=1, the pin is the active-low 8051 INT0 interrupt input signal, which is either edge triggered (IT0=1) or level triggered (IT0=0).
33	17	17	19	19	PC3 or INT1#	I/O	I (PC3)	Multiplexed pin whose function is selected by the INT1 bit of the PORTCCFG register. If INT1=0, the pin is the bi-directional I/O port bit PC3. If INT1=1, the pin is the active-low 8051 INT1 interrupt input signal, which is either edge triggered (IT1=1) or level triggered (IT1=0).
38	18	18	20	20	PC4 or T0	I/O	I (PC4)	Multiplexed pin whose function is selected by the T0 bit of the PORTCCFG register. If T0=0, the pin is the bi-directional I/O port bit PC4. If T0=1, the pin is the active-high T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit.
39	19	19	21	21	PC5 or T1	I/O	I (PC5)	Multiplexed pin whose function is selected by the T1 bit of the PORTCCFG register. If T1=0, the pin is the bi-directional I/O port bit PC5. If T1=1, the pin is the active-high T1 signal from 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T0 is 0, Timer1 does not use this bit.

Table 1-3. EZ-USB Series 2100 Pinouts by Pin Function

2131Q	2121S 2122S 2131S	2125S 2126S 2135S 2136S	2122T	2126T	Name	Type	Default	Description
40	20	20	22	22	PC6 or WR#	I/O	I (PC6)	Multiplexed pin whose function is selected by the WR bit of the PORTCCFG register. If WR=0, the pin is the bi-directional I/O port bit PC6. If WR=1, the pin is the active-low write signal for external memory. If the WR# signal is used, it should be externally pulled up to Vcc to ensure that the write strobe is inactive at power-on.
41	21	21	23	23	PC7 or RD#	I/O	I (PC7)	Multiplexed pin whose function is selected by the RD bit of the PORTCCFG register. If RD#=0, the pin is the bi-directional I/O port bit PC7. If RD#=1, the pin is the active-low read signal for external memory. If the RD# signal is used, it should be externally pulled up to Vcc to ensure that the read strobe is inactive at power-on.
4	2	2	2	2	CLK24	Output		**24-MHz clock**, phase locked to the 12-MHz input clock. It operates at 12 MHz in 12-MHz mode (48-pin package). Output is disabled by setting the OUTCLKEN bit = 0 in the CPUCS register.
66	37	37	40	40	WAKEUP#	Input	N/A	**USB Wakeup**. If the 8051 is in suspend, a high to low edge on this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Holding WAKEUP# LOW inhibits the EZ-USB chip from entering the suspend state.
65	36	36	39	39	SCL	OD	Z	**I^2C Clock**. Pull up to Vcc with a 2.2K-ohm resistor, even if no I^2C device is connected.
64	35	35	38	38	SDA	OD	Z	**I^2C Data**. Connect to Vcc with a 2.2K-ohm resistor even if no I^2C device is connected.
2, 22, 42, 62	11, 22, 33, 44	11, 22, 33, 44	12, 24, 36, 48	12, 24, 36, 48	Vcc		N/A	**Vcc**. 3.3V power source.
3, 5, 6, 13, 14, 17, 23, 43, 56, 63, 72, 78	1, 3, 4, 5, 6, 12, 23, 34, 38	1, 3, 4, 5, 6, 12, 23, 34, 38	1, 3, 4, 5, 6, 13, 25, 37, 41	1, 3, 4, 5, 6, 13, 25, 37, 41	GND		N/A	Ground. Note: On the 80-pin package, pins 5, 6, 13, 14, and 72 are test pins that must be grounded for normal operation. Driving pin 72 high floats all functional pins for automated board test. The corresponding pins on the 44-pin package are pins 3, 4, 5, 6, and 38. Driving pin 38 high floats all functional pins for automated board test. The corresponding pins on the 48-pin package are pins 3, 4, 5, 6, and 41. Driving pin 41 high floats all functional pins for automated board testing.
N/A	N/A	N/A	15	15	CPU12MHZ		N/A	This input controls the speed of the 8051: - Tied High - 12 MHz - Tied Low - 24 MHz
67	N/A	N/A	N/A	N/A	NC		N/A	This pin must be left unconnected.

2 EZ-USB CPU

2.1 Introduction

The EZ-USB built-in microprocessor, an enhanced 8051 core, is fully described in Appendices A-C. This chapter introduces the processor, its interface to the EZ-USB core, and describes architectural differences from a standard 8051.

2.2 8051 Enhancements

The enhanced 8051 core uses the standard 8051 instruction set. Instructions execute faster than with the standard 8051 due to two features:

- Wasted bus cycles are eliminated. A bus cycle uses four clocks, as compared to 12 clocks with the standard 8051.
- The 8051 runs at 24 MHz.

In addition to the speed improvement, the enhanced 8051 core also includes architectural enhancements:

1. A second data pointer.
2. A second UART.
3. A third, 16-bit timer (TIMER2).
4. A high-speed memory interface with a non-multiplexed 16-bit address bus.
5. Eight additional interrupts (INT2-INT5, PFI, T2, and UART1).
6. Variable MOVX timing to accommodate fast/slow RAM peripherals.
7. 3.3V operation.

2.3 EZ-USB Enhancements

The EZ-USB chip provides additional enhancements outside the 8051. These include:

- Fast external transfers (Autopointer, Fast Transfer Mode)
- Vectored USB interrupts (Autovector)
- Separate buffers for SETUP and DATA portions of a CONTROL transfer.
- Breakpoint Facility.

2.4 EZ-USB Register Interface

The 8051 communicates with the EZ-USB core through a set of memory mapped registers. These registers are grouped as follows:

- Endpoint buffers and FIFOs
- 8051 control
- IO ports
- Fast Transfer
- I^2C Controller
- Interrupts
- USB Functions

These registers and their functions are described throughout this manual. A full description of every register and bit appears in Chapter 12, “EZ-USB Registers.”

2.5 EZ-USB Internal RAM

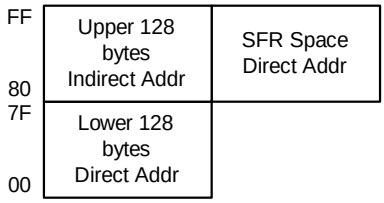


Figure 2-1. 8051 Registers

Like the standard 8051, the EZ-USB 8051 core contains 128 bytes of register RAM at 00-7F, and a partially populated SFR register space at 80-FF. An additional 128 indirectly addressed registers (sometimes called “IDATA”) are also available at 80-FF.

All internal EZ-USB RAM, which includes program/data memory, bulk endpoint buffer memory, and the EZ-USB register set, is addressed as *add-on* 8051 memory. The 8051 reads or writes these bytes as data using the MOVX (move external) instruction. Even though the MOVX instruction implies external memory, the EZ-USB RAM and register set is actually inside the EZ-USB chip. External memory attached to the AN2131Q address and data busses can also be accessed by the MOVX instruction. The EZ-USB core encodes its memory strobe and select signals (RD#, WR#, CS#, and OE#) to eliminate the need for external logic to separate the internal and external memory spaces.

2.6 I/O Ports

A standard 8051 communicates with its IO ports 0-3 through four Special Function Registers (SFRs). Standard 8051 IO pins are *quasi-bidirectional* with weak pullups that briefly drive high only when the pin makes a zero-to-one transition.

The EZ-USB core implements IO ports differently than a standard 8051, as described in Chapter 4, "EZ-USB Input/Output." Instead of using the 8051 IO ports and SFRs, the EZ-USB core implements a flexible IO system that is controlled *via* EZ-USB register set. Each EZ-USB IO pin functions identically, having the following resources:

- An output latch. Used when the pin is an output port.
- A bit that indicates the state of the IO pin, regardless of its configuration (input or output).

- An output enable bit that causes the IO pin to be driven from the output latch.
- An alternate function bit that determines whether the pin is general IO or a special 8051 or EZ-USB function.

The SFRs associated with 8051 ports 0-3 are not implemented in EZ-USB. These SFR addresses include P0 (0x80), P1 (0x90), P2 (0xA0), and P3 (0xB0). Because P2 is not implemented, the MOVX@R0/R1 instruction takes the upper address byte from an added Special Function Register (SFR) at location 0x92. This register is called “MPAGE” in the Appendices.

2.7 Interrupts

All standard 8051 interrupts are supported in the enhanced 8051 core. Table 2-1 shows the existing and added 8051 interrupts, and indicates how the added ones are used.

Table 2-1. EZ-USB Interrupts

Standard 8051 Interrupts	Enhanced 8051 Interrupts	Used As
INT0		Device Pin INT0#
INT1		Device Pin INT1#
Timer 0		Internal, Timer 0
Timer 1		Internal, Timer 1
Tx0 & Rx0		Internal, UART0
	INT2	Internal, USB
	INT3	Internal, I²C Controller
	INT4	Device Pin, PB4/INT4
	INT5	Device Pin, PB5/INT5#
	INT6	Device Pin, PB6/INT6
	PF1	Device Pin, USB WAKEUP#
	Tx1 & Rx1	Internal, UART1
	Timer 2	Internal, Timer 2

The EZ-USB chip uses 8051 INT2 for 21 different USB interrupts: 16 bulk endpoints plus SOF, Suspend, SETUP Data, SETUP Token, and USB Bus Reset. To help the 8051 determine which interrupt is active, the EZ-USB core provides a feature called Autovectoring. The core inserts an address byte into the low byte of the 3-byte jump instruction found at the 8051 INT2 vector address. This second level of vectoring automatically transfers control to the appropriate USB ISR. The Autovector mechanism, as well as the EZ-USB interrupt system is the subject of Chapter 9, "EZ-USB Interrupts."

2.8 Power Control

The EZ-USB core implements a power-down mode that allows it to be used in USB bus powered devices that must draw no more than 500 µA when suspended. Power control is accomplished using a combination of 8051 and EZ-USB core resources. The mechanism by which EZ-USB powers down for suspend, and then re-powers to resume operation, is described in detail in Chapter 11, "EZ-USB Power Management."

A suspend operation uses three 8051 resources, the *idle* mode and two interrupts. Many enhanced 8051 architectures provide power control similar (or identical) to the EZ-USB enhanced 8051 core.

A USB suspend operation is indicated by a lack of bus activity for 3 ms. The EZ-USB core detects this, and asserts an interrupt request via the USB interrupt (8051 INT2). The ISR (Interrupt Service Routine) turns off external sub-systems that draw power. When ready to suspend operation, the 8051 sets an SFR bit, PCON.0. This bit causes the 8051 to suspend, waiting for an interrupt.

When the 8051 sets PCON.0, a control signal from the 8051 to the EZ-USB core causes the core to shut down the 12-MHz oscillator and internal PLL. This stops all internal clocks to allow the EZ-USB core and 8051 to enter a very low power mode.

The suspended EZ-USB chip can be awakened two ways: USB bus activity may resume, or an EZ-USB pin (WAKEUP#) can be asserted to activate a USB *Remote Wakeup*. Either event triggers the following chain of events:

- The EZ-USB core re-starts the 12-MHz oscillator and PLL, and waits for the clocks to stabilize
- The EZ-USB core asserts a special, high-priority 8051 interrupt to signal a 'resume' interrupt.
- The 8051 vectors to the resume ISR, and upon completion resumes executing code at the instruction following the instruction that set the PCON.0 bit to 1.

2.9 SFRs

The EZ-USB family was designed to keep 8051 coding as standard as possible, to allow easy integration of existing 8051 software development tools. The added 8051 SFR registers and bits are summarized in Table 2-2.

Table 2-2. Added Registers and Bits

8051 Enhancements	SFR	Addr	Function
Dual Data Pointers	DPL0	0x82	Data Pointer 0 Low Addr
	DPH0	0x83	Data Pointer 0 High Addr
	DPL1	0x84	Data Pointer 1 Low Addr
	DPH1	0x85	Data Pointer 1 High Addr
	DPS	0x86	Data Pointer Select (LSB)
	MPAGE	0x92	Replaces standard 8051 Port 2 for indirect external data memory addressing
Timer 2	T2CON.6-7	0xC8	Timer 2 Control
	RCAP2L	0xCA	T2 Capture/Reload Value L
	RCAP2H	0xCB	T2 Capture/Reload Value H
	T2L	0xCC	T2 Count L
	T2H	0xCD	T2 Count H
	IE.5	0xA8	ET2-Enable T2 Interrupt Bit
	IP.5	0xB8	PT2-T2 Interrupt Priority Control
UART1	SCON1.0-1	0xC0	Serial Port 1 Control
	SBUF1	0xC1	Serial Port 1 Data
	IE.6	0xA8	ES1-SIO1 Interrupt Enable Bit
	IP.6	0xB8	PS1-SIO1 Interrupt Priority Control
	EICON.7	0xD8	SMOD1-SIO1 Baud Rate Doubler
Interrupts			
INT2-INT5	EXIF	0x91	INT2-INT5 Interrupt Flags
	EIE	0xE8	INT2-INT5 Interrupt Enables
	EIP.0-3	0xF8	INT2-INT5 Interrupt Priority Control
INT6	EICON.3	0xD8	INT6 Interrupt Flag
	EIE.4	0xE8	INT6 Interrupt Enable
	EIP.4	0xF8	INT6 Interrupt Priority Control
WAKEUP#	EICON.4	0xD8	WAKEUP# Interrupt Flag
	EICON.5	0xD8	WAKEUP# Interrupt Enable
Idle Mode	PCON.0	0x87	EZ-USB Power Down (Suspend)

2.10 Internal Bus

Members of the EZ-USB family that provide pins to expand 8051 memory provide separate non-multiplexed 16-bit address and 8-bit data busses. This differs from the standard 8051, which multiplexes eight device pins between three sources: IO port 0, the external data bus, and the low byte of the address bus. A standard 8051 system with external memory requires a de-multiplexing address latch, strobed by the 8051 ALE (Address Latch Enable) pin. The external latch is not required by the non-multiplexed EZ-USB chip, and no ALE signal is needed. In addition to eliminating the customary external latch, the non-multiplexed bus saves one cycle per memory fetch cycle, further improving 8051 performance.

A standard 8051 user must choose between using Port 0 as a memory expansion port or an IO port. The AN2131Q provides a separate IO system with its own control registers (in external memory space), and provides the IO port signals on dedicated (not shared) pins. This allows the external data bus to be used to expand memory without sacrificing IO pins.

The 8051 is the sole master of the memory expansion bus. It provides read and write signals to external memory. The address bus is output-only.

A special *fast transfer* mode gives the EZ-USB family the capability to transfer data to and from external memory over the expansion bus using a single MOVX instruction, which takes only two cycles (eight clocks) per byte.

2.11 Reset

The internal 8051 RESET signal is not directly controlled by the EZ-USB RESET pin. Instead, it is controlled by an EZ-USB register bit accessible to the USB host. When the EZ-USB chip is powered, the 8051 is held in reset. Using the default USB device (enumerated by the USB core), the host downloads code into RAM. Finally, the host clears an EZ-USB register bit that takes the 8051 out of reset.

The EZ-USB family also operates with external non-volatile memory, in which case the 8051 exits the reset state automatically at power-on. The various EZ-USB resets and their effects are described in Chapter 10, "EZ-USB Resets."

3 EZ-USB Memory

3.1 Introduction

EZ-USB devices divide RAM into two regions, one for code and data, and the other for USB buffers and control registers.

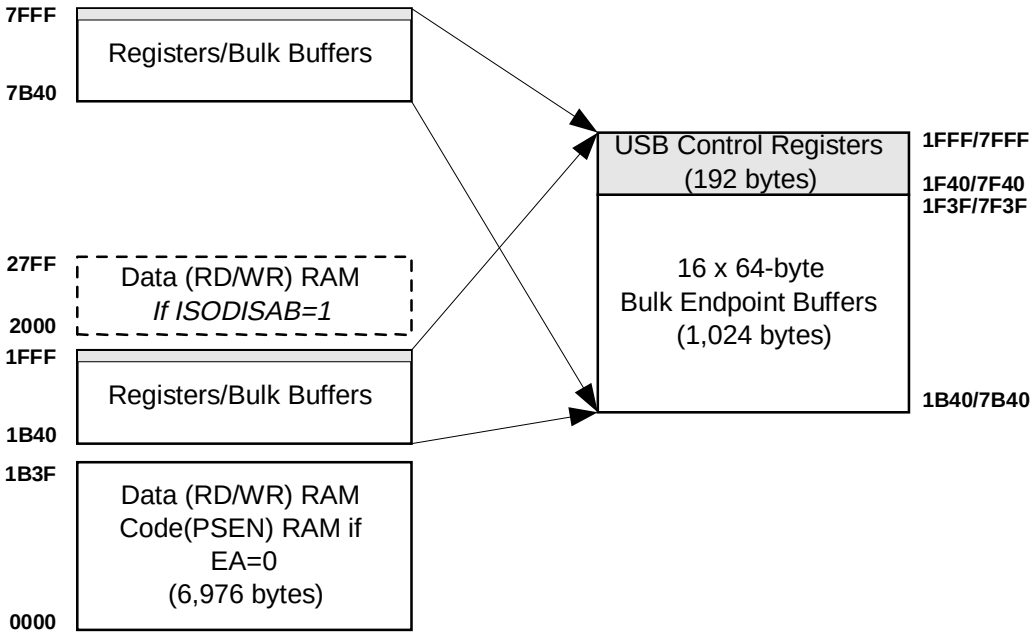


Figure 3-1. EZ-USB 8-KB Memory Map - Addresses are in Hexadecimal

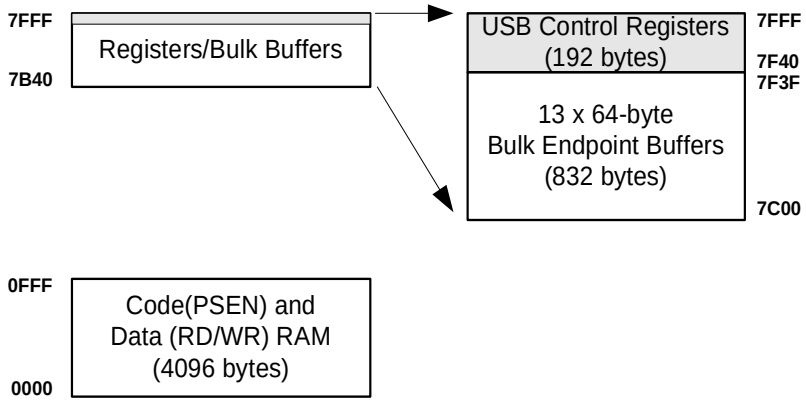


Figure 3-2. EZ-USB 4-KB Memory Map - Addresses are in Hexadecimal

3.2 8051 Memory

Figure 3-1 illustrates the two internal EZ-USB RAM regions. 6,976 bytes of general-purpose RAM occupy addresses 0x0000-0x1B3F. This RAM is loadable by the EZ-USB core or I^2C bus EEPROM, and contains 8051 code and data.
The EZ-USB EA (External Access) pin controls where the bottom segment of code (PSEN) memory is located—inside (EA=0) or outside (EA=1) the EZ-USB chip. If the EZ pin is tied low, the EZ-USB core internally ORs the two 8051 read signals PSEN and RD for this region, so that code and data share the 0x0000-0x1B3F memory space. IF EA=1, all code (PSEN) memory is external.

About 8051 Memory Spaces

The 8051 partitions its memory spaces into code memory and data memory. The 8051 reads code memory using the signal PSEN# (Program Store Enable), reads data memory using the signal RD# (Data Read) and writes data memory using the signal WR# (Data Write). The 8051 MOVX (move external) instruction generates RD# or WR# strobes.

PSEN# is a dedicated pin, while the RD# and WR# signals share pins with two IO port signals: PC7/RD and PC6/WR. Therefore, if expanded memory is used, the port pins PC7 and PC6 are not available to the system.

1,024 bytes of RAM at 0x7B40-0x7F3F implement the sixteen bulk endpoint buffers. 192 additional bytes at 0x7F40-0x7FFF contain the USB control registers. The 8051 reads and writes this memory using the MOVX instruction. In the 8-KB RAM EZ-USB version, the 1,024 bulk endpoint buffer bytes at 0x7B40-0x7F3F also appear at 0x1B40-0x1F3F. This aliasing allows unused bulk endpoint buffer memory to be added contiguously to the data memory, as illustrated Figure 3-3. The memory space at 0x1F40-0x1FFF should not be used.

Even though the 8051 can access EZ-USB endpoint buffers at either 0x1B40 or 0x7B40, the firmware should be written to access this memory only at 0x7B40-0x7FFF to maintain compatibility with future versions of EZ-USB that contain more than 8 KB of RAM. Future versions will have the bulk buffer space at 0x7B40-0x7F3F only.

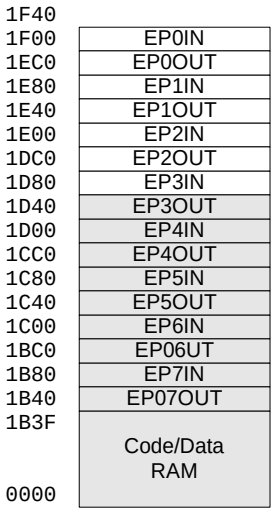


Figure 3-3. Unused Bulk Endpoint Buffers (Shaded) Used as Data Memory

In the example shown in Figure 3-3, only endpoints 0-IN through 3-IN are used for the USB function, so the data RAM (shaded) can be extended to 0x1D7F.

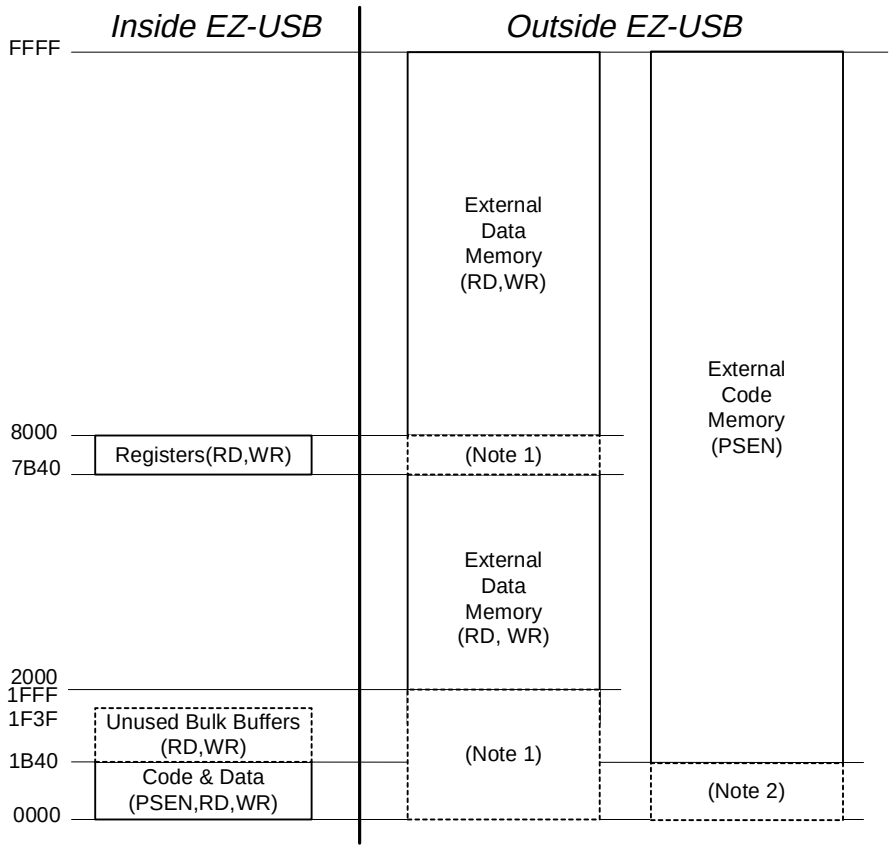
If an application uses *none* of the 16 EZ-USB isochronous endpoints, the 8051 can set the ISODISAB bit in the ISOCTL register to disable all 16 isochronous endpoints, and make the 2-KB of isochronous FIFO RAM available as 8051 data RAM at 0x2000-0x27FF.

Setting ISODISAB=1 is an *all or nothing* choice, as all 16 isochronous endpoints are disabled. An application that sets this bit must never attempt to transfer data over an isochronous endpoint.

The memory map figures in the remainder of this chapter assume that ISODISAB=0, the default (and normal) case.

3.3 Expanding EZ-USB Memory

The 80-pin EZ-USB package provides a 16-bit address bus, an 8-bit bus, and memory control signals PSEN#, RD#, and WR#. These signals are used to expand EZ-USB memory.



Note 1: OK to populate data memory here--RD#, WR#, CS# and OE# pins are inactive.
Note 2: OK to populate code memory here--no PSEN# strobe is generated.

Figure 3-4. EZ-USB Memory Map with EA=0

Figure 3-4 shows that when EA=0, the code/data memory is internal at 0x0000-0x1B40. External code memory can be added from 0x0000-0xFFFF, but it appears in the memory map only at 0x1B40-0xFFFF. Addressing external code memory at 0x0000-0x1B3F when EA=0 causes the EZ-USB core to inhibit the #PSEN strobe. This allows program memory to be added from 0x0000-0xFFFF without requiring decoding to disable it between 0x0000 and 0x1B3F.

The internal block at 0x7B40-0x7FFF (labeled “Registers”) contains the bulk buffer memory and EZ-USB control registers. As previously mentioned, they are aliased at 0x1B40-0x1FFF to allow adding unused bulk buffer RAM to general-purpose memory. 8051 code should access this memory only at the 0x7B40-0x7BFF addresses. External RAM may be added from 0x0000 to 0xFFFF, but the regions shown by Note 1 in Figure 3-4 are ignored; no external strobes or select signals are generated when the 8051 executes a MOVX instruction that addresses these regions.

3.4 CS# and OE# Signals

The EZ-USB core automatically gates the standard 8051 RD# and WR# signals to exclude selection of external memory that exists internal to the EZ-USB part. The PSEN# signal is also available on a pin for connection to external code memory.

Some 8051 systems implement external memory that is used as both data and program memory. These systems must logically OR the PSEN# and RD# signals to qualify the chip enable and output enable signals of the external memory. To save this logic, the EZ-USB core provides two additional control signals, CS# and OE#. The equations for these signals are as follows:

- CS# = RD# or WR# or PSEN#
- OE# = RD# or PSEN#

Because the RD#, WR#, and PSEN# signals are already qualified by the addresses allocated to external memory, these strobes are active only when external memory is accessed.

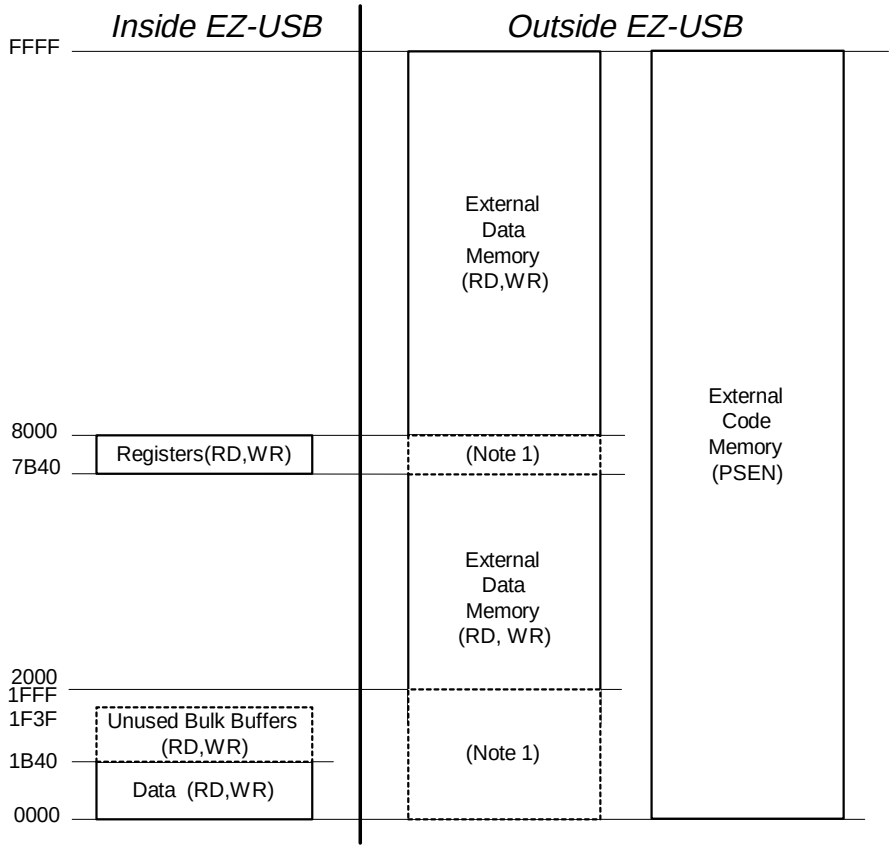


Figure 3-5. EZ-USB Memory Map with EA=1

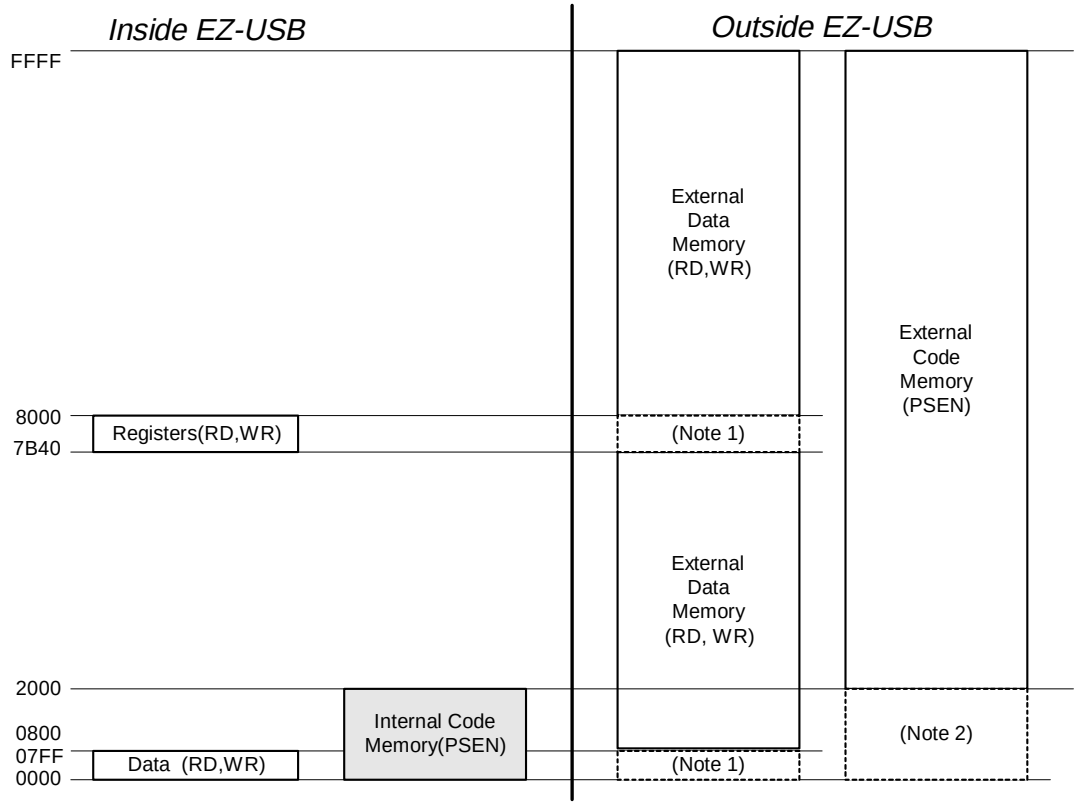
When EA=1 (Figure 3-5), all code (PSEN) memory is external. All internal EZ-USB RAM is data memory. This gives the user over 6-KB of general-purpose RAM, accessible by the MOVX instruction.

Note

Figures 3-4 and 3-5 assume that the EZ-USB chip uses isochronous endpoints, and therefore that the ISODISAB bit (ISOCTL.0) is LO. If ISODISAB=1, additional data RAM appears internally at 0x2000-0x27FF, and the RD#, WR#, CS#, and OE# signals are modified to exclude this memory space from external data memory.

3.5 EZ-USB ROM Versions

The EZ-USB 8-KB Masked ROM and 32-KB Masked ROM memory maps are shown in Figures 3-6 and 3-7.



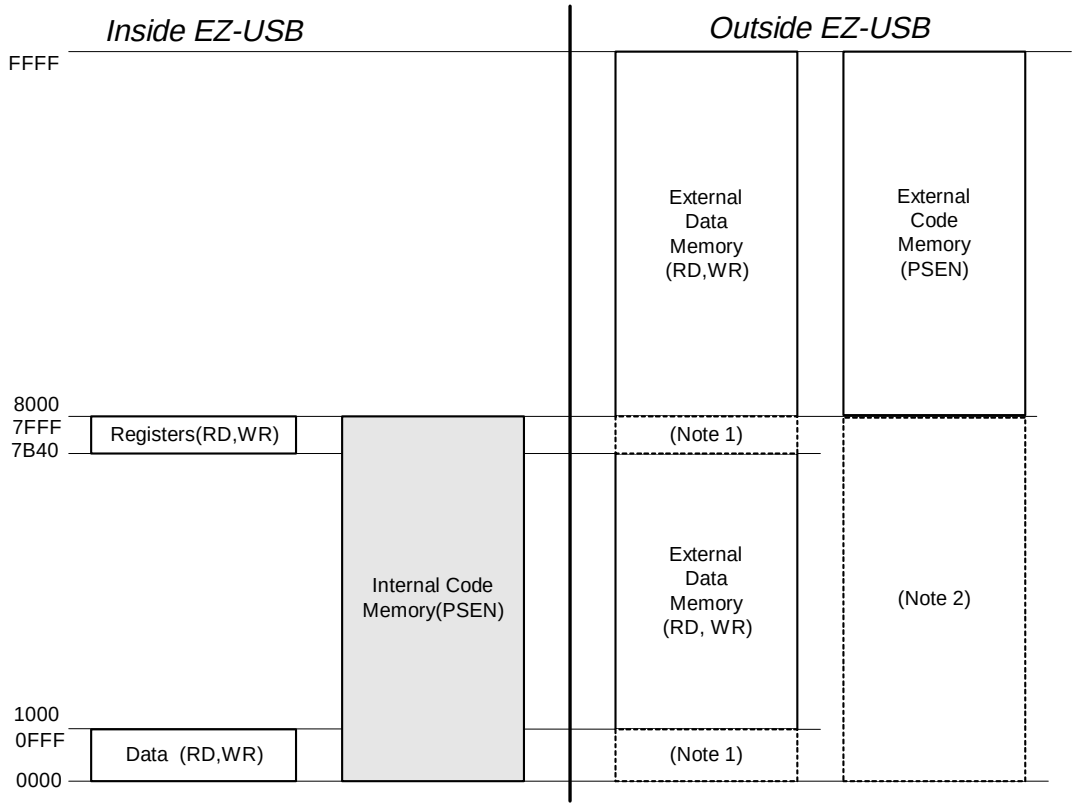
Note 1: OK to populate data memory here, but no RD# or WR# strobes are generated.

Note 2: OK to populate code memory here, but no PSEN# strobe is generated.

Figure 3-6. 8-KB ROM, 2-KB RAM Version

EZ-USB ROM versions contain program memory starting at 0x0000. In these versions, the internal RAM is implemented as data-only memory.

Code for this ROM version can be developed and tested using the AN2131Q with an external code memory (EA=1, Figure 3-5). As long as the 8051 limits internal RAM access to 0x0000-0x07FF and accesses the EZ-USB registers and bulk data at 0x7B40-0x7FFF, the code in the external memory will be the identical image of the code that will ultimately be internal at 0x0000-0x1FFF in the ROM version.



Note 1: OK to populate data memory here, but no RD# or WR# strobes are generated.

Note 2: OK to populate code memory here, but no PSEN# strobe is generated.

Figure 3-7. 32-KB ROM, 4-KB RAM Version

The EZ-USB 32-KB ROM version contains program memory from 0x0000 through 0x7FFF, and data memory from 0x0000 through 0x0FFF.

Code for this ROM version can be developed and tested using the AN2131Q with an external code memory (EA=1, Figure 3-5). As long as the 8051 limits internal RAM access to 0x0000-0x0FFF and accesses the EZ-USB registers and bulk data at 0x7B40-0x7FFF, the code in the external memory will be the identical image of the code that will ultimately be internal at 0x0000-0x7FFF in the ROM version.

4 EZ-USB Input/Output

4.1 Introduction

The EZ-USB chip provides two input-output systems:

- A set of programmable IO pins
- A programmable I^2C Controller

This chapter begins with a description of the programmable IO pins, and shows how they are shared by a variety of 8051 and EZ-USB alternate functions such as UART, timer and interrupt signals.

The I^2C controller uses the SCL and SDA pins, and performs two functions:

- General-purpose 8051 use
- Boot loading from an EEPROM

Note

2.2-KB to 4.7-KB pullups are required on the SDA and SCL lines.

This chapter describes both the programming information for the 8051 I^2C interface, and the operating details of the I^2C boot loader. The role of the boot loader is described in Chapter 5, "EZ-USB Enumeration and ReNumeration™."

4.2 IO Ports

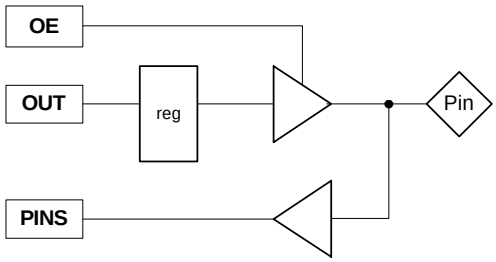


Figure 4-1. EZ-USB Input/Output Pin

The EZ-USB family implements its IO ports using memory-mapped registers. This is in contrast to a standard, which uses SFR bits for input/output.

Figure 4-1 shows the basic structure of an EZ-USB IO pin. Twenty-four IO pins are grouped into three 8-bit ports named PORTA, PORTB, and PORTC. The AN2131Q has all three ports, while the AN2131S has PORTB, PORTC, and two PORTA bits. The 8051 accesses IO pins using the three control bits shown in Figure 4-1: OE, OUT, and PINS. The OUT bit writes output data to a register, the OE bit turns on the output buffer, and the PINS bit indicates the state of the pin.

To configure a pin as an input, the 8051 sets OE=0 to turn off the output buffer. To configure a pin as an output, the 8051 sets OE=1 to turn on the output buffer, and writes data to the OUT register. The PINS bit reflects the actual pin value regardless of the value of OE.

A fourth control bit (in PORTACFG, PORTBCFG, PORTCCFG registers) determines whether a port pin is general-purpose Input/Output (GPIO) as shown in Figure 4-1, or connected to an alternate 8051 or EZ-USB function. Table 4-1 lists the alternate functions available on the IO pins. Figure 4-1 shows the registers and bits associated with the IO ports.

Table 4-1. IO Pin Functions for PORTxCFG=0 and PORTxCFG=1

PORTxCFG bit = 0	PORTxCFG bit = 1			
Signal	**Signal**	**Direction**	**Description**	**Figure**
PA0	T0OUT	OUT	Timer 0 Overflow Pulse	4-2
PA1	T1OUT	OUT	Timer 1 Overflow Pulse	4-2
PA2	OE#	OUT	EZ-USB Output Enable	4-2
PA3	CS#	OUT	EZ-USB Chip Select	4-2
PA4	FWR#	OUT	EZ-USB Fast Write Strobe	4-2
PA5	FRD#	OUT	EZ-USB Fast Read Strobe	4-2
PA6	RxD0OUT	OUT	UART0 Mode 0 Data Out	4-2
PA7	RxD1OUT	OUT	UART1 Mode 0 Data Out	4-2
PB0	T2	IN	Timer 2 Clock Input	4-3
PB1	T2EX	IN	Timer 2 Capture/Reload	4-3
PB2	RxD1	IN	UART1 Receive Data	4-3
PB3	TxD1	OUT	UART1 Transmit Data	4-2
PB4	INT4	IN	Interrupt 4	4-3
PB5	INT5	IN	Interrupt 5	4-3
PB6	INT6	IN	Interrupt 6	4-3
PB7	T2OUT	OUT	Timer 2 Overflow Pulse	4-2
PC0	RxD0	IN	UART0 Receive Data	4-3
PC1	TxD0	OUT	UART0 Transmit Data	4-2
PC2	INT0#	IN	Interrupt 0	4-3
PC3	INT1#	IN	Interrupt 1	4-3
PC4	T0	IN	Timer 0 Clock Input	4-3
PC5	T1	IN	Timer 1 Clock Input	4-3
PC6	WR#	OUT	Write Strobe	4-2
PC7	RD#	OUT	Read Strobe	4-2

Depending on whether the alternate function is an input or output, the IO logic is slightly different, as shown in Figure 4-2 (output) and Figure 4-3 (input). The last column of Table 4-1 indicates which figure applies to each pin.

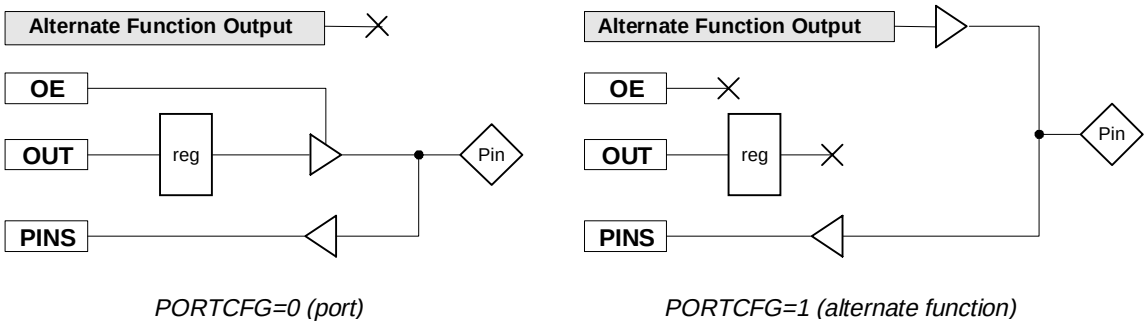


Figure 4-2. Alternate Function is an OUTPUT

Referring to Figure 4-2, when PORTCFG=0, the IO port is selected. In this case the alternate function (shaded) is disconnected and the pin functions exactly as shown in Figure 4-1. When PORTCFG=1, the alternate function is connected to the IO pin and the output register and buffer are disconnected. Note that the 8051 can still read the state of the pin, and thus the alternate function value.

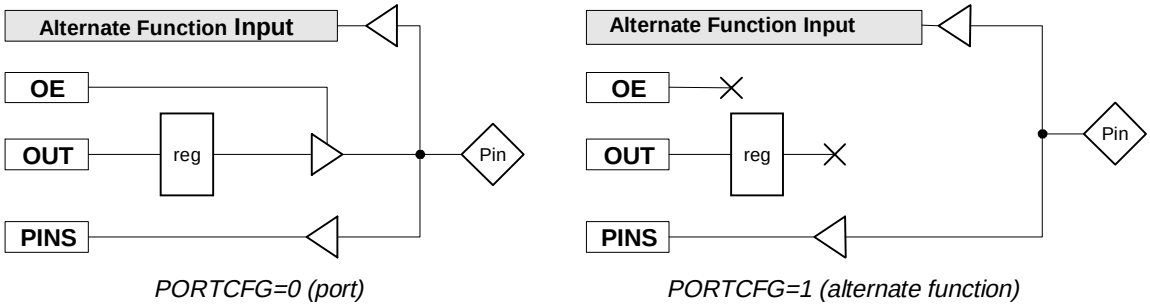


Figure 4-3. Alternate Function is an INPUT

Referring to Figure 4-3, when PORTCFG=0, the IO port is selected. This is the general IO port shown in Figure 4-1 with one important difference—the alternate function is always *listening*. Whether the port pin is set for output or input, the pin signal also drives the alternate function. 8051 firmware should ensure that if the alternate function is not used (if the pin is GPIO only), the alternate input function is disabled.

For example, suppose the PB4/INT4 pin is configured for PB4. The pin signal is also routed to INT4. If INT4 is not used by the application, it should not be enabled. Alternatively, enabling INT4 could be useful, allowing IO bit PB4 to trigger an interrupt.

When PORTxCFG=1, the alternate function is selected. The output register and buffer are disconnected. The PINS bit can still read the pin, and thus the input to the alternate function.

4.3 IO Port Registers

PORTACFG	RxD1out	RxD0out	FRD	FWR	CS	OE	T1out	T0out
OUTA	D7	D6	D5	D4	D3	D2	D1	D0
PINSA	D7	D6	D5	D4	D3	D2	D1	D0
OEA	D7	D6	D5	D4	D3	D2	D1	D0
PORTBCFG	T2OUT	INT6	INT5	INT4	TxD1	RxD1	T2EX	T2
OUTB	D7	D6	D5	D4	D3	D2	D1	D0
PINSB	D7	D6	D5	D4	D3	D2	D1	D0
OEB	D7	D6	D5	D4	D3	D2	D1	D0
PORTCCFG	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0
OUTC	D7	D6	D5	D4	D3	D2	D1	D0
PINSC	D7	D6	D5	D4	D3	D2	D1	D0
OEC	D7	D6	D5	D4	D3	D2	D1	D0

Figure 4-4. Registers Associated with PORTS A, B, and C

Figure 4-4 shows the registers associated with the EZ-USB IO ports. The power-on default for the PORTCFG bits is 0, selecting the IO port function. The power-on default for the OE bits is 0, selecting the input direction.

4.4 I²C Controller

The USB core contains an I²C controller for boot loading and general-purpose I²C bus interface. This controller uses the SCL (Serial Clock) and SDA (Serial Data) pins. I2C Controller describes how the boot load operates at power-on to read the contents of an external serial EEPROM to determine the initial EZ-USB FX configuration. The boot loader operates automatically, while the 8051 is held in reset. The last section of this chapter describes the operating details of the boot loader.

After the boot sequence completes and the 8051 is brought out of reset, the general-purpose I²C controller is available to the 8051 for interface to external I²C devices, such as other EEPROMS, I/O chips, audio/video control chips, etc.

4.5 8051 I²C Controller

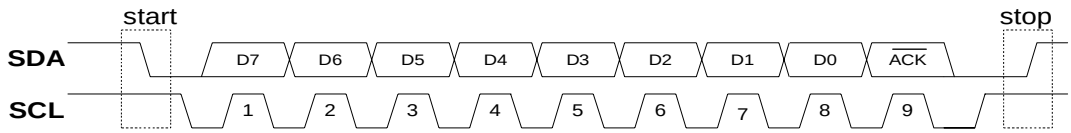


Figure 4-5. General I²C Transfer

Figure 4-5 illustrates the waveforms for an I²C transfer. SCL and SDA are open-drain EZ-USB pins, which must be pulled up to Vcc with external resistors. The EZ-USB chip is an I²C bus master only, meaning that it synchronizes data transfers by generating clock pulses on SCL by driving low. Once the master drives SCL low, external slave devices can also drive SCL low to extend clock cycle times.

To synchronize I²C data, serial data (SDA) is permitted to change state only while SCL is low, and must be valid while SCL is high. Two exceptions to this rule are used to generate START and STOP conditions. A START condition is defined as SDA going low, while SCL is high, and a STOP condition is defined as SDA going high, while SCL is high. Data is sent MSB first. During the last bit time (clock #9 in Figure 4-5), the master (EZ-USB) floats the SDA line to allow the slave to acknowledge the transfer by pulling SDA low.

Multiple I²C Bus Masters — The EZ-USB chip acts only as an I²C bus master, never a slave. However, the 8051 can detect a second master by checking for BERR=1 (Section 4.7, "Status Bits").

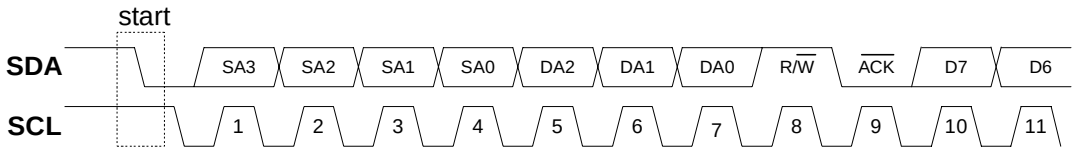


Figure 4-6. Addressing an I²C Peripheral

The first byte of an I²C bus transaction contains the address of the desired peripheral. Figure 4-7 shows the format for this first byte, which is sometimes called a *control* byte.

A master sends the bit sequence shown in Figure 4-6 after sending a START condition. The master uses this 9-bit sequence to select an I²C peripheral at a particular address, to establish the transfer direction (using R/W#), and to determine if the peripheral is present by testing for ACK#.

The four most significant bits SA3-SA0 are the peripheral chip's slave address. I²C devices are pre-assigned slave addresses by device type, for example slave address 1010 is assigned to EEPROMS. The three bits DA2-DA0 usually reflect the states of I²C device address pins. Devices with three address pins can be strapped to allow eight distinct addresses for the same device type. The eighth bit (R/W#) sets the direction for the ensuing data transfer, 1 for master read, and 0 for master write. Most address transfers are followed by one or more data transfers, with the STOP condition generated after the last data byte is transferred.

In Figure 4-6, a READ transfer follows the address byte (at clock 8, the master sets the R/W# bit high, indicating READ). At clock 9, the peripheral device responds to its address by asserting ACK. At clock 10, the master floats SDA and issues SCL pulses to clock in SDA data supplied by this slave.

Assuming the 12-MHz crystal used by the EZ-USB family, the SCL frequency is 90.9 KHz, giving an I²C transfer rate of 11 ms per bit.

I2CS **I²C Control and Status** **7FA5**

b7	b6	b5	b4	b3	b2	b1	b0
START	**STOP**	**LASTRD**	**ID1**	**ID0**	**BERR**	**ACK**	**DONE**

I2DAT **I²C Data** **7FA6**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Figure 4-7. FC Registers

The 8051 uses the two registers shown in Figure 4-7 to conduct I²C transfers. The 8051 transfers data to and from the I²C bus by writing and reading the I2DAT register. The 12CS register controls I²C transfers and reports various status conditions. The three control bits are START, STOP, and LASTRD. The remaining bits are status bits. Writing to a status bit has no effect.

4.6 Control Bits

4.6.1 START

The 8051 sets the START bit to 1 to prepare an I²C bus transfer. If START=1, the next 8051 load to I2DAT will generate the start condition followed by the serialized byte of data in I2DAT. The 8051 loads data in the format shown in Figure 4-5 after setting the START bit. The I²C controller clears the START bit during the ACK interval (clock 9 in Figure 4-5).

4.6.2 STOP

The 8051 sets STOP=1 to terminate an I²C bus transfer. The I²C controller clears the STOP bit after completing the STOP condition. If the 8051 sets the STOP bit during a byte transfer, the STOP condition will be generated immediately following the ACK phase of the byte transfer. If no byte transfer is occurring when the STOP bit is set, the STOP condition will be carried out immediately on the bus. Data should not be written to I2CS

or I2DAT until the STOP bit returns low. In the 2122/2126 only, an interrupt request is available to signal that STOP bit transmission is complete.

4.6.3 LASTRD

To read data over the I^2C bus, an I^2C master floats the SDA line and issues clock pulses on the SCL line. After every eight bits, the master drives SDA low for one clock to indicate ACK. To signal the last byte of the read transfer, the master floats SDA at ACK time to instruct the slave to stop sending. This is controlled by the 8051 by setting LASTRD=1 before reading the last byte of a read transfer. The I^2C controller clears the LASTRD bit at the end of the transfer (at ACK time).

Note

Setting LASTRD does not automatically generate a STOP condition. The 8051 should also set the STOP bit at the end of a read transfer.

4.7 Status Bits

After a byte transfer the EZ-USB controller updates the three status bits BERR, ACK, and DONE. If no STOP condition was transmitted, they are updated at ACK time. If a STOP condition was transmitted they are updated after the STOP condition is transmitted.

4.7.1 DONE

The I^2C controller sets this bit whenever it completes a byte transfer, right after the ACK stage. The controller also generates an I^2C interrupt request (8051 INT3) when it sets the DONE bit. The I^2C controller clears the DONE bit when the 8051 reads or writes the I2DAT register, and the I^2C interrupt request bit whenever the 8051 reads or writes the I2CS or I2DAT register.

4.7.2 ACK

Every ninth SCL of a write transfer, the slave indicates reception of the byte by asserting ACK. The EZ-USB controller floats SDA during this time, samples the SDA line, and updates the ACK bit with the complement of the detected value. ACK=1 indicates acknowledge, and ACK=0 indicates not-acknowledge. The EZ-USB core updates the

ACK bit at the same time it sets DONE=1. The ACK bit should be ignored for read transfers on the bus.

4.7.3 BERR

This bit indicates an I^2C bus error. BERR=1 indicates that there was bus contention, which results when an outside device drives the bus LO when it shouldn't, or when another bus master wins arbitration, taking control of the bus. BERR is cleared when the 8051 reads or writes the I2DAT register.

4.7.4 ID1, ID0

These bits are set by the boot loader (Section 4.10, "I^2C Boot Loader") to indicate whether an 8-bit address or 16-bit address EEPROM at slave address 000 or 001 was detected at power-on. They are normally used only for debug purposes. Table 4-3 shows the encoding for these bits.

4.8 Sending I^2C Data

To send a multiple byte data record over the I^2C bus, follow these steps:

1. Set the START bit.
2. Write the peripheral address and direction=0 (for write) to I2DAT.
3. Wait for DONE=1*. If BERR=1 or ACK=0, go to step 7.
4. Load I2DAT with a data byte.
5. Wait for DONE=1*. If BERR=1 or ACK=0 go to step 7.
6. Repeat steps 4 and 5 for each byte until all bytes have been transferred.
7. Set STOP=1.

* If the I^2C interrupt (8051 INT3) is enabled, each "Wait for DONE=1" step can be interrupt driven, and handled by an interrupt service routine. See Section 9.12, "I^2C Interrupt" for more details regarding the I^2C interrupt.

4.9 Receiving I²C Data

To read a multiple-byte data record, follow these steps:

1. Set the START bit.
2. Write the peripheral address and direction=1 (for read) to I2DAT.
3. Wait for DONE=1*. If BERR=1 or ACK=0, terminate by setting STOP=1.
4. Read I2DAT and discard the data. This initiates the first burst of nine SCL pulses to clock in the first byte from the slave.
5. Wait for DONE=1*. If BERR=1, terminate by setting STOP=1.
6. Read the data from I2DAT. This initiates another read transfer.
7. Repeat steps 5 and 6 for each byte until ready to read the second-to-last byte.
8. Before reading the second-to-last I2DAT byte, set LASTRD=1.
9. Read the data from I2DAT. With LASTRD=1, this initiates the final byte read on the I²C bus.
10. Wait for DONE=1*. If BERR=1, terminate by setting STOP=1.
11. Set STOP=1.
12. Read the last byte from I2DAT immediately (the next instruction) after setting the STOP bit. This retrieves the last data byte without initiating an extra read transaction (nine more SCL pulses) on the I²C bus.

* If the I²C interrupt (8051 INT3) is enabled, each “Wait for DONE=1” step can be interrupt-driven, and handled by an interrupt service routing. See Section 9.12, "I²C Interrupt” for more details regarding the I²C interrupt.

4.10 I²C Boot Loader

When the EZ-USB chip comes out of reset, the EZ-USB boot loader checks for the presence of an EEPROM on its I²C bus. If an EEPROM is detected, the loader reads the first EEPROM byte to determine how to enumerate (specifically, whether to supply ID information from the EZ-USB core or from the EEPROM). The various enumeration modes are described in Chapter 5, "EZ-USB Enumeration and ReNumeration™."

Prior to reading the first EEPROM byte, the boot loader must set an address counter inside the EEPROM to zero. It does this by sending a control byte (write) to select the EEPROM, followed by a zero address to set the internal EEPROM address pointer to zero. Then it issues a control byte (read), and reads the first EEPROM byte.

The EZ-USB boot loader supports two I²C EEPROM types:

- EEPROMs with address A[7..4]=1010 that use an 8-bit address (example: 24LC00, LC01/A, LC02/A).
- EEPROMs with address A[7..4]=1010 that use a 16-bit address (example: 24LC00, LC01/A, LC02/A).

EEPROMs with densities up to 256 bytes require loading a single address byte. Larger EEPROMs require loading two address bytes.

The EZ-USB I²C controller needs to determine which EEPROM type is connected—one or two address bytes—so that it can properly reset the EEPROM address pointer to zero before reading the EEPROM. For the single-byte address part, it must send a single zero byte of address, and for the two-byte address part it must send two zero bytes of address.

Because there is no direct way to detect which EEPROM type—single or double address—is connected, the I²C controller uses the EEPROM address pins A2, A1, and A0 to determine whether to send out one or two bytes of address. This algorithm requires that the EEPROM address lines are strapped as shown in Table 4-2. Single-byte-address EEPROMs are strapped to address 000 and double-byte-address EEPROMs are strapped to address 001.

Table 4-2. Strap Boot EEPROM Address Lines to These Values

Bytes	Example EEPROM	A2	A1	A0
16	24LC00*	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1

* This EEPROM does not have address pins

The I^2C controller performs a three-step test at power-on to determine whether a one-byte-address or a two-byte-address EEPROM is attached. This test proceeds as follows:

1. The I^2C controller sends out a "read current address" command to I^2C sub-address 000 (10100001). If no ACK is returned, the controller proceeds to step 2. If ACK is returned, the one-byte-address device is indicated. The controller discards the data and proceeds to step 3.

2. The I^2C controller sends out a "read current address" command to I^2C sub-address 001 (10100011). If ACK is returned, the two-byte-address device is indicated. The controller discards the data and proceeds to step 3. If no ACK is returned, the controller assumes that a valid EEPROM is not connected, assumes the "No Serial EEPROM" mode, and terminates the boot load.

3. The I^2C controller resets the EEPROM address pointer to zero (using the appropriate number of address bytes), then reads the first EEPROM byte. If it does not read 0xB0 or 0xB2, the controller assumes the "No Serial EEPROM" mode. If it reads either 0xB0 or 0xB2, the controller copies the next six bytes into internal storage, and if it reads 0xB2, it proceeds to load the EEPROM contents into internal RAM.

The results of this power-on test are reported in the ID1 and ID0 bits, as shown in Table 4-3.

Table 4-3. Results of Power-On I²C Test

ID1	ID0	Meaning
0	0	No EEPROM detected
0	1	One-byte-address load EEPROM detected
1	0	Two-byte-address load EEPROM detected
1	1	Not used

Other EEPROM devices (with device address of 1010) can be attached to the I²C bus for general purpose 8051 use, as long as they are strapped for address other than 000 or 001. If a 24LC00 EEPROM is used, no other EEPROMS with device address 1010 may be used, because the 24LC00 responds to all eight sub-addresses.

5 EZ-USB Enumeration and ReNumeration™

5.1 Introduction

The EZ-USB chip is *soft*. 8051 code and data is stored in internal RAM, which is loaded from the host using the USB interface. Peripheral devices that use the EZ-USB chip can operate without ROM, EPROM, or FLASH memory, shortening production lead times and making firmware updates a breeze.

To support the soft feature, the EZ-USB chip automatically enumerates as a USB device *without firmware*, so the USB interface itself may be used to download 8051 code and descriptor tables. The EZ-USB core performs this initial (power-on) enumeration and code download while the 8051 is held in reset. This initial USB device, which supports code download, is called the "Default USB Device."

After the code descriptor tables have been downloaded from the host to EZ-USB RAM, the 8051 is brought out of reset and begins executing the device code. The EZ-USB device enumerates again, this time as the loaded device. This second enumeration is called "ReNumeration™," which the EZ-USB chip accomplishes by electrically simulating a physical disconnection and re-connection to the USB.

An EZ-USB control bit called "ReNum" (ReNumerated) determines which entity, the core or the 8051, handles device requests over endpoint zero. At power-on, the RENUM bit (USBCS.1) is zero, indicating that the EZ-USB core automatically handles device requests. Once the 8051 is running, it can set ReNum=1 to indicate that user 8051 code handles subsequent device requests using its downloaded firmware. Chapter 7, "EZ-USB Endpoint Zero" describes how the 8051 handles device requests while ReNum=1.

It is also possible for the 8051 to run with ReNum=0 and have the EZ-USB core handle certain endpoint zero requests (see the text box, "Another Use for the Default USB Device" on page 5-2).

This chapter deals with the various EZ-USB startup modes, and describes the default USB device that is created at initial enumeration.

Another Use for the Default USB Device

The Default USB Device is established at power-on to set up a USB device capable of downloading firmware into EZ-USB RAM. Another useful feature of the EZ-USB default device is that 8051 code can be written to support the already-configured Generic USB device. Before bringing the 8051 out of reset, the EZ-USB core enables certain endpoints and reports them to the host via descriptors. By utilizing the USB default machine (by keeping ReNum=0), the 8051 can, with very little code, perform meaningful USB transfers that use these default endpoints. This accelerates the USB learning curve. To see an example of how little code is actually necessary, take a look at Section 6.11, "Polled Bulk Transfer Example."

5.2 The Default USB Device

The Default USB Device consists of a single USB configuration containing one interface (interface 0) with three alternate settings 0, 1, and 2. The endpoints reported for this device are shown in Table 5-1. Note that alternate setting zero uses no interrupt or isochronous bandwidth, as recommended by the USB Specification.

Table 5-1. EZ-USB Default Endpoints

Endpoint	Type	Alternate Setting		
		0	1	2
		Maximum Packet Size (Bytes)		
0	CTL	64	64	64
1-IN	INT	0	16	64
2-IN	BULK	0	64	64
2-OUT	BULK	0	64	64
4-IN	BULK	0	64	64
4-OUT	BULK	0	64	64
6-IN	BULK	0	64	64
6-OUT	BULK	0	64	64
8-IN	ISO	0	16	256
8-OUT	ISO	0	16	256
9-IN	ISO	0	16	16
9-OUT	ISO	0	16	16
10-IN	ISO	0	16	16
10 OUT	ISO	0	16	16

For purposes of downloading 8051 code, the Default USB Device requires only CONTROL endpoint zero. Nevertheless, the USB default machine is enhanced to support other endpoints as shown in Figure 5-1 (note the alternate settings 1 and 2). This enhancement is provided to allow the developer to get a head start generating USB traffic and learning the USB system. All the descriptors are automatically handled by the EZ-USB core, so the developer can immediately start writing code to transfer data over USB using these pre-configured endpoints.

When the EZ-USB core establishes the Default USB Device, it also sets the proper endpoint configuration bits to match the descriptor data supplied by the EZ-USB core. For example, bulk endpoints 2, 4, and 6 are implemented in the Default USB Device, so the EZ-USB core sets the corresponding EPVAL bits. Chapter 6, “EZ-Bulk Transfers” contains a detailed explanation of the EPVAL bits.

Tables 5-9 through 5-13 show the various descriptors returned to the host by the EZ-USB core when ReNum=0. These tables describe the USB endpoints defined in Table 5-1, along with other USB details, and should be useful to help understand the structure of USB descriptors.

5.3 EZ-USB Core Response to EP0 Device Requests

Table 5-2 shows how the EZ-USB core responds to endpoint zero requests when ReNum=0.

Table 5-2. How the EZ-USB Core Handles EP0 Requests When ReNum=0

bRequest	Name	Action: ReNum=0
0x00	Get Status/Device	Returns two zero bytes
0x00	Get Status/Endpoint	Supplies EP Stall bit for indicated EP
0x00	Get Status/Interface	Returns two zero bytes
0x01	Clear Feature/Device	None
0x01	Clear Feature/Endpoint	Clears Stall bit for indicated EP
0x02	(reserved)	None
0x03	Set Feature/Device	None
0x03	Set Feature Endpoint	Sets Stall bit for indicated EP
0x04	(reserved)	None
0x05	Set Address	Updates FNADD register
0x06	Get Descriptor	Supplies internal table
0x07	Set Descriptor	None
0x08	Get Configuration	Returns internal value
0x09	Set Configuration	Sets internal value
0x0A	Get Interface	Returns internal value (0-3)
0x0B	Set Interface	Sets internal value (0-3)
0x0C	Sync Frame	None
Vendor Requests		
0x0A	Firmware Load	Upload/Download RAM
0xA1-0xAF	Reserved	Reserved by Cypress Semiconductor
all other		None

The USB host enumerates by issuing:

- Set_Address
- Get_Descriptor
- Set_Configuration (to 1)

As shown in Table 5-2, after enumeration, the EZ-USB core responds to the following host requests.

- Set or clear an endpoint stall (Set/Clear Feature-Endpoint).
- Read the stall status for an endpoint (Get_Status_Endpoint).
- Set/Read an 8-bit configuration number (Set/Get_Configuration).
- Set/Read a 2-bit interface alternate setting (Set/Get_Interface).
- Download or upload 8051 RAM.

To ensure proper operation of the default Keil Monitor, which uses SIO-1 (RXD1 and TXD1), never change the following Port Config bits from "1":

- PORTBCFG bits 2 (RXD1) and 3 (TXD1).

To ensure the 8051 processor can access the external SRAM (including the Keil Monitor), do not change the following bits from "1":

- PORTCCFG bits 6 (WR#) and 7 (RD#).

To ensure that no bits are unintentionally changed, all writes to the PORTxCFG registers should use a read-modify-write series of instructions.

5.4 Firmware Load

The USB Specification provides for *vendor-specific requests* to be sent over CONTROL endpoint zero. The EZ-USB chip uses this feature to transfer data between the host and EZ-USB RAM. The EZ-USB core responds to two "Firmware Load" requests, as shown in Tables 5-3 and 5-4.

Table 5-3. Firmware Download

Byte	Field	Value	Meaning	8051 Response
0	bmRequest	**0x40**	Vendor Request, OUT	*None required*
1	bRequest	**0xA0**	"Firmware Load"	
2	wValueL	**AddrL**	Starting Address	
3	wValueH	**AddrH**		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLenghtL	**LenL**	Number of Bytes	
7	wLengthH	**LenH**		

Table 5-4. Firmware Upload

Byte	Field	Value	Meaning	8051 Response
0	bmRequest	**0xC0**	Vendor Request, IN	*None required*
1	bRequest	**0xA0**	"Firmware Load"	
2	wValueL	**AddrL**	Starting Address	
3	wValueH	**AddrH**		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**LenL**	Number of Bytes	
7	wLengthH	**LenH**		

These requests are always handled by the EZ-USB core (ReNum=0 or 1). This means that 0xA0 is *reserved* by the EZ-USB chip, and therefore should never be used for a vendor request. Cypress Semiconductor also reserves bRequest values 0xA1 through 0xAF, so your system should not use these bRequest values.

A host loader program typically writes 0x01 to the CPUCS register to put the 8051 into RESET, loads all or part of the EZ-USB RAM with 8051 code, and finally reloads the CPUCS register with 0 to take the 8051 out of RESET. The CPUCS register is the only USB *register* that can be written using the Firmware Download command.

Firmware loads are restricted to internal EZ-USB memory.

When ReNum=1 at Power-On

At power-on, the ReNum bit is normally set to zero so that the EZ-USB handles device requests over CONTROL endpoint zero. This allows the core to download 8051 firmware and then reconnect as the target device.

At power-on, the EZ-USB core checks the I^2C bus for the presence of an EEPROM. If it finds one, and the first byte of the EEPROM is 0xB2, the core copies the contents of the EEPROM into internal RAM, sets the ReNum bit to 1, and un-RESETS the 8051. The 8051 wakes up ready-to-run firmware in RAM. The required data form at for this load module is described in the next section.

5.5 Enumeration Modes

When the EZ-USB chip comes out of reset, the EZ-USB core makes a decision about how to enumerate based on the contents of an external EEPROM on its I^2C bus. Table 5-5 shows the choices. In Table 5-5, PID means Product ID, VID means Version ID, and DID means Device ID.

Table 5-5. EZ-USB Core Action at Power-Up

First EEPROM byte	EZ-USB Core Action
Not 0xB0 or 0xB2	Supplies descriptors, PID/VID/DID from EZ-USB Core. Sets ReNum=0.
0xB0	Supplies descriptors from EZ-USB core, PID/VID/DID from EEPROM. Sets ReNum=0.
0xB2	Loads EEPROM into EZ-USB RAM. Sets ReNum=1; therefore 8051 supplies descriptors, PID/VID/DID.

If no EEPROM is present, or if one is present but the first byte is neither 0xB0 nor 0xB2, the EZ-USB core enumerates using internally stored descriptor data, which contains the Cypress Semiconductor VID, PID, and DID. These ID bytes cause the host operating system to load a Cypress Semiconductor device driver. The EZ-USB core also establishes the *Default USB device*. This mode is only used for code development and debug.

If a serial EEPROM is attached to the I^2C bus and its first byte is 0xB0, the EZ-USB core enumerates with the same internally stored descriptor data as for the no-EEPROM case, but with one difference. It supplies the PID/VID/DID data from six bytes in the external EEPROM rather than from the EZ-USB core. The custom VID/PID/DID in the EEPROM causes the host operating system to load a device driver that is matched to the EEPROM VID/PID/DID. This EZ-USB operating mode provides a *soft* USB device using ReNumeration™.

If a serial EEPROM is attached to the I^2C bus and its first byte is 0xB2, the EZ-USB core transfers the contents of the EEPROM into internal RAM. The EZ-USB core also sets the ReNum bit to 1 to indicate that the 8051 (and not the EZ-USB core) responds to device requests over CONTROL endpoint zero (see the text box, “When ReNum=1 at Power-On” on page 5-6). Therefore, all descriptor data, including VID/DID/PID values, are supplied by the 8051 firmware. The last byte loaded from the EEPROM (to the CPUCS register) releases the 8051 reset signal, allowing the EZ-USB chip to come up as a fully custom device with firmware in RAM.

The following sections discuss these enumeration methods in detail.

The Other Half of the I²C Story

The EZ-USB I²C controller serves two purposes. First, as described in this chapter, it manages the serial EEPROM interface that operates automatically at power-on to determine the enumeration method. Second, once the 8051 is up and running, the 8051 can access the I²C controller for general-purpose use. This makes a wide range of standard I²C peripherals available to an EZ-USB system.

Other I²C devices can be attached to the SCL and SDA lines of the I²C bus as long as there is no address conflict with the serial EEPROM described in this chapter. Chapter 4, "EZ-USB Input/Output" describes the general-purpose nature of the I²C interface.

5.6 No Serial EEPROM

In the simplest case, no serial EEPROM is present on the I²C bus, or an EEPROM is present but its first byte is not 0xB0 or 0xB2. In this case, descriptor data is supplied by a table internal to the EZ-USB core. The EZ-USB chip comes on as the *USB Default Device*, with the ID bytes shown in Table 5-6.

Table 5-6. EZ-USB Device Characteristics, No Serial EEPROM

Vendor ID	0x0547 (Cypress Semiconductor)
Product ID	0x2131 (EZ-USB)
Device Release	0xXXYY (depends on revision)

The USB host queries the device during enumeration, reads the device descriptor, and uses the Table 5-6 bytes to determine which software driver to load into the operating system. This is a major USB feature—drivers are dynamically matched with devices and automatically loaded when a device is plugged in.

The no_EEPROM case is the simplest configuration, but also the most limiting. This mode is used only for code development, utilizing Cypress software tools matched to the ID values in Table 5-6.

Reminder

The EZ-USB core uses the Table 5-6 data for enumeration only if the ReNum bit is zero. If ReNum=1, enumeration data is supplied by 8051 code.

5.7 Serial EEPROM Present, First Byte is 0xB0

Table 5-7. EEPROM Data Format for "B0" Load

EEPROM Address	Contents
0	**0xB0**
1	Vendor ID (VID) L
2	Vendor ID (VID) H
3	Product ID (PID) L
4	Product ID (PID) H
5	Device ID (DID) L
6	Device ID (DID) H
7	Not used

If, at power-on, the EZ-USB core detects an EEPROM connected to its I^2C port with the value **0xB0** at address 0, the EZ-USB core copies the Vendor ID (VID), Product ID (PID), and Device ID (DID) from the EEPROM (Table 5-7) into internal storage. The EZ-USB core then supplies these bytes to the host as part of the Get_Descriptor-Device request. (These six bytes replace only the VID/PID/DID bytes in the default USB device descriptor.) This causes a driver matched to the VID/PID/DID values in the EEPROM, instead of those in the EZ-USB core, to be loaded into the OS.

After initial enumeration, the driver downloads 8051 code and USB descriptor data into EZ-USB RAM and starts the 8051. The code then ReNumerates™ to come on as the fully custom device.

A recommended EEPROM for this application is the Microchip 24LC00, a small (5-pin SOT package) inexpensive 16-byte serial EEPROM. A 24LC01 (128 bytes) or 24LC02 (256 bytes) may be substituted for the 24LC00, but as with the 24LC00, only the first seven bytes are used.

5.8 Serial EEPROM Present, First Byte is 0xB2

If, at power-on, the EZ-USB core detects an EEPROM connected to its I^2C port with the value **0xB2** at address 0; the EZ-USB core loads the EEPROM data into EZ-USB RAM. It also sets the ReNum bit to 1, causing device requests to be fielded by the 8051 instead of the EZ-USB core. The EEPROM data format is shown in Table 5-8.

Table 5-8. EEPROM Data Format for "B2" Load

EEPROM Address	Contents
0	**0xB2**
1	Vendor ID (VID) L
2	Vendor ID (VID) H
3	Product ID (PID) L
4	Product ID (PID) H
5	Device ID (DID) L
6	Device ID (DID) H
7	Length H
8	Length L
9	StartAddr H
10	StartAddr L
---	Data block

---	Length H
---	Length L
---	StartAddr H
---	StartAddr L
---	Data block

---	0x80
---	0x01
---	0x7F
---	0x92

Last	00000000

The first byte tells the EZ-USB core to copy EEPROM data into RAM. The next six bytes (1-6) are ignored (see the text box, "VID/PID/DID in a "B2" EEPROM" on page 5-11).

One or more data records follow, starting at EEPROM address 7. The maximum value of Length H is 0x03, allowing a maximum of 1,023 bytes per record. Each data record consists of a length, a starting address, and a block of data bytes. The last data record must have the MSB of its Length H byte set to 1. The last data record consists of a single-byte load to the CPUCS register at 0x7F92. Only the LSB of this byte is significant—8051RES (CPUCS.0) is set to zero to bring the 8051 out of reset.

Serial EEPROM data can be loaded into two EZ-USB RAM spaces only.

- 8051 program/data RAM at 0x0000-0x1B40.
- The CPUCS register at 0x7F92 (only bit 0, 8051 RESET, is host-loadable).

VID/PID/DID in a "B2" EEPROM

Bytes 1-6 of a **B2** EEPROM can be loaded with VID/PID/DID bytes if it is desired at some point to run the 8051 program with ReNum=0 (EZ-USB core handles device requests), using the EEPROM VID/PID/DID rather than the Cypress Semiconductor values built into the EZ-USB core.

5.9 ReNumeration™

Three EZ-USB control bits in the USBCS (USB Control and Status) register control the ReNumeration™ process: DISCON, DISCOE, and RENUM.

USBCS **USB Control and Status** **7FD6**

b7	b6	b5	b4	b3	b2	b1	b0
WAKESRC	-	-	-	**DISCON**	**DISCOE**	**RENUM**	**SIGRSUME**
R/W	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

Figure 5-1. USB Control and Status Register

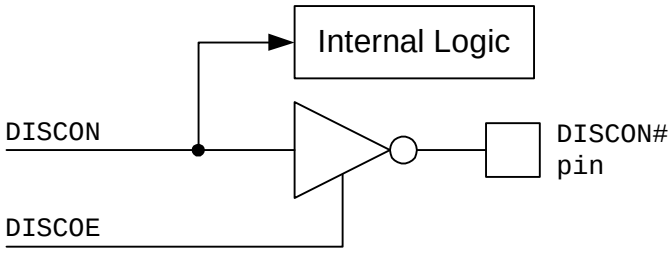


Figure 5-2. Disconnect Pin Logic

The logic for the DISCON and DISCOE bits is shown in Figure 5-2. To simulate a USB disconnect, the 8051 writes the value 00001010 to USBCS. This floats the DISCON# pin, and provides an internal DISCON signal to the USB core that causes it to perform disconnect housekeeping.

To re-connect to USB, the 8051 writes the value 00000110 to USBCS. This presents a logic HI to the DISCON# pin, enables the output buffer, and sets the RENUM bit HI to indicate that the 8051 (and not the USB core) is now in control for USB transfers. This arrangement allows connecting the 1,500-ohm resistor directly between the DISCON# pin and the USB D+ line (Figure 5-3).

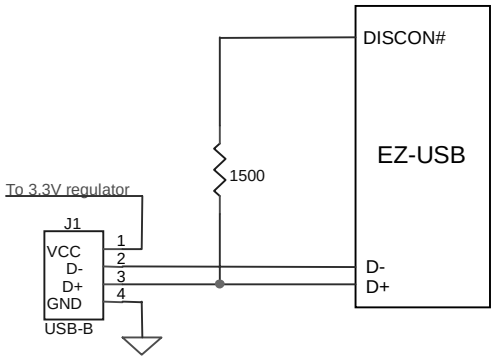


Figure 5-3. Typical Disconnect Circuit (DISCOE=1)

5.10 Multiple ReNumerations™

The 8051 can ReNumerate™ anytime. Once use for this capability might be to *fine tune* an isochronous endpoint's bandwidth requests by trying various descriptor values and ReNumerating.

5.11 Default Descriptor

Tables 5-9 through 5-19 show the descriptor data built into the EZ-USB core. The tables are presented in the order that the bytes are stored.

Table 5-9. USB Default Device Descriptor

Offset	Field	Description	Value
0	bLength	Length of this Descriptor = 18 bytes	12H
1	bDescriptorType	Descriptor Type = **Device**	01H
2	bcdUSB (L)	USB Specification Version 1.00 (L)	00H
3	bcdUSB (H)	USB Specification Version 1.00 (H)	01H
4	bDeviceClass	Device Class (FF is Vendor-Specific)	FFH
5	bDeviceSubClass	Device Sub-Class (FF is Vendor-Specific)	FFH
6	bDeviceProtocol	Device Protocol (FF is Vendor-Specific)	FFH
7	bMaxPacketSize0	Maximum Packet Size for EP0 = **64 bytes**	40H
8	idVendor (L)	Vendor ID (L) Cypress Semiconductor = 0547H	47H
9	idVendor (H)	Vendor ID (H)	05H
10	idProduct (L)	Product ID (L) EZ-USB = 2131H	31H
11	idProduct (H)	Product ID (H)	21H
12	bcdDevice (L)	Device Release Number (BCD,L) (see individual data sheet)	21H
13	bcdDevice (H)	Device Release Number (BCD,H) (see individual data sheet)	YYH
14	iManufacturer	Manufacturer Index String = None	00H
15	iProduct	Product Index String = None	00H
16	iSerialNumber	Serial Number Index String = None	00H
17	bNumConfigurations	Number of Configurations in this Interface = 1	01H

The Device Descriptor specifies a MaxPacketSize of 64 bytes for endpoint 0, contains Cypress Semiconductor Vendor, Product and Release Number IDs, and uses no string indices. Release Number IDs (*XX* and *YY*) are found in individual Cypress Semiconductor data sheets. The EZ-USB core returns this information response to a "Get_Descriptor/ Device" host request.

Table 5-10. USB Default Configuration Descriptor

Offset	Field	Description	Value
0	bLength	Length of this Descriptor = 9 bytes	09H
1	bDescriptorType	Descriptor Type = **Configuration**	02H
2	wTotalLength (L)	Total Length (L) Including Interface and Endpoint Descriptors	DAH
3	wTotalLength (H)	Total Length (H)	00H
4	bNumInterfaces	Number of Interfaces in this Configuration	01H
5	bConfigurationValue	Configuration Value Used by Set_Configuration Request to Select this Configuration	01H
6	iConfiguration	Index of String Describing this Configuration = None	00H
7	bmAttributes	Attributes - Bus-Powered, No Wakeup	80H
8	MaxPower	Maximum Power - 100 mA	32H

The configuration descriptor includes a total length field (offset 2-3) that encompasses all interface and endpoint descriptors that follow the configuration descriptor. This configuration describes a single interface (offset 4). The host selects this configuration by issuing a Set_Configuration requests specifying configuration #1 (offset 5).

Table 5-11. USB Default Interface 0, Alternate Setting 0 Descriptor

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero-based Index of this Interface = **0**	00H
3	bAlternateSetting	Alternate Setting Value = **0**	00H
4	bNumEndpoints	Number of Endpoints in this Interface (Not Counting EPO) = **0**	00H
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to String Descriptor for this Interface = None	00H

Interface 0, alternate setting 0 describes endpoint 0 only. This is a *zero bandwidth* setting. The interface has no string index.

Table 5-12. USB Default Interface 0, Alternate Setting 1 Descriptor

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptorType	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero-based Index of this Interface = **0**	00H
3	bAlternateSetting	Alternate Setting Value = **1**	01H
4	bNumEndpoints	Number of Endpoints in this Interface (Not Counting EPO) = **13**	0DH
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to String Descriptor for this Interface = None	00H

Interface 0, alternate setting 1 has thirteen endpoints, whose individual descriptors follow the interface descriptor. The alternate settings have no string indices.

Table 5-13. USB Default Interface 0, Alternate Setting 1, Interrupt Endpoint Descriptor

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN1**	81H
3	bmAttributes	XFR Type = **INT**	03H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds = **10 ms**	0AH

Interface 0, alternate setting 1 has one interrupt endpoint, IN1, which has a maximum packet size of 16 and a polling interval of 10 ms.

Table 5-14. USB Default Interface 0, Alternate Setting 1, Bulk Endpoint Descriptors

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN2**	82H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT2**	02H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN4**	84H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT4**	04H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN6**	86H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Table 5-14. USB Default Interface 0, Alternate Setting 1, Bulk Endpoint Descriptors

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT6**	06H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

Interface 0, alternate setting 1 has six bulk endpoints with max packet sizes of 64 bytes. Even numbered endpoints were chosen to allow endpoint pairing. For more on endpoint pairing, see Chapter 6, "EZ-USB Bulk Transfers."

Table 5-15. USB Default Interface 0, Alternate Setting 1, Isochronous Endpoint Descriptors

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN8**	88H
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT8**	08H
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN9**	89H
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT9**	09H
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN10**	8AH
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT10**	0AH
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

Interface 0, alternate setting 1 has six isochronous endpoints with maximum packet sizes of 16 bytes. This is a *low bandwidth* setting.

Table 5-16. USB Default Interface 0, Alternate Setting 2 Descriptor

Offset	Field	Description	Value
0	bLength	Length of the Interface Descriptor	09H
1	bDescriptor Type	Descriptor Type = **Interface**	04H
2	bInterfaceNumber	Zero-based Index of this Interface = **0**	00H
3	bAlternateSetting	Alternate Setting Value = **2**	02H
4	bNumEndpoints	Number of Endpoints in this Interface (Not Counting EPO) = **13**	0DH
5	bInterfaceClass	Interface Class = Vendor Specific	FFH
6	bInterfaceSubClass	Interface Sub-class = Vendor Specific	FFH
7	bInterfaceProtocol	Interface Protocol = Vendor Specific	FFH
8	iInterface	Index to String Descriptor for this Interface = None	00H

Interface 0, alternate setting 2 has thirteen endpoints, whose individual descriptors follow the interface descriptor. Alternate setting 2 differs from alternate setting 1 in the maximum packet sizes of its interrupt endpoint and two of its isochronous endpoints (EP8IN and EP8OUT).

Table 5-17. USB Default Interface 0, Alternate Setting 1, Interrupt Endpoint Descriptor

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN1**	81H
3	bmAttributes	XFR Type = **INT**	03H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds = **10 ms**	0AH

Alternate setting 2 for the interrupt 1-IN increases the maximum packet size for the interrupt endpoint to 64.

Table 5-18. USB Default Interface 0, Alternate Setting 2, Bulk Endpoint Descriptors

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptor Type	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN2**	82H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT2**	02H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN4**	84H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT4**	04H
3	bmAttributes	XFR Type = **ISO**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN6**	86H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT6**	06H
3	bmAttributes	XFR Type = **BULK**	02H
4	wMaxPacketSize (L)	Maximum Packet Size = **64 Bytes**	40H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	00H

The bulk endpoints for alternate setting 2 are identical to alternate setting 1.

Table 5-19. USB Default Interface 0, Alternate Setting 2, Isochronous Endpoint Descriptors

Offset	Field	Description	Value
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN8**	88H
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **256 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	01H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT8**	08H
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **256 Bytes**	00H
5	wMaxPacketSize (H)	Maximum Packet Size - High	10H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN9**	89H
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT9**	09H
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **IN10**	8AH
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H
0	bLength	Length of this Endpoint Descriptor	07H
1	bDescriptorType	Descriptor Type = **Endpoint**	05H
2	bEndpointAddress	Endpoint Direction (1 is in) and Address = **OUT10**	0AH
3	bmAttributes	XFR Type = **ISO**	01H
4	wMaxPacketSize (L)	Maximum Packet Size = **16 Bytes**	10H
5	wMaxPacketSize (H)	Maximum Packet Size - High	00H
6	bInterval	Polling Interval in Milliseconds (1 for iso)	01H

The only differences between alternate settings 1 and 2 are the maximum packet sizes for EP8IN and EP8OUT. This is a *high-bandwidth* setting using 256 bytes each.

6 EZ-USB Bulk Transfers

6.1 Introduction

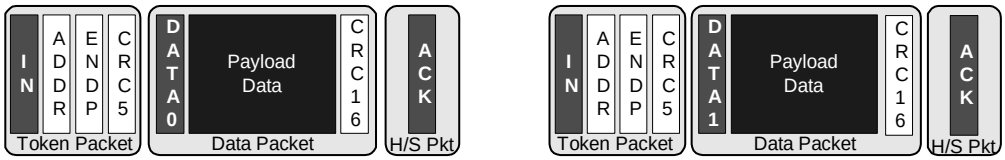


Figure 6-1. Two BULK Transfers, IN and OUT

EZ-USB provides sixteen endpoints for BULK, CONTROL, and INTERRUPT transfers, numbered 0-7 as shown in Table 6-1. This chapter describes BULK and INTERRUPT transfers. INTERRUPT transfers are a special case of BULK transfers. EZ-USB CONTROL endpoint zero is described in Chapter 7, "EZ-USB Endpoint Zero."

Table 6-1. EZ-USB Bulk, Control, and Interrupt Endpoints

Endpoint	Direction	Type	Size
0	Bidir	Control	64/64
1	IN	Bulk/Int	64
1	OUT	Bulk/Int	64
2	IN	Bulk/Int	64
2	OUT	Bulk/Int	64
3	IN	Bulk/Int	64
3	OUT	Bulk/Int	64
4	IN	Bulk/Int	64
4	OUT	Bulk/Int	64
5	IN	Bulk/Int	64
5	OUT	Bulk/Int	64
6	IN	Bulk/Int	64
*6	OUT	Bulk/Int	64
7	IN	Bulk/Int	64
7	OUT	Bulk/Int	64

* The highlighted endpoints do not exist in the AN2122 or AN2126. See also Table 1-2.

The USB specification allows maximum packet sizes of 8, 16, 32, or 64 bytes for bulk data, and 1 - 64 bytes for interrupt data. EZ-USB provides the maximum 64 bytes of buffer space for each of its sixteen endpoints 0-7 IN and 0-7 OUT. Six of the bulk endpoints, 2-IN, 4-IN, 6-IN, 2-OUT, 4-OUT, and 6-OUT may be paired with the next consecutively numbered endpoint to provide double-buffering, which allows one data packet to be serviced by the 8051 while another is in transit over USB. Six *endpoint pairing bits* (USBPAIR register) control double-buffering.

The 8051 sets fourteen *endpoint valid bits* (IN07VAL, OUT07VAL registers) at initialization time to tell the EZ-USB core which endpoints are active. The default CONTROL endpoint zero is always valid.

Bulk data appears in RAM. Each bulk endpoint has a reserved 64-byte RAM space, a 7-bit count register, and a 2-bit control and status (CS) register. The 8051 can read one bit of the CS register to determine *endpoint busy,* and write the other to force an endpoint STALL condition.

The 8051 should never read or write an endpoint buffer or byte count register while the endpoint's busy bit is set.

When an endpoint becomes ready for 8051 service, the EZ-USB core sets an interrupt request bit. The EZ-USB vectored interrupt system separates the interrupt requests by endpoint to automatically transfer control to the ISR (Interrupt Service Routine) for the endpoint requiring service. Chapter 9, "EZ-USB Interrupts" fully describes this mechanism.

Figure 6-2 illustrates the registers and bits associated with bulk transfers.

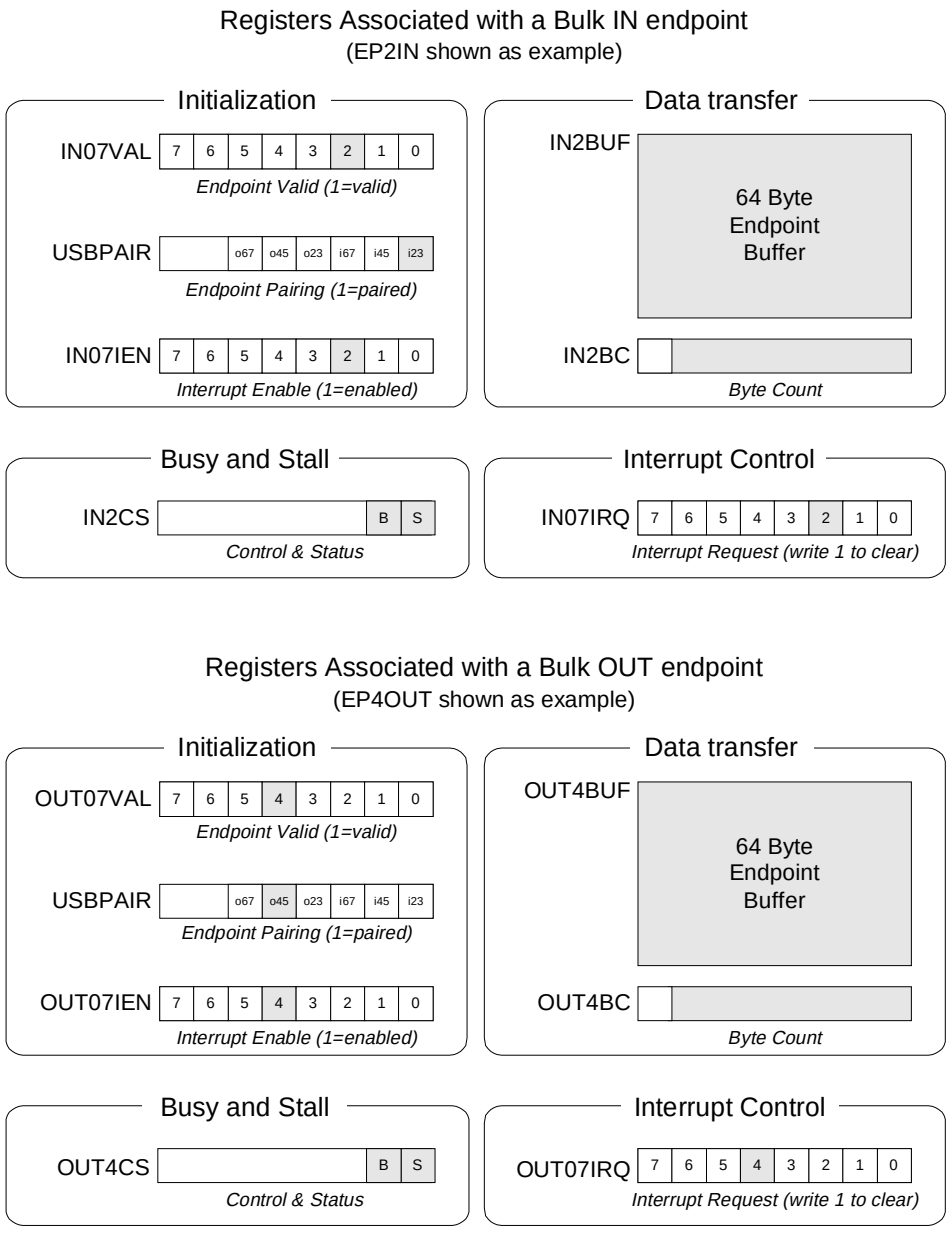


Figure 6-2. Registers Associated with Bulk Endpoints

6.2 Bulk IN Transfers

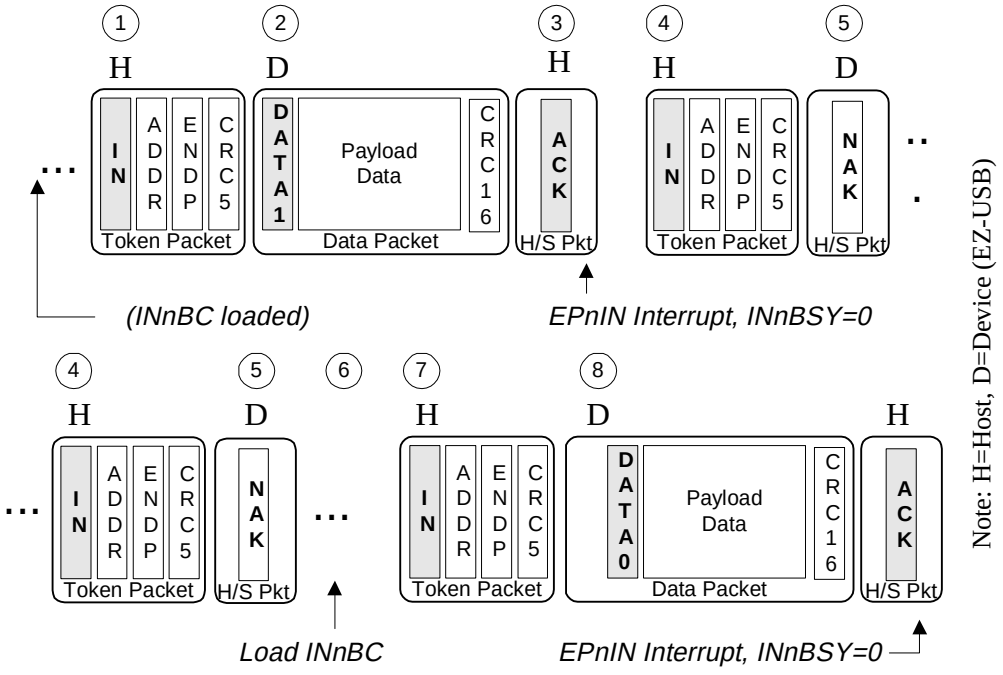


Figure 6-3. Anatomy of a Bulk IN Transfer

USB bulk *IN* data travels from device to host. The host requests an IN transfer by issuing an IN token to the EZ-USB core, which responds with data when it is ready. The 8051 indicates *ready* by loading the endpoint's byte count register. If the EZ-USB core receives an IN token for an endpoint that is not ready, it responds to the IN token with a *NAK* handshake.

In the bulk IN transfer illustrated in Figure 6-3, the 8051 has previously loaded an endpoint buffer with a data packet, and then loaded the endpoint's byte count register with the number of bytes in the packet to arm the next IN transfer. This sets the endpoint's BUSY Bit. The host issues an IN token (1), to which the USB core responds by transmitting the data in the IN endpoint buffer (2). When the host issues an ACK (3), indicating that the data has been received error-free, the USB core clears the endpoint's BUSY Bit and sets its interrupt request bit. This notifies the 8051 that the endpoint buffer is empty. If this is a multi-packet transfer, the host then issues another IN token to get the next packet.

If the second IN token (4) arrives before the 8051 has had time to fill the endpoint buffer, the EZ USB core issues a NAK handshake, indicating *busy* (5). The host continues to send

IN tokens (4) and (7) until the data is ready. Eventually, the 8051 fills the endpoint buffer with data, and then loads the endpoint's byte count register (INnBC) with the number of bytes in the packet (6). Loading the byte count re-arms the given endpoint. When the next IN token arrives (7) the USB core transfers the next data packet (8).

6.3 Interrupt Transfers

Interrupt transfers are handled just like bulk transfers.

The only difference between a bulk endpoint and an interrupt endpoint exists in the endpoint descriptor, where the endpoint is identified as type *interrupt*, and a *polling interval* is specified. The polling interval determines how often the USB host issues IN tokens to the interrupt endpoint.

6.4 EZ-USB Bulk IN Example

Suppose 220 bytes are to be transferred to the host using endpoint 2-IN. Further assume that MaxPacketSize of 64 bytes for endpoint 2-IN has been reported to the host during enumeration. Because the total transfer size exceeds the maximum packet size, the 8051 divides the 220-byte transfer into four transfers of 64, 64, 64, and 28 bytes.

After loading the first 64 bytes into IN2BUF (at 0x7C00), the 8051 loads the byte count register IN6BC with the value 64. Writing the byte count register instructs the EZ-USB core to respond to the next host IN token by transmitting the 64 bytes in the buffer. Until the byte count register is loaded to *arm* the IN transfer, any IN tokens issued by the host are answered by EZ-USB with NAK (Not-Acknowledge) tokens, telling the USB host that the endpoint is not yet ready with data. The host continues to issue IN tokens to endpoint 2-IN until data is ready for transfer—whereupon the EZ-USB core replaces NAKs with valid data.

When the 8051 initiates an IN transfer by loading the endpoint's byte count register, the EZ-USB core sets a busy bit to instruct the 8051 to hold off loading IN2BUF until the USB transfer is finished. When the IN transfer is complete and successfully acknowledged, the EZ-USB core resets the endpoint 2-IN busy bit and generates an endpoint 2-IN interrupt request. If the endpoint 2-IN interrupt is enabled, program control automatically vectors to the data transfer routine for further action (Autovectoring is enabled by setting AVEN=1; refer to Chapter 9, "EZ-USB Interrupts").

The 8051 now loads the next 64 bytes into IN2BUF and then loads the EPINBC register with 64 for the next two transfers. For the last portion of the transfer, the 8051 loads the final 28 bytes into IN2BUF, and loads IN2BC with 28. This completes the transfer.

Initialization Note

When the EZ-USB chip comes out of RESET, or when the USB host issues a bus reset, the EZ-USB core **unarms** IN endpoint 1-7 by setting their busy bits to 0. Any IN transfer requests are NAKd until the 8051 loads the appropriate INxBC register(s). The endpoint valid bits are not affected by an 8051 reset or a USB reset. Chapter 10, "EZ-USB Resets" describes the various reset conditions in detail.

The EZ-USB core takes care of USB housekeeping chores such as handshake verification. When an endpoint 2-IN interrupt occurs, the user is assured that the data loaded by the 8051 into the endpoint buffer was received error-free by the host. The EZ-USB core automatically checks the handshake information from the host and re-transmits the data if the host indicates an error by not ACKing.

6.5 Bulk OUT Transfers

USB bulk *OUT* data travels from host to device. The host requests an OUT transfer by issuing an OUT token to EZ-USB, followed by a packet of data. The EZ-USB core then responds with an ACK, if it correctly received the data. If the endpoint buffer is not ready to accept data, the EZ-USB core discards the host's OUT data and returns a NAK token, indicating "not ready." In response, the host continues to send OUT tokens *and data* to the endpoint until the EZ-USB core responds with an ACK.

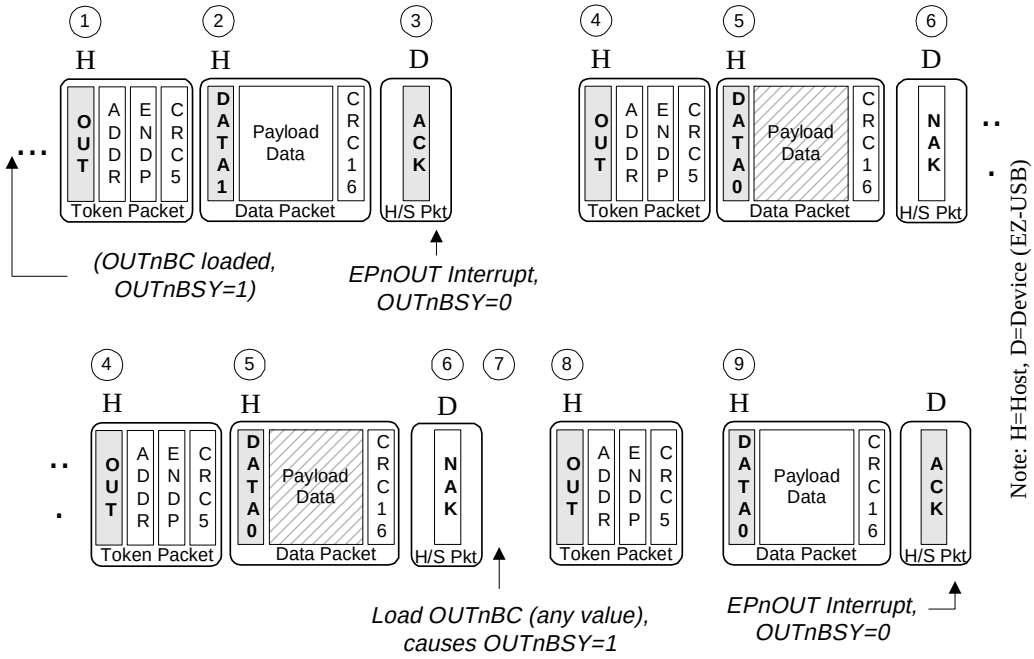


Figure 6-4. Anatomy of a Bulk OUT Transfer

Each EZ-USB bulk OUT endpoint has a byte count register, which serves two purposes. The 8051 *reads* the byte count register to determine how many bytes were received during the last OUT transfer from the host. The 8051 *writes* the byte count register (with any value) to tell the EZ-USB core that is has finished reading bytes from the buffer, making the buffer available to accept the next OUT transfer. The OUT endpoints come up (after reset) *armed*, so the byte count register writes are required only for OUT transfers after the first one.

In the bulk OUT transfer illustrated in Figure 6-4, the 8051 has previously loaded the endpoint's byte count register with any value to arm receipt of the next OUT transfer. Loading the byte count register causes the EZ-USB core to set the OUT endpoint's busy bit to 1, indicating that the 8051 should not use the endpoint's buffer.
The host issues an OUT token (1), followed by a packet of data (2), which the USB core acknowledges, clears the endpoint's busy bit and generates an interrupt request (3). This notifies the 8051 that the endpoint buffer contains valid USB data. The 8051 reads the endpoint's byte count register to find out how many bytes were sent in the packet, and transfers that many bytes out of the endpoint buffer.

In a multi-packet transfer, the host then issues another OUT token (4) along with the next data packet (5). If the 8051 has not finished emptying the endpoint buffer, the EZ-USB FX

host issues a NAK, indicating *busy* (6). The data at (5) is shaded to indicate that the USB core discards it, and does not over-write the data in the endpoint's OUT buffer.

The host continues to send OUT tokens (4, 5, and 6) that are greeted by NAKs until the buffer is ready. Eventually, the 8051 empties the endpoint buffer data, and then loads the endpoint's byte count register (7) with any value to re-arm the USB core. Once armed and when the next OUT token arrives (8) the USB core accepts the next data packet (9).

Initializing OUT Endpoints

When the EZ-USB chip comes out of reset, or when the USB host issues a bus reset, the EZ-USB core *arms* OUT endpoints 1-7 by setting their busy bits to 1. Therefore, they are initially ready to accept one OUT transfer from the host. Subsequent OUT transfers are NAKd until the appropriate OUTnBC register is loaded to re-arm the endpoint.

The EZ-USB core takes care of USB housekeeping chores such as CRC checks and data toggle PIDs. When an endpoint 6-OUT interrupt occurs and the busy bit is cleared, the user is assured that the data in the endpoint buffer was received error-free from the host. The EZ-USB core automatically checks for errors and requests the host to re-transmit data if it detects any errors using the built-in USB error checking mechanisms (CRC checks and data toggles).

6.6 Endpoint Pairing

Table 6-2. Endpoint Pairing Bits (in the USB PAIR Register)

Bit	5	4	3	2	1	0
Name	PR6OUT	PR4OUT	PR2OUT	PR6IN	PR4IN	PR2IN
Paired	6 OUT	4 OUT	2 OUT	6 IN	4 IN	2 IN
Endpoints	7 OUT	5 OUT	3 OUT	7 IN	5 IN	3 IN

The 8051 sets endpoint pairing bits to 1 to enable double-buffering of the bulk endpoint buffers. With double buffering enabled, the 8051 can operate on one data packet while another is being transferred over USB. The endpoint busy and interrupt request bits function identically, so the 8051 code requires little code modification to support double-buffering.

When an endpoint is paired, the 8051 uses only the even-numbered endpoint of the pair. The 8051 should not use the paired odd endpoint. For example, suppose it is desired to

use endpoint 2-IN as a double-buffered endpoint. This pairs the IN2BUF and IN3BUF buffers, although the 8051 accesses the IN2BUF buffer only. The 8051 sets PR2IN=1 (in the USBPAIR register) to enable pairing, sets IN2VAL=1 (in the IN07VAL register) to make the endpoint valid, and then uses the IN2BUF buffer for all data transfers. The 8051 should not write the IN3VAL bit, enable IN3 interrupts, access the EP3IN buffer, or load the IN3BC byte count register.

Note

Bits 2 and 5 must be set to "0" in the AN2122 and AN2126 devices.

6.7 Paired IN Endpoint Status

INnBSY=1 indicates that *both* endpoint buffers are in use, and the 8051 should not load new IN data into the endpoint buffer. When INnBSY=0, either one or both of the buffers is available for loading by the 8051. The 8051 can keep an internal count that increments on EPnIN interrupts and decrements on byte count loads to determine whether one or two buffers are free. Or, the 8051 can simply check for INnBSY=0 after loading a buffer (and loading its byte count register to re-arm the endpoint) to determine if the other buffer is free.

Important Note

If an IN endpoint is paired and it is desired to clear the busy bit for that endpoint, do the following: (a) write any value to the even endpoint's byte count register *twice*, and (b) clear the busy bit for both endpoints in the pair. This is the only code difference between paired and unpaired use of an IN endpoint.

A bulk IN endpoint interrupt request is generated whenever a packet is successfully transmitted over USB. The interrupt request is independent of the busy bit. If both buffers are filled and one is sent, the busy bit transitions from 1-0; if one buffer is filled and then sent, the busy bit starts and remains at 0. In either case an interrupt request is generated to tell the 8051 that a buffer is free.

6.8 Paired OUT Endpoint Status

OUTnBSY=1 indicates that both endpoint buffers are empty, and no data is available to the 8051. When OUTnBSY=0, either one or both of the buffers holds USB OUT data. The 8051 can keep an internal count that increments on EPnOUT interrupts and decrements on byte count loads to determine whether one or two buffers contain data. Or, the 8051 can simply check for OUTnBSY=0 after unloading a buffer (and loading its byte count register to re-arm the endpoint) to determine if the *other* buffer contains data.

6.9 Using Bulk Buffer Memory

Table 6-3. EZ-USB Endpoint 0-7 Buffer Addresses

Endpoint Buffer	Address	Mirrored
IN0BUF	7F00-7F3F	1F00-1F3F
OUT0BUF	7EC0-7EFF	1EC0-1EFF
IN1BUF	7E80-7EBF	1E80-1EBF
OUT1BUF	7E40-7E7F	1E40-1E7F
IN2BUF	7E00-7E3F	1E00-1E3F
OUT2BUF	7DC0-7DFF	1DC0-1DFF
IN3BUF	7D80-7DBF	1D80-1DBF
OUT3BUF	7D40-7D7F	1D40-1D7F
IN4BUF	7D00-7D3F	1D00-1D3F
OUT4BUF	7CC0-7CFF	1CC0-1CFF
IN5BUF	7C80-7CBF	1C80-1CBF
OUT5BUF	7C40-7C7F	1C40-1C7F
IN6BUF	7C00-7C3F	1C00-1C3F
OUT6BUF	7BC0-7BFF	1BC0-1BFF
IN7BUF	7B80-7BBF	1B80-1BBF
OUT7BUF	7B40-7B7F	1B40-1B7F

Table 6-3 shows the RAM locations for the sixteen 64-byte buffers for endpoints 0-7 IN and OUT. These buffers are positioned at the bottom of the EZ-USB register space so that any buffers not used for endpoints can be reclaimed as general purpose data RAM. The top of memory for the 8-KB EZ-USB part is at 0x1B3F. However, if the endpoints are allocated in ascending order starting with the lowest numbered endpoints, the higher numbered unused endpoints can effectively move the top of memory to utilize the unused endpoint buffer RAM as data memory. For example, an application that uses endpoint 1-IN,

2-IN/OUT (paired), 4-IN and 4-OUT can use 0x1B40-0x1CBF as data memory. Chapter 3 gives full details of the EZ-USB memory map.

Note

AN2122 endpoint memory starts at 0x1C00 and AN2126 endpoint memory starts at address 0x7C00.

Note

Uploads or Downloads to unused bulk memory can be done only at the *Mirrored* (low) addresses shown in Table 6-3.

6.10 Data Toggle Control

The EZ-USB core automatically maintains the data toggle bits during bulk, control and interrupt transfers. As explained in Chapter 1, "Introducing EZ-USB," the toggle bits are used to detect certain transmission errors so that erroneous data can be re-sent.

In certain circumstances, the host resets its data toggle to “DATA0”:

- After sending a Clear_Feature: Endpoint Stall request to an endpoint.
- After setting a new interface.
- After selecting a new alternate setting.

In these cases, the 8051 can directly clear the data toggle for each of the bulk/interrupt/ control endpoints, using the TOGCTL register (Figure 6-5).

TOGCTL **Data Toggle Control** **7FD7**

b7	b6	b5	b4	b3	b2	b1	b0
Q	**S**	**R**	**IO**	**0**	**EP2**	**EP1**	**EP0**
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 6-5. Bulk Endpoint Toggle Control

The IO bit selects the endpoint direction (1=IN, 0=OUT), and the EP2-EP1-EP0 bits select the endpoint number. The *Q* bit, which is read-only, indicates the state of the data toggle for the selected endpoint. Writing R=1 sets the data toggle to DATA0, and writing S=1 sets the data toggle to DATA1.

Note

At the present writing, there appears to be no reason to set a data toggle to DATA1. The *S* bit is provided for generality.

To clear an endpoint's data toggle, the 8051 performs the following sequence:

- Select the endpoint by writing the value 000D0EEE to the TOGCTL register, where D is the direction and EEE is the endpoint number.
- Clear the toggle bit by writing the value 001D0EEE to the TOGCTL register.

After step 1, the 8051 may read the state of the data toggle by reading the TOGCTL register checking bit 7.

6.11 Polled Bulk Transfer Example

The following code illustrates the EZ-USB registers used for a simple bulk transfer. In this example, 8051 register R1 keeps track of the number of endpoint 2-IN transfers and register R2 keeps track of the number of endpoint 2-OUT transfers (mod-256). Every endpoint 2-IN transfer consists of 64 bytes of a decrementing count, with the first byte replaced by the number of IN transfers and the second byte replaced by the number of OUT transfers.

```
1  start:          mov       SP,#STACK-1         ; set stack
2                  mov       dptr,#IN2BUF        ; fill EP2IN buffer with
3                  mov       r7,#64              ; decrementing counter
4  fill:           mov       a,r7
5                  movx      @dptr,a
6                  inc       dptr
7                  djnz      r7,rill
8  ;
9                  mov       r1,#0               ; r1 is IN token counter
10                 mov       r2,#0               ; r2 is OUT token counter
11                 mov       dptr,#IN2BC         ; Point to EP2 Byte Count register
12                 mov       a,#40h              ; 64-byte transfer
13                 movx      @dptr,a             ; arm the IN2 transfer
14 ;
15 loop:           mov       dptr,#IN2CS         ; poll the EP2-IN Status
16 movx            a,@dptr
17                 jnb       acc.1,serviceIN2    ; not busy--keep looping
18                 mov       dptr,#OUT2CS
19                 movx      a,@dptr
20                 jb        acc.1,loop          ; EP2OUT is busy--keep looping
21 ;
22 serviceOUT2:
23                 inc       r2                  ; OUT packet counter
24                 mov       dptr,#OUT2BC        ; load byte count register to re-arm
25                 movx      @dptr,a             ; (any value)
26                 sjmp      loop
27 ;
28 serviceIN2:
29                 inc       r1                  ; IN packet counter
30                 mov       dptr,3IN2BUF        ; update the first data byte
31                 mov       a,r1                ; in EP2IN buffer
32                 movx      @dptr,a
33                 inc       dptr                ; second byte in buffer
34                 mov       a,r2                ; get number of OUT packets
35                 movx      @dptr,a
36                 mov       dptr,#IN2BC         ; point to EP2IN Byte Count Register
37                 mov       a,#40h
38                 movx      @dptr,a             ; load bc=64 to re-arm IN2
39                 sjmp      loop
40 ;
41                 END
```

Figure 6-6. Example Code for a Simple (Polled) BULK Transfer

The code at lines 2-7 fills the endpoint 2-IN buffer with 64 bytes of a decrementing count. Two 8-bit counts are initialized to zero at lines 9 and 10. An endpoint 2-IN transfer is *armed* at lines 11-13, which load the endpoint 2-IN byte count register IN2BC with 64. Then the program enters a polling loop at lines 15-20, where it checks two flags for endpoint 2 servicing. Lines 15-17 check the endpoint 2-IN busy bit in IN2CS bit 1. Lines 18-20 check the endpoint 2-OUT busy bit in OUT2CS bit 1. When busy=1, the EZ-USB core is currently using the endpoint buffers and the 8051 should not access them. When busy=0, new data is ready for service by the 8051.

For both IN and OUT endpoints, the busy bit is set when the EZ-USB core is using the buffers, and cleared by loading the endpoint's byte count register. The byte count value is meaningful for IN transfers because it tells the EZ-USB core how many bytes to transfer in response to the next IN token. The 8051 can load any byte count OUT transfers, because only the act of loading the register is significant—loading OUTnBC arms the OUT transfer and sets the endpoint's busy bit.

When an OUT packet arrives in OUT2BUF, the service routine at lines 22-26 increments R2, loads the byte count (any value) into OUT2BC to re-arm the endpoint (lines 24-25), and jumps back to the polling routine. This program does not use OUT2BUF data; it simply counts the number of endpoint 2-OUT transfers.

When endpoint 2-IN is ready for the 8051 to load another packet into IN2BUF, the polling loop jumps to the endpoint 2-IN service routine at lines 28-39. First, R1 is incremented (line 29). The data pointer is set to IN2BUF at line 30, and register R1 is loaded into the first byte of the buffer (lines 31-32). The data pointer is advanced to the second byte of IN2BUF at line 33, and register R2 is loaded into the buffer (lines 34-35). Finally, the byte count 40H (64 decimal bytes) is loaded into the byte count register IN2BC to arm the next IN transfer at lines 36-38, and the routine returns the polling loop.

6.12 Enumeration Note

The code in this example is complete, and runs on the EZ-USB chip. You may be wondering about the *missing step*, which reports the endpoint characteristics to the host during the enumeration process. The reason this code runs without any enumeration code is that the EZ-USB chip comes on as a fully-functional USB device with certain endpoints already configured and reported to the host. Endpoint 2 is included in this default configuration. The full default configuration is described in Chapter 5, "EZ-USB Enumeration and ReNumeration™"

6.13 Bulk Endpoint Interrupts

All USB interrupts activate the 8051 *INT 2* interrupt. If enabled, INT2 interrupts cause the 8051 to push the current program counter onto the stack, and then execute a jump to location 0x43, where the programmer has inserted a jump instruction to the interrupt service routine (ISR). If the AVEN (Autovector Enable) bit is set, the EZ-USB core inserts a special byte at location 0x45, which directs the jump instruction to a table of jump instructions which transfer control the endpoint-specific ISR.

Table 6-4. 8051 INT2 Interrupt Vector

Location	Op-Code	Instruction
0x43	02	LJMP
0x44	AddrH	
0x45	AddrL*	

* Replaced by EZ-USB Core if AVEN=1.

The byte inserted by the EZ-USB core at address 0x45 depends on which bulk endpoint requires service. Table 6-5 shows all INT2 vectors, with the bulk endpoint vectors unshaded. The shaded interrupts apply to all the bulk endpoints.

Table 6-5. Byte Inserted by EZ-USB Core at Location 0x45 if AVEN=1

Interrupt	Inserted Byte at 0x45
SUDAV	**0x00**
SOF	**0x04**
SUTOK	**0x08**
SUSPEND	**0x0C**
USBRES	**0x10**
Reserved	**0x14**
EP0-IN	**0x18**
EP0-OUT	**0X1C**
EP1-IN	**0x20**
EP1OUT	**0x24**
EP2IN	**0x28**
EP2OUT	**0x2C**
EP3-IN	**0x30**
EP3-OUT	**0x34**
EP4-IN	**0x38**
EP4-OUT	**0x3C**
EP5-IN	**0x40**
EP5-OUT	**0x44**
EP6-IN	**0x48**
EP6-OUT	**0x4C**
EP7-IN	**0x50**
EP7-OUT	**0x54**

The vector values are four bytes apart. This allows the programmer to build a jump table to each of the interrupt service routines. Note that the jump table must begin on a page (256 byte) boundary because the first vector starts at 00. If Autovectoring is not used (AVEN=0), the IVEC register may be directly inspected to determine the USB interrupt source (see Section 9.11, "Autovector Coding").

Each bulk endpoint interrupt has an associated interrupt enable bit (in IN07IEN and OUT07IEN), and an interrupt request bit (in IN07IRQ and OUT07IRQ). The interrupt service routine. *IRQ bits are cleared by writing a "1."* Because all USB registers are accessed using "movx@dptr" instructions, USB interrupt service routines must save and restore both data pointers, the DPS register, and the accumulator before clearing interrupt request bits.

Note

Any USB ISR should clear the 8051 INT2 interrupt request bit before clearing any of the EZ-USB endpoint IRQ bits, to avoid losing interrupts. Interrupts are discussed in more detail in Chapter 9, "EZ-USB Interrupts."

Individual interrupt request bits are cleared by writing "1" to them to simplify code. For example, to clear the endpoint 2-IN IRQ, simply write "0000100" to IN07IRQ. This will not disturb the other interrupt request bits. **Do *not* read the contents of IN07IRQ, logical-OR the contents with 01, and write it back**. This clears all other pending interrupts because you are writing "1"s to them.

6.14 Interrupt Bulk Transfer Example

This simple (but fully-functional) example illustrates the bulk transfer mechanism using interrupts. In the example program, BULK endpoint 6 is used to loop data back to the host. Data sent by the host over endpoint 2-OUT is sent back over endpoint 2-IN.

1. Set up the jump table.

```
                CSEG    AT 300H         ; any page boundary
USB_Jump_Table:
                ljmp    SUDAV_ISR       ; SETUP Data Available
                db      0               ; make a 4-byte entry
                ljmp    SOF_ISR         ; SOF
                db      0
                ljmp    SUTOK_ISR       ; SETUP Data Loading
                db      0
                ljmp    SUSP_ISR        ; Global Suspend
                db      0
                ljmp    URES_ISR        ; USB Reset
                db      0
                ljmp    SPARE_ISR
                db      0
                ljmp    EP0IN_ISR
                db      0
                ljmp    EP0OUT_ISR
                db      0
                ljmp    EP1IN_ISR
                db      0
                ljmp    EP1OUT_ISR
                db      0
                ljmp    EP2IN_ISR
                db      0
                ljmp    EP2OUT_ISR
                db      0
                ljmp    EP3IN_ISR
                db      0
                ljmp    EP3OUT_ISR
                db      0
                ljmp    EP4IN_ISR
                db      0
                ljmp    EP4OUT_ISR
                db      0
                ljmp    EP5IN_ISR
                db      0
                ljmp    EP5OUT_ISR
                db      0
                ljmp    EP6IN_ISR       ; Used by this example
                db      0
                ljmp    EP6OUT_ISR      ; Used by this example
                db      0
                ljmp    EP7IN_ISR
                db      0
                ljmp    EP7OUT_ISR
                db      0
```

Figure 6-7. Interrupt Jump Table

This table contains all of the USB interrupts, even though only the jumps for endpoint 2 are used for the example. It is convenient to include this table in any USB application that uses interrupts. Be sure to locate this table on a page boundary (xx00).

2. Write the INT2 interrupt vector.

```
; -----------------
; Interrupt Vectors
; -----------------
        org             43h                     ; int2 is the USB vector
        ljmp            USB_Jump_Table          ; Autovector will replace byte 45
```

Figure 6-8. INT2 Interrupt Vector

3. Write the interrupt service routine.

Put it anywhere in memory and the jump table in step 1 will automatically jump to it.

```
; ----------------------------
; USB Interrupt Service Routine
; ----------------------------
EP2OUT_ISR   push   dps             ; save both dptrs, dps, and acc
             push   dpl
             push   dph
             push   dpl1
             push   dph1
             push   acc

             mov    a,EXIF           ; clear USB IRQ (INT2)
             clr    acc.4
             mov    EXIF,a

             mov    dptr,#OUT07IRQ
             mov    a,#01000000b     ;  a “1” clears the IRQ bit
             movx   @dptr,a          ; clear OUT2 int request
             setb   got_EP2_data     ; set my flag

             pop    acc              ; restore vital registers
             pop    dph1
             pop    dpl1
             pop    dph
             pop    dpl
             pop    dps
             reti
```

Figure 6-9. Interrupt Service Routine (ISR) for Endpoint 2-OUT

In this example, the ISR simply sets the 8051 flag “got_EP2_data” to indicate to the background program that the endpoint requires service. Note that both data pointers and the DPS (Data Pointer Select) registers must be saved and restored in addition to the accumulator.

4. Write the endpoint 2 transfer program.

```
1  loop:      jnb    got_EP2_data,loop
2             clr    got_EP2_data          ; clear my flag
3  ;
4  ; The user sent bytes to OUT2 endpoint using the USB Control Panel.
5  ; Find out how many bytes were sent.
6  ;
7             mov    dptr,#OUT2BC          ; point to OUT2 byte count register
8             movx   a,@dptr               ; get the value
9             mov    r7,a                  ; stash the byte count
10            mov    r6,a                  ; save here also
11 ;
12 ; Transfer the bytes received on the OUT2 endpoint to the IN2 endpoint
13 ; buffer.  Number of bytes in r6 and r7.
14 ;
15            mov    dptr,#OUT2BUF         ; first data pointer points to EP2OUT buffer
16            inc    dps                   ; select the second data pointer
17            mov    dptr,#IN2BUF          ; second data pointer points to EP2IN buffer
18            inc    dps                   ; back to first data pointer
19 transfer:  movx   movx                  get OUT byte
20            inc    dptr                  ; bump the pointer
21            inc    dps                   ; second data pointer
22            movx   @dptr,a               ; put into IN buffer
23            inc    dptr                  ; bump the pointer
24            inc    dps                   ; first data pointer
25            djnz   r7,transfer
26 ;
27 ; Load the byte count into IN2BC.  This arms in IN transfer
28 ;
29            mov    dptr,#IN2BC
30            mov    a,r6                  ; get other saved copy of byte count
31            movx   @dptr,a               ; this arms the IN transfer
32 ;
33 ; Load any byte count into OUT2BC.  This arms the next OUT transfer.
34 ;
35            mov    dptr,#OUT2BC
36            movx   @dptr,a               ; use whatever is in acc
37            sjmp   loop                  ; start checking for another OUT2 packet
```

Figure 6-10. Background Program Transfers Endpoint 2-OUT Data to Endpoint 2-IN

The main program loop tests the “got_EP2_data” flag, waiting until it is set by the endpoint 2 OUT interrupt service routine in Figure 6-10. This indicates that a new data packet has arrived in OUT2BUF. Then the service routine is entered, where the flag is cleared in line 2. The number of bytes received in OUT2BUF is retrieved from the OUT2BC register (Endpoint 2 Byte Count) and saved in registers R6 and R7 in lines 7-10.

The dual data pointers are initialized to the source (OUT2BUF) and destination (IN2BUF) buffers for the data transfer in lines 15-18. These labels represent the start of the 64-byte buffers for endpoint 2-OUT and endpoint 2-IN, respectively. Each byte is read from the OUT2BUF buffer and written to the IN2BUF buffer in lines 19-25. The saved value of

OUT2BC is used as a loop counter in R7 to transfer the exact number of bytes that were received over endpoint 2-OUT.

When the transfer is complete, the program loads the endpoint 2-IN byte count register IN2BC with the number of loaded bytes (from R6) to *arm* the next endpoint 2-IN transfer in lines 29-31. Finally, the 8051 loads any value into the endpoint 2 OUT byte count register OUT2BC to arm the next OUT transfer in lines 35-36. Then the program loops back to check for more endpoint 2-OUT data.

5. Initialize the endpoints and enable the interrupts.

```
start:    mov     SP,#STACK-1       ; set stack
;
; Enable USB interrupts and Autovector
;
          mov     dptr,#USBBAV      ; enable Autovector
          movx    a,@dptr,a
          setb    acc.0             ; AVEN bit is bit 0
          movx    @dptr,a
;
          mov     dptr,#OUT07IEN    ; 'EP0-7 OUT int enables' register
;         mov     a,#01000000b      ; set bit 6 for EP2OUT interrupt enable
          movx    @dptr,a           ; enable EP2OUT interrupt
;
; Enable INT2 and 8051 global interrupts
;
          setb    ex2               ; enable int2 (USB interrupt)
          setb    EA                ; enable 8051 interrupts
          clr     got_EP2_data      ; clear my flag
```

Figure 6-11. Initialization Routine

The initialization routine sets the stack pointer, and enables the EZ-USB Autovector by setting USBBAV.0 to 1. Then it enables the endpoint 2-OUT interrupt, all USB interrupts (INT2), and the 8051 global interrupt (EA) and finally clears the flag indicating that endpoint 2-OUT requires service.

Once this structure is put into place, it is quite easy to service any or all of the bulk endpoints. To add service for endpoint 2-IN, for example, simply write an endpoint 2-IN interrupt service routine with starting address EP2IN_ISR (to match the address in the jump table in step 1), and add its valid and interrupt enable bits to the "init" routine.

6.15 Enumeration Note

The code in this example is complete, and runs on the EZ-USB chip. You may be wondering about the *missing step*, which reports the endpoint characteristics to the host during the enumeration process. The reason this code runs without any enumeration code is that the EZ-USB chip comes on as a fully-functional USB device with certain endpoints already configured and reported to the host. Endpoint 2 is included in this default configuration. The full default configuration is described in Chapter 5, "EZ-USB Enumeration and ReNumeration™"

Portions of the above code are not necessary for the default configuration (such as setting the endpoint valid bits) but the code is included to illustrate all of the EZ-USB registers used for bulk transfers.

6.16 The Autopointer

Bulk endpoint data is available in 64-byte buffers in EZ-USB RAM. In some cases it is preferable to access bulk data as a FIFO register rather than as a RAM. The EZ-USB core provides a special data pointer which automatically increments when data is transferred. Using this Autopointer, the 8051 can access any contiguous block of internal EZ-USB RAM as a FIFO.

AUTOPTRH **Autopointer Address High** **7FE3**

b7	b6	b5	b4	b3	b2	b1	b0
A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

AUTOPTRL **Autopointer Address Low** **7FE4**

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

AUTODATA **Autopointer Data** **7FE5**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 6-12. Autopointer Registers

The 8051 first loads AUTOPTRH and AUTOPTRL with a RAM address (for example the address of a bulk endpoint buffer). Then, as the 8051 reads or writes data to the data register AUTODATA, the address is supplied by AUTOPTRH/L, which automatically increments after every read or write to the AUTODATA register. The AUTOPTRH/L registers may be written or read at anytime. These registers maintain the current pointer address, so the 8051 can read them to determine where the next byte will be read or written.

The 8051 code example in Figure 6-13 uses the Autopointer to transfer a block of eight data bytes from the endpoint 4 OUT buffer to internal 8051 memory.

```
Init:   mov     dptr,#AUTOPTRH
        mov     a,#HIGH(OUT4BUF)  ; High portion of OUT4BUF buffer
        movx    @dptr,a           ; Load OUTOPTRH
        mov     dptr,#AUTOPTRL
        mov     a,#LOW(OUT4BUF)   ; Low portion of OUT4BUF buffer address
        movx    @dptr,a           ; Load AUTOPTRL
        mov     dptr,#AUTODATA    ; point to the 'fifo' register
        mov     r0,#80H           ; store data in upper 128 bytes of 8051 RAM
        mov     r2,#8             ; loop counter
;
loop:   movx    a,@dptr           ; get a 'fifo' byte
        mov     @r0,a             ; store it
        inc     r0                ; bump destination pointer
                                  ; (NOTE: no 'inc dptr' required here)
        djnz    r2,loop           ; do it eight times
```

Figure 6-13. Use of the Autopointer

As the comment in the penultimate line indicates, the Autopointer saves an "inc dptr" instruction that would be necessary if one of the 8051 data pointers were used to access the OUT4BUF RAM data. This improves the transfer time.

Note

Fastest bulk transfer speed in and out of EZ-USB bulk buffers is achieved when the Autopointer is used in conjunction with the EZ-USB Fast Transfer mode.

As described in Chapter 8, "EZ-USB Isochronous Transfers," the EZ-USB core provides a method for transferring data directly between an internal FIFO and external memory in two 8051 cycles (333 ns). The fast transfer mode is active for bulk data when:

- The 8051 sets FBLK=1 in the FASTXFR register, enabling fast bulk transfers,
- The 8051 DPTR points to the AUTODATA register, and
- The 8051 executes a "movx a,@dptr" or a "movx @dptr,a" instruction.

The 8051 code example in Figure 6-14 shows a transfer loop for moving 64 bytes of external FIFO data into the endpoint 4-IN buffer. The FASTXFR register bits are explained in Chapter 8, "EZ-USB Isochronous Transfers."

Note

The Autopointer works only with internal program/data RAM. It does not work with memory outside the chip, or with internal RAM that is made available when ISO-DISAB=1. See Section 8.9.1, "Disable ISO" for a description of the ISODISAB bit.

```
        mov     dptr,#FASTXFR     ; set up the fast BULK transfer mode
        mov     a,#01000000b      ; FBLK=1, RPOL=0, RM1-0 = 00
        movx    @dptr,a           ; load the FASTXFR register
Init:   mov     dptr,#AUTOPTRH
        mov     a,HIGH(IN4BUF)    ; High portion of IN4BUF
        movx    @dptr,a           ; Load AUTOPTRH
        mov     dptr,#AUTOPTRL
        mov     a,LOW(IN4BUF)     ; Low portion of IN4BUF buffer address
        movx    @dptr,a           ; Load AUTOPTRH
        mov     dptr,#AUTODATA    ; point to the 'fifo' register
        mov     r7,#8             ; r7 is loop counter, 8 bytes per loop
;
loop:   movx    @dptr,a           ; (2) write IN 'fifo' using byte from external bus
        movx    @dptr,a           ; (2) again
        movx    @dptr,a           ; (2) again
        movx    @dptr,a           ; (2) again
        movx    @dptr,a           ; (2) again
        movx    @dptr,a           ; (2) again
        movx    @dptr,a           ; (2) again
        movx    @dptr,a           ; (2) again
        djnz    r7,loop           ; (3) do eight more, 'r7' times
```

Figure 6-14. 8051 Code to Transfer External Data to a Bulk IN Buffer

This transfer loop takes 19 cycles per loop times 8 passes, or 22 ms (152 cycles). A USB bulk transfer of 64 bytes takes more that 42 ms (64*8*83 ns) of bus time to transfer the data bytes to or from the host. This calculation neglects USB overhead time.

From this simple example, it is clear that by using the Autopointer and the EZ-USB Fast Transfer mode, the 8051 can transfer data in and out of EZ-USB endpoint buffers significantly faster than the USB can transfer it to and from the host. This means that the EZ-USB chip should never be a speed bottleneck in a USB system. It also gives the 8051 ample time for other processing duties between endpoint buffer loads.

The Autopointer can be used to quickly move data anywhere in RAM, not just the bulk endpoint buffers. For example, it can be used to good effect in an application that calls for transferring a block of data into RAM, processing the data, and then transferring the data to a bulk endpoint buffer.

7 EZ-USB Endpoint Zero

7.1 Introduction

Endpoint Zero has special significance in a USB system. It is a CONTROL endpoint, and is required by every USB device. Only CONTROL endpoints accept special SETUP tokens that the host uses to signal transfers that deal with device control. The USB host sends a repertoire of standard device requests over endpoint zero. These standard requests are fully defined in Chapter 9 of the USB Specification. This chapter describes how the EZ-USB chip handles endpoint zero requests.

Because the EZ-USB chip can enumerate without firmware (see Chapter 5, "EZ-USB Enumeration and ReNumeration™"), the EZ-USB core contains logic to perform enumeration on its own. This hardware assist of endpoint zero operations is make available to the 8051, simplifying the code required to service device requests. This chapter deals with 8051 control of endpoint zero (ReNum=1, Chapter 5), and describes EZ-USB resources such as the Setup Data Pointer that simplify 8051 code that handles endpoint zero requests.

Endpoint zero is the only CONTROL endpoint in the EZ-USB chip. Although CONTROL endpoints are *bi-directional*, the EZ-USB chip provides two 64-byte buffers, IN0BUF and OUT0BUF, which the 8051 handles exactly like bulk endpoint buffers for the data stages of a CONTROL transfer. A second 8-byte buffer, SETUPDAT, which is unique to endpoint zero, holds data that arrives in the SETUP stage of a CONTROL transfer. This relieves the 8051 programmer of having to keep track of the three CONTROL transfer phases—SETUP, DATA, and STATUS. The EZ-USB core also generates separate interrupt requests for the various transfer phases, further simplifying code.

The IN0BUF and OUT0BUF buffers have two special properties that result from being used by CONTROL endpoint zero:

- Endpoints 0-IN and 0-OUT are always valid, so the valid bits (LSB of IN07VAL and OUT07VAL registers) are permanently set to 1. Writing any value to these two bits has no effect, and reading these bits always returns a 1.

- Endpoint 0 cannot be paired with endpoint 1, so there is no pairing bit in the USBPAIR register for endpoint 0 or 1.

7.2 Control Endpoint EP0

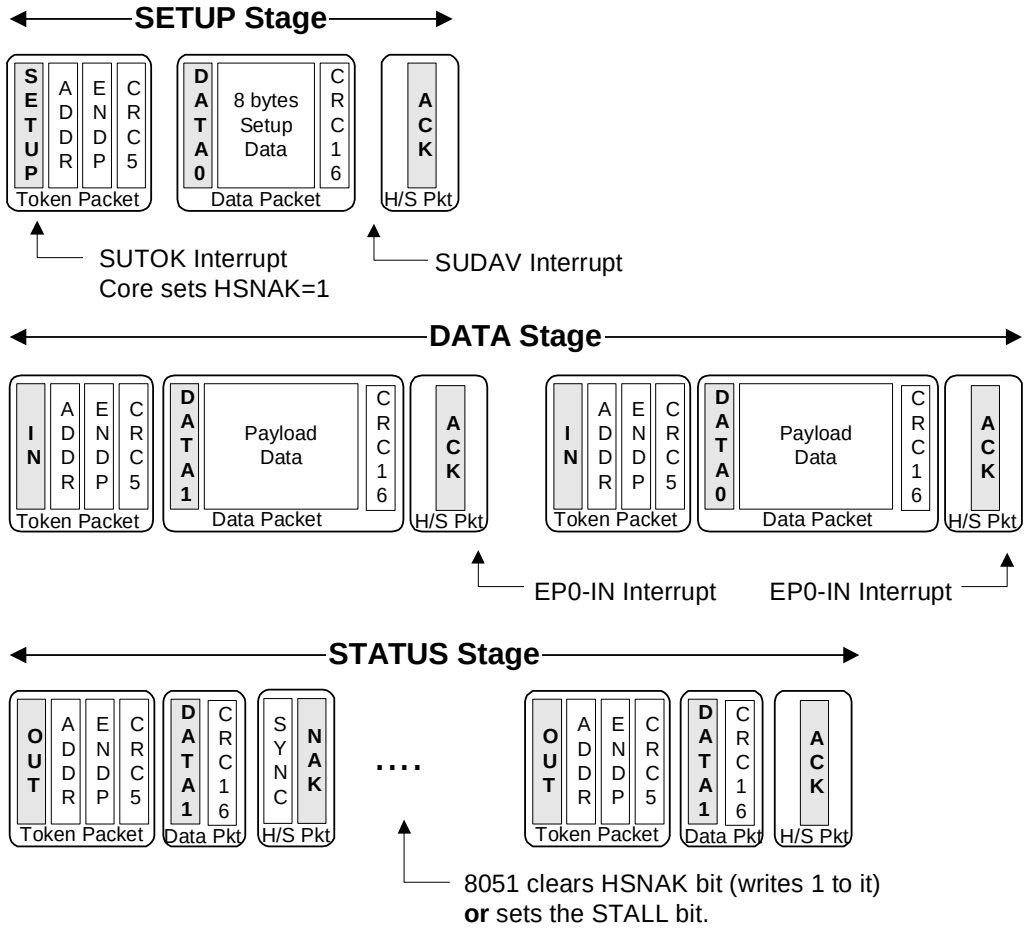


Figure 7-1. A USB Control Transfer (This One Has a Data Stage)

Endpoint zero accepts a special SETUP packet, which contains an 8-byte data structure that provides host information about the CONTROL transaction. CONTROL transfers include a final STATUS phase, constructed from standard PIDs (IN/OUT, DATA1, and ACK/NAK).

Some CONTROL transactions include all required data in their 8-byte SETUP Data packet. Other CONTROL transactions require more OUT data than will fit into the eight bytes, or require IN data from the device. These transactions use standard bulk-like transfers to move the data. Note in Figure 7-1 that the "DATA Stage" looks exactly like a bulk transfer. As with BULK endpoints, the endpoint zero byte count registers must be loaded to ACK the data transfer stage of a CONTROL transfer.

The STATUS stage consists of an empty data packet with the opposite direction of the data stage, or an IN if there was no data stage. This empty data packet gives the device a chance to ACK or NAK the entire CONTROL transfer. The 8051 writes a "1" to a bit call HSNAK (Handshake NAK) to clear it and instruct the EZ-USB core to ACK the STATUS stage.

The HSNAK bit is used to hold off completing the CONTROL transfer until the device has had time to respond to a request. For example, if the host issues a Set_Interface request, the 8051 performs various housekeeping chores such as adjusting internal modes and re-initializing endpoints. During this time the host issues handshake (STATUS stage) packets to which the EZ-USB core responds with NAKs, indicating "busy." When the 8051 completes the desired operation, it sets HSNAK=1 (by writing a "1" to the bit) to terminate the CONTROL transfer. This handshake prevents the host from attempting to use a partially configured interface.

To perform an endpoint stall for the DATA or STATUS stage of an endpoint zero transfer (the SETUP stage can never stall), the 8051 must set both the STALL and HSNAK bits for endpoint zero.

Some CONTROL transfers do not have a DATA stage. Therefore the 8051 code that processes the SETUP data should check the length field in the SETUP data (in the 8-byte buffer at SETUPDAT) and arm endpoint zero for the DATA phase (by loading IN0BC or OUT0BC) only if the length is non-zero.

Two 8051 interrupts provide notification that a SETUP packet has arrived, as shown in Figure 7-2.

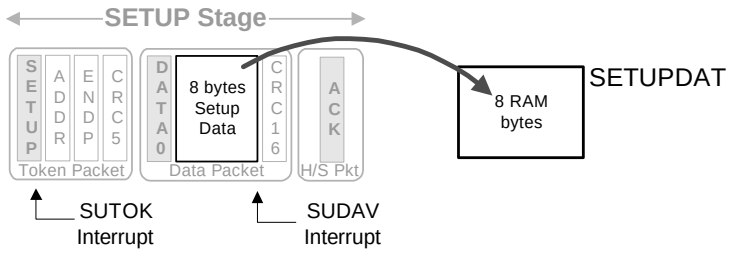


Figure 7-2. The Two Interrupts Associated with EP0 CONTROL Transfers

The EZ-USB core sets the SUTOKIR bit (SETUP Token Interrupt Request) when the EZ-USB core detects the SETUP token at the beginning of a CONTROL transfer. This interrupt is normally used only for debug.

The EZ-USB core sets the SUDAVIR bit (Setup Data Available Interrupt Request) when the eight bytes of SETUP data have been received error-free and transferred to eight EZ-

USB registers starting at SETUPDAT. The EZ-USB core takes care of any re-tries if it finds any errors in the SETUP data. These two interrupt request bits are set by the EZ-USB core, and must be cleared by firmware.

An 8051 program responds to the SUDAV interrupt request by either directly inspecting the eight bytes at SETUPDAT or by transferring them to a local buffer for further processing. Servicing the SETUP data should be a high 8051 priority, since the USB Specification stipulates that CONTROL transfers must always be accepted and never NAKd. It is therefore possible that a CONTROL transfer could arrive while the 8051 is still servicing a previous one. In this case the previous CONTROL transfer service should be aborted and the new one serviced. The SUTOK interrupt gives advance warning that a new CONTROL transfer is about to over-write the eight SETUPDAT bytes.

If the 8051 stalls endpoint zero (by setting the EP0STALL and HSNAK bits to 1), the EZ-USB core automatically clears this stall bit when the next SETUP token arrives.

Like all EZ-USB interrupt requests, the SUTOKIR and SUDAVIR bits can be directly tested and reset by the CPU (they are reset by writing a “1”). Thus, if the corresponding interrupt enable bits are zero, the interrupt request conditions can still be directly polled.

Figure 7-3 shows the EZ-USB registers that deal with CONTROL transactions over EP0.

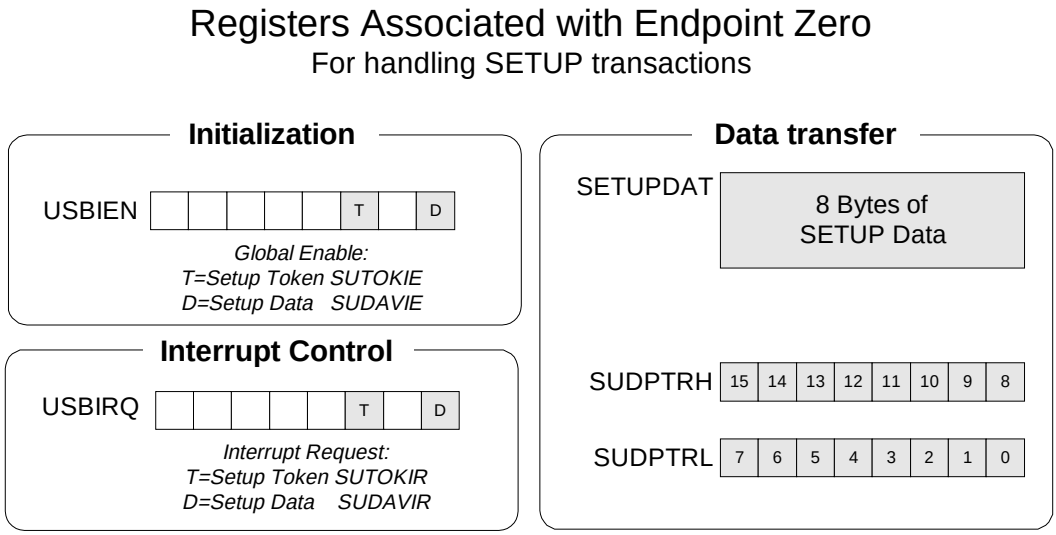


Figure 7-3. Registers Associated with EP0 Control Transfers

These registers augment those associated with normal bulk transfers over endpoint zero, which are described in Chapter 6, "EZ-USB Bulk Transfers."

Two bits in the USBIEN (USB Interrupt Enable) register enable the SETUP Token (SUTOKIE) and SETUP Data interrupts. The actual interrupt request bits are in the USBIRQ (USB Interrupt Requests) register. They are called STOKIR (SETUP Token Interrupt Request) and SUDAVIR (SETUP Data Interrupt Request).

The EZ-USB core transfers the eight SETUP bytes into eight bytes of RAM at SETUP-DAT. A 16-bit pointer, SUDPTRH/L gives hardware assistance for handling CONTROL IN transfers, in particular, the USB Get_Descriptor requests described later in this chapter.

7.3 USB Requests

The *Universal Serial Bus Specification Version 1.1, Chapter 9, "USB Device Framework"* defines a set of *Standard Device Requests*. When the 8051 is in control (ReNum=1), the EZ-USB core handles one of these requests (Set Address) directly, and relies on the 8051 to support the others. The 8051 acts on device requests by decoding the eight bytes contained in the SETUP packet. Table 7-1 shows the meaning of these eight bytes.

Table 7-1. The Eight Bytes in a USB SETUP Packet

Byte	Field	Meaning
0	bmRequestType	Request Type, Direction, and Recipient
1	bRequest	The actual request (see Table 7-2)
2	wValueL	Word-size value, varies according to bRequest
3	wValueH	
4	wIndexL	Word-size field, varies according to bRequest
5	wIndexH	
6	wLengthL	Number of bytes to transfer if there is a data phase
7	wLengthH	

The **Byte** column in the previous table shows the byte offset from SETUPDAT. The **Field** column shows the different bytes in the request, where the “bm” prefix means bit-map, “b” means byte, and “w” means word (16 bits). Table 7-2 shows the different values defined for bRequest, and how the 8051 responds to each request. The remainder of this chapter describes each of the Table 7-2 requests in detail.

Note

Table 7-2 applies when ReNum=1, which signifies that the 8051, and not the EZ-USB core, handles device requests. Table 5-2 shows how the core handles each of these device requests when ReNum=0, for example when the chip is first powered and the 8051 is not running.

Table 7-2. How the 8051 Handles USB Device Requests (ReNum=1)

bRequest	Name	Action	8051 Response
0x00	Get Status	SUDAV Interrupt	Supply RemWU, SelfPwr or Stall bits
0x01	Clear Feature	SUDAV Interrupt	Clear RemWU, SelfPwr or Stall bits
0x02	(reserved)	none	Stall EP0
0x03	Set Feature	SUDAV Interrupt	Set RemWU, SelfPwr or Stall bits
0x04	(reserved)	none	Stall EP0
0x05	Set Address	Update FNADDR register	none
0x06	Get Descriptor	SUDAV Interrupt	Supply table data over EP0-IN
0x07	Set Descriptor	SUDAV Interrupt	Application dependent
0x08	Get Configuration	SUDAV Interrupt	Send current configuration number
0x09	Set Configuration	SUDAV Interrupt	Change current configuration
0x0A	Get Interface	SUDAV Interrupt	Supply alternate setting No. from RAM
0x0B	Set Interface	SUDAV Interrupt	Change alternate setting No.
0x0C	Sync Frame	SUDAV Interrupt	Supply a frame number over EP0-IN
Vendor Requests			
0xA0 (Firmware Load)		Up/Download RAM	---
0xA1 - 0xAF		SUDAV Interrupt	Reserved by Cypress Semiconductor
All except 0xA0		SUDAV Interrupt	Depends on application

In the ReNumerated condition (ReNum=1), the EZ-USB core passes all USB requests except Set Address onto the 8051 *via* the SUDAV interrupt. This, in conjunction with the USB disconnect/connect feature, allows a completely new and different USB device (yours) to be characterized by the downloaded firmware.

The EZ-USB core implements one vendor-specific request, namely “Firmware Load,” 0xA0. (The bRequest value of 0xA0 is valid only if byte 0 of the request, bmRequest-Type, is also “x10xxxxx,” indicating a vendor-specific request.) The load request is valid at all times, so even after ReNumeration the load feature maybe used. If your application implements vendor-specific USB requests, and you do *not* wish to use the Firmware Load feature, be sure to refrain from using the bRequest value 0xA0 for your custom requests. The Firmware Load feature is fully described in Chapter 5, "EZ-USB Enumeration and ReNumeration™."

Note

To avoid future incompatibilities, vendor requests A0-AF (hex) are reserved by Cypress Semiconductor.

7.3.1 Get Status

The USB Specification version 1.0 defines three USB status requests. A fourth request, to an interface, is indicated in the spec as "reserved." The four status requests are:

- Remote Wakeup (Device request)
- Self-Powered (Device request)
- Stall (Endpoint request)
- Interface request ("reserved")

The EZ-USB core activates the SUDAV interrupt request to tell the 8051 to decode the SETUP packet and supply the appropriate status information.

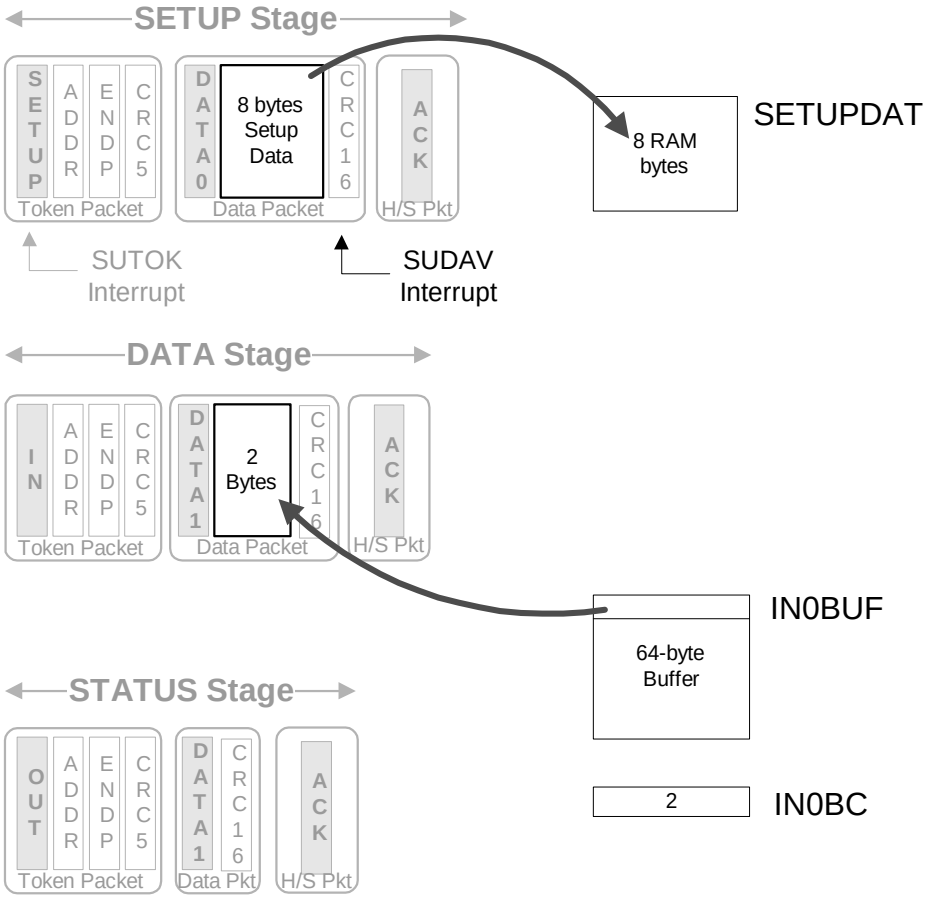


Figure 7-4. Data Flow for a Get_Status Request

As Figure 7-4 illustrates, the 8051 responds to the SUDAV interrupt by decoding the eight bytes the EZ-USB core has copied into RAM at SETUPDAT. The 8051 answers a Get_Status request (bRequest=0) by loading two bytes into the IN0BUF buffer and loading the byte count register IN0BC with the value "2." The EZ-USB core transmits these two bytes in response to an IN token. Finally, the 8051 clears the HSNAK bit (by writing "1" to it) to instruct the EZ-USB core to ACK the status stage of the transfer.

The following tables show the eight SETUP bytes for Get_Status requests.

Table 7-3. Get Status-Device (Remote Wakeup and Self-Powered Bits)

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x80**	IN, Device	
1	bRequest	**0x00**	"Get Status"	*Load two bytes into IN0BUF*
2	wValueL	0x00		
3	wValueH	0x00		*Byte 0 : bit 0 = Self Powered bit*
4	wIndexL	0x00		*: bit 1 = Remote Wakeup*
5	wIndexH	0x00		*Byte 1 : zero*
6	wLengthL	**0x02**	Two bytes requested	
7	wLengthH	**0x00**		

Get_Status-*Device* queries the state of two bits, Remote Wakeup and Self-Powered. The Remote Wakeup bit indicates whether or not the device is currently enabled to request remote wakeup. Remote wakeup is explained in Chapter 11, "EZ-USB Power Management." The Self-Powered bit indicates whether or not the device is self-powered (as opposed to USB bus-powered).

The 8051 returns these two bits by loading two bytes into IN0BUF, and then loading a byte count of two into IN0BC.

Table 7-4. Get Status-Endpoint (Stall Bits)

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x82**	IN, Endpoint	*Load two bytes into IN0BUF*
1	bRequest	**0x00**	"Get Status"	*Byte 0 : bit 0 = Stall bit for EP(n)*
2	wValueL	0x00		*Byte 1 : zero*
3	wValueH	0x00		
4	wIndexL	**EP**	Endpoint Number	EP(n):
5	wIndexH	0x00		0x00-0x07: OUT0-OUT7
6	wLengthL	**0x02**	Two bytes requested	0x80-0x87: IN0-IN7
7	wLengthH	**0x00**		

Each bulk endpoint (IN or OUT) has a STALL bit in its Control and Status register (bit 0). If the CPU sets this bit, any requests to the endpoint return a STALL handshake rather than ACK or NAK. The Get Status-Endpoint request returns the STALL state for the endpoint indicated in byte 4 of the request. Note that bit 7 of the endpoint number EP (byte 4) specifies direction.

Endpoint zero is a CONTROL endpoint, which by USB definition is *bi-directional*. Therefore, it has only one stall bit.

About STALL

The USB STALL handshake indicates that something unexpected has happened. For instance, if the host requests an invalid alternate setting or attempts to send data to a non-existent endpoint, the device responds with a STALL handshake over endpoint zero instead of ACK or NAK.

Stalls are defined for all endpoint types except ISOCHRONOUS, which do not employ handshakes. Every EZ-USB bulk endpoint has its own stall bit. The 8051 sets the stall condition for an endpoint by setting the stall bit in the endpoint's CS register. The host tells the 8051 to set or clear the stall condition for an endpoint using the Set_Feature/Stall and Clear_Feature/Stall requests.

An example of the 8051 setting a stall bit would be in a routine that handles endpoint zero device requests. If an undefined or non-supported request is decoded, the 8051 should stall EP0. (EP0 has a single stall bit because it is a bi-directional endpoint.)

Once the 8051 stalls an endpoint, it should not remove the stall until the host issues a Clear_Feature/Stall request. An exception to this rule is endpoint 0, which reports a stall condition only for the current transaction, and then automatically clears the stall condition. This prevents endpoint 0, the default CONTROL endpoint, from locking out device requests.

Table 7-5. Get Status-Interface

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x81**	IN, Endpoint	*Load two bytes into IN0BUF*
1	bRequest	**0x00**	"Get Status"	*Byte 0 : zero*
2	wValueL	0x00		*Byte 1 : zero*
3	wValueH	0x00		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**0x02**	Two bytes requested	
7	wLengthH	**0x00**		

Get_Status/Interface is easy: the 8051 returns two zero bytes through IN0BUF and clears the HSNAK bit. The requested bytes are shown as "Reserved (Reset to zero)" in the USB Specification

7.3.2 Set Feature

Set Feature is used to enable remote wakeup or stall an endpoint. No data stage is required.

Table 7-6. Set Feature-Device (Set Remote Wakeup Bit)

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x00**	OUT, Device	*Set the Remote Wakeup bit*
1	bRequest	**0x03**	"Set Feature"	
2	wValueL	**0x01**	Feature Selector: Remote Wakeup	
3	wValueH	0x00		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	0x00		
7	wLengthH	0x00		

The only Set_Feature/Device request presently defined in the USB specification is to set the remote wakeup bit. This is the same bit reported back to the host as a result of a Get Status-Device request (Table 7-3). The host uses this bit to enable or disable remote wakeup by the device.

Table 7-7. Set Feature-Endpoint (Stall)

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x02**	OUT, Endpoint	*Set the STALL bit for the*
1	bRequest	**0x03**	"Set Feature"	*indicated endpoint:*
2	wValueL	**0x00**	Feature Selector: STALL	
3	wValueH	0x00		
4	wIndexL	**EP**		EP(n):
5	wIndexH	0x00		0x00-0x07: OUT0-OUT7
6	wLengthL	0x00		0x80-0x87: IN0-IN7
7	wLengthH	0x00		

The only Set_Feature/Endpoint request presently defined in the USB Specification is to stall an endpoint. The 8051 should respond to this request by setting the stall bit in the Control and Status register for the indicated endpoint EP (byte 4 of the request). The 8051 can either stall an endpoint on its own, or in response to the device request. Endpoint stalls are cleared by the host Clear_Feature/Stall request.

The 8051 should respond to the Set_Feature/Stall request by performing the following steps:

1. Set the stall bit in the indicated endpoint's CS register.
2. Reset the data toggle for the indicated endpoint.
3. For an IN endpoint, clear the busy bit in the indicated endpoint's CS register.
4. For an OUT endpoint, load any value into the endpoint's byte count register.
5. Clear the HSNAK bit in the EP0CS register (by writing 1 to it) to terminate the Set_Feature/Stall CONTROL transfer.

Steps 3 and 4 restore the stalled endpoint to its default condition, ready to send or accept data after the stall condition is removed by the host (using a Clear_Feature/Stall request). These steps are also required when the host sends a Set_Interface request.

Data Toggles

The EZ-USB core automatically maintains the endpoint toggle bits to ensure data integrity for USB transfers. The 8051 should directly manipulate these bits only for a very limited set of circumstances:

- Set_Feature/Stall
- Set_Configuration
- Set_Interface

7.3.3 Clear Feature

Clear Feature is used to disable remote wakeup or to clear a stalled endpoint.

Table 7-8. Clear Feature-Device (Clear Remote Wakeup Bit)

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x00**	OUT, Device	*Clear the remote wakeup bit*
1	bRequest	**0x01**	"Clear Feature"	
2	wValueL	**0x01**	Feature Selector: Remote Wakeup	
3	wValueH	0x00		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	0x00		
7	wLengthH	0x00		

Table 7-9. Clear Feature-Endpoint (Clear Stall)

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x02**	OUT, Endpoint	*Clear the STALL bit for the*
1	bRequest	**0x01**	"Clear Feature"	*indicated endpoint:*
2	wValueL	**0x00**	Feature Selector: STALL	
3	wValueH	0x00		
4	wIndexL	**EP**		EP(n):
5	wIndexH	0x00		0x00-0x07: OUT0-OUT7
6	wLengthL	0x00		0x80-0x87: IN0-IN7
7	wLengthH	0x00		

If the USB device supports remote wakeup (as reported in its descriptor table when the device is enumerated), the Clear_Feature/Remote Wakeup request disables the wakeup capability.

The Clear_Feature/Stall removes the stall condition from an endpoint. The 8051 should respond by clearing the stall bit in the indicated endpoint's CS register.

7.3.4 Get Descriptor

During enumeration, the host queries a USB device to learn its capabilities and requirements using Get_Descriptor requests. Using tables of *descriptors*, the device sends back

(over EP0-IN) such information as what device driver to load, how many endpoints it has, its different configurations, alternate settings it may use, and informative text strings about the device.

The EZ-USB core provides a special *Setup Data Pointer* to simplify 8051 service for Get_Descriptor requests. The 8051 loads this 16-bit pointer with the beginning address of the requested descriptor, clears the HSNAK bit (by writing "1" to it), and the EZ-USB core does the rest.

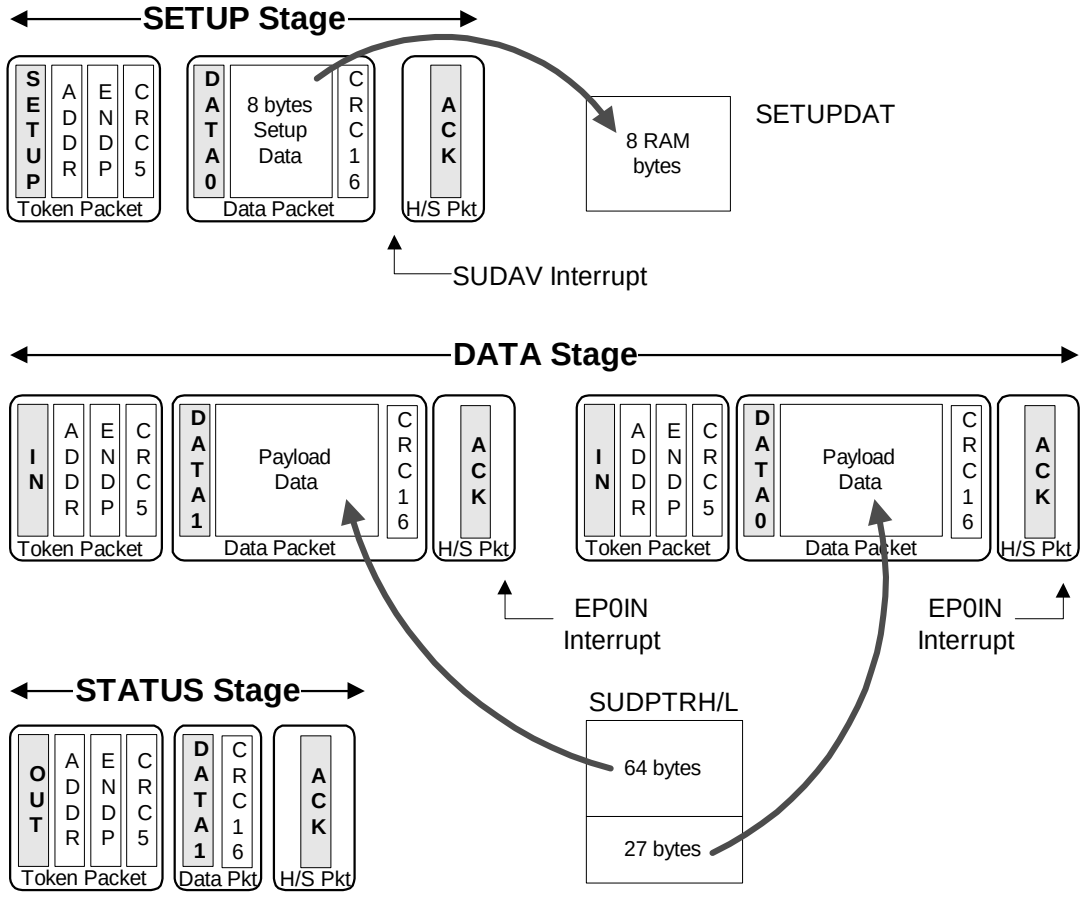


Figure 7-5. Using the Setup Data Pointer (SUDPTR) for Get_Descriptor Requests

Figure 7-5 illustrates use of the Setup Data Pointer. This pointer is implemented as two registers, SUDPTRH and SUDPTRL. Most Get_Descriptor requests involve transferring more data than will fit into one packet. In the Figure 7-5 example, the descriptor data consists of 91 bytes.

The CONTROL transaction starts in the usual way, with the EZ-USB core transferring the eight bytes in the SETUP packet into RAM at SETUPDAT and activating the SUDAV interrupt request. The 8051 decodes the Get_Descriptor request, and responds by clearing the HSNAK bit (by writing "1" to it), and then loading the SUDPTR registers with the address of the requested descriptor. Loading the SUDPTRL register causes the EZ-USB core to automatically respond to two IN transfers with 64 bytes and 27 bytes of data using SUDPTR as a base address, and then to respond to (ACK) the STATUS stage.

The usual endpoint zero interrupts, SUDAV and EP0IN, remain active during this automated transfer. The 8051 normally disables these interrupts because the transfer requires no 8051 intervention.

Three types of descriptors are defined: Device, Configuration, and String.

7.3.4.1 Get Descriptor-Device

*Table 7-10. Get Descriptor-**Device***

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x80**	IN, Device	*Set SUDPTR H-L to start of*
1	bRequest	**0x06**	"Get_Descriptor"	*Device Descriptor table in RAM*
2	wValueL	0x00		
3	wValueH	**0x01**	Descriptor Type: Device	
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**LenL**		
7	wLengthH	**LenH**		

As illustrated in Figure 7-5, the 8051 loads the 2-byte SUDPTR with the starting address of the Device Descriptor table. When SUDPTRL is loaded, the EZ-USB core performs the following operations:

1. Reads the requested number of bytes for the transfer from bytes 6 and 7 of the SETUP packet (**LenL** and **LenH** in Table 7-11).

2. Reads the requested string's descriptor to determine the actual string length.

3. Sends the smaller of (a) the requested number of bytes or (b) the actual number of bytes in the string, over IN0BUF using the Setup Data Pointer as a data table

index. This constitutes the second phase of the three-phase CONTROL transfer. The core Packetizes the data into multiple data transfers as necessary.

4. Automatically checks for errors and re-transmits data packets if necessary.

5. Responds to the third (handshake) phase of the CONTROL transfer to terminate the operation.

The Setup Data Pointer can be used for any Get_Descriptor request; for example, Get_Descriptor-String. It can also be used for vendor-specific requests (that you define), as long as bytes 6-7 contain the number of bytes in the transfer (for step 1).

It is possible for the 8051 to do *manual* CONTROL transfers, directly loading the IN0BUF buffer with the various packets and keeping track of which SETUP phase is in effect. This would be a good USB training exercise, but not necessary due to the hardware support built into the EZ-USB core for CONTROL transfers.

For DATA stage transfers of fewer than 64 bytes, moving the data into the IN0BUF buffer and then loading the EP0INBC register with the byte count would be equivalent to loading the Setup Data Pointer. However, this would waste 8051 overhead because the Setup Data Pointer requires no byte transfers into the IN0BUF buffer.

7.3.4.2 Get Descriptor-Configuration

*Table 7-11. Get Descriptor-**Configuration***

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x80**	IN, Device	*Set SUDPTR H-L to start of Configuration Descriptor table in RAM*
1	bRequest	**0x06**	"Get_Descriptor"	
2	wValueL	**CFG**	Config Number	
3	wValueH	**0x02**	Descriptor Type: Configuration	
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**LenL**		
7	wLengthH	**LenH**		

7.3.4.3 Get Descriptor-String

*Table 7-12. Get Descriptor-**String***

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x80**	IN, Device	*Set SUDPTR H-L to start of Configuration Descriptor table in RAM*
1	bRequest	**0x06**	"Get_Descriptor"	
2	wValueL	**CFG**	String Number	
3	wValueH	**0x02**	Descriptor Type: String	
4	wIndexL	0x00	(Language ID L)	
5	wIndexH	0x00	(Language ID H)	
6	wLengthL	**LenL**		
7	wLengthH	**LenH**		

Configuration and string descriptors are handled similarly to device descriptors. The 8051 firmware reads byte 2 of the SETUP data to determine which configuration or string is being requested, loads the corresponding table pointer into SUDPTRH-L, and the EZ-USB core does the rest.

7.3.5 Set Descriptor

*Table 7-13. Set Descriptor-**Device***

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x00**	OUT, Device	*Read device descriptor data over OUT0BUF*
1	bRequest	**0x07**	"Set_Descriptor"	
2	wValueL	0x00		
3	wValueH	0x01	Descriptor Type: Device	
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**LenL**		
7	wLengthH	**LenH**		

*Table 7-14. Set Descriptor-**Configuration***

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x00**	OUT, Device	*Read configuration descriptor data over OUT0BUF*
1	bRequest	**0x07**	"Set_Descriptor"	
2	wValueL	0x00		
3	wValueH	0x02	Descriptor Type: Configuration	
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**LenL**		
7	wLengthH	**LenH**		

*Table 7-15. Set Descriptor-**String***

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x00**	IN, Device	*Read string descriptor data over OUT0BUF*
1	bRequest	**0x07**	"Get_Descriptor"	
2	wValueL	0x00	Config Number	
3	wValueH	0x03	Descriptor Type: String	
4	wIndexL	0x00	(Language ID L)	
5	wIndexH	0x00	(Language ID H)	
6	wLengthL	**LenL**		
7	wLengthH	**LenH**		

The 8051 handles Set_Descriptor requests by clearing the HSNAK bit (by writing "1" to it), then reading descriptor data directly from the OUT0BUF buffer. The EZ-USB core keeps track of the number of byes transferred from the host into OUT0BUF, and compares this number with the length field in bytes 6 and 7. When the proper number of bytes has been transferred, the EZ-USB core automatically responds to the status phase, which is the third and final stage of the CONTROL transfer.

Note

The 8051 controls the flow of data in the Data Stage of a Control Transfer. After the 8051 processes each OUT packet, it loads any value into the OUT endpoint's byte count register to re-arm the endpoint.

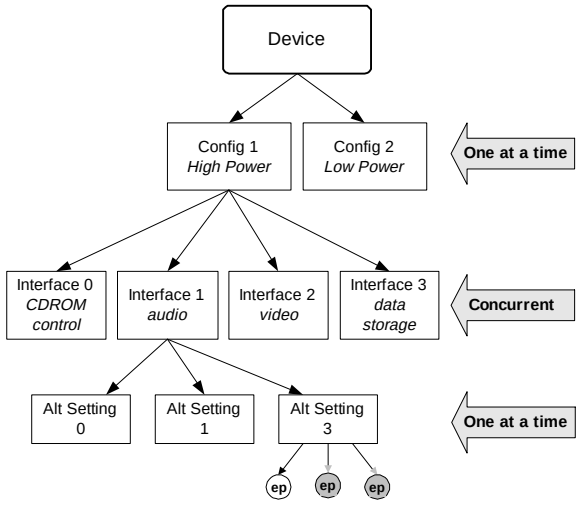
Configurations, Interfaces, and Alternate Settings

Configurations, Interfaces, and Alternate Settings

A USB device has one or more **configuration**. Only one configuration is active at any time.

A configuration has one or more **interface**, all of which are concurrently active. Multiple interfaces allow different host-side device drivers to be associated with different portions of a USB device.

Each interface has one or more **alternate setting**. Each alternate setting has a collection of one or more endpoints.



This structure is a software model; the EZ-USB core takes no action when these settings change. However, the 8051 **must re-initialize endpoints** when the host changes configurations or interfaces alternate settings.

As far as 8051 firmware is concerned, a *configuration* is simply a byte variable that indicates the current setting.

The host issues a Set_Coniguration request to select a configuration, and a Get_Configuration request to determine the current configuration.

7.3.6 Set Configuration

Table 7-16. Set Configuration

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x00**	OUT, Device	*Read and stash byte 2, change configurations in firmware*
1	bRequest	**0x09**	"Set_Configuration"	
2	wValueL	**CFG**	Config Number	
3	wValueH	0x00		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	0x00		
7	wLengthH	0x00		

When the host issues the Set_Configuration request, the 8051 saves the configuration number (byte 2 in Table Table 7-16), performs any internal operations necessary to support the configuration, and finally clears the HSNAK bit (by writing "1" to it) to terminate the Set_Configuration CONTROL transfer.

Note

After setting a configuration, the host issues *Set_Interface* commands to set up the various interfaces contained in the configuration.

7.3.7 Get Configuration

Table 7-17. Get Configuration

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x80**	IN, Device	*Send CFG over IN0BUF after re-configuring*
1	bRequest	**0x08**	"Get_Configuration"	
2	wValueL	0x00		
3	wValueH	0x00		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**1**	LenL	
7	wLengthH	**0**	LenH	

The 8051 returns the current configuration number. It loads the configuration number into EP0IN, loads a byte count of one into EP0INBC, and finally clears the HSHAK bit (by writing "1" to it) to terminate the Set_Configuration CONTROL transfer.

7.3.8 Set Interface

This confusingly named USB command actually sets and reads back *alternate settings* for a specified interface.

USB devices can have multiple concurrent interfaces. For example a device may have an audio system that supports different sample rates, and a graphic control panel that supports different languages. Each interface has a collection of endpoints. Except for endpoint 0, which each interface uses for device control, endpoints may not be shared between interfaces.

Interfaces may report alternate settings in their descriptors. For example, the audio interface may have setting 0, 1, and 2 for 8-KHz, 22-KHz, and 44-KHz sample rates, and the panel interface may have settings 0 and 1 for English and Spanish. The Set/Get_Interface requests select between the various alternate settings in an interface.

Table 7-18. Set Interface (Actually, Set Alternate Setting AS for Interface IF)

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x00**	OUT, Device	*Read and stash byte 2 (AS) for Interface IF, change setting for Interface IF in firmware*
1	bRequest	**0x0B**	"Set_Interface"	
2	wValueL	**AS**	Alt Setting Number	
3	wValueH	0x00		
4	wIndexL	**IF**	For this interface	
5	wIndexH	0x00		
6	wLengthL	0x00		
7	wLengthH	0x00		

The 8051 should respond to a Set_Interface request by performing the following steps:

- Perform the internal operation requested (such as adjusting a sampling rate).
- Reset the data toggles for every endpoint in the interface.
- For an IN endpoint, clear the busy bit for every endpoint in the interface.
- For an OUT endpoint, load any value into the byte count register for every endpoint in the interface.
- Clear the HSNAK bit (by writing "1" to it) to terminate the Set_Feature/Stall CONTROL transfer.

7.3.9 Get Interface

Table 7-19. Get Interface (Actually, Get Alternate Setting AS for interface IF)

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x81**	IN, Device	*Send AS for Interface IF over*
1	bRequest	**0x0A**	"Get_Interface"	*OUT0BUF (1 byte)*
2	wValueL	0x00		
3	wValueH	0x00		
4	wIndexL	**IF**	For this interface	
5	wIndexH	0x00		
6	wLengthL	**1**	LenL	
7	wLengthH	**0**	LenH	

The 8051 simply returns the alternate setting for the requested interface IF, and clears the HSNAK bit by writing "1" to it.

7.3.10 Set Address

When a USB device is first plugged in, it responds to device address 0 until the host assigns it a unique address using the Set_Address request. The EZ-USB core copies this device address into the FNADDR (Function Address) register, and subsequently responds only to requests to this address. This address is in effect until the USB device is unplugged, the host issues a USB Reset, or the host powers down.

The FNADDR register can be read, but not written by the 8051. Whenever the EZ-USB core ReNumerates™, it automatically resets the FNADDR to zero allowing the device to come back as *new.*

An 8051 program does not need to know the device address, because the EZ-USB core automatically responds only to the host-assigned FNADDR value. The EZ-USB core makes it readable by the 8051 for debug/diagnostic purposes.

7.3.11 Sync Frame

Table 7-20. Sync Frame

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x82**	IN, Endpoint	*Send a frame number over*
1	bRequest	**0x0C**	"Sync_Frame"	*IN0BUF to synchronize endpoint*
2	wValueL	0x00		*EP*
3	wValueH	0x00		
4	wIndexL	**EP**	Endpoint number	
5	wIndexH	0x00		EP(n):
6	wLengthL	**2**	LenL	0x08-0x0F: OUT8-OUT15
7	wLengthH	**0**	LenH	0x88-0x8F: IN8-IN15

The Sync_Frame request is used to establish a marker in time so the host and USB device can synchronize multi-frame transfers over isochronous endpoints.

Suppose an isochronous transmission consists of a repeating sequence of five 300 byte packets transmitted from host to device over EP8-OUT. Both host and device maintain sequence counters that count repeatedly from 1 to 5 to keep track of the packets inside a transmission. To start up in sync, both host and device need to reset their counts to 1 at the same time (in the same frame).

To get in sync, the host issues the Sync_Frame request with EP=EP-OUT (byte 4). The 8051 firmware responds by loading IN0BUF with a two-byte frame count for some future time; for example, the current frame plus 20. This marks frame "current+20" as the sync frame, during which both sides will initialize their sequence counters to 1. The 8051 reads the current frame count in the USBFRAMEL and USBFRAMEH registers.

Multiple isochronous endpoints can be synchronized in this manner. The 8051 keeps separate internal sequence counts for each endpoint.

About USB Frames

The USB host issues a SOF (Start Of Frame) packet once every millisecond. Every SOF packet contains an 11-bit (mod-2048) frame number. The 8051 services all isochronous transfers at SOF time, using a single SOF interrupt request and vector. If the EZ-USB core detects a missing SOF packet, it uses an internal counter to generate the SOF interrupt.

7.3.12 Firmware Load

The USB endpoint zero protocol provides a mechanism for mixing vendor-specific requests with the previously described standard device requests. Bits 6:5 of the bmRequest field are set to 00 for a standard device request, and to 10 for a vendor request.

Table 7-21. Firmware Download

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0x40**	Vendor Request, OUT	*None required*
1	bRequest	**0xA0**	"Firmware Load"	
2	wValueL	**AddrL**	Starting address	
3	wValueH	**AddrH**		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**LenL**	Number of bytes	
7	wLengthH	**LenH**		

Table 7-22. Firmware Upload

Byte	Field	Value	Meaning	8051 Response
0	bmRequestType	**0xC0**	Vendor Request, IN	*None Required*
1	bRequest	**0xA0**	"Firmware Load"	
2	wValueL	**AddrL**	Starting address	
3	wValueH	**AddrH**		
4	wIndexL	0x00		
5	wIndexH	0x00		
6	wLengthL	**LenL**	Number of Bytes	
7	wLengthH	**LenH**		

The EZ-USB core responds to two endpoint zero vendor requests, RAM Download and RAM Upload. These requests are active in all modes (ReNum=0 or 1).

Because bit 7 of the first byte of the SETUP packet specifies direction, only one bRequest value (0xA0) is required for the upload and download requests. These RAM load commands are available to any USB device that uses the EZ-USB chip.

A host loader program typically writes 0x01 to the CPUCS register to put the 8051 into RESET, loads all or part of the EZ-USB internal RAM with 8051 code, and finally reloads the CPUCS register with 0 to take the 8051 out of RESET. The CPUCS register is the only USB register that can be written using the Firmware Download command.

8 EZ-USB Isochronous Transfers

8.1 Introduction

Isochronous endpoints typically handle time-critical, streamed data that is delivered or consumed in byte-sequential order. Examples might be audio data sent to a DAC over USB, or teleconferencing video data sent from a camera to the host. Due to the byte-sequential nature of this data, the EZ-USB chip makes isochronous data available as a single byte that represents the head or tail of an endpoint FIFO.

The EZ-USB chips that support isochronous transfers implement sixteen isochronous endpoints, IN8-IN15 and OUT8-OUT15. 1,024 bytes of FIFO memory may be distributed over the 16 endpoint addresses. FIFO sizes for the isochronous endpoints are programmable.

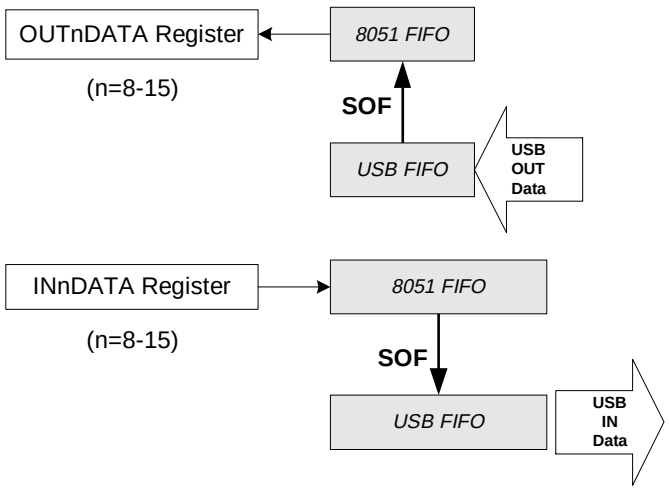


Figure 8-1. EZ-USB Isochronous Endpoints 8-15

The 8051 reads or writes isochronous data using sixteen FIFO data registers, one per endpoint. These FIFO registers are shown in Figure 8-1 as INnDATA (Endpoint n IN Data) and OUTnDATA (Endpoint n OUT Data).

The EZ-USB core provides a total of 2,048 bytes of FIFO memory (1,024 bytes, double-buffered) for ISO endpoints. This memory is in addition to the 8051 program/data memory, and normally exists outside of the 8051 memory space. The 1,024 FIFO bytes may be divided among the sixteen isochronous endpoints. The 8051 writes sixteen EZ-USB registers to allocate the FIFO buffer space to the isochronous endpoints. The 8051 also sets *endpoint valid* bits to enable isochronous endpoints.

8.2 Isochronous IN Transfers

IN transfers travel from device to host. Figure 8-2 shows the EZ-USB registers and bits associated with isochronous IN transfers.

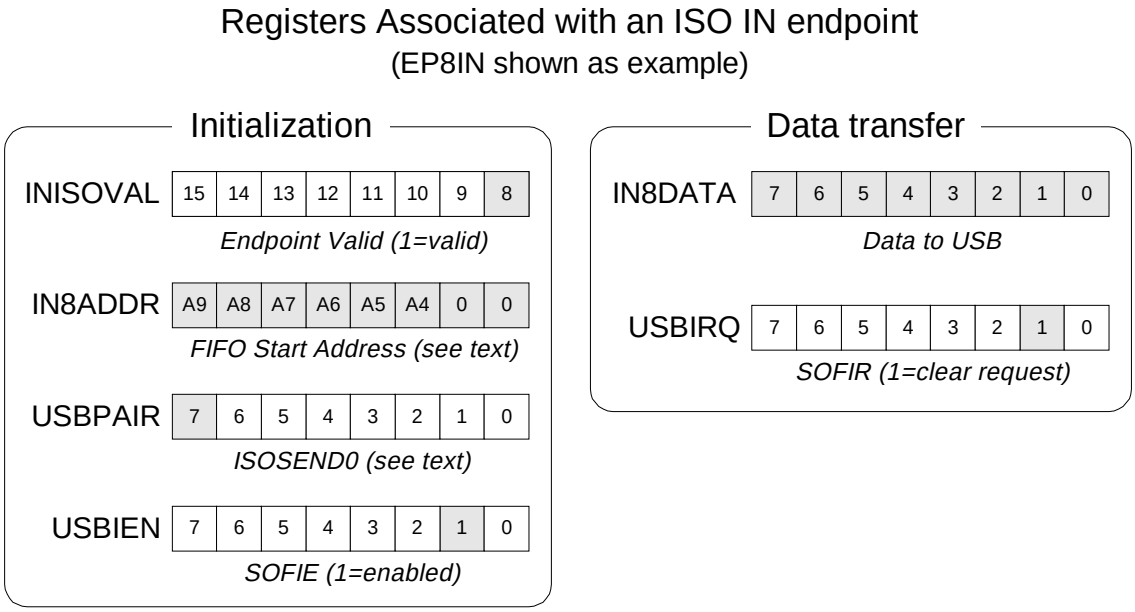


Figure 8-2. Isochronous IN Endpoint Registers

8.2.1 Initialization

To initialize an isochronous IN endpoint, the 8051 performs the following:

- Sets the endpoint valid bit for the endpoint.
- Sets the endpoint's FIFO size by loading a starting address (Section 8.4, "Setting Isochronous FIFO Sizes").
- Sets the ISOSEND0 bit in the USBPAIR register for the desired response.
- Enables the SOF interrupt. All isochronous endpoints are serviced in response to the SOF interrupt.

The EZ-USB core uses the ISOSEND0 bit to determine what to do if:

- The 8051 does not load any bytes to an INnDATA register during the previous frame, and
- An IN token for that endpoint arrives from the host.

If ISOSEND0=0 (the default value), the EZ-USB core does not respond to the IN token. If ISOSEND0=1, the EZ-USB core sends a zero-length data packet in response to the IN token. Which action to take depends on the overall system design. The ISOSEND0 bit applies to all of the isochronous IN endpoints, EP8IN through EP15IN.

8.2.2 IN Data Transfers

When an SOF interrupt occurs, the 8051 is presented with empty IN FIFOs that it fills with data to be transferred to the host during the next frame. The 8051 has 1 ms to transfer data into these FIFOs before the next SOF interrupt arrives.

To respond to the SOF interrupt, the 8051 clears the USB interrupt (8051 INT2), and clears the SOFIR (Start Of Frame Interrupt Request) bit writing a "1" to it. Then, the 8051 loads data into the appropriate isochronous endpoint. The EZ-USB core keeps track of the number of bytes the 8051 loads to each INnDATA register, and subsequently transfers the correct number of bytes in response to the USB IN token during the next frame.

The EZ-USB FIFO swap occurs every SOF, even if during the previous frame the host did not issue an IN token to read the isochronous FIFO data, or if the host encountered an error in the data. USB isochronous data has no *re-try* mechanism like bulk data.

8.3 Isochronous OUT Transfers

OUT transfers travel from host to device. Figure 8-3 shows the EZ-USB registers and bits associated with isochronous OUT transfers.

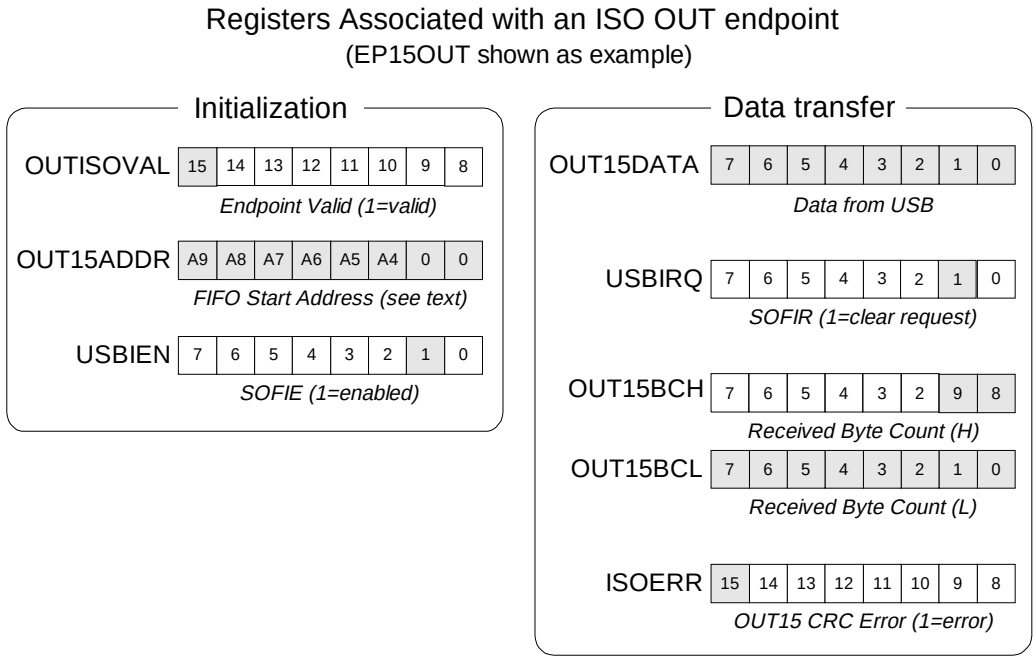


Figure 8-3. Isochronous OUT Registers

8.3.1 Initialization

To initialize an isochronous OUT endpoint, the 8051:

- Sets the endpoint valid bit for the endpoint.
- Sets the endpoint's FIFO size by loading a starting address (Section 8.4, "Setting Isochronous FIFO Sizes").
- Enables the SOF interrupt. All isochronous endpoints are serviced in response to the SOF interrupt.

8.3.2 OUT Data Transfer

When an SOF interrupt occurs, the 8051 is presented with FIFOs containing OUT data sent from the host in the previous frame, along with 10-bit byte counts, indicating how many bytes are in the FIFOs. The 8051 has 1 ms to transfer data out of these FIFOs before the next SOF interrupt arrives.

To respond to the SOF interrupt, the 8051 clears the USB interrupt (8051 INT2), and clears the SOFIR bit by writing one to it. Then, the 8051 reads data from the appropriate OUTnDATA FIFO register(s). The 8051 can check an error bit in the ISOERR register to determine if a CRC error occurred for the endpoint data. Isochronous data is never present, so the firmware must decide what to do with *bad-CRC* data.

8.4 Setting Isochronous FIFO Sizes

Up to sixteen EZ-USB isochronous endpoints share an EZ-USB 1,024-byte RAM which can be configured as one to sixteen FIFOs. The 8051 initializes the endpoint FIFO sizes by specifying the starting address for each FIFO within the 1,024 bytes, starting at address zero. The isochronous FIFOs can exist anywhere in the 1,024 bytes, but the user must take care to ensure that there is sufficient space between start addresses to accommodate the endpoint FIFO size.

Sixteen start address registers set the isochronous FIFO sizes (Table 8-1). The EZ-USB core constructs the address writing the 1,024 byte range from the register value as shown in Figure 8-4.

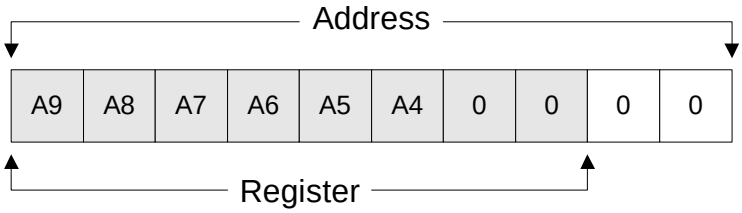


Figure 8-4. FIFO Start Address Format

Table 8-1. Isochronous Endpoint FIFO Starting Address Registers

Register	Function	b7	b6	b5	b4	b3	b2	b1	b0
OUT8ADDR	Endpoint 8 OUT Start Address	A9	A8	A7	A6	A5	A4	0	0
OUT9ADDR	Endpoint 9 OUT Start Address	A9	A8	A7	A6	A5	A4	0	0
OUT10ADDR	Endpoint 10 OUT Start Address	A9	A8	A7	A6	A5	A4	0	0
OUT11ADDR	Endpoint 11 OUT Start Address	A9	A8	A7	A6	A5	A4	0	0
OUT12ADDR	Endpoint 12 OUT Start Address	A9	A8	A7	A6	A5	A4	0	0
OUT13ADDR	Endpoint 13 OUT Start Address	A9	A8	A7	A6	A5	A4	0	0
OUT14ADDR	Endpoint 14 OUT Start Address	A9	A8	A7	A6	A5	A4	0	0
OUT15ADDR	Endpoint 15 OUT Start Address	A9	A8	A7	A6	A5	A4	0	0
IN8ADDR	Endpoint 8 IN Start Address	A9	A8	A7	A6	A5	A4	0	0
IN9ADDR	Endpoint 9 IN Start Address	A9	A8	A7	A6	A5	A4	0	0
IN10ADDR	Endpoint 10 IN Start Address	A9	A8	A7	A6	A5	A4	0	0
IN11ADDR	Endpoint 11 IN Start Address	A9	A8	A7	A6	A5	A4	0	0
IN12ADDR	Endpoint 12 IN Start Address	A9	A8	A7	A6	A5	A4	0	0
IN13ADDR	Endpoint 13 IN Start Address	A9	A8	A7	A6	A5	A4	0	0
IN14ADDR	Endpoint 14 IN Start Address	A9	A8	A7	A6	A5	A4	0	0
IN15ADDR	Endpoint 15 IN Start Address	A9	A8	A7	A6	A5	A4	0	0

The size of an isochronous endpoint FIFO is determined by subtracting consecutive addresses in Table 8-1, and multiplying by four. Values written to these registers should have the two LSBs set to zero. The last endpoint, EP15IN, has a size of 1,024 minus IN15ADDR times four. Because the 10-bit effective address has the four LSBs set to zero (Figure 8-4), the FIFO sizes are allocated in increments of 16 bytes. For example, if OUT8ADDR=0x00 and OUT9ADDR=0x04, EP8OUT has a FIFO size of the difference multiplied by four or 16 bytes.

An 8051 assembler or C compiler may be used to translate FIFO sizes into starting addresses. The assembler example in Figure 8-5 shows a block of equates for the 16 isochronous FIFO sizes, followed by assembler equations to compute the corresponding FIFO relative address values. To initialize all sixteen FIFO sizes, the 8051 merely copies the table starting at 8OUTAD to the sixteen EZ-USB registers starting at OUT8ADDR.

```
0100   EP8INSZ     equ   256     ; Iso FIFO sizes in bytes
0100   EP8OUTSZ    equ   256
0010   EP9INSZ     equ   16
0010   EP9OUTSZ    equ   16
0010   EP10INSZ    equ   16
0010   EP10OUTSZ   equ   16
0000   EP11INSZ    equ   0
0000   EP11OUTSZ   equ   0
0000   EP12INSZ    equ   0
0000   EP12OUTSZ   equ   0
0000   EP13INSZ    equ   0
0000   EP13OUTSZ   equ   0
0000   EP14INSZ    equ   0
0000   EP14OUTSZ   equ   0
0000   EP15INSZ    equ   0
0000   EP15OUTSZ   equ   0
;
0000   8OUTAD      equ   0       ; Load these 16 bytes into ADDR regs starting OUT8ADDR
0040   9OUTAD      equ   8OUTAD  + Low(EP8OUTSZ/4)
0044   10OUTAD     equ   9OUTAD  + Low(EP9OUTSZ/4)
0048   11OUTAD     equ   10OUTAD + Low(EP10OUTSZ/4)
0048   12OUTAD     equ   11OUTAD + Low(EP11OUTSZ/4)
0048   13OUTAD     equ   12OUTAD + Low(EP12OUTSZ/4)
0048   14OUTAD     equ   13OUTAD + Low(EP13OUTSZ/4)
0048   15OUTAD     equ   14OUTAD + Low(EP14OUTSZ/4)
0048   8INAD       equ   15OUTAD + Low(EP15OUTSZ/4)
0088   9INAD       equ   8INAD   + Low(EP8INSZ/4)
008C   10INAD      equ   9INAD   + Low(EP9INSZ/4)
0090   11INAD      equ   10INAD  + Low(EP10INSZ/4)
0090   12INAD      equ   11INAD  + Low(EP11INSZ/4)
0090   13INAD      equ   12INAD  + Low(EP12INSZ/4)
0090   14INAD      equ   13INAD  + Low(EP13INSZ/4)
0090   15INAD      equ   14INAD  + Low(EP14INSZ/4)
```

Figure 8-5. Assembler Translates FIFO Sizes to Addresses

The assembler computes starting addresses in Figure 8-5 by adding the previous end-point's address to the desired size shifted right twice. This aligns A9 with bit 7 as shown in Table 8-1. The LOW operator takes the low byte of the resulting 16 bit expression

The user of this code must ensure that the sizes given in the first equate block are all multiples of 16. This is easy to tell by inspection—the least significant digit of the hex values in the first column should be zero.

8.5 Isochronous Transfer Speed

The amount of data USB can transfer during a 1-ms frame is slightly more than 1,000 bytes per frame (1,500 bytes theoretical, without accounting for USB overhead and bus utilization). A device's actual isochronous transfer bandwidth is usually determined by how fast the CPU can move data in and out of its isochronous endpoint FIFOs.

The 8051 code example in Figure 8-6 shows a typical transfer loop for moving external FIFO data into an IN endpoint FIFO. This code assumes that the 8051 is moving data from an external FIFO attached to the EZ-USB data bus and strobed by the RD signal, into an internal isochronous IN FIFO.

```
        mov   dptr,#8000H       ; pointer to any outside address
        inc   dps               ; switch to second data pointer
        mov   dptr,#IN8DATA     ; pointer to an IN endpoint FIFO (IN8 as example)
        inc   dps               ; back to first data pointer
        mov   r7,#nBytes        ; r7 is loop counter—transfer this many bytes
;
loop:   movx  a,@dptr           ; (2) read byte from external bus to acc
        inc   dps               ; (1) switch to second data pointer
        movx  @dptr,a           ; (2) write to ISO FIFO
        inc   dps               ; (1) switch back to first data pointer
        djnz  r7,loop           ; (3) loop 'nBytes' times
```

Figure 8-6. 8051 Code to Transfer Data to an Isochronous FIFO (IN8DATA)

The numbers in parentheses indicate 8051 cycles. One cycle is four clocks, and the EZ-USB 8051 is clocked at 24 MHz (42 ns). Thus, an 8051 cycle takes 4*42=168 ns, and the loop takes 9 cycles or 1.5 μs. This loop can transfer about 660 bytes into an IN FIFO every millisecond (1 ms/1.5 μs).

If more speed is required, the loop can be *unrolled* by in-line coding the first four instructions in the loop. Then, a byte is transferred in 6 cycles (24 clocks) which equates to 1 μs per byte. Using this method, the 8051 could transfer 1,000 bytes into an IN FIFO every millisecond. In practice, a better solution is to in-line code only a portion of the loop code, which decreases full in-line performance only slightly and uses far fewer bytes of program code.

8.6 Fast Transfers

EZ-USB has a special *fast transfer* mode for applications that use external FIFOs connected to the EZ-USB data bus. These applications typically require very high transfer speeds in and out of EZ-USB endpoint buffers.

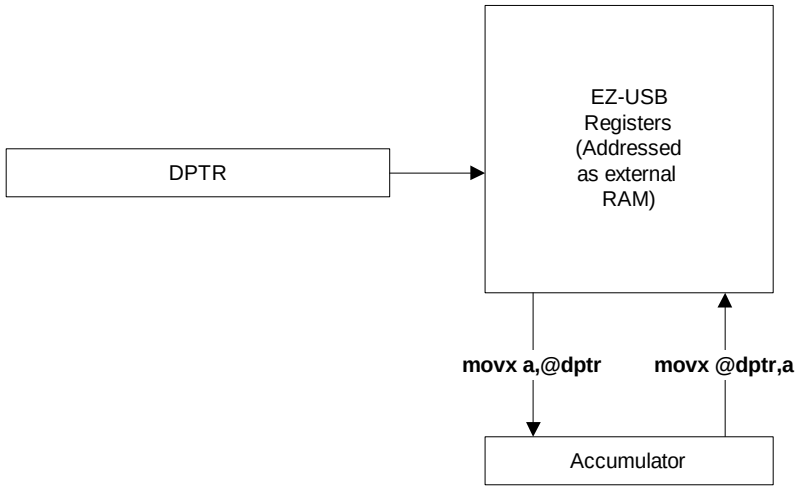


Figure 8-7. 8051 MOVX Instructions

The 8051 transfers data to and from EZ-USB registers and RAM using the MOVX (move external) instruction (Figure 8-7). The 8051 loads one of its two 16-bit data pointers (DPTR) with an address in RAM, and then executes a MOVX instruction to transfer data between the accumulator and the byte addressed by DPTR. The "@" symbol indicates that the address is supplied indirectly, by the DPTR.

The EZ-USB core monitors MOVX transfers between the accumulator and *any of the sixteen isochronous FIFO registers*. If an enable bit is set (FISO=1 in the FASTXFR register), any read or write to an isochronous FIFO register causes the EZ-USB core to connect the data to the EZ-USB data bus D[7..0], and generate external read/write strobes. One MOVX instruction thus transfers a byte of data in or out of an endpoint FIFO and generates timing strobes for an outside FIFO or memory. The 2-cycle MOVX instruction takes 2 cycles or 333 ns. Figures 8-8 and 8-9 show the data flow for fast writes and reads over the EZ-USB data bus.

Fast Bulk Transfers

The EZ-USB core provides a special auto-incrementing data pointer that makes the fast transfer mechanism available for bulk transfers. The 8051 loads a 16-bit RAM address into the AUTOPTRH/L registers, and then accesses RAM data as a FIFO using the AUTODATA register. Section 6.16, "The Autopointer" describes this special pointer and register.

8.6.1 Fast Writes

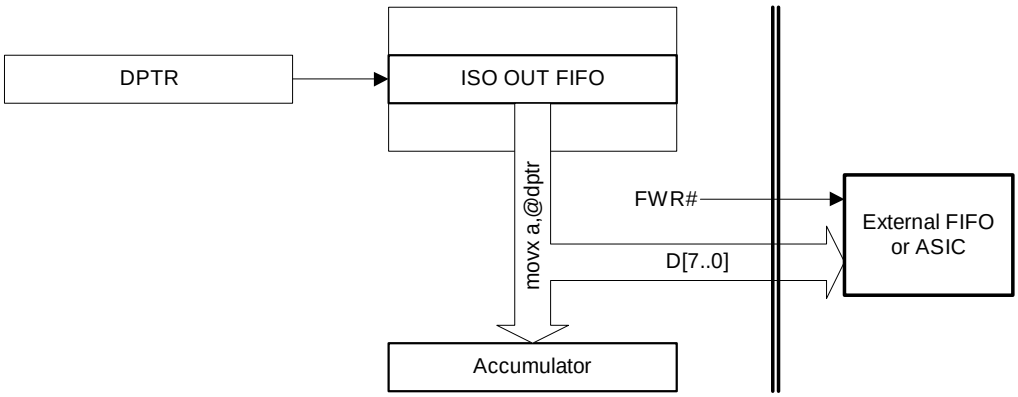


Figure 8-8. Fast Transfer, EZ-USB to Outside Memory

Fast writes are illustrated in Figure 8-8. When the fast mode is enabled, the DPTR points to an isochronous OUT FIFO register, and the 8051 executes the “movx a,@dptr” instruction, the EZ-USB core broadcasts the data from the isochronous FIFO to the outside world via the data bus D[7..0], and generates a Write Strobe FWR# (Fast Write). A choice of eight waveforms is available for the write strobe, as shown in the next section.

8.6.2 Fast Reads

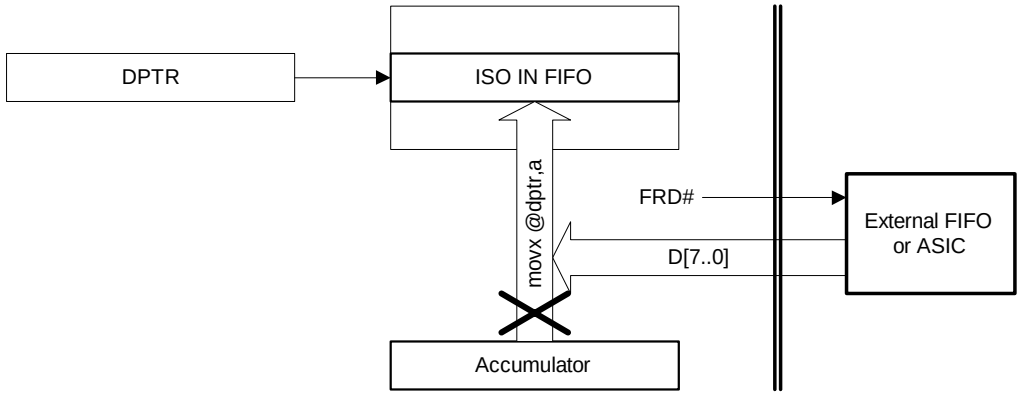


Figure 8-9. Fast Transfer, Outside Memory to EZ-USB

Fast reads are illustrated in Figure 8-9. When the fast mode is enabled, the DPTR points to an isochronous OUT FIFO register, and the 8051 executes the "movx @dptr,a" instruction, the EZ-USB core breaks the data path from the accumulator to the IN FIFO register, and instead writes the IN FIFO using outside data from D[7..0]. The EZ-USB core synchronizes this transfer by generating a FIFO Read Strobe FRD# (Fast Read). A choice of eight waveform is available for the read strobe, as shown in the next section.

8.7 Fast Transfer Timing

The 8051 sets bits in the FASTXFR register to select the fast ISO and/or fast BULK mode and to adjust the timing and polarity of the read and write strobes FRD# and FWR#.

FASTXFR **Fast Transfer Control** **7FE2**

b7	b6	b5	b4	b3	b2	b1	b0
FISO	**FBLK**	**RPOL**	**RMOD1**	**RMOD0**	**WPOL**	**WMOD1**	**WMOD0**

Figure 8-10. The FASTXFR Register Controls FRD# and FWR# Strobes

The 8051 sets FISO=1 to select the fast ISO mode and FBLK=1 to select the fast Bulk mode. The 8051 selects read and write strobe pulse polarities with the RPOL and WPOL bits, where 0=active low, and 1=active high. Read and write strobe timings are set by

RMOD1-RMOD0 for read strobes and WMOD1-WMOD0 for write strobes, as shown in Figure 8-11 (write) and Figure 8-12 (read).

> ***Note***
>
> When using the fast transfer feature, be sure to enable the FRD# and FWR# strobe signals in the PORTACFG register.

8.7.1 Fast Write Waveforms

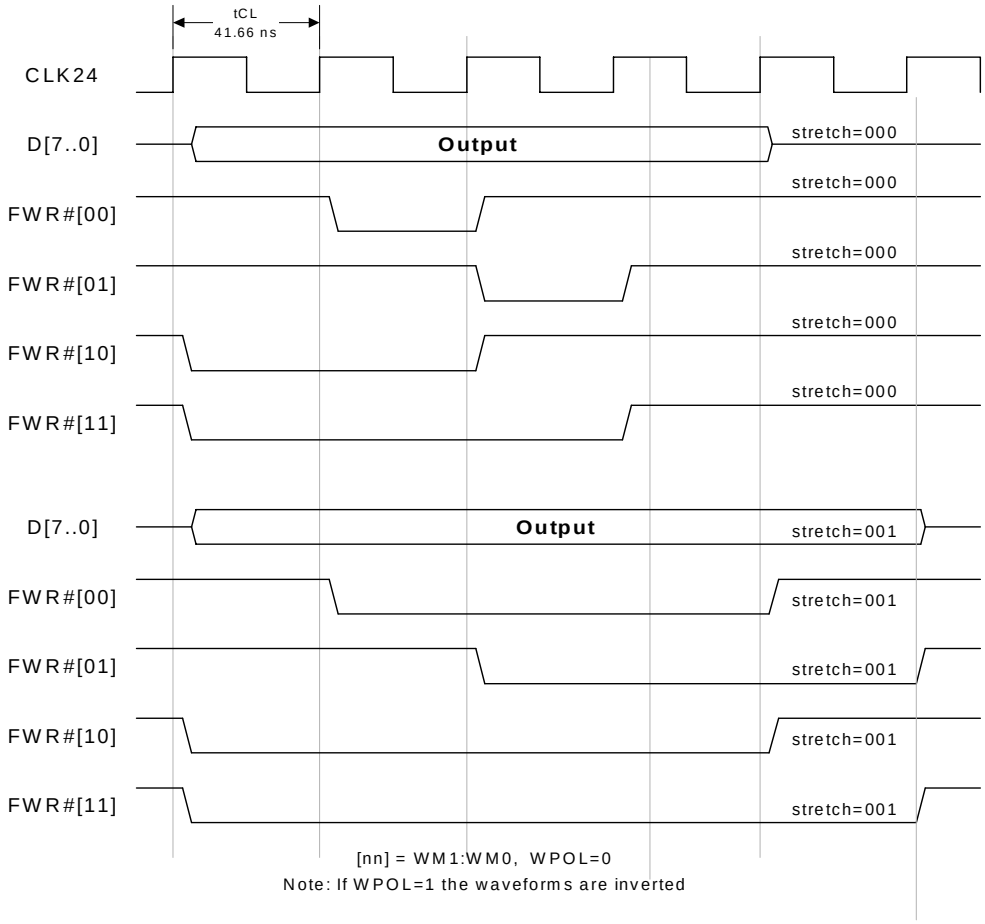


Figure 8-11. Fast Write Timing

The timing choices for fast write pulses (FWR#) are shown in Figure 8-11. The 8051 can extend the output data and widths of these pulses by setting cycle stretch values greater than zero in the 8051 Clock Control Register CKCON (at SFR location 0x8E). The top five waveforms show the fastest write timings, with a stretch value of 000, which performs the write in eight 8051 clocks. The bottom five waveforms show the same waveforms with a stretch value of 001.

8.7.2 Fast Read Waveforms

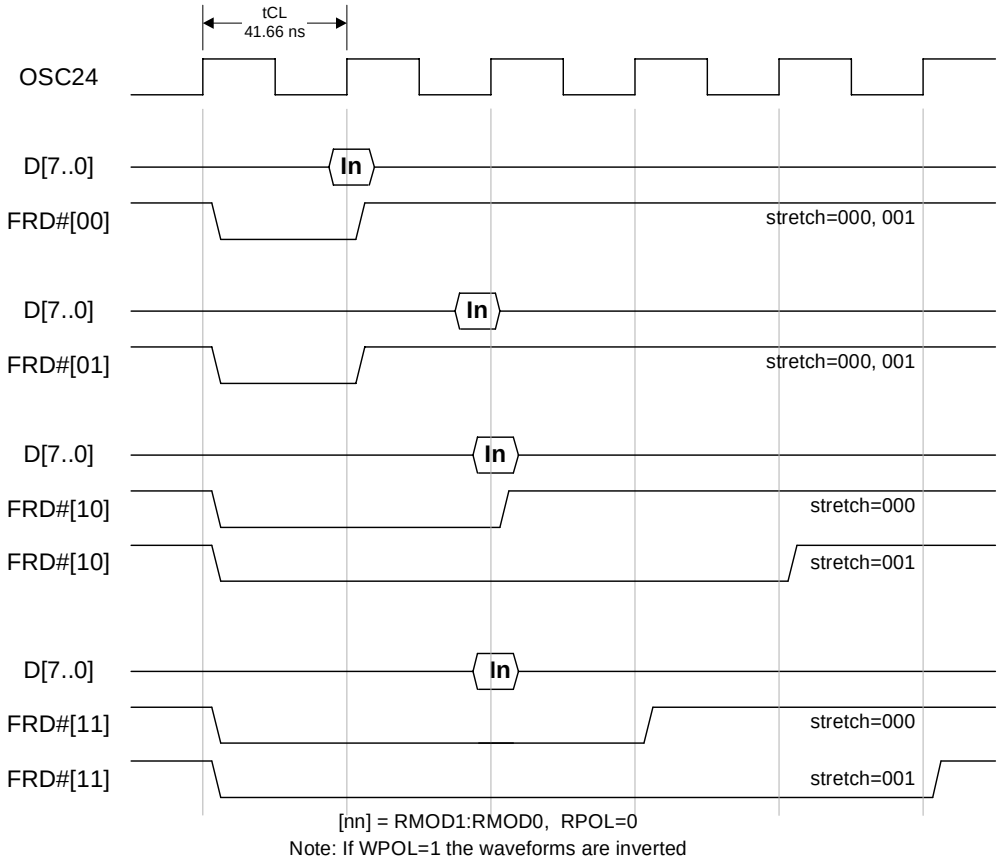


Figure 8-12. Fast Read Timing

The timing choices for fast read pulses (FRD#) are shown in Figure 8-12. Read Strobe waveforms for stretch values of 000 and 001 are indicated. Although two of the read strobe widths can be extended using stretch values greater than 000, the times that the input data is sampled by the EZ-USB core remains the same as shown.

FRD# strobes[00] and [01], along with the OSC24 clock signal are typically used to connect to an external synchronous FIFO. The on-clock-wide read strobe ensures that the FIFO address advances only once per clock. The second strobe [01] is for FIFOs that put data on the bus one clock after the read strobe. Stretch values above 000 serve only to extend the 8051 cycle times, without affecting the width of the FRD# strobe.

FRD# strobes [10] and [11] are typically connected to an external *asynchronous* FIFO, where no clock is required. Strobe [10] samples the data at the same time as strobe [11], but provides a wider pulse width (for stretch=000), which is required by some audio CODECS. Timing values for these strobe signals are given in Chapter 13, "EZ-USB AC/DC Parameters."

8.8 Fast Transfer Speed

The 8051 code example in Figure 8-13 shows a transfer loop for moving external FIFO data into the endpoint 8-IN FIFO. This code moves data from an external FIFO attached to the EZ-USB data bus and strobed by the FRD# signal, into the FIFO register IN8DATA

```
(init)   mov   dptr,#FASTXFR     ; set up the fast ISO transfer mode
         mov   a,#10000000b      ; FISO=1, RPOL=0, RM1-0 = 00
         movx  @dptr,a           ; load the FASTXFR register
         mov   dptr,#IN8DATA     ; pointer to IN endpoint FIFO
         mov   r7,#80            ; r7 is loop counter, 8 bytes per loop
;
loop:    movx  @dptr,a           ; (2) write IN FIFO using byte from external bus
         movx  @dptr,a           ; (2) again
         movx  @dptr,a           ; (2) again
         movx  @dptr,a           ; (2) again
         movx  @dptr,a           ; (2) again
         movx  @dptr,a           ; (2) again
         movx  @dptr,a           ; (2) again
         movx  @dptr,a           ; (2) again
         djnz  r7,loop           ; (3) do eight more, 'r7' times
```

Figure 8-13. 8051 Code to Transfer 640 Bytes of External Data to an Isochronous IN FIFO

This routine uses a combination of in-line and looped code to transfer 640 bytes into the EP8IN FIFO from an external FIFO. The loop transfers eight bytes in 19 cycles, and it takes 80 times through the loop to transfer 640 bytes. Therefore, the total transfer time is 80 times 19 cycles, or 1,520 cycles. The 640 byte transfer thus takes 1,520*166 ns or 252 μs, or approximately *one-fourth* of the 1-ms USB frame time.

Using this routine, the time to completely fill one isochronous FIFO with 1,024 bytes (assuming all 1,024 isochronous FIFO bytes are assigned to one endpoint) would be 128

times 19 cycles, or 2,432 cycles. The 1,024 byte transfer would take 403 μs, *less than half* of the 1-ms USB frame time.

If still faster time is required, the routine can be modified to put more of the MOVX instructions in-line. For example, with 16 in-line MOVX instructions, the transfer time for 1,024 bytes would be 35 cycles times 64 loops or 2,240 cycles, or 371 μs, an 8% speed improvement over the eight instruction loop.

8.9 Other Isochronous Registers

Two additional registers, ISOCTL and ZBCOUT, provide additional isochronous endpoint features.

8.9.1 Disable ISO

ISOCTL **Isochronous Control** **7FA1**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	**PPSTAT**	**MBZ**	**MBZ**	**ISODISAB**

Figure 8-14. ISOCTL Register

Bit zero of the ISOCTL register is called ISODISAB. When the 8051 sets ISODISAB=1, all sixteen of EZ-USB endpoints are disabled. If ISODISAB=1, EP8IN=EP15IN and EP8OUT-EP15OUT should not be used. ISODISAB is cleared at power-on.

When ISODISAB=1, the 2,048 bytes of RAM normally used for isochronous buffers is available to the 8051 as XDATA RAM (*not* program memory), from 0x2000 to 0x27FF in internal memory. When ISODISAB=1, the behavior of the RD# and WR# strobe signals changes to reflect the additional 2 KB of memory inside the EZ-USB chip. This is shown in Table 8-2.

Table 8-2. Addresses for RD# and WR# vs. ISODISAB bit

ISODISAB	RD#, WR#
0 (default)	2000-7B40, 8000-FFFF
1	**2800**-7B40, 8000-FFFF

ISOCTL register bits shown as MBZ (must be zero) must be written with zeros. The PPSTAT bit toggles every SOF, and may be written with any value (no effect). Therefore, to disable the isochronous endpoints, the 8051 should write the value 0x01 to the ISOCTL register.

Caution!

If you use this option, be absolutely certain that the host never sends isochronous data to your device. Isochronous data directed to a disabled isochronous endpoint system will cause unpredictable operation.

Note

The Autopointer is not usable from 0x2000-0x27FF (the reclaimed ISO buffer RAM) when ISODISAB=1.

8.9.2 Zero Byte Count Bits

When the SOF interrupt is asserted, the 8051 normally checks the isochronous OUT endpoint FIFOs for data. Before reading the byte count registers and unloading an isochronous FIFO, the firmware may wish to check for a zero byte count. In this case, the 8051 can check bits in the ZBCOUT register. Any endpoint bit set to "1" indicates that no OUT bytes were received for that endpoint during the previous frame. Figure 8-15 shows this register.

ZBCOUT **Zero Byte Count Bits** **7FA2**

b7	b6	b5	b4	b3	b2	b1	b0
EP15	**EP14**	**EP13**	**EP12**	**EP11**	**EP10**	**EP9**	**EP8**

Figure 8-15. ZBCOUT Register

The EZ-USB core updates these bits every SOF.

8.10 ISO IN Response with No Data

The ISOSEND0 bit (bit 7 in the USBPAIR register) is used when the EZ-USB chip receives an isochronous IN token while the IN FIFO is empty. If ISOSEND0=0 (the default value) the EZ-USB core does not respond to the IN token. If ISOSEND0=1, the EZ-USB core sends a zero-length data packet in response to the IN token. Which action to take depends on the overall system design. The ISOSEND0 bit applies to all of the isochronous IN endpoints, IN-8 through IN-15.

8.11 Using the Isochronous FIFOs

There is a window of time before and after each SOF (Start of Frame) when accessing the Isochronous FIFOs will cause data corruption or loss of data.

This is because each isochronous endpoint is actually a pair of FIFOs, and the FIFOs are swapped at SOF time. The swap occurs about 10 µs before the SOF interrupt signals the 8051 code. (Between SOFs, one FIFO of the pair is accessible to the 8051, while the other FIFO of the pair transfers data to or from the USB.)

Workaround#1: If you can pre-assemble the data into a buffer, blast the data (in a tight loop) into the new FIFO *just after* the SOF interrupt, typically inside the SOF ISR (Interrupt Service Routine).

Workaround#2: If you can't pre-assemble the data into a buffer, prevent access during SOFs by setting a time (in the SOF ISR) to time out and halt access just before the *next* SOF. Set the timer for about 950 µs (ms minus 50 µs).

Be careful of interrupt latency delaying the timeout ISR. That is, the timeout ISR may be prevented from halting access by getting preempted by a higher priority interrupt(s), made worse by the necessary practice of disabling interrupts to manage shared resources, resources that are shared between the ISRs and background process.

To prevent drift of the timer relative to SOFs, restart the timer after each SOF (typically in the SOF ISR).

9 EZ-USB Interrupts

9.1 Introduction

The EZ-USB enhanced 8051 responds to the interrupts shown in Table 9-1. Interrupt sources that are not present in the standard 8051 are shown as checked in the "New" column. The three interrupts used by the EZ-USB core are shown in **bold** type.

Table 9-1. EZ-USB Interrupts

New	8051 Interrupt (IRQ name)	Source	Vector (hex)	Natural Priority
	IE0	INT0# Pin	03	1
	TF0	Timer 0 Overflow	0B	2
	IE1	INT1# Pin	13	3
	TF1	Timer 1 Overflow	1B	4
	RI_0 & TI_0	UART0 Rx & Tx	23	5
P	TF2	Timer 2 Overflow	2B	6
P	**Resume (PFI)**	**WAKEUP# Pin or USB Core**	33	0
P	RI_1 & TI_1	UART1 Rx & Tx	3B	7
P	**USB (INT2)**	**USB Core**	43	8
P	I²C (INT3)	**USB Core**	4B	9
P	IE4	IN4 Pin	53	10
P	IE5	INT5# Pin	5B	11
P	IE6	INT6 Pin	63	12

The **Natural Priority** column in Table 9-1 shows the 8051 interrupt priorities. As explained in Appendix C, the 8051 can assign each interrupt to a high or low priority group. The 8051 resolves priorities within the groups using the natural priorities.

9.2 USB Core Interrupts

The EZ-USB core provides three interrupt request types, which are described in the following sections:

Wakeup - After the EZ-USB chip detects USB suspend and the 8051 has entered its idle state, the EZ-USB core responds to an external signal on its WAKEUP# pin or resumption of USB bus activity by re-starting the EZ-USB oscillator and resuming 8051 operation.

USB Signaling - These include 16 bulk endpoint interrupts, three interrupts not specific to a particular endpoint (SOF), Suspend, USB Reset), and two interrupts for CONTROL transfers (SUTOK, SUDAV). These interrupts share the USB interrupt (INT2). The AN2122/26 versions have an interrupt indicating that a bulk packet was NAKd.

I^2C Transfers - (INT3).

9.3 Wakeup Interrupt

Chapter 10, "EZ-USB Resets" describes suspend-resume signaling in detail, along with a code example that uses the Wakeup interrupt.

Briefly, the USB host puts a device into SUSPEND by stopping bus activity to the device. When the EZ-USB core detects 3 ms of no bus activity, it activates the USB suspend interrupt request. If enabled, the 8051 takes the suspend interrupt, does power management housekeeping (shutting down power to external logic), and finishes by setting SFR bit PCON.0. This signals the EZ-USB core to enter a very low power mode by turning off the 12-MHz oscillator.

When the 8051 sets PCON.0, it enters an idle state. 8051 execution is resumed by activation of any enabled interrupt. The EZ-USB chip uses a dedicated interrupt for USB Resume. When external logic pulls WAKEUP# low (for example, when a keyboard key is pressed or a modem receives a ring signal) or USB bus activity resumes, the EZ-USB core re-starts the 12-MHz oscillator, allowing the 8051 to recognize the interrupt and continue executing instructions.

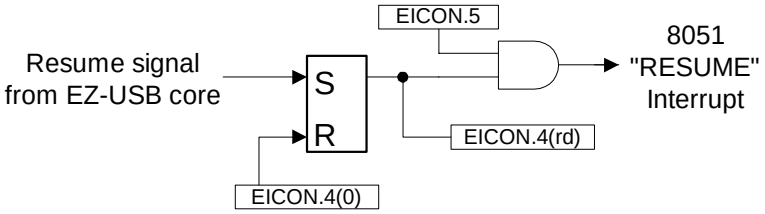


Figure 9-1. EZ-USB Wakeup Interrupt

Figure 9-1 shows the 8051 SFR bits associated with the RESUME interrupt. The EZ-USB core asserts the resume signal when the EZ-USB core senses a USB Global Resume, or when the EZ-USB WAKEUP# pin is pulled low. The 8051 enables the RESUME interrupt by setting EICON.5.

```
tb     EICON.5     ; enable Resume interrupt
```

The 8051 reads the RESUME interrupt request bit in EICON.4, and clears the interrupt request by writing a zero to EICON.4.

```
Resume_isr:   clr      EICON.4     ; clear the 8051 W/U
                                   ; interrupt request
              reti
```

9.4 USB Signaling Interrupts

Figure 9-2 shows the 21 USB requests that share the 8051 USB (INT2) interrupt. The bottom IRQ, EP7-OUT, is expanded in the diagram to show the logic associated with each USB interrupt request. Vector 05, not shown in the diagram, exists only in the AN2122/ AN2126, and is described later in this chapter.

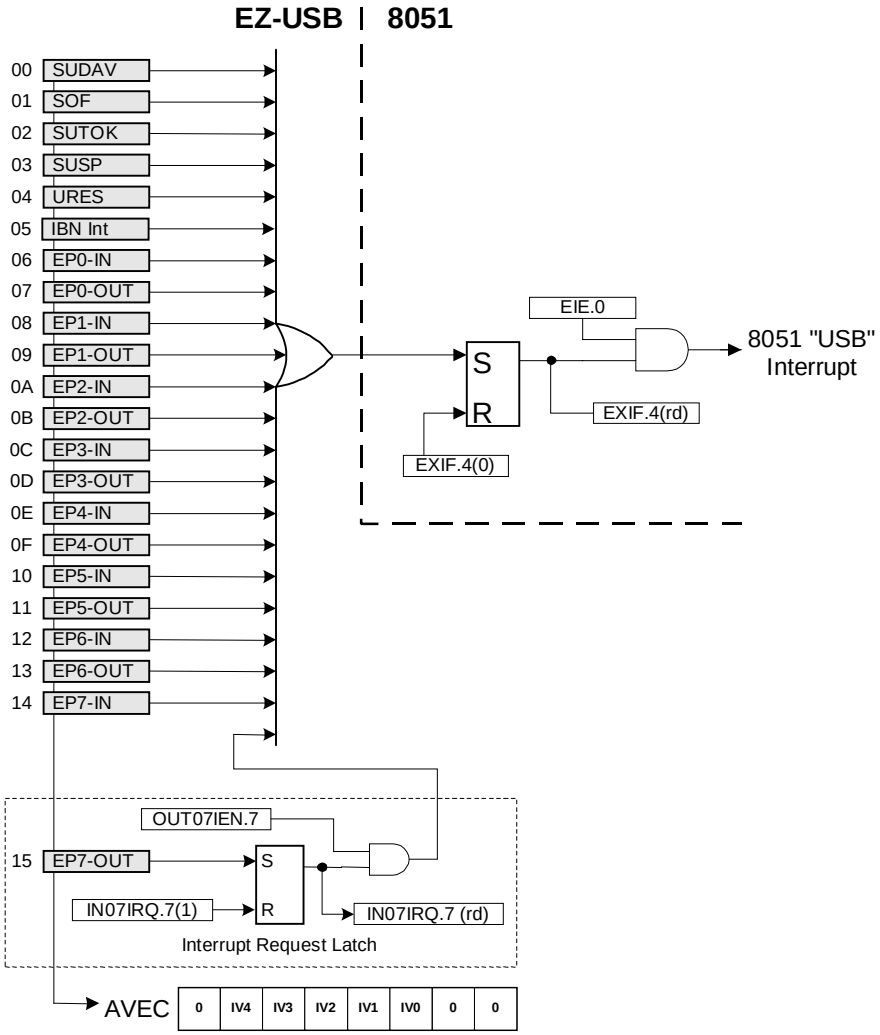


Figure 9-2. USB Interrupts

Referring to the logic inside the dotted lines, each USB interrupt source has an interrupt request latch. The EZ-USB core sets an IRQ bit, and the 8051 clears an IRQ bit by writing a “1” to it. The output of each latch is ANDed with an IEN (Interrupt Enable) bit and then ORd with all the other USB interrupt request sources.

The EZ-USB core prioritizes the USB interrupts, and constructs an Autovector, which appears in the AVEC register. The interrupt vector values IV[4..0] are shown to the left of the interrupt sources (shaded boxes). 00 is the highest priority, 15 is the lowest. If two USB interrupts occur simultaneously, the prioritization affects which one is first indicated in the AVEC register. If the 8051 has enabled Autovectoring, the AVEC byte replaces byte 0x45 in 8051 program memory. This causes the USB interrupt automatically to vector to different addresses for each USB interrupt source. This mechanism is explained in detail in Section 9.10, "USB Autovectors."

Due to the OR gate in Figure 9-2, any of the USB interrupt sources sets the 8051 *USB* interrupt request latch, whose state appears as an interrupt request in the 8051 SFR bit EXIF.4. The 8051 enables the USB interrupt by setting SFR bit EIE.0. To clear the USB interrupt request the 8051 writes a zero to the EXIF.4 bit. Note that this is the opposite of clearing any of the individual USB interrupt sources, which the 8051 does by writing a “1” to the IRQ bit.

When a USB resource requires service (for example, a SOF token arrives or an OUT token arrives on a BULK endpoint), two things happen. First, the corresponding Interrupt Request Latch is set. Second, a pulse is generated, ORd with the other USB interrupt logic, and routed to the 8051 INT2 input. The pulse is required because INT2 is edge triggered.

When the 8051 finishes servicing a USB interrupt, it clears the particular IRQ bit by writing a “1” to it. If any other USB interrupts are pending, the act of clearing the IRQ causes the EZ-USB core logic to generate another pulse for the highest-priority pending interrupt. If more that one is pending, they are serviced in the priority order shown in Figure 9-2, starting with SUDAV (priority 00) as the highest priority, and ending with EP7-OUT (priority 15) as the lowest.

Important

It is important in any USB Interrupt Service Routine (ISR) to clear the 8051 INT2 interrupt **before** clearing the particular USB interrupt request latch. This is because as soon as the USB interrupt is cleared, any pending USB interrupt will pulse the 8051 INT2 input, and if the INT2 interrupt request latch has not been previously cleared the pending interrupt will be lost.

Figure 9-3 illustrates a typical USB ISR for endpoint 2-IN.

```
USB_ISR:  push   dps
          push   dpl
          push   dph
          push   dpl1
          push   dph1
          push   acc
;
          mov    a,EXIF         ; FIRST clear the USB (INT2) interrupt request
          clr    acc.4
          mov    EXIF,a         ; Note:  EXIF reg is not 8051 bit-addressable
;
          mov    dptr,#IN07IRQ  ; now clear the USB interrupt request
          mov    a,#00000100b   ; use IN2 as example
          movx   @dptr,a
;
; (perform interrupt routine stuff)
;
          pop    acc
          pop    dph1
          pop    dpl1
          pop    dph
          pop    dpl
          pop    dps
;
          reti
```

Figure 9-3. The Order of Clearing Interrupt Requests is Important

IN07IRQ **Endpoints 0-7 IN Interrupt Requests** **7FA9**

b7	b6	b5	b4	b3	b2	b1	b0
IN7IR	**IN6IR**	**IN5IR**	**IN4IR**	**IN3IR**	**IN2IR**	**IN1IR**	**IN0IR**

OUT07IRQ **Endpoints 0-7 OUT Interrupt Requests** **7FAA**

b7	b6	b5	b4	b3	b2	b1	b0
OUT7IR	**OUT6IR**	**OUT5IR**	**OUT4IR**	**OUT3IR**	**OUT2IR**	**OUT1IR**	**OUT0IR**

USBIRQ **USB Interrupt Request** **7FAB**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	**USESIR**	**SUSPIR**	**SUTOKIR**	**SOFIR**	**SUDAVIR**

IN07IEN **Endpoints 0-7 IN Interrupt Enables** **7FAC**

b7	b6	b5	b4	b3	b2	b1	b0
IN7IEN	**IN6IEN**	**IN5IEN**	**IN4IEN**	**IN3IEN**	**IN2IEN**	**IN1IEN**	**IN0IEN**

OUT07IEN **Endpoints 0-7 OUT Interrupt Enables** **7FAD**

b7	b6	b5	b4	b3	b2	b1	b0
OUT7IEN	**OUT6IEN**	**OUT5IEN**	**OUT4IEN**	**OUT3IEN**	**OUT2IEN**	**OUT1IEN**	**OUT0IEN**

USBIEN **USB Interrupt Enables** **7FAE**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	**URESIE**	**SUSPIE**	**SUTOKIE**	**SOFIE**	**SUDAVIE**

Figure 9-4. EZ-USB Interrupt Registers

Figure 9-4 shows the registers associated with the USB interrupts. Each interrupt source has an enable (IEN) and a request (IRQ) bit. The 8051 sets the IEN bit to enable the interrupt. The USB core sets an IRQ bit high to request an interrupt, and the 8051 clears an IRQ bit by writing a “1” to it.

The USBIEN and USBIRQ registers control the first five interrupts shown in Figure 9-2. The IN07IEN and OUT07 registers control the remaining 16 USB interrupts, which correspond to the 16 bulk endpoints IN0-IN7 and OUT0-OUT7.

The 21 USB interrupts are now described in detail.

9.5 SUTOK, SUDAV Interrupts

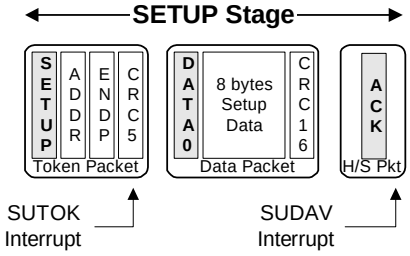


Figure 9-5. SUTOK and SUDAV Interrupts

SUTOK and SUDAV are supplied to the 8051 by EZ-USB CONTROL endpoint zero. The first portion of a USB CONTROL transfer is the SETUP stage shown in Figure 9-5. (A full CONTROL transfer is the SETUP stage shown in Figure 7-1.) When the EZ-USB core decodes a SETUP packet, it asserts the SUTOK (SETUP Token) interrupt request. After the EZ-USB core has received the eight bytes error-free and copied them into eight internal registers at SETUPDAT, it asserts the SUDAV interrupt request.

The 8051 program responds to the SUDAV interrupt by reading the eight SETUP data bytes in order to decode the USB request (Chapter 7, "EZ-USB Endpoint Zero").

The SUTOK interrupt is provided to give advance warning that the eight register bytes at SETUPDAT are about to be over-written. It is useful for debug and diagnostic purposes.

9.6 SOF Interrupt

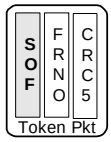


Figure 9-6. A Start Of Frame (SOF) Packet

USB Start of Frame interrupt requests occur every millisecond. When the EZ-USB core receives an SOF packet, it copies the eleven-bit frame number (FRNO in Figure 9-6) into the USBFRAMEH and USBFRAMEL registers, and activates the SOF interrupt request. The 8051 services all isochronous endpoint data as a result of the SOF interrupt.

9.7 Suspend Interrupt

If the EZ-USB detects 3 ms of no bus activity, it activates the SUSP (Suspend) interrupt request. A full description of Suspend-Resume signaling appears in Chapter 11, "EZ-USB Power Management."

9.8 USB RESET Interrupt

The USB signals a bus reset by driving both D+ and D- low for at least 10 ms. When the EZ-USB core detects the onset of USB bus reset, it activates the URES interrupt request.

9.9 Bulk Endpoint Interrupts

The remaining 16 USB interrupt requests are indexed to the 16 EZ-USB bulk endpoints. The EZ-USB core activates a bulk interrupt request when the endpoint buffer requires service. For an OUT endpoint, the interrupt request signifies that OUT data has been sent from the host, validated by the EZ-USB core, and is sitting in the endpoint buffer memory. For an IN endpoint, the interrupt request signifies that the data previously loaded by the 8051 into the IN endpoint buffer has been read and validated by the host, making the IN endpoint buffer ready to accept new data.

The EZ-USB core sets an endpoint's interrupt request bit when the endpoint's busy bit (in the endpoint CS register) goes low, indicating that the endpoint buffer is available to the 8051. For example, when endpoint 4-OUT receives a data packet, the busy bit in the OUT4CS register goes low, and OUT07IRQ.4 goes high, requesting the endpoint 4-OUT interrupt.

9.10 USB Autovectors

The USB interrupt is shared by 21 interrupt sources. To save the code and processing time required to sort out which USB interrupt occurred, the EZ-USB core provides a second level of interrupt vectoring, called "Autovectoring." When the 8051 takes a USB interrupt, it pushes the program counter onto its stack, and then executes a jump to address 43, where it expects to find a jump instruction to an interrupt service routine. The 8051 jump instruction is encoded as follows:

Table 9-2. 8051 JUMP Instruction

Address	Op-Code	Hex Value
0043	Jump	0x02
0044	AddrH	0xHH
0045	AddrL	0xLL

If Autovectoring is enabled (AVEN=1 in the USBBAV register), the EZ-USB core substitutes its AVEC byte for the byte at address 0x0045. Therefore, if the programmer preloads the high byte ("page") of a jump table address at location 0x0044, the core-inserted byte at 0x45 will automatically direct the JUMP to one of 21 addresses within the page. In the jump table, the programmer then puts a series of jump instructions to each particular ISR.

Table 9-3. A Typical USB Jump Table

Table Offset	Instruction
00	JMP SUDAV_ISR
04	JMP SOF_ISR
08	JMP SUTOK_ISR
0C	JMP SUSPEND_ISR
10	JMP USBRESET_ISR
14	JMP IBN_ISR (2122/2126 only, otherwise NOP)
18	JMP EP0IN _ISR
1C	JMP EP0OUT_ISR
20	JMP IN1BUF_ISR
24	JMP EP1OUT_ISR
28	JMP EP2IN_ISR
2C	JMP EP2OUT_ISR
30	JMP EP3IN_ISR
34	JMP EP3OUT_ISR
38	JMP EP4IN_ISR
3C	JMP EP4OUT_ISR
40	JMP EP5IN_ISR
44	JMP EP5OUT_ISR
48	JMP EP6IN_ISR
4C	JMP EP6OUT_ISR
50	JMP EP7IN_ISR
54	JMP EP7OUT_ISR

9.11 Autovector Coding

A detailed example of a program that uses Autovectoring is presented in Section 6.14, "Interrupt Bulk Transfer Example." The coding steps are summarized here. To employ EZ-USB Autovectoring:

1. Insert a jump instruction at 0x43 to a table of jump instructions to the various USB interrupt service routines.

2. Code the jump table with jump instructions to each individual USB interrupt service routine. This table has two important requirements, arising from the format of the AVEC byte (zero-based, with 2 LSBs set to 0):

   - It must begin on a page boundary (address 0xNN00).
   - The jump instructions must be four bytes apart.
   - The interrupt service routines can be placed anywhere in memory.
   - Write initialization code to enable the USB interrupt (INT2), and Autovectoring.

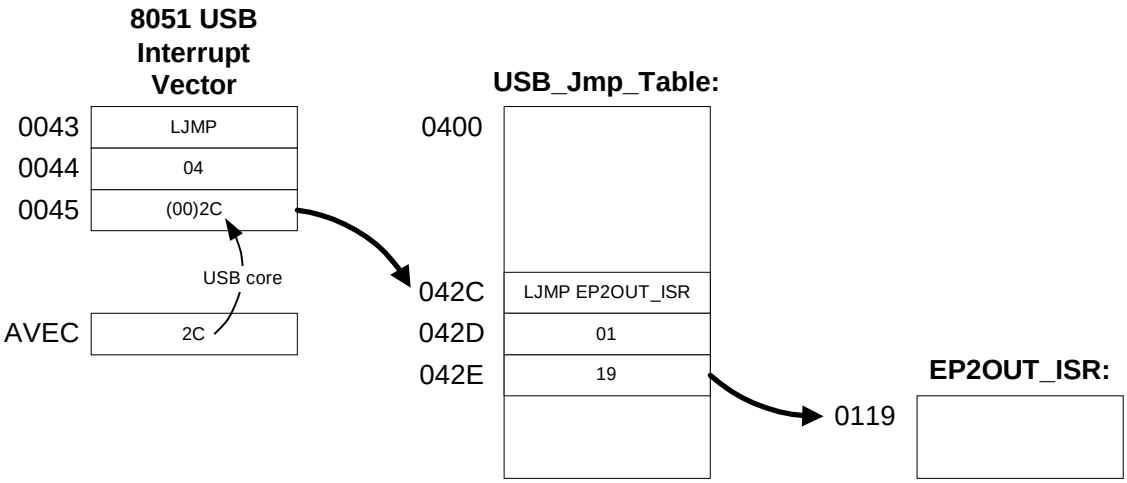


Figure 9-7. The Autovector Mechanism in Action

Figure 9-7 illustrates an ISR that services endpoint 2-OUT. When endpoint 2-OUT requires service, the EZ-USB core activates the USB interrupt request, vectoring the 8051 to location 0x43. The jump instruction at this location, which was originally coded as "LJMP 04-**00**" becomes "LJMP 04-**2C**" due to the EZ-USB core substituting **2C** as the Autovector byte for Endpoint 2-OUT (Table 9-3). The 8051 jumps to 042C, where it executes the jump instruction to the endpoint 2-OUT ISR shown in this example at address 0119. Once the 8051 takes the vector at 0043, initiation of the endpoint-specific ISR takes only eight 8051 cycles.

9.12 I²C Interrupt

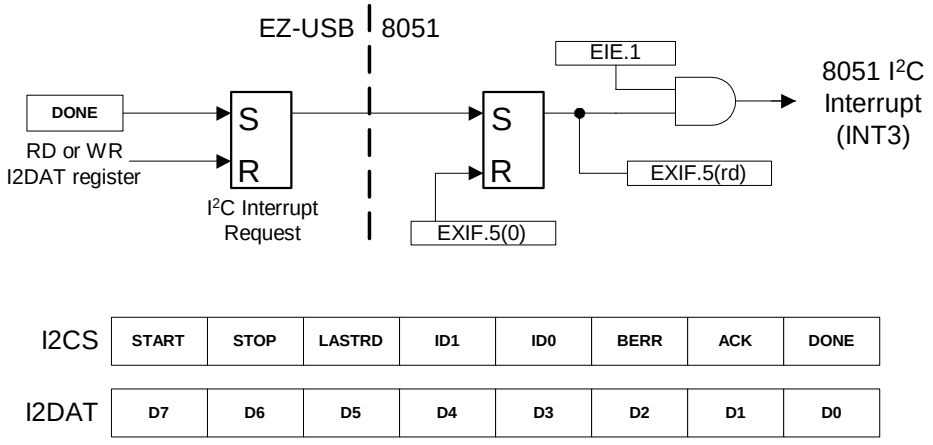


Figure 9-8. I²C Interrupt Enable Bits and Registers

Chapter 4, "EZ-USB Input/Output" describes the 8051 interface to the EZ-USB I²C controller. The 8051 uses two registers, I2CS (I²C Control and Status) and I2DAT (I²C Data) to transfer data over the I²C bus. The EZ-USB core signals completion of a byte transfer by setting the DONE bit (I2CS.0) high, which also sets an I²C interrupt request latch (Figure 9-8). This interrupt request is routed to the 8051 INT3 interrupt.

The 8051 enables the I²C interrupt by setting EIE.1=1. The 8051 determines the state of the interrupt request flag by reading EXIF.5, and resets the INT3 interrupt request by writing a zero to EXIF.5. Any 8051 read or write to the I2DAT or I2CS register automatically clears the I²C interrupt request.

9.13 In Bulk NAK Interrupt - (AN2122/AN2126 only)

The EZ-USB family responds to an IN token from the host by loading an IN endpoint buffer and then *arming* the endpoint by loading a byte count for the endpoint. After the host successfully receives the IN data, the 8051 receives an EP-IN interrupt, signifying that the IN endpoint buffer is once again ready to accept data.

In some situations, the host may send IN tokens before the 8051 has loaded and armed an IN endpoint. To alert the 8051 that an IN endpoint is being *pinged*, the AN2122/26 add a set of interrupts, one per IN endpoint, that indicate that an IN endpoint just sent a NAK to the host. This happens when the host sends an IN token and the IN endpoint does not have data (yet) for the host.

The new interrupt is called "IBN," for IN Bulk NAK. Its INT2 Autovector is 05, which was previously reserved in the EZ-USB family.

The IBN interrupt requests and enables are controlled by two new registers. Note that because the IBN interrupt exists only in the AN2122/AN2126, which has 6 bulk IN endpoints, there are IRQ and IEN bits endpoints IN0 through IN6.

IBNIRQ **IN Bulk NAK Interrupt Requests** **7FB0**

b7	b6	b5	b4	b3	b2	b1	b0
-	**EP6IN**	**EP5IN**	**EP4IN**	**EP3IN**	**EP2IN**	**EP1IN**	**EP0IN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 9-9. IN Bulk NAK Interrupt Request Register

IBNEN **IN Bulk NAK Interrupt Enables** **7FB1**

b7	b6	b5	b4	b3	b2	b1	b0
-	**EP6IN**	**EP5IN**	**EP4IN**	**EP3IN**	**EP2IN**	**EP1IN**	**EP0IN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	0	0	0	0	0	0	0

Figure 9-10. IN Bulk NAK Interrupt Enable Register

Each of the individual IN endpoints may be enabled for an IBN interrupt using the IBNEN register. The 8051 sets an interrupt enable bit to "1" to enable the corresponding interrupt. The ISR tests the IBNIRQ bits to determine which endpoint or endpoints generated the interrupt request. As with all other EZ-USB interrupt requests, the 8051 clears an IBNIRQ bit by writing a "1" to it.

9.14 I²C STOP Complete Interrupt - (AN2122/AN2126 only)

I2CMODE **I²C Mode** **7FA7**

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	STOPIE	0
R	R	R	R	R	R	R/W	R
0	0	0	0	0	0	0	0

Figure 9-11. I²C Mode Register

The I²C interrupt includes one additional interrupt source in the AN2122/AN2126, a 1-0 transition of the STOP bit. To enable this interrupt, set the STOPIE bit in the I2CMODE register. The 8051 determines the interrupt source by checking the DONE and STOP bits in the I2CS register.

I2CS **I²C Control and Status** **7FA5**

b7	b6	b5	b4	b3	b2	b1	b0
START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE
R/W	R/W	R/W	R	R	R	R	R
0	0	0	X	X	0	0	0

Figure 9-12. I²C Control and Status Register

I2DAT **I²C Data** **7FA6**

b7	b6	b5	b4	b3	b2	b1	b0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 9-13. I²C Data

The two registers that the 8051 uses to control I^2C transfers are shown above. In the EZ-USB family, an I^2C interrupt request occurs on INT3 whenever the DONE bit (I2CS.0) makes a 0-to-1 transition. This interrupt signals the 8051 that the I^2C controller is ready for another command.

The 8051 concludes I^2C transfers by setting the STOP bit (I2CS.6). When the STOP condition has been sent over the I^2C bus, the I^2C controller resets I2CS.6 to zero. *During the time the I^2C controller is generating the stop condition, it ignores accesses to the I2CS and I2DAT registers.* The 8051 code should therefore check the STOP bit for zero before writing new data to I2CS or I2DAT. In the EZ-USB family, it does this by polling the I2CS.6 bit.

10 EZ-USB Resets

10.1 Introduction

The EZ-USB chip has three resets:

- A Power-On Reset (POR), which turns on the EZ-USB chip in a known state.
- An 8051 reset, controlled by the EZ-USB core.
- A USB bus reset, sent by the host to reset a device.

This chapter describes the effects of these three resets.

10.2 EZ-USB Power-On Reset (POR)

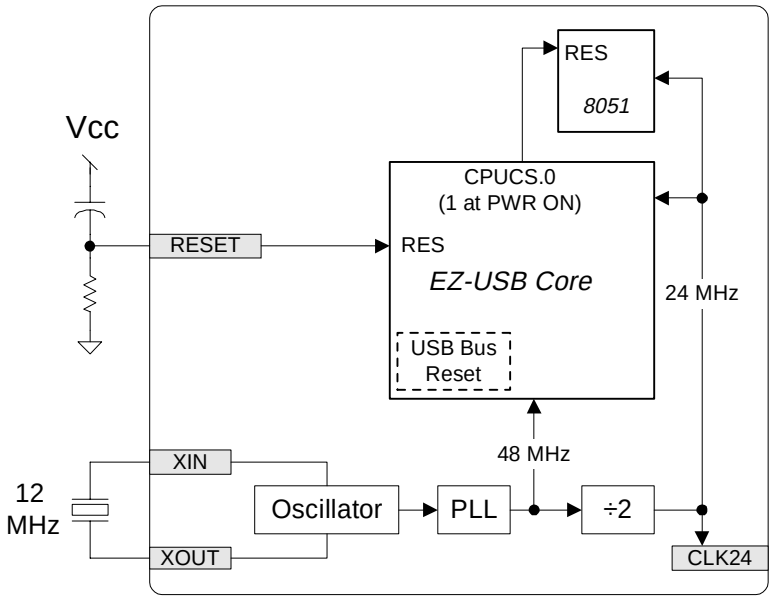


Figure 10-1. EZ-USB Resets

When power is first applied to the EZ-USB chip, the external R-C circuit holds the EZ-USB core in reset until the on-chip PLL stabilizes. The CLK24 pin is active as soon as power is applied. The 8051 may clear an EZ-USB control bit, CLK24OE, to inhibit the CLK24 output pin for EMI-sensitive applications that do not need this signal. External logic can force a chip reset by pulling the RESET pin HI. The RESET pin is normally

connected to Vcc through a 1 μF capacitor and to GND through a 10-K resistor (Figure 10-1). The oscillator and PLL are unaffected by the state of the RESET pin.

The CLK24 signal is active while RESET = HI. When RESET returns LO, the activity on the CLK24 pin depends on whether or not the EZ-USB chip is in suspend state. If in suspend, CLK24 stops. Resumption of USB bus activity or asserting the WAKEUP# pin LO re-starts the CLK24 signal.

Power-on default values for all EZ-USB register bits are shown in Chapter 12, "EZ-USB Registers." Table 10-1 summarizes reset states that affect USB device operation. Note that the term “Power-On Reset” refers to a reset initiated by application of power, *or* by assertion of the RESET pin.

Table 10-1. EZ-USB States After Power-On Reset (POR)

Item	Register	Default Value	Comment
1	Endpoint Data	xxxxxxxx	
2	Byte Counts	xxxxxxxx	
3	CPUCS	rrrr0011	rrrr=rev number, b1 =CLK24OE, b0=8051RES
4	PORT Configs	00000000	IO, not alternate functions
5	PORT Registers	xxxxxxxx	
6	PORT OEs	00000000	Inputs
7	Interrupt Enables	00000000	Disabled
8	Interrupt Reqs	00000000	Cleared
9	Bulk IN C/S	00000000	Bulk IN endpoints not busy (unarmed)
10	Bulk OUT C/S*	00000000	Bulk OUT endpoints not busy (unarmed)
11	Toggle Bits	00000000	Data toggles = 0
12	USBCS	00000100	RENUM=0, DISCOE=1 (Discon pin drives)
13	FNADDR	00000000	USB Function Address
14	IN07VAL	01010111	EP0,1,2,4,6 IN valid
15	OUT07VAL	01010101	EP0,2,4,6 OUT valid
16	INISOVAL	00000111	EP8,9,10 IN valid
17	OUTISOVAL	00000111	EP8,910OUT valid
18	USBPAIR	0x000000	ISOsend0 (b7) = 0, no pairing
19	USBBAV	00000000	Break condition cleared, no Autovector
20	Configuration	0	Internal EZ-USB core value
21	Alternate Setting	0	Internal EZ-USB core value

* When the 8051 is released from reset, the EZ-USB automatically arms the Bulk OUT endpoints by setting their CS registers to 000000010b.

From Table 10-1, at power-on:

- Endpoint data buffers and byte counts are un-initialized (1,2).
- The 8051 is held in reset, and the CLK24 pin is enabled (3).
- All port pins are configured as input ports (4-6).
- USB interrupts are disabled, and USB interrupt requests are cleared (7-8).
- Bulk IN and OUT endpoints are unarmed, and their stall bits are cleared (9). The EZ-USB core will NAK IN or OUT tokens while the 8051 is reset. OUT endpoints are enabled when the 8051 is released from reset.
- Endpoint toggle bits are cleared (11).
- The ReNum bit is cleared. This means that the EZ-USB core, and not the 8051, initially responds to USB device requests (12).
- The USB function address register is set to zero (13).
- The endpoint valid bits are set to match the endpoints used by the default USB device (14-17).
- Endpoint pairing is disabled. Also, ISOSend0=0, meaning that if an Isochronous endpoint receives an IN token without being loaded by the 8051 in the previous frame, the EZ-USB core does not generate any response (18).
- The breakpoint condition is cleared, and autovectoring is turned off (19).
- Configuration Zero, Alternate Setting Zero is in effect (20-21).

10.3 Releasing the 8051 Reset

The EZ-USB register bit CPUCS.0 resets the 8051. This bit is HI at power-on, initially holding the 8051 in reset. There are three ways to release the 8051 from reset:

- By the host, as the final step of a RAM download.
- Automatically, as part of an EEPROM load.
- Automatically, when external ROM is used (EA=1).

10.3.1 RAM Download

Once enumerated, the host can download code into the EZ-USB RAM using the “Firmware Load” vendor request (Chapter 7, "EZ-USB Endpoint Zero"). The last packet loaded writes 0 to the CPUCS register, which clears the 8051 RESET bit.

Note

The other bit in the CPUCS register, CLK24OE, is writable only by the 8051, so the host writing a zero byte to this register does not turn off the CLK24 signal.

10.3.2 EEPROM Load

Chapter 5 describes the EEPROM boot loads in detail. Briefly, at power-on, the EZ-USB core checks for the presence of an EEPROM on its I^2C bus. If found, it reads the first EEPROM byte. If it reads 0xB2 as the first byte, the EZ-USB core downloads 8051 code from the EEPROM into internal RAM. The last byte of a “B2” load writes 0x00 to the CPUCS register (at 0x7F92), which releases the 8051 from reset.

10.3.3 External ROM

EZ-USB systems can use external program memory containing 8051 code and USB device descriptors, which include the VID/DID/PID bytes. Because these systems do no require and I^2C EEPROM to supply the VID/DID/PID, the EZ-USB core automatically releases 8051 reset when:

1. EA=1 (External code memory), *and*

2. No “B0/B2” EEPROM is detected on the I^2C bus.

The EZ-USB core also sets the ReNum bit to “1,” giving USB control to the 8051.

10.4 8051 Reset Effects

Once the 8051 is running, the USB host may reset the 8051 by downloading the value 0x01 to the CPUCS register. The host might do this in preparation for loading code overlays, effectively magnifying the size of the internal EZ-USB RAM. For such applications it is important to know the state of the EZ-USB chip during and after an 8051 reset. In this

section, this particular reset is called an “8051 Reset,” and should not be confused with the POR described in Section 10.2, "EZ-USB Power-On Reset (POR)." This discussion applies only to the condition where the EZ-USB chip is powered, and the 8051 is reset by the host setting the CPUCS register to 0.

The basic USB device configuration remains intact through an 8051 reset. Valid endpoints remain valid, the USB function address remains the same, and the IO ports retain their configurations and values. Stalled endpoints remain stalled, and data toggles don’t change. The only effects of an 8051 reset are as follows:

- USB interrupts are disabled, but pending interrupt requests remain pending.
- **During** the 8051 Reset, all bulk endpoints are unarmed, causing the EZ-USB core to NAK and IN or OUT tokens.
- **After** the 8051 Reset is removed, the OUT bulk endpoints are automatically armed. OUT endpoints are thus ready to accept *one* OUT packet before 8051 intervention is required.
- The breakpoint condition is cleared.

The ReNum bit is not affected by an 8051 reset.

When the 8051 comes out of reset, the pending interrupts are kept pending, but disabled (1). This gives the firmware writer the choice of acting on pre-8051-reset USB events, or ignoring them by clearing the pending interrupt(s).

During the 8051 reset time, the EZ-USB core holds off any USB traffic by NAKing IN and OUT tokens (2). The EZ-USB core automatically arms the OUT endpoints when the 8051 exits the reset state (3).

USBBAV.3, the breakpoint BREAK bit, is cleared (4). The other bits in the USBBAV register are unaffected.

10.5 USB Bus Reset

The host signals a USB Bus Reset by driving an SE0 state (both D+ and D- data lines low) for a minimum of 10 ms. The EZ-USB core senses this condition, requests the 8051 USB Interrupt (INT2), and supplies the interrupt vector for a USB Reset. A USB reset affects the EZ-USB resources as shown in Table 10-2.

Table 10-2. EZ-USB States After a USB Bus Reset

Item	Register	Default Value	Comment
1	Endpt Data	uuuuuuuu	u = unchanged
2	Byte Counts	uuuuuuuu	
3	CPUCS	uuuuuuuu	
4	PORT Configs	uuuuuuuu	
5	PORT Registers	uuuuuuuu	
6	PORT OEs	uuuuuuuu	
7	Interrupt Enables	uuuuuuuu	
8	Interrupt Reqs	uuuuuuuu	
9	Bulk IN C/S	00000000	unarm
10	Bulk OUT C/S	uuuuuuuu	retain armed/unarmed state
11	Toggle Bits	00000000	
12	USBCS	uuuuuuuu	ReNum bit unchanged
13	FNADDR	00000000	USB Function Address
14	IN07VAL	uuuuuuuu	
15	OUT07VAL	uuuuuuuu	
16	INISOVAL	uuuuuuuu	
17	OUTISOVAL	uuuuuuuu	
18	USBPAIR	uuuuuuuu	
19	Configuration	0	
20	Alternate Setting	0	

A USB bus reset leaves most EZ-USB resources unchanged. From Table 10-2, after USB bus reset:

- The EZ-USB core *unarms* all Bulk IN endpoints (9). Data loaded by the 8051 into an IN endpoint buffer remains there, and the 8051 firmware can either re-send it by loading the endpoint byte count register to re-arm the transfer, or send new data by re-loading the IN buffer before re-arming the endpoint.

- Bulk OUT endpoints retain their *busy* states (10). Data sent by the host to an OUT endpoint buffer remains in the buffer, and the 8051 firmware can either read the data or reject it as *stale* simply by not reading it. In either case, the 8051 loads a dummy value to the endpoint byte count register to re-arm OUT transfers.

- Toggle bits are cleared (11).

- The device address is reset to zero (13).

Note from item 12 that the ReNum bit is unchanged after a USB bus reset. Therefore, if a device has ReNumerated™ and loaded a new personality, it retains the new personality through a USB bus reset.

10.6 EZ-USB Disconnect

Table 10-3. Effects of an EZ-USB Disconnect and Re-connect

Item	Register	Default Value	Comment
1	Endpt Data	uuuuuuuu	u = unchanged
2	Byte Counts	uuuuuuuu	
3	CPUCS	uuuuuuuu	
4	PORT Configs	uuuuuuuu	
5	PORT Registers	uuuuuuuu	
6	PORT OEs	uuuuuuuu	
7	Interrupt Enables	uuuuuuuu	
8	Interrupt Reqs	uuuuuuuu	
9	Bulk IN C/S	00000000	unarm, clear stall bit
10	Bulk OUT C/S	00000000	Arm, clear stall bit
11	Toggle Bits	00000000	reset
12	USBCS	uuuuuuuu	ReNum bit unchanged
13	FNADDR	00000000	USB Function Address
14	IN07VAL	uuuuuuuu	
15	OUT07VAL	uuuuuuuu	
16	INISOVAL	uuuuuuuu	
17	OUTISOVAL	uuuuuuuu	
18	USBPAIR	uuuuuuuu	
19	Configuration	0	
20	Alternate Setting	0	

Although not strictly a “reset,” when the EZ-USB simulates a disconnect-reconnect in order to ReNumerate™, there are effects on the EZ-USB core:

- Bulk IN endpoints are unarmed, and bulk OUT endpoints are armed (9-10).
- Endpoint STALL bits are cleared (9-10).
- Data toggles are reset (11).

- The function address is reset to zero (13).
- The configuration is reset to zero (19).
- Alternate settings are reset to zero (20).

10.7 Reset Summary

Table 10-4. Effects of Various EZ-USB Resets ("U" Means "Unaffected")

Resource	RESET pin	USB Bus Reset	Disconnect	8051 Reset
8051 Reset	reset	U	U	N/A
EP0-7 IN EPs	unarm	unarm	unarm	unarm
EP0-7 OUT EPs	unarm	U	arm	unarm/arm
Breakpoint	reset	U	U	reset
Stall Bits	reset	U	reset	U
Interrupt Enables	reset	U	U	reset
Interrupt Reqs	reset	U	U	U
CLK24	run	U	U	U
Data Toggles	reset	reset	reset	U
Function Address	reset	reset	reset	U
Configuration	0	0	0	U
ReNum	0	U	U	U

Table 10-4 summarizes the effects of the four EZ-USB resets.

Note

The I^2C controller is not reset for any of the conditions laid out in Table 10-4. Only the EZ-USB RESET pin resets it.

11 EZ-USB Power Management

11.1 Introduction

The USB host can suspend a device to put it into a power-down mode. When the USB signals a SUSPEND operation, the EZ-USB chip goes through a sequence of steps to allow the 8051 to first turn off external power-consuming subsystems, and then enter an ultra-low-power mode by turning off its oscillator. Once suspended, the EZ-USB chip is awakened either by resumption of USB bus activity, or by assertion of its WAKEUP# pin. This chapter describes the suspend-resume mechanism.

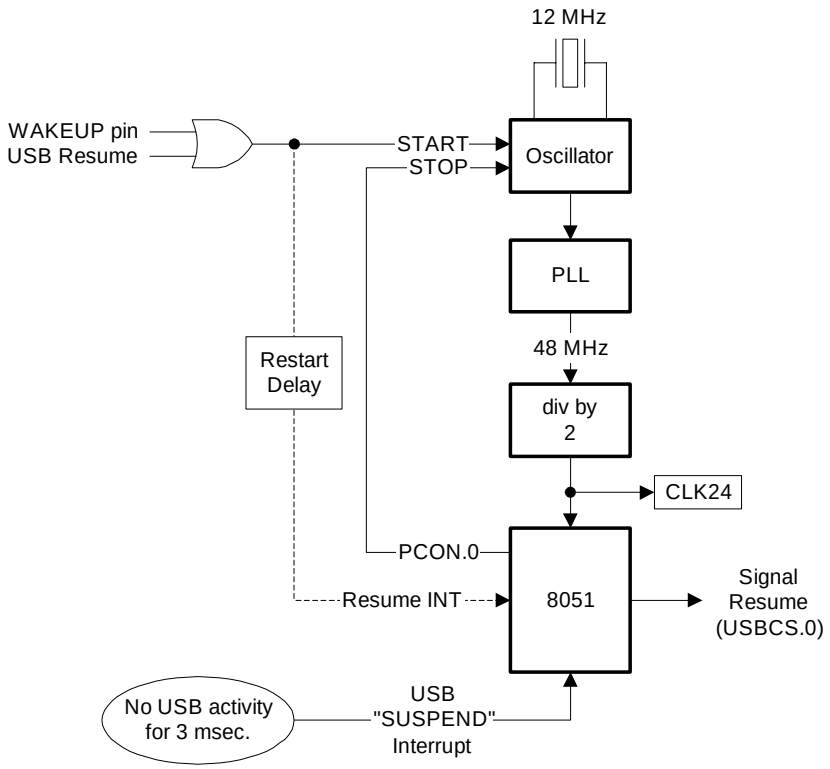


Figure 11-1. Suspend-Resume Control

Figure 11-1 illustrates the EZ-USB logic that implements USB suspend and resume. These operations are explained in the next sections.

11.2 Suspend

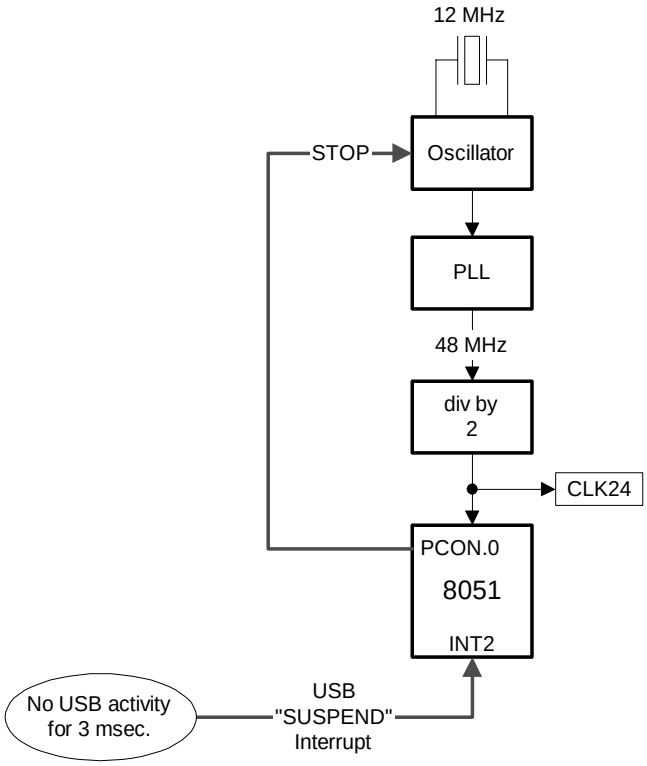


Figure 11-2. EZ-USB Suspend Sequence

A USB device recognizes SUSPEND as 3 ms of a bus idle (“J”) state. The EZ-USB core alerts the 8051 by asserting the USB (INT2) interrupt and the SUSPEND interrupt vector. This gives the 8051 code a chance to perform power SUSPEND interrupt vector. This gives the 8051 code a chance to perform power conservation housekeeping before shutting down the oscillator.

The 8051 code responds to the SUSPEND interrupt by taking the following steps:

1. Performs any necessary housekeeping such as shutting off external power-consuming devices.

2. Sets bit 0 of the PCON SFR (Special Function Register). This has two effects:

   - The 8051 enters its *idle* mode, which is exited by any interrupt.

   - The 8051 sends an internal signal to the EZ-USB core which causes it to turn off the oscillator and PLL.

These actions put the EZ-USB chip into a low-power mode, as required by the USB Specification.

11.3 Resume

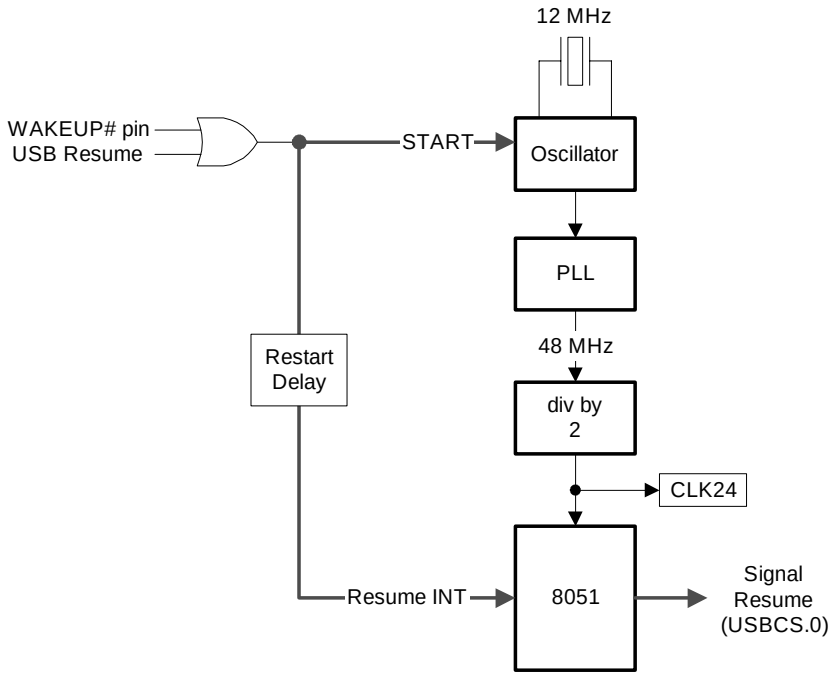


Figure 11-3. EZ-USB Resume Sequence

The EZ-USB oscillator re-starts when:

- USB bus activity resumes (shown as “USB Resume” in Figure 11-3), or
- External logic asserts the EZ-USB WAKEUP# pin low.

After an oscillator stabilization time, the EZ-USB core asserts the 8051 Resume interrupt (Figure 9-1). This causes the 8051 to exit its *idle* mode. The Resume interrupt is the highest priority 8051 interrupt. *It is always enabled, unaffected by the EA bit.*

The resume ISR clears the interrupt request flag, and executes an “reti” (return from interrupt) instruction. This causes the 8051 to continue program execution at the instruction following the one that set PCON.0 to initiate the suspend operation.

About the ‘Resume’ Interrupt

The 8051 enters the idle mode when PCON.0 is set to “1.” Although the 8051 exits its idle state when *any* interrupt occurs, the EZ-USB logic supports only the RESUME interrupt for the USB resume operation. This is because the EZ-USB core asserts this particular interrupt after restarting the 8051 clock.

11.4 Remote Wakeup

USBCS **USB Control and Status** **7FD6**

b7	b6	b5	b4	b3	b2	b1	b0
WAKESRC	-	-	-	**DISCON**	**DISCOE**	**RENUM**	**SIGRSUME**

Figure 11-4. USB Control and Status Register

Two bits in the USBCS register are used for remote wakeup, WAKESRC and SIGRSUME.

After exiting the idle state, the 8051 reads the WAKESRC bit in the USBCS register to discover how the wakeup was initiated. WAKESRC=1 indicates assertion of the WAKEUP# pin, and WAKESRC=0 indicates a resumption of USB bus activity. The 8051 clears the WAKESRC bit by writing a “1” to it.

Note

If your design does not use remote wakeup, tie the WAKEUP# pin high. Holding the WAKEUP# pin low inhibits the EZ-USB chip from suspending.

When a USB device is suspended, the hub driver is tri-stated, and the bus pullup and pull-down resistors cause the bus to assume the "J," or idle state. A suspended device signals a remote wakeup by asserting the "K" state for 10-15 ms. The 8051 controls this using the SIGRSUME bit in the USBCS register.

If the 8051 finds WAKESRC=1 after exiting the idle mode, it drives the "K" state for 10-15 ms to signal the USB remote wakeup. It does this by setting SIGRSUME=1, waiting 10-15 ms, and then setting SIGRSUME=0. When SIGRSUME=0, the EZ-USB bus buffer reverts to normal operation. The resume routine should also write a "1" to the WAKESRC bit to clear it.

J and K States

The USB Specification uses differential data signals D+ and D-. Instead of defining a logical "1" and "0," it defines the "J" and "K" states. For a high speed device, the "J" state means (D+ > D-).

The USB Default device does not support remote wakeup. This fact is reported at enumeration time in byte 7 of the built-in Configuration Descriptor (Table 5-10).

Remote Wakeup: The Big Picture

Additional factors besides the EZ-USB suspend-resume mechanism described in this section determine whether remote wakeup is possible. These are:

1. The device must report that it is capable of signaling a remote wakeup in the "bAttributes" field of its Configuration Descriptor. See Table 5-10 for an example of this descriptor.
2. The host must issue a "Set_Feature/Device" request with the feature selector field set to 0x01 to enable remote wakeup. See Table 7-6 for the detailed request.

12 EZ-USB Registers

12.1 Introduction

This section describes the EZ-USB registers in the order they appear in the EZ-USB memory map. The registers are named according to the following conventions.

Most registers deal with endpoints. The general register format is DDDnFFF, where:

DDD is endpoint direction, IN or OUT with respect to the USB host.

n is the endpoint number, where:

- "07" refers to endpoints 0-7 as a group.
- 0-7 refers to each individual BULK/INTERRUPT/CONTROL endpoint.
- "ISO" indicates isochronous endpoints as a group.

FFF is the function, where:

- CS is a control and status register
- IRQ is an Interrupt Request bit
- IE is an Interrupt Enable bit
- BC, BCL, and BCH are byte count registers. BC is used for single byte counts, and BCL/H are used as the low and high bytes of 16-bit byte counts.
- DATA is a single-register access to a FIFO.
- BUF is the start address of a buffer.

Examples:

- IN7BC is the Endpoint 7 IN byte count.
- OUT07IRQ is the register containing interrupt request bits for OUT endpoints 0-7.
- INISOVAL contains valid bits for the isochronous IN endpoints (EP8IN-EP15IN).

Other Conventions

USB	Indicates a global (not endpoint-specific) USB function.
ADDR	Is an address.
VAL	Means “valid.”
FRAME	Is a frame count.
PTR	Is an address pointer.

Register Name	Register Function	Address

b7	b6	b5	b4	b3	b2	b1	b0
bitname	**bitname**	**bitname**	**bitname**	**bitname**	**bitname**	**bitname**	**bitname**
R, W access	R, W access	R, W access	R, W access	R, W access	R, W access	R, W access	R, W access
Default val	Default val	Default val	Default val	Default val	Default val	Default val	Default val

Figure 12-1. Register Description Format

Figure 12-1 illustrates the register description format used in this chapter.

- The top line shows the register name, functional description, and address in the EZ-USB memory.
- The second line shows the bit position in the register.
- The third line shows the name of each bit in the register.
- The fourth line shows 8051 accessibility: R(ead), W(rite), or R/W.
- The fifth line shows the default value. These values apply after a Power-On-Reset (POR).

12.2 Bulk Data Buffers

INnBUF,OUTnBUF Endpoint 0-7 IN/OUT Data Buffers 1B40-1F3F*

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

* See Table 12-1 for individual endpoint buffer addresses.

Figure 12-2. Bulk Data Buffers

Table 12-1. Bulk Endpoint Buffer Memory Addresses

Address	Address	Name	Size
1F00-1F3F	7F00-7F3F	IN0BUF	64
1EC0-1EFF	7EC0-7EFF	OUT0BUF	64
1E80-1EBF	7E80-7EBF	IN1BUF	64
1E40-1E7F	7E40-7E7F	OUT1BUF	64
1E00-1E3F	7E00-7E3F	IN2BUF	64
1DC0-1DFF	7DC0-7DFF	OUT2BUF	64
1D80-1DBF	7D80-7DBF	IN3BUF	64
1D40-1D7F	7D40-7D7F	OUT3BUF	64
1D00-1D3F	7D00-7D3F	IN4BUF	64
1CC0-1CFF	7CC0-7CFF	OUT4BUF	64
1C80-1CBF	7C80-7CBF	IN5BUF	64
1C40-1C7F	7C40-7C7F	OUT5BUF	64
1C00-1C3F	7C00-7C3F	IN6BUF	64
1BC0-1BFF	7BC0-7BFF	OUT6BUF	64
1B80-1BBF	7B80-7BBF	IN7BUF	64
1B40-1B7F	7B40-7B7F	OUT7BUF	64

Sixteen 64-byte bulk data buffers appear at 0x1B40 **and** 0x7B40 in the 8K version of EZ-USB, and only at 0x7B40 in the 32K version of EZ-USB. The endpoints are ordered to permit the reuse of the buffer space as contiguous RAM when the higher numbered endpoints are not used. These registers default to unknown states.

12.3 Isochronous Data FIFOs

OUTnDATA **EP8OUT-EP15OUT FIFO Registers** **7F60-7F67***

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

INnDATA **EP8IN-EP15IN FIFO Registers** **7F68-7F6F***

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
W	W	W	W	W	W	W	W
x	x	x	x	x	x	x	x

* See Table 12-2 for individual endpoint buffer addresses.

Figure 12-3. Isochronous Data FIFOs

Table 12-2. Isochronous Endpoint FIFO Register Addresses

Address	Isochronous Data	Name
7F60	Endpoint 8 OUT Data	OUT8DATA
7F61	Endpoint 9 OUT Data	OUT9DATA
7F62	Endpoint 10 OUT Data	OUT10DATA
7F63	Endpoint 11 OUT Data	OUT11DATA
7F64	Endpoint 12 OUT Data	OUT12DATA
7F65	Endpoint 13 OUT Data	OUT13DATA
7F66	Endpoint 14 OUT Data	OUT14DATA
7F67	Endpoint 15 OUT Data	OUT15DATA
7F68	Endpoint 8 IN Data	IN8DATA
7F69	Endpoint 9 IN Data	IN9DATA
7F6A	Endpoint 10 IN Data	IN10DATA
7F6B	Endpoint 11 IN Data	IN11DATA
7F6C	Endpoint 12 IN Data	IN12DATA
7F6D	Endpoint 13 IN Data	IN13DATA
7F6E	Endpoint 14 IN Data	IN14DATA
7F6F	Endpoint 15 IN Data	IN15DATA

Sixteen addressable data registers hold data from the eight isochronous IN endpoints and the eight isochronous OUT endpoints. Reading a Data Register reads a Receive FIFO byte (USB OUT data); writing a Data Register loads a Transmit FIFO byte (USB IN data).

12.4 Isochronous Byte Counts

OUTnBCH **OUT(8-15) Byte Count High** **7F70-7F7F***

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**BC9**	**BC8**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

INnBCL **OUT(8-15) Byte Count Low** **7F70-7F7F***

b7	b6	b5	b4	b3	b2	b1	b0
BC7	**BC6**	**BC5**	**BC4**	**BC3**	**BC2**	**BC1**	**BC0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

* See Table 12-3 for individual endpoint buffer addresses.

Figure 12-4. Isochronous Byte Counts

Table 12-3. Isochronous Endpoint Byte Count Register Addresses

Address	Isochronous Data	Name
7F70	Endpoint 8 Byte Count High	OUT8BCH
7F71	Endpoint 8 Byte Count Low	OUT8BCL
7F72	Endpoint 9 Byte Count High	OUT9BCH
7F73	Endpoint 9 Byte Count Low	OUT9BCL
7F74	Endpoint 10 Byte Count High	OUT10BCH
7F75	Endpoint 10 Byte Count Low	OUT10BCL
7F76	Endpoint 11 Byte Count High	OUT11BCH
7F77	Endpoint 11 Byte Count Low	OUT11BCL
7F78	Endpoint 12 Byte Count High	OUT12BCH
7F79	Endpoint 12 Byte Count Low	OUT12BCL
7F7A	Endpoint 13 Byte Count High	OUT13BCH
7F7B	Endpoint 13 Byte Count Low	OUT13BCL
7F7C	Endpoint 14 Byte Count High	OUT14BCH
7F7D	Endpoint 14 Byte Count Low	OUT14BCL
7F7E	Endpoint 15 Byte Count High	OUT15BCH
7F7F	Endpoint 15 Byte Count Low	OUT15BCL

The EZ-USB core uses the byte count registers to report isochronous data payload sizes for OUT data transferred from the host to the USB core. Ten bits of byte count data allow payload sizes up to 1,023 bytes. A byte count of zero is valid, meaning that the host sent no isochronous data during the previous frame. The default values of these registers are unknown.

Byte counts are valid only for OUT endpoints. The byte counts indicate the number of bytes remaining in the endpoint's Receive FIFO. Every time the 8051 reads a byte from the ISODATA register, the byte count decrements by one.

To read USB OUT data, the 8051 first reads byte count registers OUTnBCL and OUTnBCH to determine how many bytes to transfer out of the OUT FIFO. (The 8051 can also quickly test ISO output endpoints for zero byte counts using the ZBCOUT register.) Then, the CPU reads that number of bytes from the ISODATA register. Separate byte counts are maintained for each endpoint, so the CPU can read the FIFOs in a discontinuous manner. For example, if EP8 indicates a byte count of 100, and EP9 indicates a byte count of 50, the CPU could read 50 bytes from EP8, then read 10 bytes from EP9, and resume reading EP8. At this moment the byte count for EP8 would read 50.

There are no byte count registers for the IN endpoints. The USB core automatically tracks the number of bytes loaded by the 8051.

If the 8051 does not load an IN isochronous endpoint FIFO during a 1-ms frame, and the host requests data from that endpoint during the next frame (IN token), the USB Core responds according to the setting of the ISOSEND0 bit (USBPAIR.7). If ISOSEND0=1, the core returns a zero-length data packet in response to the host IN token. If ISOSEND=0, the core does not respond to the IN token.

It is the responsibility of the 8051 programmer to ensure that the number of bytes written to the IN FIFO does not exceed the maximum packet size as reported during enumeration.

12.5 CPU Registers

CPUCS **CPU Control and Status** **7F92**

b7	b6	b5	b4	b3	b2	b1	b0
RV3	**RV2**	**RV1**	**RV0**	**0**	**0**	**CLK24OE**	**8051RES**
R	R	R	R	R	R	R/W	R
RV3	RV2	RV1	RV0	0	0	1	1

Figure 12-5. CPU Control and Status Register

This register enables the CLK24 output and permits the host to reset the 8051 using a Firmware Download.

Bit 7-4: **RV[3..0]** *Silicon Revision*

These register bits define the silicon revision. Consult individual Cypress Semiconductor data sheets for values.

Bit 1: **CLK24OE** *Output enable - CLK24 pin*

When this bit is set to 1, the internal 24-MHz clock is connected to the EZ-USB CLK24 pin. When this bit is 0, the CLK24 pin drives HI. This bit can be written by the 8051 only.

Bit 0: **8051RES** *8051 reset*

The USB host writes “1” to this bit to reset the 8051, and “0” to run the 8051. Only the USB host can write this bit.

12.6 Port Configuration

PORTACFG **IO Port A Configuration** **7F93**

b7	b6	b5	b4	b3	b2	b1	b0
RxD1OUT	**RxD0OUT**	**FRD**	**FWR**	**CS**	**OE**	**T1OUT**	**T0OUT**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

PORTBCFG **IO Port B Configuration** **7F94**

b7	b6	b5	b4	b3	b2	b1	b0
T2OUT	**INT6**	**INT5**	**INT4**	**TXD1**	**RXD1**	**T2EX**	**T2**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

PORTCCFG **IO Port C Configuration** **7F95**

b7	b6	b5	b4	b3	b2	b1	b0
RD	**WR**	**T1**	**T0**	**INT1**	**INT0**	**TXD0**	**RXD0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 12-6. IO Port Configuration Registers

These three registers control the three IO ports on the EZ-USB chip. They select between IO ports and various alternate functions. They are read/write by the 8051.

When PORTnCFG=0, the port pin functions as IO, using the OUT, PINS, and OE control bits. Data written to an OUTn registers appears on an IO Port pin if the corresponding output enable bit (OEn) is HI.

When PORTnCFG=1, the pin assumes the alternate function shown in Table 12-4 on the following page.

Table 12-4. IO Pin Alternate Functions

I/O	Name	Alternate Functions
PA0	T0OUT	Timer 0 Output
PA1	T1OUT	Timer 1 Output
PA2	OE#	External Memory Output Enable
PA3	CS#	External Memory Chip Select
PA4	FWR#	Fast Access Write Strobe
PA5	FRD#	Fast Access Read Strobe
PA6	RXD0OUT	Mode 0: UART0 Synchronous Data Output
PA7	RXD1OUT	Mode 0: UART1 Synchronous Data Output
PB0	T2	Timer/Counter 2 Clock Input
PB1	T2EX	Timer/Counter 2 Capture/Reload Input
PB2	RxD1	Serial Port 1 Input
PB3	TxD1	Mode 0: Clock Output Modes 1-3: Serial Port 1 Data Output
PB4	INT4	INT4 Interrupt Request
PB5	INT5#	INT5 Interrupt Request
PB6	INT6	INT6 Interrupt Request
PB7	T2OUT	Timer/Counter 2 Overflow Indication
PC0	RxD0	Serial Port 0 Input
PC1	TxD0	Mode 0: Clock Output Modes 1-3: Serial Port 0 Data Output
PC2	INT0#	INT0 Interrupt Request
PC3	INT1#	INT1 Interrupt Request
PC4	T0	Timer/Counter 0 External Input
PC5	T1	Timer/Counter 1 External Input
PC6	WR#	External Memory Write Strobe
PC7	RD#	External Memory Read Strobe

12.7 Input-Output Port Registers

OUTA **Port A Outputs** **7F96**

b7	b6	b5	b4	b3	b2	b1	b0
OUTA7	**OUTA6**	**OUTA5**	**OUTA4**	**OUTA3**	**OUTA2**	**OUTA1**	**OUTA0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OUTB **Port B Outputs** **7F97**

b7	b6	b5	b4	b3	b2	b1	b0
OUTB7	**OUTB6**	**OUTB5**	**OUTB4**	**OUTB3**	**OUTB2**	**OUTB1**	**OUTB0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OUTC **Port C Outputs** **7F98**

b7	b6	b5	b4	b3	b2	b1	b0
OUTC7	**OUTC6**	**OUTC5**	**OUTC4**	**OUTC3**	**OUTC2**	**OUTC1**	**OUTC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 12-7. Output Port Configuration Registers

The OUTn registers provide the data that drives the port pin when OE=1 **and** the PORTnCFG pin is 0. If the port pin is selected a an input (OE=0), the value stored in the corresponding OUTn bit is stored in an output latch but not used.

PINSA **Port A Pins** **7F99**

b7	b6	b5	b4	b3	b2	b1	b0
PINA7	**PINA6**	**PINA5**	**PINA4**	**PINA3**	**PINA2**	**PINA1**	**PINA0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

PINSB **Port B Pins** **7F9A**

b7	b6	b5	b4	b3	b2	b1	b0
PINB7	**PINB6**	**PINB5**	**PINB4**	**PINB3**	**PINB2**	**PINB1**	**PINB0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

OUTC **Port C Pins** **7F98**

b7	b6	b5	b4	b3	b2	b1	b0
PINC7	**PINC6**	**PINC5**	**PINC4**	**PINC3**	**PINC2**	**PINC1**	**PINC0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 12-8. PINSn Registers

The PINSn registers contain the current value of the port pins, whether they are selected as IO ports or alternate functions.

OEA **Port A Output Enable** **7F9C**

b7	b6	b5	b4	b3	b2	b1	b0
OEA7	**OEA6**	**OEA5**	**OEA4**	**OEA3**	**OEA2**	**OEA1**	**OEA0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

OEB **Port B Output Enable** **7F9D**

b7	b6	b5	b4	b3	b2	b1	b0
OEB7	**OEB6**	**OEB5**	**OEB4**	**OEB3**	**OEB2**	**OEB1**	**OEB0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

OEC **Port C Output Enable** **7F9E**

b7	b6	b5	b4	b3	b2	b1	b0
OEC7	**OEC6**	**OEC5**	**OEC4**	**OEC3**	**OEC2**	**OEC1**	**OEC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-9. Output Enable Registers

The OE registers control the output enables on the tri-state drivers connected to the port pins. When these bits are "1," the port is an output, unless the corresponding PORTnCFG bit is set to a "1."

12.8 230-Kbaud UART Operation - AN2122, AN2126

UART230 **230-Kbaud UART Control** **7F9F**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	**UART1**	**UART0**
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0

Figure 12-10. 230-Kbaud UART Operation Register

Bit 1: **UART1** *Universal 115/230 Kbaud operation for UART1*

Bit 0: **UART0** *Universal 115/230 Kbaud operation for UART0*

These bits, when set to "1," connect an internal 3.69-MHz clock to UART0 and/or UART1. The UARTs divide this frequency by 16, giving a 230-KHz baud clock if the corresponding SMOD bit is set, or 115 baud clock if the corresponding SMOD bit is clear. (NOTE: SMOD0 is bit 7 or SFR 0x87, SMOD1 is bit 7 or SFR 0xD8). When the UART0 or UART1 bit is clear, the normal UART clock sources are used.

12.9 Isochronous Control/Status Registers

ISOERR **Isochronous OUT EP Error** **7FA0**

b7	b6	b5	b4	b3	b2	b1	b0
ISO15ERR	**ISO14ERR**	**ISO13ERR**	**ISO12ERR**	**ISO11ERR**	**ISO10ERR**	**ISO9ERR**	**ISO8ERR**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 12-11. Isochronous OUT Endpoint Error Register

The ISOERR bits are updated at every SOF. They indicate that a CRC error was received on a data packet for the current frame. The ISOERR bit status refers to the USB data received in the previous frame, and which is currently in the endpoint's OUT FIFO. If the ISOERR bit = 1, indicating a bad CRC check, the data is still available in the OUTnDATA register.

ISOCTL **Isochronous Control** **7FA1**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	**PPSTAT**	**MBZ**	**MBZ**	**ISODISAB**
R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 12-12. Isochronous Control Register

Bit 3: **PPSTAT** *Ping-Pong Status*

This bit indicates the isochronous buffer currently in use by the EZ-USB core. It is used only for diagnostic purposes.

Bits 2,1: **MBZ** *Must be zero*

These bits must always be written with zeros.

Bit 0: **ISODISAB** *ISO Endpoints Disable*

ISODISAB=0 enables all 16 isochronous endpoints

ISODISAB=1 disables *all 16* isochronous endpoints, making the 2,048 bytes of isochronous FIFO memory available as 8051 data memory at 0x2000-0x27FF.

ZBCOUT **Zero Byte Count Bits** **7FA2**

b7	b6	b5	b4	b3	b2	b1	b0
EP15	**EP14**	**EP13**	**EP12**	**EP11**	**EP10**	**EP9**	**EP8**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 12-13. Zero Byte Count Register

Bits 0-7: **EP(n)** *Zero Byte Count for ISO OUT Endpoints*

The 8051 can check these bits as a fast way to check all of the OUT isochronous endpoints at once for no data received during the previous frame. A “1” in any bit position means that a zero byte Isochronous OUT packet was received for the indicated endpoint.

12.10 I²C Registers

I2CS **I²C Control and Status** **7FA5**

b7	b6	b5	b4	b3	b2	b1	b0
START	**STOP**	**LASTRD**	**ID1**	**ID0**	**BERR**	**ACK**	**DONE**
R/W	R/W	R/W	R	R	R	R	R
0	0	0	x	x	0	0	0

I2DAT **I²C Data** **7FA6**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-14. I²C Transfer Registers

The 8051 uses these registers to transfer data over the EZ-USB I²C bus.

Bit 7: **START** *Signal START condition*

The 8051 sets the START bit to "1" to prepare an I²C bus transfer. If START=1, the next 8051 load to I2DAT will generate the start condition followed by the serialized byte of data in I2DAT. The 8051 loads byte data into I2DAT after setting the START bit. The I²C controller clears the START bit during the ACK interval.

Bit 6: **STOP** *Signal STOP condition*

The 8051 sets STOP=1 to terminate an I²C bus transfer. The I²C controller clears the STOP bit after completing the STOP condition. If the 8051 sets the STOP bit during a byte transfer, the STOP condition will be generated immediately following the ACK phase of the byte transfer. If no byte transfer is occurring when the STOP bit is set, the STOP condition will be carried out immediately on the bus. Data should not be written to I2CS or I2DAT until the STOP bit returns low.

Bit 5: **LASTRD** *Last Data Read*

To read data over the I^2C bus, an I^2C master floats the SDA line and issues clock pulses on the SCL line. After every eight bits, the master drives SDA low for one clock to indicate ACK. To signal the last byte of the read transfer, the master floats SDA at ACK time to instruct the slave to stop sending. This is controlled by the 8051 by setting LastRD=1 before reading the last byte of a read transfer. The I^2C controller clears the LastRD bit at the end of the transfer (at ACK time).

Note

Setting LastRD does not automatically generate a STOP condition. The 8051 should also set the STOP bit at the end of a read transfer.

Bit 4-3: **ID1,ID0** *Boot EEPROM ID*

These bits are set by the boot loader to indicate whether an 8-bit address or 16-bit address EEPROM at slave address 000 or 001 was detected at power-on. Normally, they are used for debug purposes only.

Bit 2: **BERR** *Bus Error*

This bit indicates an I^2C bus error. BERR=1 indicates that there was bus contention, which results when an outside device drives the bus LO when it shouldn't, or when another bus master wins arbitration, taking control of the bus. BERR is cleared when 8051 reads or writes the IDATA register.

Bit 1: **ACK** *Acknowledge bit*

Every ninth SCL or a write transfer the slave indicates reception of the byte by asserting ACK. The EZ-USB controller floats SDA during this time, samples the SDA line, and updates the ACK bit with the complement of the detected value. ACK=1 indicates acknowledge, and ACK=0 indicates not-acknowledge. The EZ-USB core updates the ACK bit at the same time it sets DONE=1. The ACK bit should be ignored for read transfers on the bus.

Bit 0: **DONE** *I²C Transfer DONE*

The I²C controller sets this bit whenever it completes a byte transfer, right after the ACK stage. The controller also generates an I²C interrupt request (8051 INT3) when it sets the DONE bit. The I²C controller automatically clears the DONE bit and the I²C interrupt request bit whenever the 8051 reads or writes the I2DAT register.

I2CMODE **I²C Mode** **7FA7**

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**0**	**STOPIE**	**0**
R	R	R	R	R	R	R/W	R
0	0	0	0	0	0	0	0

Figure 12-15. I²C Mode Register

The I²C interrupt includes one additional interrupt source in the AN2122/AN2126, a 1-0 transition of the STOP bit. To enable this interrupt, set the STOPIE bit in the I2CMODE register. The 8051 determines the interrupt source by checking the DONE and STOP bits in the I2CS register.

IVEC **Interrupt Vector** **7FA8**

b7	b6	b5	b4	b3	b2	b1	b0
0	**IV4**	**IV3**	**IV2**	**IV1**	**IV0**	**0**	**0**
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 12-16. Interrupt Vector Register

IVEC indicates the source of an interrupt from the USB Core. When the USB core generates an INT2 (USB) interrupt request, it updates IVEC to indicate the source of the interrupt. The interrupt sources are encoded on IV[4..0] as shown in Figure 9-2.

IN07IRQ **Endpoint 0-7 IN Interrupt Request** **7FA9**

b7	b6	b5	b4	b3	b2	b1	b0
IN7IR	**IN6IR**	**IN5IR**	**IN4IR**	**IN3IR**	**IN2IR**	**IN1IR**	**IN0IR**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OUT07IRQ **Endpoint 0-7 OUT Interrupt Requests** **7FAA**

b7	b6	b5	b4	b3	b2	b1	b0
OUT7IR	**OUT6IR**	**OUT5IR**	**OUT4IR**	**OUT3IR**	**OUT2IR**	**OUT1IR**	**OUT0IR**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-17. IN/OUT Interrupt Request (IRQ) Registers

These interrupt request (IRQ) registers indicate the pending interrupts for each bulk endpoint. An interrupt request (IR) bit becomes active when the BSY bit for an endpoint makes a transition from one to zero (the endpoint becomes *un-busy*, giving access to the 8051). The IR bits function independently of the Interrupt Enable (IE) bits, so interrupt requests are held whether or not the interrupts are enabled.

The 8051 clears an interrupt request bit by writing a "1" to it (see the following Note).

Note

Do **not** clear an IRQ bit by reading an IRQ register, ORing its contents with a bit mask, and writing back the IRQ register. This will clear ALL pending interrupts. Instead, simply write the bit mask value (with the IRQ you want to clear) directly to the IRQ register.

USBIRQ **USB Interrupt Request** **7FAB**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	**IBNIR***	**URESIR**	**SUSPIR**	**SUTOKIR**	**SOFIR**	**SUDAVIR**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

* AN2122/AN2126 only.

Figure 12-18. USB Interrupt Request (IRQ) Registers

USBIRQ indicates the interrupt request status of the USB reset, suspend, setup token, start of frame, and setup data available interrupts.

Bit 5: IBNIR *IN Bulk NAK Interrupt Request*

This bit is in the AN2122 and AN2126 versions only. The EZ-USB core sets this bit when any of the IN bulk endpoints responds to an IN token with a NAK. This interrupt occurs when the host sends an IN token to a bulk IN endpoint which has not been *armed* by the 8051 writing its byte count register. Individual enables and requests (per endpoint) are controlled by the IBNIRQ and IBNIEN registers (7FB0, 7FB1).

Bit 4: URESIR *USB Reset Interrupt Request*

The EZ-USB core sets this bit to “1” when it detects a USB bus reset.

Because this bit can change state while the 8051 is in reset, it may be active when the 8051 comes out of reset, although it is reset to “0” by a power-on reset. Write a “1” to this bit to clear the interrupt request. See Chapter 10, "EZ-USB Resets" for more information about this bit.

Bit 3: SUSPIR *USB Suspend Interrupt Request*

The EZ-USB core sets this bit to “1” when it detects USB SUSPEND signaling (no bus activity for 3 ms). Write a “1” to this bit to clear the interrupt request.

Because this bit can change state while the 8051 is in reset, it may be active when the 8051 comes out of reset, although it is reset to “0” by a power-on reset. See Chapter 11, "EZ-USB Power Management" for more information about this bit.

Bit 2: **SUTOKIR** *SETUP Token Interrupt Request*

The EZ-USB core sets this bit to “1” when it receives a SETUP token. Write a “1” to this bit to clear the interrupt request. See Chapter 7, "EZ-USB Endpoint Zero" for more information on the handling of SETUP tokens.

Because this bit can change state while the 8051 is in reset, it may be active when the 8051 comes out of reset, although it is reset to “0” by a power-on reset.

Bit 1: **SOFIR** *Start of frame Interrupt Request*

The EZ-USB core sets this bit to “1” when it receives a SOF packet. Write a “1” to this bit to clear the interrupt condition.

Because this bit can change state while the 8051 is in reset, it may be active when the 8051 comes out of reset, although it is reset to “0” by a power-on reset.

Bit 0: **SUDAVIR** *SETUP data available Interrupt Request*

The EZ-USB core sets this bit to “1” when it has transferred the eight data bytes from an endpoint zero SETUP packet into internal registers (at SETUPDAT). Write a “1” to this bit to clear the interrupt condition.

Because this bit can change state while the 8051 is in reset, it may be active when the 8051 comes out of reset, although it is reset to “0” by a power-on reset.

IN07EN **Endpoint 0-7 IN Interrupt Enables** **7FAC**

b7	b6	b5	b4	b3	b2	b1	b0
IN7IEN	**IN6IEN**	**IN5IEN**	**IN4IEN**	**IN3IEN**	**IN2IEN**	**IN1IEN**	**IN0IEN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OUT07IEN **Endpoint 0-7 OUT Interrupt Enables** **7FAD**

b7	b6	b5	b4	b3	b2	b1	b0
OUT7IEN	**OUT6IEN**	**OUT5IEN**	**OUT4IEN**	**OUT3IEN**	**OUT2IEN**	**OUT1IEN**	**OUT0IEN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-19. IN/OUT Interrupt Enable Registers

The Endpoint Interrupt Enable registers define which endpoints have active interrupts. They do not affect the endpoint action, only the generation of an interrupt in response to endpoint events.

When the IEN bit for an endpoint is "0," the interrupt request bit for that endpoint is ignored, but saved. When the IEN bit for an endpoint is "1," any IRQ bit equal to "1" generates an 8051 INT2 request.

Note

The INT2 interrupt (EIE.0) and the 8051 global interrupt enable (EA) must be enabled for the endpoint interrupts to propagate to the 8051. Once the INT2 interrupt is active, it must be cleared by software.

USBIEN **USB Interrupt Enable** **7FAE**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	**IBNIE***	**URESIE**	**SUSPIE**	**SUTOKIE**	**SOFIE**	**SUDAVIE**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

* AN2122/AN2126 only.

Figure 12-20. USB Interrupt Enable Register

USBIEN bits gate the interrupt request to the 8051 for USB reset, suspend, SETUP token, start of frame, and SETUP data available.

Bit 5: **IBNIE** *IN bulk NAK Interrupt Enable*

This bit is in the AN2122 and AN2126 versions only. The 8051 sets this bit to enable the IN-bulk-NAK interrupt. This interrupt occurs when the host sends an IN token to a bulk IN endpoint which has not been *armed* by the 8051 writing its byte count register. Individual enables and requests (per endpoint) are controlled by the IBNIRQ and IBNIEN registers (7FB0, 7FB1).

Bit 4: **URESIE** *USB Reset Interrupt Enable*

This bit is the interrupt mask for the URESIR bit. When this bit is “1,” the interrupt is enabled, when it is “0,” the interrupt is disabled.

Bit 3: **SUSPIE** *USB Suspend Interrupt Enable*

This bit is the interrupt mask for the SUSPIR bit. When this bit is “1,” the interrupt is enabled, when it is “0,” the interrupt is disabled.

Bit 2: **SUTOKIE** *SETUP Token Interrupt Enable*

This bit is the interrupt mask for the SUTOKIR bit. When this bit is “1,” the interrupt is enabled, when it is “0,” the interrupt is disabled.

Bit 1: **SOFIE** *Start of frame Interrupt Enable*

This bit is the interrupt mask for the SOFIE bit. When this bit is "1," the interrupt is enabled, when it is "0," the interrupt is disabled.

Bit 0: **SUDAVIE** *SETUP data available Interrupt Enable*

This bit is the interrupt mask for the SUDAVIE bit. When this bit is "1," the interrupt is enabled, when it is "0," the interrupt is disabled.

USBBAV **Breakpoint and Autovector** **7FAF**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	**BREAK**	**BPPULSE**	**BPEN**	**AVEN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 12-21. Breakpoint and Autovector Register

Bit 3: **BREAK** *Breakpoint enable*

The BREAK bit is set when the 8051 address bus matches the address held in the bit breakpoint address registers (next page). The BKPT pin reflects the state of this bit. The 8051 writes a "1" to the BREAK bit to clear it. It is not necessary to clear the BREAK bit if the pulse mode bit (BPPULSE) is set.

Bit 2: **BPPULSE** *Breakpoint pulse mode*

The 8051 sets this bit to "1" to pulse the BREAK bit (and BKPT pin) high for 8 CLK24 cycles when the 8051 address bus matches the address held in the breakpoint address registers. when this bit is set to "0," the BREAK bit (and BKPT pin) remains high until it is cleared by the 8051.

Bit 1: **BPEN** *Breakpoint enable*

If this bit is "1," a BREAK signal is generated whenever the 16-bit address lines match the value in the Breakpoint Address Registers (BPADDRH/L). The behavior of the BREAK bit and associated BKPT pin signal is either latched or pulsed, depending on the state of the BPPULSE bit.

Bit 0: **AVEN** *Auto-vector enable*

If this bit is "1," the EZ-USB Auto-vector feature is enabled. If it is 0, the auto-vector feature is disabled. See Chapter 9, "EZ-USB Interrupts" for more information on the auto-vector feature.

IBNIRQ IN Bulk NAK Interrupt Requests 7FB0

b7	b6	b5	b4	b3	b2	b1	b0
-	**EP6IN**	**EP5IN**	**EP4IN**	**EP3IN**	**EP2IN**	**EP1IN**	**EP0IN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

* AN2122/AN2126 only.

Figure 12-22. IN Bulk NAK Interrupt Request Register

These bits are set when a bulk IN endpoint (0-6) received an IN token while the endpoint was not *armed* for data transfer. In this case the SIE automatically sends a NAK response, and sets the corresponding IBNIRQ bit. If the IBN interrupt is enabled (USBIEN.5=1), and the endpoint interrupt is enabled in the IBNIEN register, an interrupt is request generated. The 8051 can test the IBNIRQ register to determine which of the endpoints caused the interrupt. The 8051 clears an IBNIRQ bit by writing a "1" to it.

IBNIEN IN Bulk NAK Interrupt Enables 7FB1

b7	b6	b5	b4	b3	b2	b1	b0
-	**EP6IN**	**EP5IN**	**EP4IN**	**EP3IN**	**EP2IN**	**EP1IN**	**EP0IN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	0	0	0	0	0	0

Figure 12-23. IN Bulk NAK Interrupt Enable Register

Each of the individual IN endpoints may be enabled for an IBN interrupt using the IBNEN register. The 8051 sets an interrupt enable bit to 1 to enable the corresponding interrupt.

BPADDRH **Breakpoint Address High** **7FB2**

b7	b6	b5	b4	b3	b2	b1	b0
A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BPADDRL **Breakpoint Address Low** **7FB3**

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-24. IN/OUT Interrupt Enable Registers

When the current 16-bit address (code or xdata) matches the BPADDRH/BPADDRL address, a breakpoint event occurs. The BPPULSE and BPEN bits in the USBBAV register control the action taken on a breakpoint event.

If the BPEN bit is “0,” address breakpoints are ignored. If BPEN is “1” and BPPULSE is “1,” an 8 CLK24 wide pulse appears on the BKPT pin. If BPEN is “1” and BPPULSE is “0,” the BKPT pin remains active until the 8051 clears the BREAK bit by writing “1” to it.

12.12 Endpoint 0 Control and Status Registers

EP0CS **Endpoint Zero Control and Status** **7FB4**

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	**OUTBSY**	**INBSY**	**HSNAK**	**EP0STALL**
R	R	R	R	R	R	R/W	R/W
0	0	0	0	1	0	0	0

IN0BC **Endpoint Zero IN Byte Count** **7FB5**

b7	b6	b5	b4	b3	b2	b1	b0
-	**BC6**	**BC5**	**BC4**	**BC3**	**BC2**	**BC1**	**BC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

OUT0BC **Endpoint Zero OUT Byte Count** **7FC5**

b7	b6	b5	b4	b3	b2	b1	b0
-	**BC6**	**BC5**	**BC4**	**BC3**	**BC2**	**BC1**	**BC0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Figure 12-25. Port Configuration Registers

These registers control EZ-USB CONTROL endpoint zero. Because endpoint zero is a bi-directional endpoint, the IN and OUT functionality is controlled by a single control and status (CS) register, unlike endpoints 1-7, which have separate INCS and OUTCS registers.

Bit 3: **OUTBSY** *OUT Endpoint Busy*

OUTBSY is a read-only bit that is automatically cleared when a SETUP token arrives. The 8051 sets the OUTBSY bit by writing a byte count to EPOUTBC.

If the CONTROL transfer uses an OUT data phase, the 8051 must load a dummy byte count into OUT0BC to arm the OUT endpoint buffer. Until it does, the EZ-USB core will NAK the OUT tokens.

Bit 2: INBSY *IN Endpoint Busy*

INBSY is a read-only bit that is automatically cleared when a SETUP token arrives. The 8051 sets the INBSY bit by writing a byte count to IN0BC.

If the CONTROL transfer uses an IN data phase, the 8051 loads the requested data into the IN0BUF buffer, and then loads the byte count into IN0BC to arm the data phase of the CONTROL transfer. Alternatively, the 8051 can arm the data transfer by loading an address into the Setup Data Pointer registers SUDPTRH/L. Until armed, the EZ-USB core will NAK the IN tokens.

Bit 1: HSNAK *Handshake NAK*

HSNAK (Handshake NAK) is a read/write bit that is automatically set when a SETUP token arrives. The 8051 clears HSNAK by writing a "1" to the register bit.

While HSNAK=1, the EZ-USB core NAKs the handshake (status) phase of the CONTROL transfer. When HSNAK=0, it ACKs the handshake phase. The 8051 can clear HSNAK at any time during a CONTROL transfer.

Bit 0: EP0STALL *Endpoint Zero Stall*

EP0STALL is a read/write bit that is automatically cleared when a SETUP token arrives. The 8051 sets EP0STALL by writing a "1" to the register bit.

While EP0STALL=1, the EZ-USB core sends the STALL PID for any IN or OUT token. This can occur in either the data or handshake phase of the CONTROL transfer.

Note

To indicate an endpoint stall on endpoint zero, set both EP0STALL and HSNAK bits. Setting the EP0STALL bit alone causes endpoint zero to NAK forever because the host keeps the control transfer pending.

12.13 Endpoint 1-7 Control and Status Registers

Endpoints 1-7 IN and OUT are used for bulk or interrupt data. Table 12-5 shows the addresses for the control/status and byte count registers associated with these endpoints. The bi-directional CONTROL endpoint zero registers are described in Section 12.12, "Endpoint 0 Control and Status Registers."

Table 12-5. Control and Status Register Addresses for Endpoints 0-7

Address	Function	Name
7FB4	Control and Status - Endpoint IN0	EP0CS
7FB5	Byte Count - Endpoint IN0	IN0BC
7FB6	Control and Status - Endpoint IN1	IN1CS
7FB7	Byte Count - Endpoint IN1	IN1BC
7FB8	Control and Status - Endpoint IN2	IN2CS
7FB9	Byte Count - Endpoint IN2	IN2BC
7FBA	Control and Status - Endpoint IN3	IN3CS
7FBB	Byte Count - Endpoint IN3	IN3BC
7FBC	Control and Status - Endpoint IN4	IN4CS
7FBD	Byte Count - Endpoint IN4	IN4BC
7FBE	Control and Status - Endpoint IN5	IN5CS
7FBF	Byte Count - Endpoint IN5	IN5BC
7FC0	Control and Status - Endpoint IN6	IN6CS
7FC1	Byte Count - Endpoint IN6	IN6BC
7FC2	Control and Status - Endpoint IN7	IN7CS
7FC3	Byte Count - Endpoint IN7	IN7BC
7FC4	*Reserved*	
7FC5	Byte Count - Endpoint OUT0	OUT0BC
7FC6	Control and Status - Endpoint OUT1	OUT1CS
7FC7	Byte Count - Endpoint OUT1	OUT1BC
7FC8	Control and Status - Endpoint OUT2	OUT2CS
7FC9	Byte Count - Endpoint OUT2	OUT2BC
7FCA	Control and Status - Endpoint OUT3	OU37CS
7FCB	Byte Count - Endpoint OUT3	OUT3BC
7FCC	Control and Status - Endpoint OUT4	OUT4CS
7FCD	Byte Count - Endpoint OUT4	OUT4BC
7FCE	Control and Status - Endpoint OUT5	OUT5CS
7FCF	Byte Count - Endpoint OUT5	OUT5BC
7FD0	Control and Status - Endpoint OUT6	OUT6CS
7FD1	Byte Count - Endpoint OUT6	OUT6BC
7FD2	Control and Status - Endpoint OUT7	OUT7CS
7FD3	Byte Count - Endpoint OUT7	OUT7BC

INnCS **Endpoint (1-7) IN Control and Status** **7FB6-7FC2***

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	**INnBSY**	**INnSTL**
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0

* See Table 12-5 for individual control/status register addresses.

Figure 12-26. IN Control and Status Registers

Bit 1: INnBSY *IN Endpoint (1-7) Busy*

The BSY bit indicates the status of the endpoint's IN Buffer INnBUF. The EZ-USB core sets BSY=0 when the endpoint's IN buffer is empty and ready for loading by the 8051. The 8051 sets BSY=1 by loading the endpoint's byte count register.

When BSY=1, the 8051 should not write data to an IN endpoint buffer, because the endpoint FIFO could be in the act of transferring data to the host over the USB. BSY=0 when the USB IN transfer is complete and endpoint RAM data is available for 8051 access. USB IN tokens for the endpoint are NAKd while BSY=0 (the 8051 is still loading data into the endpoint buffer).

A 1-to-0 transition of BSY (indicating that the 8051 can access the buffer) generates an interrupt request for the IN endpoint. After the 8051 writes the data to be transferred to the IN endpoint buffer, it loads the endpoint's byte count register with the number of bytes to transfer, which automatically sets BSY=1. This enables the IN transfer of data to the host in response to the next IN token. Again, the CPU should never load endpoint data while BSY=1.

The 8051 writes a "1" to an IN endpoint busy bit to disarm a previously armed endpoint. (This sets BSY=0.) The 8051 program should do this only after a USB bus reset, or when the host selects a new interface or alternate setting that uses the endpoint. This prevents stale data from a previous setting from being accepted by the host's first IN transfer that uses the new setting.

Note:

Even though the register description shows bit 1 as "R/W," the 8051 can only clear this bit by writing a "1" to it. The 8051 can not directly set this bit.

To disarm a paired IN endpoint, write a "1" to the busy bit for *both* endpoints in the pair.

Bit 0: **INnSTL** *IN Endpoint (1-7) Stall*

The 8051 sets this bit to "1" to *stall* an endpoint, and to "0" to clear a stall.

When the stall bit is "1," the EZ-USB core returns a STALL Handshake for all requests to the endpoint. This notifies the host that something unexpected has happened.

The 8051 sets an endpoint's stall bit under two circumstances:

1. The host sends a "Set_Feature—Endpoint Stall" request to the specific endpoint.

2. The 8051 encounters any *show stopper* error on the endpoint, and sets the stall bit to tell the host to halt traffic to the endpoint.

The 8051 clears an endpoint's stall bit under two circumstances:

1. The host sends a "Clear_Feature--Endpoint Stall" request to the specific endpoint.

2. The 8051 receives some other indication from the host that the stall should be cleared (this is referred to as "host intervention" in the USB Specification). This indication could be a USB bus reset.

All stall bits are automatically cleared when the EZ-USB chip ReNumerates™ by pulsing the DISCON bit HI.

INnBC	Endpoint (1-7) IN Byte Count	7FB7-7FC3*

b7	b6	b5	b4	b3	b2	b1	b0
-	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

* See Table 12-5 for individual byte count register addresses.

Figure 12-27. IN Byte Count Registers

The 8051 writes this register with the number of bytes it loaded into the IN endpoint buffer INnBUF. Writing this register also *arms* the endpoint by setting the endpoint BSY bit to 1.

Legal values for these registers are 0-64. A zero transfer size is used to terminate a transfer that is an integral multiple of MaxPacketSize. For example, a 256-byte transfer with maxPacketSize = 64, would require four packets of 64 bytes each plus one packet of 0 bytes.

The IN byte count should never be written while the endpoint's BUSY bit is set.

When the register pairing feature is used (Section 6, "EZ-USB Bulk Transfers") IN2BC is used for the EP2/EP3 pair, IN4BC is used for the EP4/EP5 pair, and IN6BC is used for the EP6/EP7 pair. In the *paired* (double-buffered) mode, after the first write to the even-numbered byte count register, the endpoint BSY bit remains at 0, indicating that only one of the buffers is full, and the other is still empty. The odd numbered byte count register is not used when endpoints are paired.

OUTnCS **Endpoint (1-7) OUT Control and Status** **7FC6-7FD2***

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	**OUTnBSY**	**OUTnSTL**
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0

* See Table 12-5 for individual control/status register addresses.

Figure 12-28. OUT Control and Status Registers

Bit 1: **OUTnBSY** *OUT Endpoint (1-7) Busy*

The BSY bit indicates the status of the endpoint's OUT Buffer OUTnBUF. The EZ-USB core sets BSY=0 when the host data is available in the OUT buffer. The 8051 sets BSY=1 by loading the endpoint's byte count register.

When BSY=1, endpoint RAM data is invalid--the endpoint buffer has been emptied by the 8051 and is waiting for new OUT data from the host, or it is the process of being loaded over the USB. BSY=0 when the USB OUT transfer is complete and endpoint RAM data in OUTnBUF is available for the 8051 to read. USB OUT tokens for the endpoint are NAKd while BSY=1 (the 8051 is still reading data from the OUT endpoint).

A 1-to-0 transition of BSY (indicating that the 8051 can access the buffer) generates an interrupt request for the OUT endpoint. After the 8051 reads the data from the OUT endpoint buffer, it loads the endpoint's byte count register with any value to re-arm the endpoint, which automatically sets BSY=1. This enables the OUT transfer of data from the host in response to the next OUT token. The CPU should never read endpoint data while BSY=1.

Bit 0: **OUTnSTL** *OUT Endpoint (1-7) Stall*

The 8051 sets this bit to "1" to *stall* an endpoint, and to "0" to clear a stall.

When the stall bit is "1," the EZ-USB core returns a STALL Handshake for all requests to the endpoint. This notifies the host that something unexpected has happened.

The 8051 sets an endpoint's stall bit under two circumstances:

1. The host sends a "Set_Feature—Endpoint Stall" request to the specific endpoint.

2. The 8051 encounters any *show stopper* error on the endpoint, and sets the stall bit to tell the host to halt traffic to the endpoint.

The 8051 clears an endpoint's stall bit under two circumstances:

1. The host sends a "Clear_Feature—Endpoint Stall" request to the specific endpoint.

2. The 8051 receives some other indication from the host that the stall should be cleared (this is referred to as "host intervention" in the USB Specification).

All stall bits are automatically cleared when the EZ-USB chip ReNumerates™.

OUTnBC **Endpoint (1-7) OUT Byte Count** **7FC7-7FD3***

b7	b6	b5	b4	b3	b2	b1	b0
-	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0

* See Table 12-5 for individual control/status register addresses.

Figure 12-29. OUT Byte Count Registers

The 8051 reads this register to determine the number of bytes sent to an OUT endpoint. Legal sizes are 0 - 64 bytes.

Each EZ-USB bulk OUT endpoint has a byte count register, which serves two purposes. The 8051 *reads* the byte count register to determine how many bytes were received during the last OUT transfer from the host. The 8051 *writes* the byte count register (with any value) to tell the EZ-USB core that it has finished reading bytes from the buffer, making the buffer available to accept the next OUT transfer. Writing the byte count register sets the endpoint's BSY bit to "1."

When the register-pairing feature is used, OUT2BC is used for the EP2/EP3 pair, OUT4BC is used for the EP4/EP5 pair, and OUT6BC is used for the EP6/EP7 pair. The odd-numbered byte count registers should not be used. When the 8051 writes a byte to the even numbered byte count register, the EZ-USB core switches buffers. If the other buffer already contains data to be read by the 8051, the OUTnBSY bit remains at "0."

All OUT tokens are NAKd until the 8051 is released from RESET, whereupon the ACK/ NAK behavior is based on pairing.

12.14 Global USB Registers

SUDPTRH **Setup Data Pointer High** **7FD4**

b7	b6	b5	b4	b3	b2	b1	b0
A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

SUDPTRL **Setup Data Pointer Low** **7FD5**

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-30. Setup Data Pointer High/Low Registers

When the EZ-USB chip receives a “Get_Descriptor” request on endpoint zero, it can instruct the EZ-USB core to handle the multi-packet IN transfer by loading these registers with the address of an internal table containing the descriptor data. The descriptor data tables may be placed in internal program/data RAM or in unused *Endpoint 0-7 RAM*. The SUDPTR does not operate with external memory. The SUDPTR registers should be loaded in HIGH/LOW order.

In addition to loading SUDPTRL, the 8051 must also clear the HSNAK bit in the EP0CS register (by writing a “1” to it) to complete the CONTROL transfer.

Note

Any host request that uses the EZ-USB Setup Data Pointer to transfer IN data must indicate the number of bytes to transfer in bytes 6 (wLenghthL) and 7 (wLengthH) of the SETUP packet. These bytes are pre-assigned in the USB Specification to be length bytes in all standard device requests such as “Get_Descriptor.” If vendor-specific requests are used to transfer large blocks of data using the Setup Data Pointer, they must include this pre-defined length field in bytes 6-7 to tell the EZ-USB core how many bytes to transfer using the Setup Data Pointer.

USBCS	USB Control and Status	7FD6

b7	b6	b5	b4	b3	b2	b1	b0
WAKESRC	-	-	-	**DISCON**	**DISCOE**	**RENUM**	**SIGRSUME**
R/W	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

Figure 12-31. USB Control and Status Registers

Bit 7: WAKESRC *Wakeup source*

This bit indicates that a high to low transaction was detected on the WAKEUP# pin. Writing a “1” to this bit resets it to “0.”

Bit 3: DISCON *Signal a Disconnect on the DISCON# pin*

The EZ-USB DISCON# pin reflects the complement of this bit. This bit is normally set to 0 so that the action of the DISCOE bit (below) either floats the DISCON# pin or drives it HI.

Bit 2: DISCOE *Disconnect Output Enable*

DISCOE controls the output buffer on the DISCON# pin. When DISCOE=0, the pin floats, and when DISCOE=1, it drives to the complement of the DISCON bit (above).

DISCOE is used in conjunction with the RENUM bit to perform ReNumeration™ (Chapter 5, "EZ-USB Enumeration and ReNumeration™").

Bit 1: **RENUM** *ReNumerate*

This bit controls which entity, the USB core or the 8051, handles USB device requests. When RENUM=0, the EZ-USB core handles all device requests. When RENUM=1, the 8051 handles all device requests except Set_Address.

The 8051 sets RENUM=1 during a bus disconnect to transfer USB control to the 8051. The EZ-USB core automatically sets RENUM=1 under two conditions:

1. Completion of a “B2” boot load (Chapter 5, "EZ-USB Enumeration and ReNumeration™").

2. When external memory is used (EA=1) and no boot I^2C EEPROM is used (see Section 10.3.3, "External ROM").

Bit 0: **SIGRSUME** *Signal remote device resume*

The 8051 sets SIGRSUME=1 to drive the “K” state onto the USB bus. This should be done only by a device that is capable of remote wakeup, and then only during the SUSPEND state. To signal RESUME, the 8051 sets SIGRSUME=1, waits 10-15 ms, then sets SIGRSUME=0.

TOGCTL **Data Toggle Control** **7FD7**

b7	b6	b5	b4	b3	b2	b1	b0
Q	**S**	**R**	**IO**	**0**	**EP2**	**EP1**	**EP0**
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-32. Data Toggle Control Register

Bit 7: **Q** *Data Toggle Value*

Q=0 indicates DATA0 and Q=1 indicates DATA1, for the endpoint selected by the IO and EP[2..0] bits. The 8051 writes the endpoint select bits (IO and EP[2..0]), before reading this value.

Bit 6: **S** *Set Data Toggle to DATA1*

After selecting the desired endpoint by writing the endpoint select bits (IO and EP[2..0]) the 8051 sets S=1 to set the data toggle to DATA1. The endpoint selection bits should not be changed while this bit is written.

Note

At this writing there is no known reason to set an endpoint data toggle to 1. This bit is provided for generality and testing only.

Bit 5: **R** *Set Data Toggle to DATA0*

After selecting the desired endpoint by writing the endpoint select bits (IO and EP[2..0]) the 8051 sets R=1 to set the data toggle to DATA0. The endpoint selection bits should not be changed while this bit is written. For advice on when to reset the data toggle, see Chapter 7, "EZ-USB Endpoint Zero."

Bit 4: **IO** *Select IN or OUT endpoint*

The 8051 sets this bit to select an endpoint direction prior to setting its R or S bit. IO=0 selects an OUT endpoint, IO=1 selects an IN endpoint.

Bit 2-0: EP *Select endpoint*

The 8051 sets these bits to select an endpoint prior to setting its R or S bit. Valid values are 0-7 to correspond to bulk endpoints IN0-IN7 and OUT0-OUT7.

USBFRAMEL USB Frame Count Low 7FD8

b7	b6	b5	b4	b3	b2	b1	b0
FC7	**FC6**	**FC5**	**FC4**	**FC3**	**FC2**	**FC1**	**FC0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

USBFRAMEH USB Frame Count High 7FD9

b7	b6	b5	b4	b3	b2	b1	b0
0	**0**	**0**	**0**	**0**	**FC10**	**FC9**	**FC8**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 12-33. USB Frame Count High/Low Registers

Every millisecond the host sends a SOF token indicating “Start Of Frame,” along with an 11-bit incrementing frame count. The EZ-USB copies the frame count into these registers at every SOF. One use of the frame count is to respond to the USB SYNC_FRAME request (Chapter 7, "EZ-USB Endpoint Zero").

If the USB core detects a missing or garbled SOF, it generates an internal SOF and increments USBFRAMEL-USBRAMEH.

FNADDR **Function Address** **7FDB**

b7	b6	b5	b4	b3	b2	b1	b0
0	**FA6**	**FA5**	**FA4**	**FA3**	**FA2**	**FA1**	**FA0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 12-34. Function Address Register

During the USB enumeration process, the host sends a device a unique 7-bit address, which the EZ-USB core copies into this register. There is normally no reason for the CPU to know its USB device address because the USB Core automatically responds only to its assigned address.

Note

During ReNumeration™ the USB Core sets register to 0 to allow the EZ-USB chip to respond to the default address 0.

USBPAIR **USB Endpoint Pairing** **7FDD**

b7	b6	b5	b4	b3	b2	b1	b0
ISOSEND0	**-**	**PR6OUT**	**PR4OUT**	**PR2OUT**	**PR6IN**	**PR4IN**	**PR2IN**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	x	0	0	0	0	0	0

Figure 12-35. USB Endpoint Pairing Register

Bit 7: **ISOSEND0** *Isochronous Send Zero Length Data Packet*

The ISOSEND0 bit is used when the EZ-USB chip receives an isochronous IN token while the IN FIFO is empty. If ISOSEND0=0 (the default value), the EZ-USB core does not respond to the IN token. If ISOSEND0=1, the EZ-USB core sends a zero-length data packet in response to the IN token. Which action to take depends on the overall system design. The ISOSEND0 bit applies to all of the isochronous IN endpoints, IN8BUF through IN15BUF.

Bit 5-3: **PRnOUT** *Pair Bulk OUT Endpoints*

Set the endpoint pairing bits (PRxOUT) to "1" to enable double-buffering of the bulk OUT endpoint buffers. With double buffering enabled, the 8051 can operate on one buffer while another is being transferred over USB. The endpoint busy and interrupt request bits function identically, so the 8051 code requires no code modification to support double buffering.

When an endpoint is paired, the 8051 uses only the even-numbered endpoint of the pair. The 8051 should not use the paired odd endpoint's IRQ, IEN, VALID bits or the buffer associated with the odd numbered endpoint.

Bit 2-0: **PRnIN** *Pair Bulk IN Endpoints*

Set the endpoint pairing bits (PRxIN) to "1" to enable double-buffering of the bulk IN endpoint buffers. With double buffering enabled, the 8051 can operate on one buffer while another is being transferred over USB.

When an endpoint is paired, the 8051 should access only the even-numbered endpoint of the pair. The 8051 should not use the IRQ, IEN, VALID bits or the buffer associated with the odd numbered endpoint.

IN07VAL **Endpoints 0-7 IN Valid Bits** **7FDE**

b7	b6	b5	b4	b3	b2	b1	b0
IN7VAL	**IN6VAL**	**IN5VAL**	**IN4VAL**	**IN3VAL**	**IN2VAL**	**IN1VAL**	**IN0VAL**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	1	0	1	1	1

OUT07VAL **Endpoints 0-7 OUT Valid Bits** **7FDF**

b7	b6	b5	b4	b3	b2	b1	b0
OUT7VAL	**OUT6VAL**	**OUT5VAL**	**OUT4VAL**	**OUT3VAL**	**OUT2VAL**	**OUT1VAL**	**OUT0VAL**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	1	0	1	0	1

Figure 12-36. IN/OUT Valid Bits Register

The 8051 sets VAL=1 for any active endpoints, and VAL=0 for inactive endpoints. These bits instruct the EZ-USB core to return a “no response” if an invalid endpoint is addressed, instead of a NAK.

The default values of these registers are set to support all endpoints that exist in the default USB device (see Table 5-1).

INISOVAL **Isochronous IN Endpoint Valid Bits** **7FE0**

b7	b6	b5	b4	b3	b2	b1	b0
IN15VAL	**IN14VAL**	**IN13VAL**	**IN12VAL**	**IN11VAL**	**IN10VAL**	**IN9VAL**	**IN8VAL**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

OUTISOVAL **Isochronous OUT Endpoint Valid Bits** **7FE1**

b7	b6	b5	b4	b3	b2	b1	b0
OUT15VAL	**OUT14VAL**	**OUT13VAL**	**OUT12VAL**	**OUT11VAL**	**OUT10VAL**	**OUT9VAL**	**OUT8VAL**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Figure 12-37. Isochronous IN/OUT Endpoint Valid Bits Register

The 8051 sets VAL=1 for active endpoints, and VAL=0 for inactive endpoints. These bits instruct the EZ-USB core to return a “no response” if an invalid endpoint is addressed.

The default values of these registers are set to support all endpoints that exist in the default USB device (see Table 5-1).

12.15 Fast Transfers

FASTXFR **Fast Transfer Control** **7FE2**

b7	b6	b5	b4	b3	b2	b1	b0
FISO	**FBLK**	**RPOL**	**RMOD1**	**RMOD0**	**WPOL**	**WMOD1**	**WMOD0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-38. Fast Transfer Control Register

The EZ-USB core provides a fast transfer mode that improves the8051 transfer speed between external logic and the isochronous and bulk endpoint buffers. The FASTXFR register enables the modes for bulk and/or isochronous transfers, and selects the timing waveforms for the FRD# and FWR# signals.

Bit 7: **FISO** *Enable Fast ISO Transfers*

The 8051 sets FISO=1 to enable fast isochronous transfers for all16 isochronous endpoint FIFOs. When FISO=0, fast transfers are disabled for all 16 isochronous endpoints.

Bit 6: **FBLK** *Enable Fast BULK Transfers*

The 8051 sets FBLK=1 to enable fast bulk transfers using the Autopointer (see Section 12.16, "SETUP Data") with BULK endpoints. When FBLK=0 fast transfers are disabled for BULK endpoints.

Bit 5: **RPOL** *FRD# Pulse Polarity*

The 8051 sets RPOL=0 for active-low FRD# pulses, and RPOL=1 for active high FRD# pulses.

Bit 4-3: **RMOD** *FRD# Pulse Mode*

These bits select the phasing and width of the FRD# pulse. See Figure 8-12.

Bit 2: **WPOL** *FWR# Pulse Polarity*

The 8051 sets WPOL=0 for active-low FWR# pulses, and WPOL=1 for active high FWR# pulses.

Bit 1-0: **WMOD** *FWR# Pulse Mode*

These bits select the phasing and width of the FWR# pulse. See Figure 8-11.

AUTOPTRH **Auto Pointer Address High** **7FE3**

b7	b6	b5	b4	b3	b2	b1	b0
A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

AUTOPTRL **Auto Pointer Address Low** **7FE4**

b7	b6	b5	b4	b3	b2	b1	b0
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

AUTODATA **Auto Pointer Data** **7FE5**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

Figure 12-39. Auto Pointer Registers

These registers implement the EZ-USB *Autopointer.*

AUTOPTRH/L

The 8051 loads a 16-bit address into the AUTOPTRH/L registers. Subsequent reads or writes to the AUTODATA register increment the 16-bit value in these registers. The loaded address must be in internal EZ-USB RAM. The 8051 can read these registers to determine the address must be in internal EZ-USB RAM. The 8051 can read these registers to determine the address of the next byte to be accessed via the AUTODATA register.

AUTODATA

8051 data read or written to the AUTODATA register accesses the memory addressed by the AUTOPTRH/L registers, and increments the address *after* the read or write.

These registers allow FIFO access to the bulk endpoint buffers, as well as being useful for internal data movement. Chapter 6, "EZ-USB Bulk Transfers" and Chapter 8, "EZ-USB Isochronous Transfers" explain how to use the Autopointer for fast transfers to and from the EZ-USB endpoint buffers.

12.16 SETUP Data

SETUPBUF **SETUP Data Buffer (8 Bytes)** **7FE8-7FEF**

b7	b6	b5	b4	b3	b2	b1	b0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R	R	R	R	R	R	R	R
x	x	x	x	x	x	x	x

Figure 12-40. SETUP Data Buffer

This buffer contains the 8 bytes of SETUP packet data from the most recently received CONTROL transfer.

The data in SETUPBUF is valid when the SUDAVIR (Setup Data Available Interrupt Request) bit is set. The 8051 responds to the SUDAV interrupt by reading the SETUP bytes from this buffer.

12.17 Isochronous FIFO Sizes

OUTnADDR ISO OUT Endpoint Start Address 7FF0-7FF7*

b7	b6	b5	b4	b3	b2	b1	b0
A9	**A8**	**A7**	**A6**	**A5**	**A4**	**0**	**0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

INnADDR ISO IN Endpoint Start Address 7FF8-7FFF*

b7	b6	b5	b4	b3	b2	b1	b0
A9	**A8**	**A7**	**A6**	**A5**	**A4**	**0**	**0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	x	x	x	x	x	x	x

* See Table 12-6 for individual start address register addresses.

Figure 12-41. SETUP Data Buffer

Table 12-6. Isochronous FIFO Start Address Registers

Address	Endpoint Start Address
7FF0	Endpoint 8 OUT Start Address
7FF1	Endpoint 9 OUT Start Address
7FF2	Endpoint 10 OUT Start Address
7FF3	Endpoint 11 OUT Start Address
7FF4	Endpoint 12 OUT Start Address
7FF5	Endpoint 13 OUT Start Address
7FF6	Endpoint 14 OUT Start Address
7FF7	Endpoint 15 OUT Start Address
7FF8	Endpoint 8 IN Start Address
7FF9	Endpoint 9 IN Start Address
7FFA	Endpoint 10 IN Start Address
7FFB	Endpoint 11 IN Start Address
7FFC	Endpoint 12 IN Start Address
7FFD	Endpoint 13 IN Start Address
7FFE	Endpoint 14 IN Start Address
7FFF	Endpoint 15 IN Start Address

EZ-USB Isochronous endpoints use a pool of 1,024 double-buffered FIFO bytes. The 1,024 FIFO bytes can be divided between any or all of the isochronous endpoints. The 8051 sets isochronous endpoint FIFO sizes by writing starting addresses to these registers, starting with address 0. Address bits A3-A0 are internally set to zero, so the minimum FIFO size is 16 bytes.

See Section 8.8, "Fast Transfer Speed" for details about how to set these registers.

13 EZ-USB AC/DC Parameters

13.1 Electrical Characteristics

13.1.1 Absolute Maximum Ratings

Storage Temperature . . . . . -65ºC to +150ºC
Ambient Temperature Under Bias . . . . . -40ºC to +85ºC
Supply Voltage to Ground Potential . . . . . -0.5V to +4.0V
DC Input Voltage to Any Pin . . . . . -0.5V to +5.8V

13.1.2 Operating Conditions

Ta (Ambient Temperature Under Bias). . . . . 0ºC to +70ºC
Supply Voltage . . . . . +3.0V to +3.6V
Ground Voltage 0V
F_{osc} (Oscillator or Crystal Frequency) . . . . . 12 MHz +/- 0.25%

13.1.3 DC Characteristics

Table 13-1. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
V_{CC}	Supply Voltage		3.0		3.6	V	
V_{IH}	Input High Voltage		2		5.25	V	
V_{IL}	Input Low Voltage		-.5		.8	V	
I_I	Input Leakage Current	$0 < V_{IN} < V_{CC}$			$\pm$ 10	µA	
V_{OH}	Output Voltage High	I_{OUT} = 1.6 mA	2.4			V	
V_{OL}	Output Low Voltage	I_{OUT} = -1.6 mA			.8	V	
C_{IN}	Input Pin Capacitance				10	pF	
I_{SUSP}	Suspend Current			110		µA	
I_{CC}	Supply Current	8051 running, connected to USB			50	mA	

13.1.4 AC Electrical Characteristics

Specified Conditions: Capacitive load on all pins = 30 pF

13.1.5 General Memory Timing

Table 13-2. General Memory Timing

Symbol	Parameter	Min	Typ	Max	Unit	Notes
tCL	1/CLK24 Frequency		41.66		ns	
tAV	Delay from Clock to Valid Address	0		10	ns	
tCD	Delay from CLK24 to CS#	2		15	ns	
tOED	Delay from CLK24 to OE#	2		15	ns	
tWD	Delay from CLK24 to WR#	2		15	ns	
tRD	Delay from CLK24 to RD#	2		15	ns	
tPD	Delay from CLK24 to PSEN#	2		15	ns	

13.1.6 Program Memory Read

Table 13-3. Program Memory Read

Symbol	Parameter	Formula	Min	Max	Unit	Notes
tAA1	Address Access Time	3tCL-tAV-TDSU1	103		ns	
tAH1	Address Hold from CLK24	tCL+1	42		ns	
tDSU1	Data setup to CLK24		12		ns	
tDH1	Data Hold from CLK24		0		ns	

13.1.7 Data Memory Read

Table 13-4. Data Memory Read

Symbol	Parameter	Formula	Min	Max	Unit	Notes
tAA2	Address Access Time	3tCL-tAV-TDSU1	103		ns	
tAH2	Address Hold from CLK24	tCL+1	42		ns	
tDSU2	Data setup to CLK24		12		ns	
tDH2	Data Hold from CLK24		0		ns	

13.1.8 Data Memory Write

Table 13-5. Data Memory Write

Symbol	Parameter	Formula	Min	Max	Unit	Notes
tAH3	Address Hold from CLK24	tCL+2	43		ns	
tDV	CLK24 to Data Valid			15	ns	
tDVZ	CLK24 to High Impedance	tCL+16	57		ns	

13.1.9 Fast Data Write

Table 13-6. Fast Data Write

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
tCDO	Clock to Data Output Delay		3	15	ns	
tCWO	Clock to FIFO Write Output Delay		2	10	ns	
tPFWD	Propagation Delay Difference from FIFO Write to DATA Out		1		ns	

13.1.10 Fast Data Read

Table 13-7. Fast Data Read

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
tCRO	Clock to FIFO Read Output Delay		2	10	ns	
tDSU4	Data Setup to Rising CLK24		12		ns	
tDH4	Data Hold to Rising CLK24		2		ns	

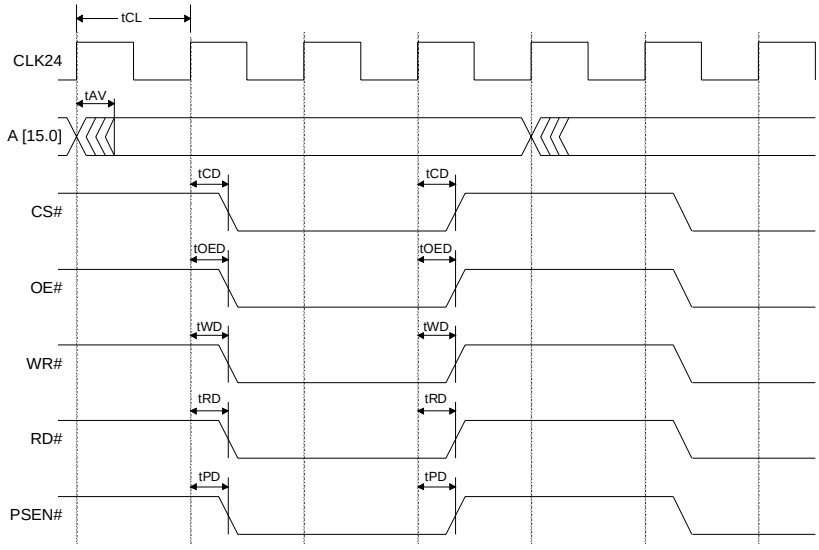


Figure 13-1. External Memory Timing

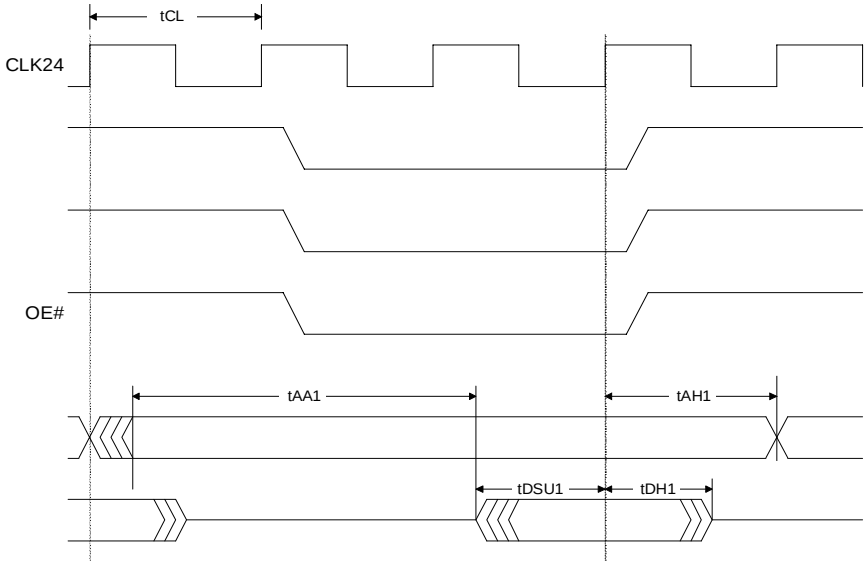


Figure 13-2. Program Memory Read Timing

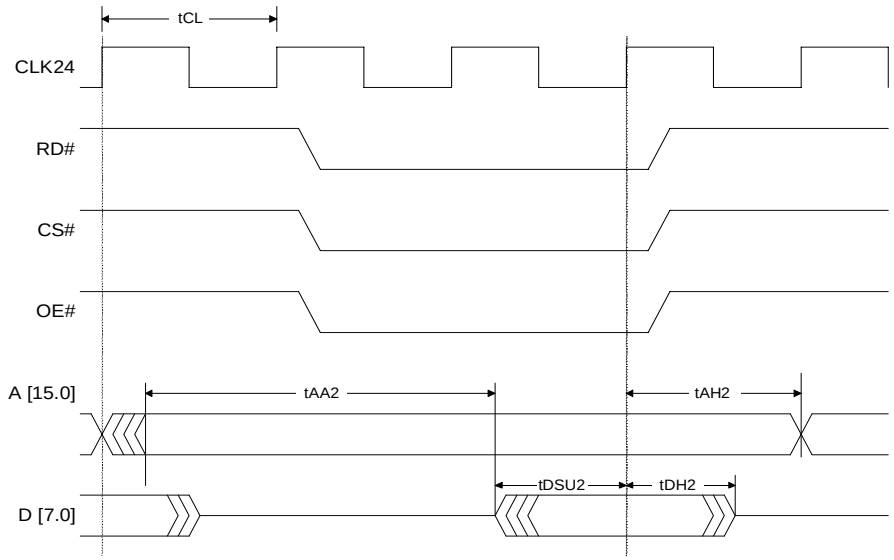


Figure 13-3. Data Memory Read Timing

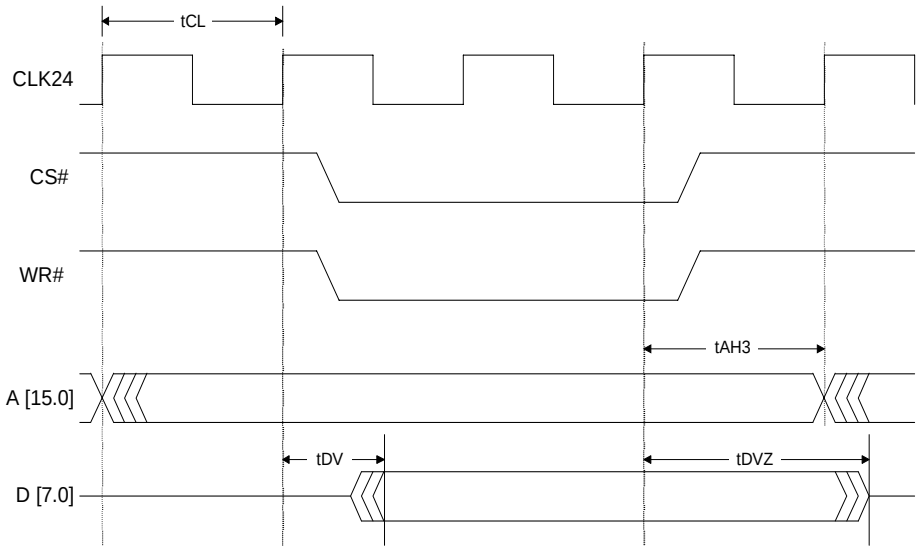


Figure 13-4. Data Memory Write Timing

EZ-USB
Fast Transfer Block Diagram

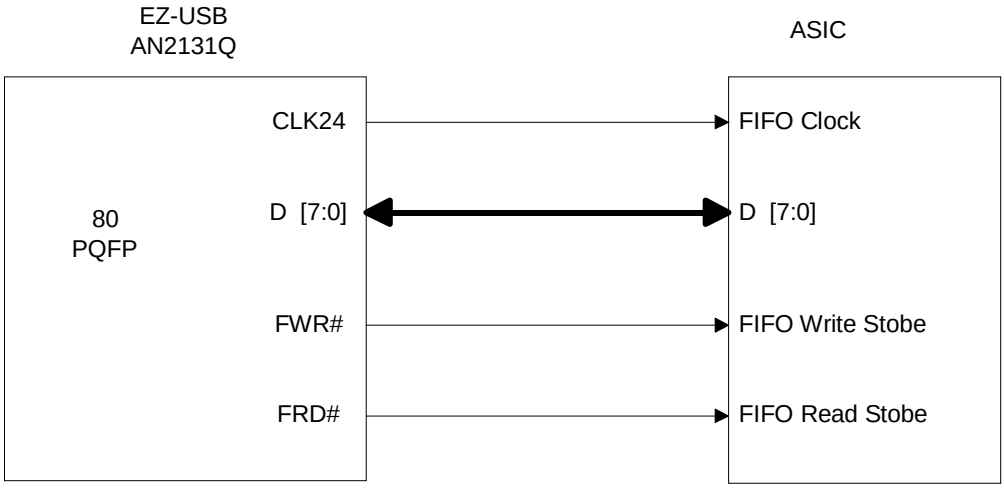


Figure 13-5. Fast Transfer Mode Block Diagram

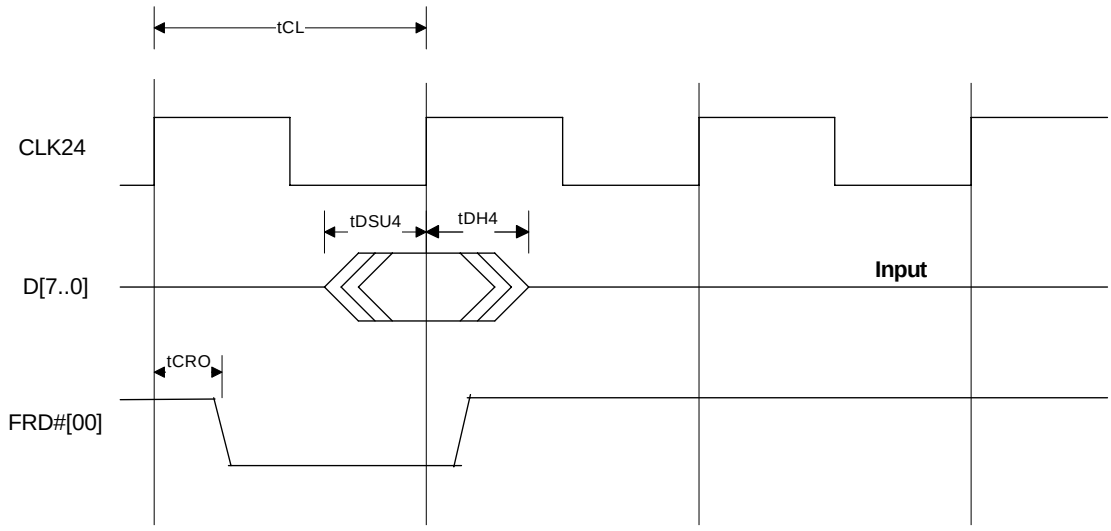


Figure 13-6. Fast Transfer Read Timing [Mode 00]

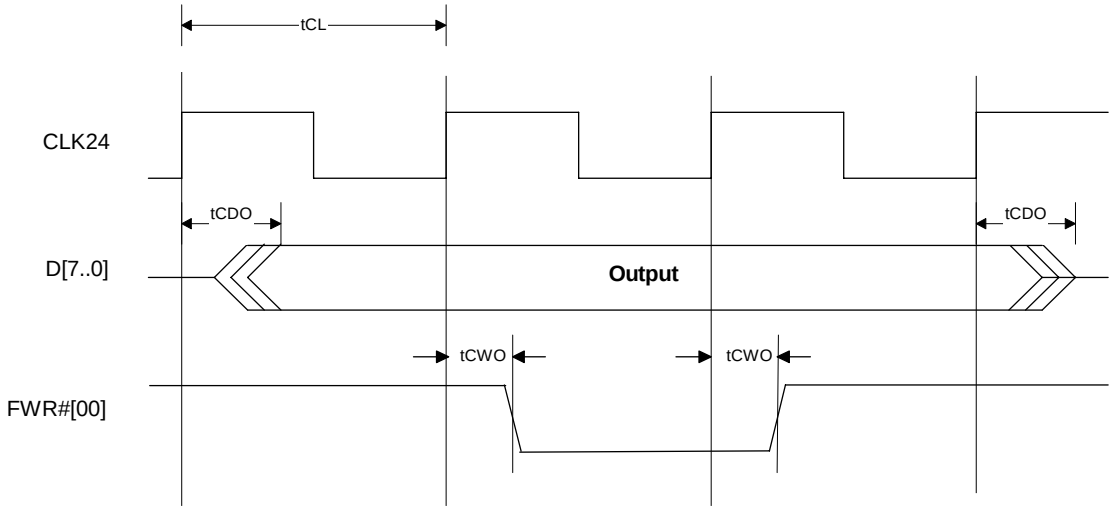


Figure 13-7. Fast Transfer Write Timing [Mode 00]

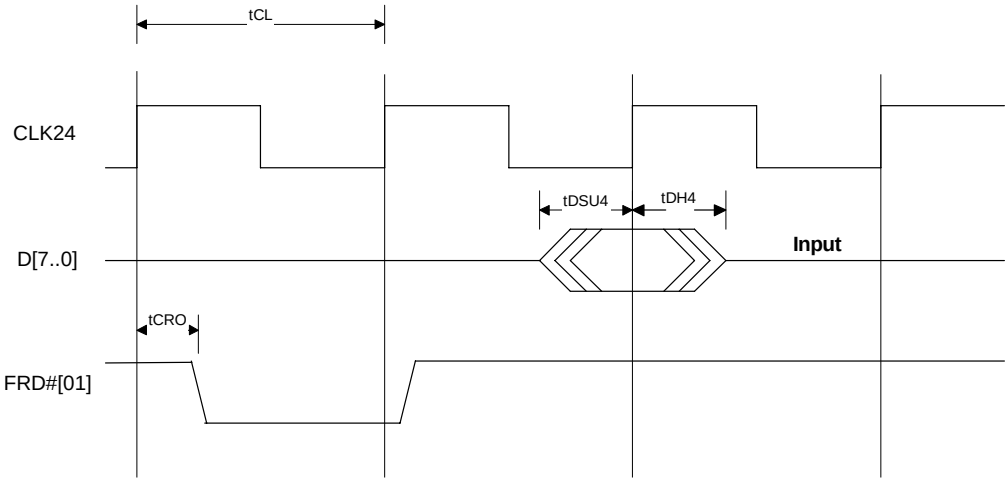


Figure 13-8. Fast Transfer Read Timing [Mode 01]

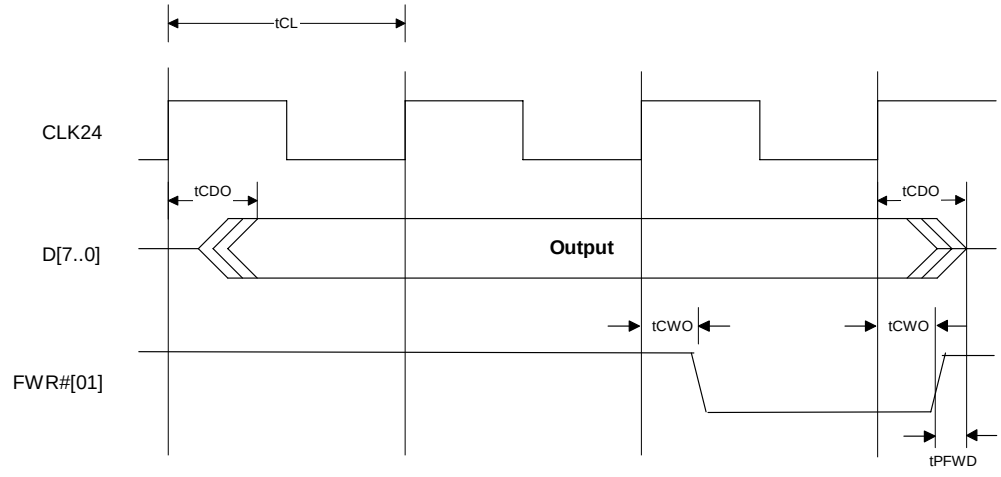


Figure 13-9. Fast Transfer Write Timing [MODE 01]

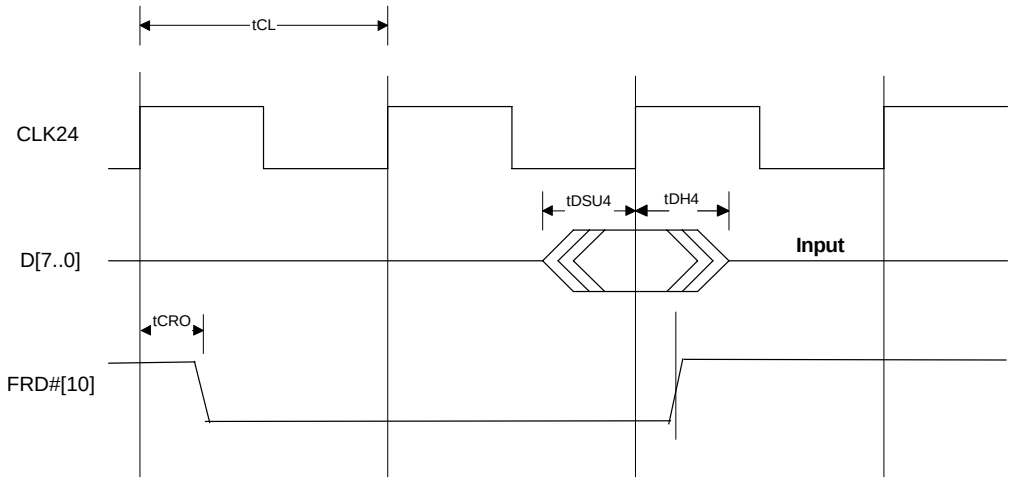


Figure 13-10. Fast Transfer Read Timing [Mode 10]

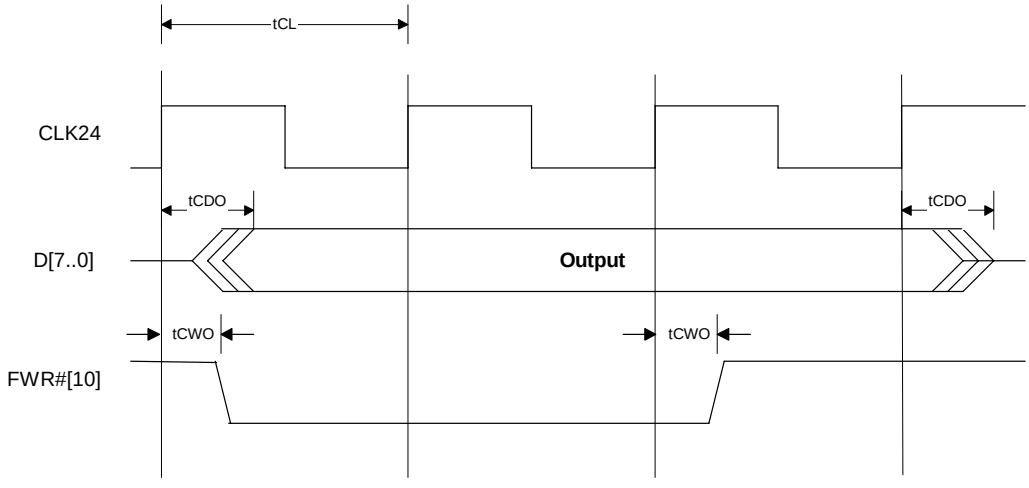


Figure 13-11. Fast Transfer Write Timing [Mode 10]

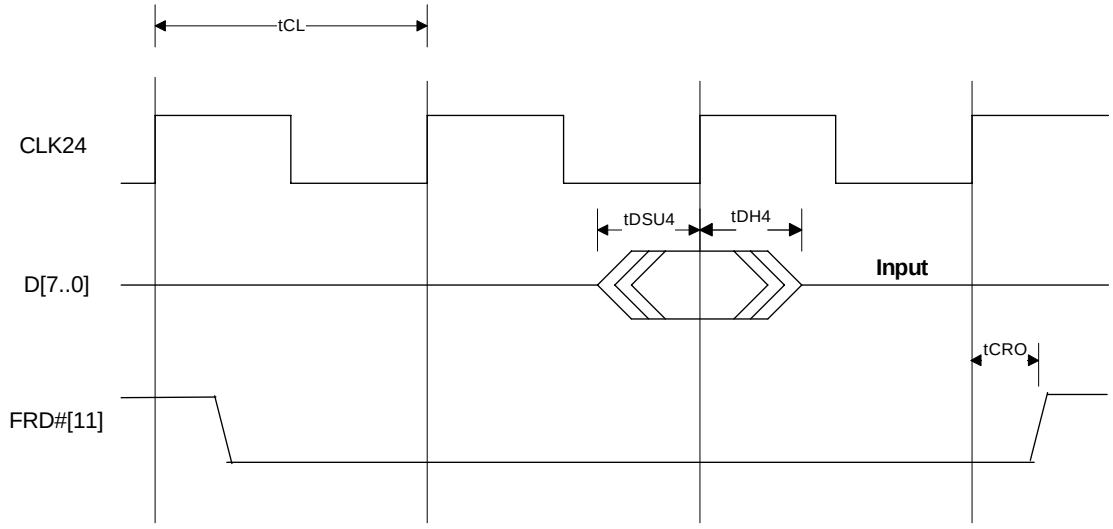


Figure 13-12. Fast Transfer Read Timing [Mode 11]

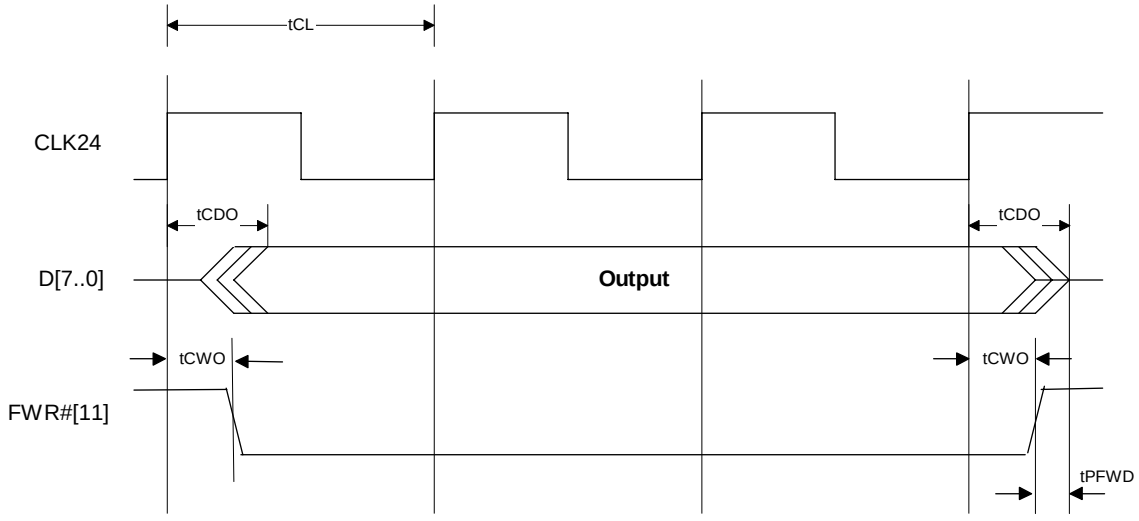


Figure 13-13. Fast Transfer Write Timing [Mode 11]

14 EZ-USB Packaging

14.1 44-Pin PQFP Package

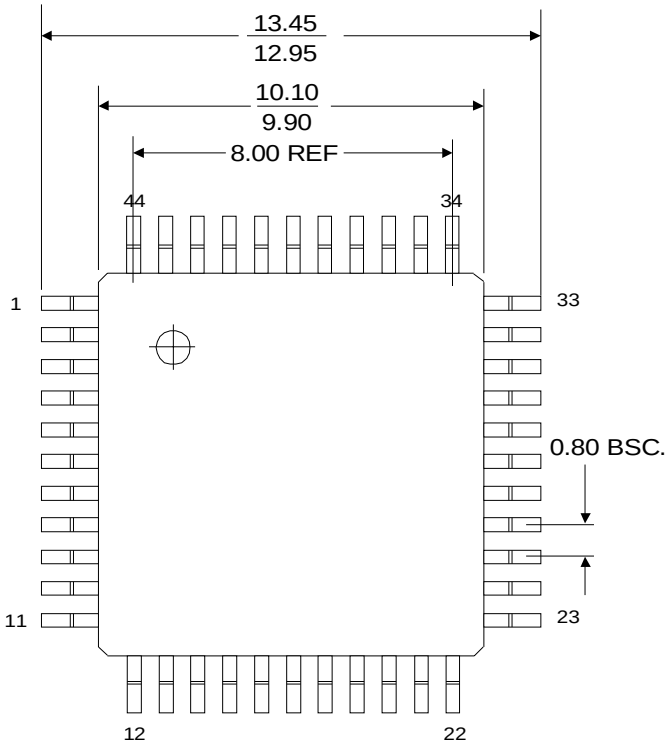


Figure 14-1. 44-Pin PQFP Package (Top View)

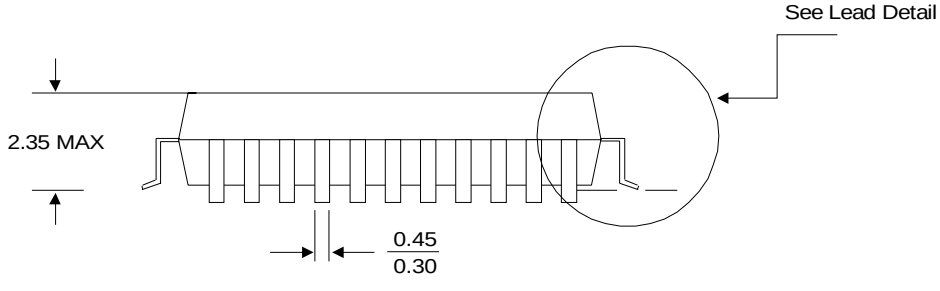
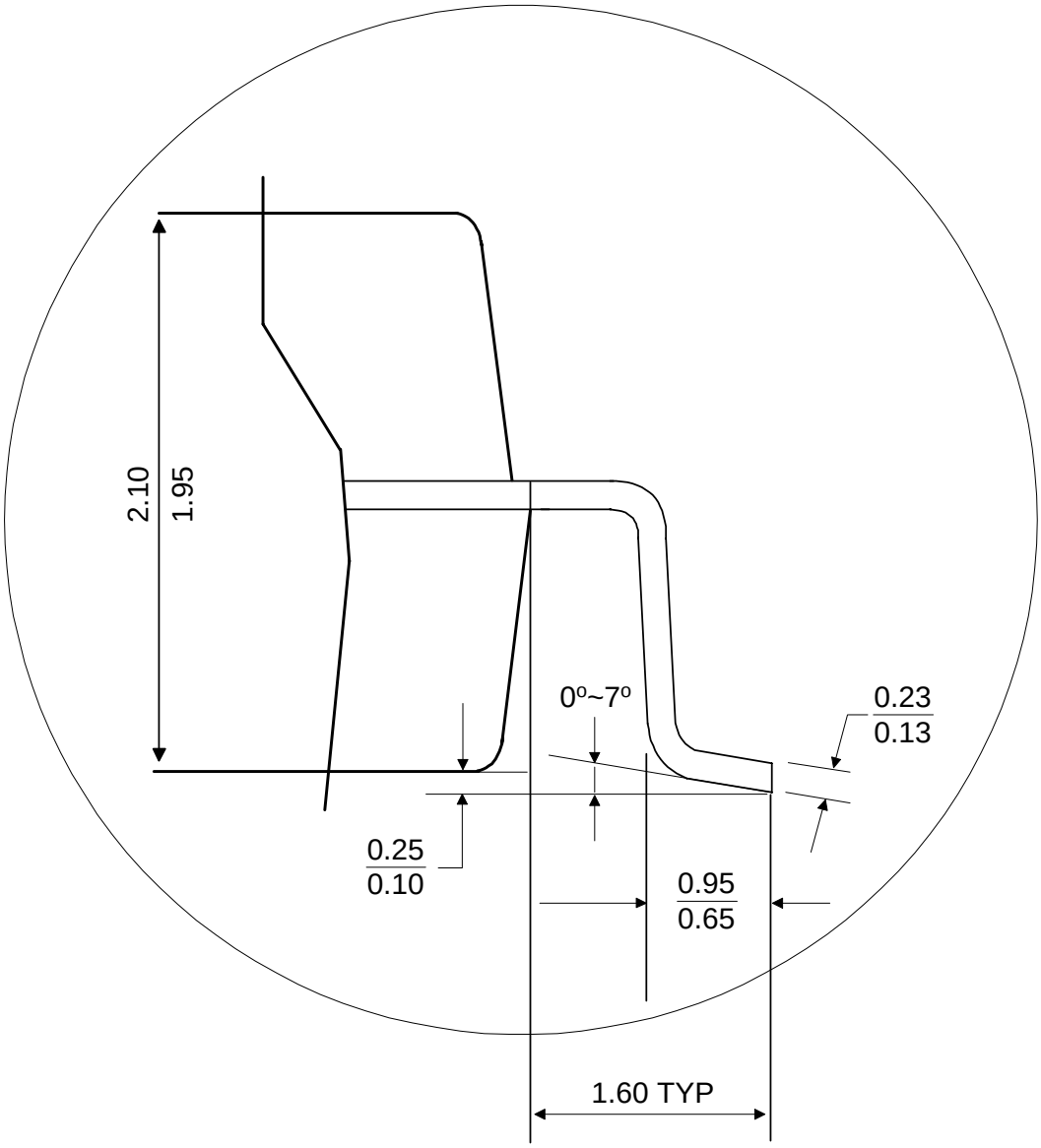


Figure 14-2. 44-Pin PQFP Package (Side View)



Lead Detail: A(S=N/S)

Figure 14-3. 44-Pin PQFP Package (Detail View)

14.2 80-Pin PQFP Package

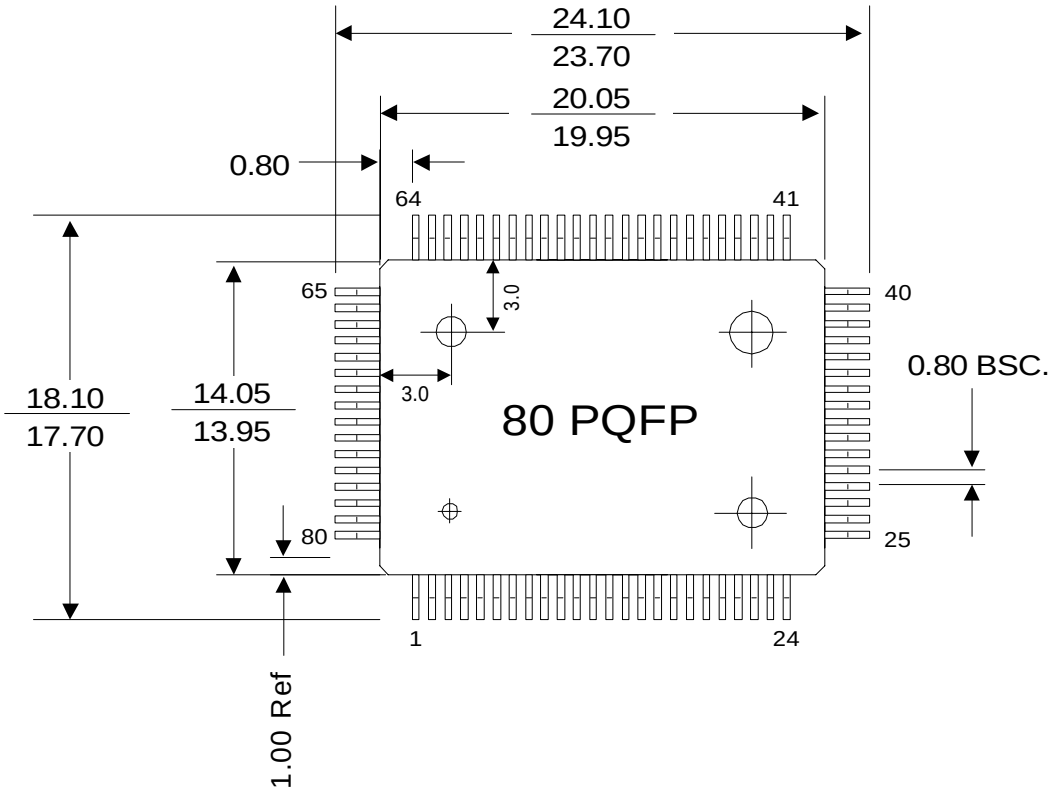


Figure 14-4. 80-Pin PQFP Package (Top View)

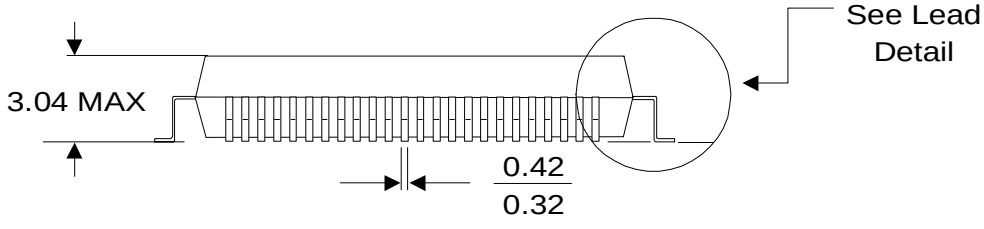


Figure 14-5. 80-Pin PQFP Package (Side View)

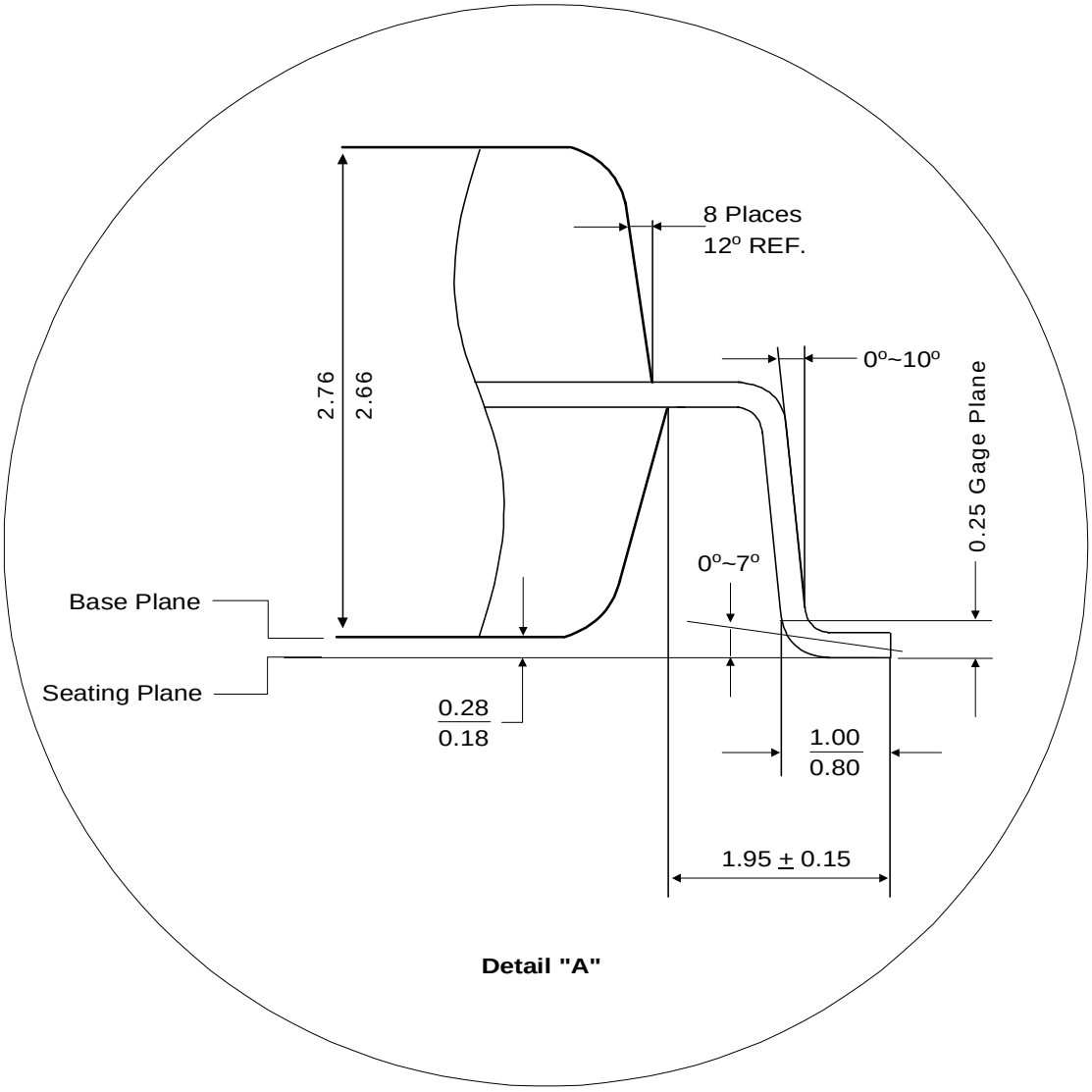


Figure 14-6. 80-Pin PQFP Package (Detail View)

14.3 48-Pin TQFP Package

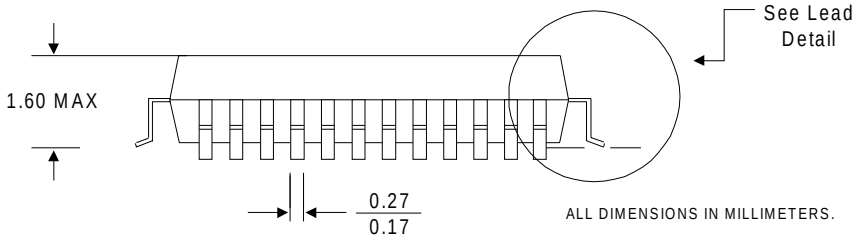


Figure 14-7. 48-Pin TQFP Package (Side View)

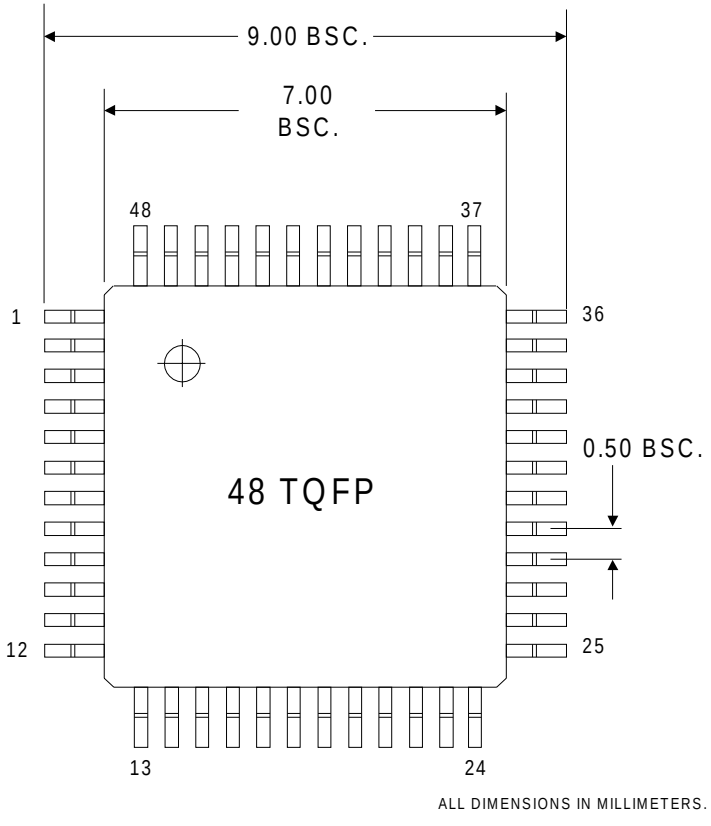


Figure 14-8. 48-Pin TQFP Package (Top View)

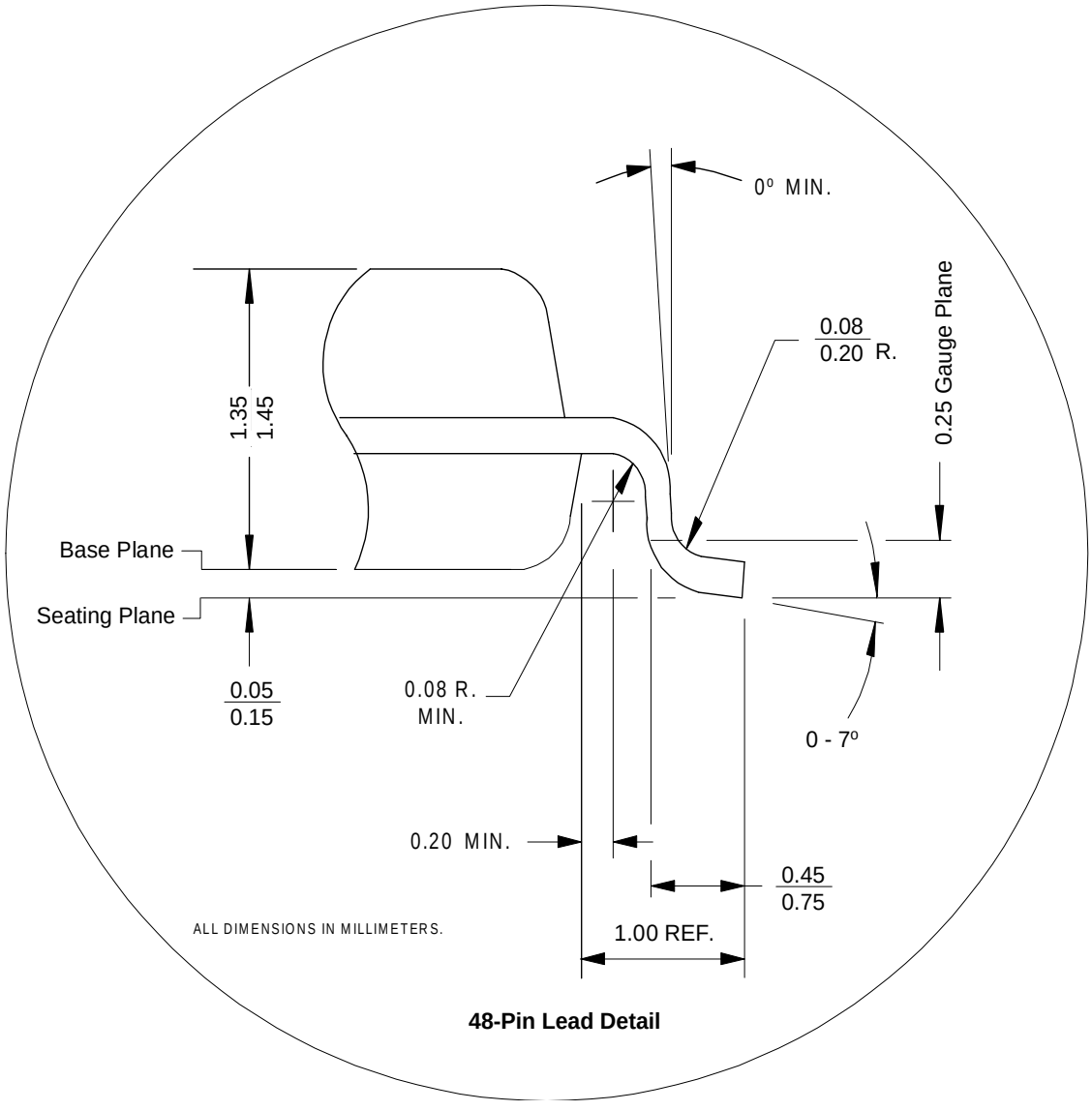


Figure 14-9. 48-Pin TQFP Package (Detail View)

EZ-USB v 1.9 Appendices

Table of Contents

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0			Notes
	Endpoint 0-7 Data Buffers												*CPU Access Codes:*
7B40	OUT7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			RW = Read or Write,
7B80	IN7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			R, r = read-only,
7BC0	OUT6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			W, w = write-only
7C00	IN6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			b = both (Read & Write)
7C40	OUT5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7C80	IN5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7CC0	OUT4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7D00	IN4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7D40	OUT3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7D80	IN3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7DC0	OUT2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7E00	IN2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7E40	OUT1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7E80	IN1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7EC0	OUT0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7F00	IN0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
	7F40-7F5F (reserved)												
	Isochronous Data												
7F60	OUT8DATA	Endpoint 8 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F61	OUT9DATA	Endpoint 9 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F62	OUT10DATA	Endpoint 10 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F63	OUT11DATA	Endpoint 11 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F64	OUT12DATA	Endpoint 12 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F65	OUT13DATA	Endpoint 13 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F66	OUT14DATA	Endpoint 14 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F67	OUT15DATA	Endpoint 15 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F68	IN8DATA	Endpoint 8 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F69	IN9DATA	Endpoint 9 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6A	IN10DATA	Endpoint 10 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6B	IN11DATA	Endpoint 11 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6C	IN12DATA	Endpoint 12 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6D	IN13DATA	Endpoint 13 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6E	IN14DATA	Endpoint 14 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6F	IN15DATA	Endpoint 15 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0			Notes
	Endpoint 0-7 Data Buffers												*CPU Access Codes:*
7B40	OUT7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			RW = Read or Write,
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7BC0	OUT6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			W, w = write-only
7C00	IN6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			b = both (Read & Write)
7C40	OUT5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7C80	IN5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7CC0	OUT4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7D00	IN4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7D40	OUT3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7D80	IN3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7DC0	OUT2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7E00	IN2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7E40	OUT1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7E80	IN1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7EC0	OUT0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
7F00	IN0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0			
	7F40-7F5F (reserved)												
	Isochronous Data												
7F60	OUT8DATA	Endpoint 8 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F61	OUT9DATA	Endpoint 9 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F62	OUT10DATA	Endpoint 10 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F63	OUT11DATA	Endpoint 11 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F64	OUT12DATA	Endpoint 12 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F65	OUT13DATA	Endpoint 13 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F66	OUT14DATA	Endpoint 14 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F67	OUT15DATA	Endpoint 15 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F68	IN8DATA	Endpoint 8 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F69	IN9DATA	Endpoint 9 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6A	IN10DATA	Endpoint 10 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6B	IN11DATA	Endpoint 11 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6C	IN12DATA	Endpoint 12 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6D	IN13DATA	Endpoint 13 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6E	IN14DATA	Endpoint 14 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			
7F6F	IN15DATA	Endpoint 15 IN Data	d7	d6	d5	d4	d3	d2	d1	d0			

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0			Notes
	Isochronous Byte Counts												
7F70	OUT8BCH	EP8 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F71	OUT8BCL	EP8 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F72	OUT9BCH	EP9 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F73	OUT9BCL	EP9 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F74	OUT10BCH	EP10 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F75	OUT10BCL	EP10 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F76	OUT11BCH	EP11 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F77	OUT11BCL	EP11 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F78	OUT12BCH	EP12 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F79	OUT12BCL	EP12 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F7A	OUT13BCH	EP13 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F7B	OUT13BCL	EP13 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F7C	OUT14BCH	EP14 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F7D	OUT14BCL	EP14 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F7E	OUT15BCH	EP15 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F7F	OUT15BCL	EP15 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
		7F80-7F91 (reserved)											
	CPU Registers												
7F92	CPUCS	Control & Status	rv3	rv2	rv1	rv0	0	0	CLK24OE	8051RES			rv[3..0] = chip rev
7F93	PORTACFG	Port A Configuration	RxD1out	RxD0out	FRD	FWR	CS	OE	T1out	T0out			0=port, 1=alt function
7F94	PORTBCFG	Port B Configuration	T2OUT	INT6	INT5	INT4	TxD1	RxD1	T2EX	T2			0=port, 1=alt function
7F95	PORTCCFG	Port C Configuration	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0			0=port, 1=alt function
	Input-Output Port Registers												
7F96	OUTA	Output Register A	OUTA7	OUTA6	OUTA5	OUTA4	OUTA3	OUTA2	OUTA1	OUTA0			
7F97	OUTB	Output Register B	OUTB7	OUTB6	OUTB5	OUTB4	OUTB3	OUTB2	OUTB1	OUTB0			
7F98	OUTC	Output Register C	OUTC7	OUTC6	OUTC5	OUTC4	OUTC3	OUTC2	OUTC1	OUTC0			
7F99	PINSA	Port Pins A	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0			
7F9A	PINSB	Port Pins B	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0			
7F9B	PINSC	Port Pins C	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0			
7F9C	OEA	Output Enable A	OEA7	OEA6	OEA5	OEA4	OEA3	OEA2	OEA1	OEA0			0=off, 1=drive
7F9D	OEB	Output Enable B	OEB7	OEB6	OEB5	OEB4	OEB3	OEB2	OEB1	OEB0			0=off, 1=drive
7F9E	OEC	Output Enable C	OEC7	OEC6	OEC5	OEC4	OEC3	OEC2	OEC1	OEC0			0=off, 1=drive
7F9F	UART230	230Kbaud support	0	0	0	0	0	0	UART1	UART0			1 = 230Kbaud rate
	Isochronous Control/Status Registers												
7FA0	ISOERR	ISO OUT Endpoint Error	ISO15ERR	ISO14ERR	ISO13ERR	ISO12ERR	ISO11ERR	ISO10ERR	ISO9ERR	ISO8ERR			
7FA1	ISOCTL	Isochronous Control	*	*	*	*	PPSTAT	MBZ	MBZ	ISODISAB			"MBZ" = Must Be Zero
7FA2	ZBCOUT	Zero Byte Count bits	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8			
7FA3		(reserved)											
7FA4		(reserved)											
	I^{2}C Registers												
7FA5	I2CS	Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE			
7FA6	I2DAT	Data	d7	d6	d5	d4	d3	d2	d1	d0			
7FA7	I2CMODE	I2C STOP interrupt enable	0	0	0	0	0	0	STOPIE	0			1=Enable INT3 on STOP

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0			Notes
	Interrupts												
7FA8	IVEC	Interrupt Vector	0	IV4	IV3	IV2	IV1	IV0	0	0			
7FA9	IN07IRQ	EPIN Interrupt Request	IN7IR	IN6IR	IN5IR	IN4IR	IN3IR	IN2IR	IN1IR	IN0IR			1=request
7FAA	OUT07IRQ	EPOUT Interrupt Request	OUT7IR	OUT6IR	OUT5IR	OUT4IR	OUT3IR	OUT2IR	OUT1IR	OUT0IR			1=request
7FAB	USBIRQ	USB Interrupt Request	*	*	IBNIR	URESIR	SUSPIR	SUTOKIR	SOFIR	SUDAVIR			1=request
7FAC	IN07IEN	EP0-7IN Int Enables	IN7IEN	IN6IEN	IN5IEN	IN4IEN	IN3IEN	IN2IEN	IN1IEN	IN0IEN			1=enabled
7FAD	OUT07IEN	EP0-7OUT Int Enables	OUT7IEN	OUT6IEN	OUT5IEN	OUT4IEN	OUT3IEN	OUT2IEN	OUT1IEN	OUT0IEN			1=enabled
7FAE	USBIEN	USB Int Enables	*	*	IBNIE	URESIE	SUSPIE	SUTOKIE	SOFIE	SUDAVIE			1=enabled
7FAF	USBBAV	Breakpoint & Autovector	*	*	*	*	BREAK	BPPULSE	BPEN	AVEN			1=enabled
7FB0	IBNIRQ	IBN Interrupt request		EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN			1=request
7FB1	IBNIE	IBN Interrupt Enable		EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN			1=enabled
7FB2	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8			
7FB3	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0			
	Bulk Endpoints 0-7												
7FB4	EP0CS	Control & Status	*	*	*	*	OUTBSY	INBSY	HSNAK	EP0STALL			For EP0IN and EP0OUT
7FB5	IN0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			* this bits are random
7FB6	IN1CS	Control & Status	*	*	*	*	*	*	in1bsy	in1stl			at power-on. Once
7FB7	IN1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			operational, these bits
7FB8	IN2CS	Control & Status	*	*	*	*	*	*	in2bsy	in2stl			read as zeros.
7FB9	IN2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FBA	IN3CS	Control & Status	*	*	*	*	*	*	in3bsy	in3stl			
7FBB	IN3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FBC	IN4CS	Control & Status	*	*	*	*	*	*	in4bsy	in4stl			
7FBD	IN4BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FBE	IN5CS	Control & Status	*	*	*	*	*	*	in5bsy	in5stl			
7FBF	IN5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC0	IN6CS	Control & Status	*	*	*	*	*	*	in6bsy	in6stl			
7FC1	IN6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC2	IN7CS	Control & Status	*	*	*	*	*	*	in7bsy	in7stl			
7FC3	IN7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC4		(reserved)											
7FC5	OUT0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC6	OUT1CS	Control & Status	*	*	*	*	*	*	out1bsy	out1stl			
7FC7	OUT1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC8	OUT2CS	Control & Status	*	*	*	*	*	*	out2bsy	out2stl			
7FC9	OUT2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FCA	OUT3CS	Control & Status	*	*	*	*	*	*	out3bsy	out3stl			
7FCB	OUT3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FCC	OUT4CS	Control & Status	*	*	*	*	*	*	out4bsy	out4stl			
7FCD	OU4TBC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FCE	OUT5CS	Control & Status	*	*	*	*	*	*	out5bsy	out5stl			
7FCF	OUT5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FD0	OUT6CS	Control & Status	*	*	*	*	*	*	out6bsy	out6stl			
7FD1	OUT6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FD2	OUT7CS	Control & Status	*	*	*	*	*	*	out7bsy	out7stl			
7FD3	OUT7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0			Notes
	Global USB Registers												
7FD4	SUDPTRH	Setup Data Ptr H	A15	A14	A13	A12	A11	A10	A9	A8			
7FD5	SUDPTRL	Setup Data Ptr L	A7	A6	A5	A4	A3	A2	A1	A0			
7FD6	USBCS	USB Control & Status	WakeSRC	*	*	*	DisCon	DiscOE	ReNum	SIGRSUME			Clear b7 by writing "1"
7FD7	TOGCTL	Toggle Control	Q	S	R	IO	0	EP2	EP1	EP0			
7FD8	USBFRAMEL	Frame Number L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0			
7FD9	USBFRAMEH	Frame Number H	0	0	0	0	0	FC10	FC9	FC8			
7FDA		(reserved)											
7FDB	FNADDR	Function Address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0			
7FDC		(reserved)											
7FDD	USBPAIR	Endpoint Control	ISOsend0	*	PR6OUT	PR4OUT	PR2OUT	PR6IN	PR4IN	PR2IN			PRx = 1 to pair EP
7FDE	IN07VAL	Input Endpoint 0-7 valid	IN7VAL	IN6VAL	IN5VAL	IN4VAL	IN3VAL	IN2VAL	IN1VAL	1			VAL =1 means valid
7FDF	OUT07VAL	Output Endpoint 0-7 valid	OUT7VAL	OUT6VAL	OUT5VAL	OUT4VAL	OUT3VAL	OUT2VAL	OUT1VAL	1			VAL =1 means valid
7FE0	INISOVAL	Input EP 8-15 valid	IN15VAL	IN14VAL	IN13VAL	IN12VAL	IN11VAL	IN10VAL	IN9VAL	IN8VAL			VAL =1 means valid
7FE1	OUTISOVAL	Output EP 8-15 valid	OUT15VAL	OUT14VAL	OUT13VAL	OUT12VAL	OUT11VAL	OUT10VAL	OUT9VAL	OUT8VAL			VAL =1 means valid
7FE2	FASTXFR	Fast Transfer Mode	FISO	FBLK	RPOL	RMOD1	RMOD0	WPOL	WMOD1	WMOD0			
7FE3	AUTOPTRH	Auto-Pointer H	A15	A14	A13	A12	A11	A10	A9	A8			
7FE4	AUTOPTRL	Auto-Pointer L	A7	A6	A5	A4	A3	A2	A1	A0			
7FE5	AUTODATA	Auto Pointer Data	D7	D6	D5	D4	D3	D2	D1	D0			
7FE6		(reserved)											
7FE7		(reserved)											
	Setup Data												
7FE8	SETUPDAT	8 bytes of SETUP data	d7	d6	d5	d4	d3	d2	d1	d0			
	Isochronous FIFO Sizes												
7FF0	OUT8ADDR	Endpt 8 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF1	OUT9ADDR	Endpt 9 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF2	OUT10ADDR	Endpt 10 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF3	OUT11ADDR	Endpt 11 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF4	OUT12ADDR	Endpt 12 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF5	OUT13ADDR	Endpt 13 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF6	OUT14ADDR	Endpt 14 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF7	OUT15ADDR	Endpt 15 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF8	IN8ADDR	Endpt 8 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF9	IN9ADDR	Endpt 9 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFA	IN19ADDR	Endpt 10 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFB	IN11ADDR	Endpt 11 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFC	IN12ADDR	Endpt 12 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFD	IN13ADDR	Endpt 13 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFE	IN14ADDR	Endpt 14 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFF	IN15ADDR	Endpt 15 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0			Notes
	Isochronous Byte Counts												
7F70	OUT8BCH	EP8 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F71	OUT8BCL	EP8 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F72	OUT9BCH	EP9 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F73	OUT9BCL	EP9 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F74	OUT10BCH	EP10 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F75	OUT10BCL	EP10 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F76	OUT11BCH	EP11 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F77	OUT11BCL	EP11 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F78	OUT12BCH	EP12 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F79	OUT12BCL	EP12 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F7A	OUT13BCH	EP13 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F7B	OUT13BCL	EP13 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F7C	OUT14BCH	EP14 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F7D	OUT14BCL	EP14 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
7F7E	OUT15BCH	EP15 Out Byte Count H	0	0	0	0	0	0	d9	d8			
7F7F	OUT15BCL	EP15 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0			
		7F80-7F91 (reserved)											
	CPU Registers												
7F92	CPUCS	Control & Status	rv3	rv2	rv1	rv0	0	0	CLK24OE	8051RES			rv[3..0] = chip rev
7F93	PORTACFG	Port A Configuration	RxD1out	RxD0out	FRD	FWR	CS	OE	T1out	T0out			0=port, 1=alt function
7F94	PORTBCFG	Port B Configuration	T2OUT	INT6	INT5	INT4	TxD1	RxD1	T2EX	T2			0=port, 1=alt function
7F95	PORTCCFG	Port C Configuration	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0			0=port, 1=alt function
	Input-Output Port Registers												
7F96	OUTA	Output Register A	OUTA7	OUTA6	OUTA5	OUTA4	OUTA3	OUTA2	OUTA1	OUTA0			
7F97	OUTB	Output Register B	OUTB7	OUTB6	OUTB5	OUTB4	OUTB3	OUTB2	OUTB1	OUTB0			
7F98	OUTC	Output Register C	OUTC7	OUTC6	OUTC5	OUTC4	OUTC3	OUTC2	OUTC1	OUTC0			
7F99	PINSA	Port Pins A	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0			
7F9A	PINSB	Port Pins B	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0			
7F9B	PINSC	Port Pins C	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0			
7F9C	OEA	Output Enable A	OEA7	OEA6	OEA5	OEA4	OEA3	OEA2	OEA1	OEA0			0=off, 1=drive
7F9D	OEB	Output Enable B	OEB7	OEB6	OEB5	OEB4	OEB3	OEB2	OEB1	OEB0			0=off, 1=drive
7F9E	OEC	Output Enable C	OEC7	OEC6	OEC5	OEC4	OEC3	OEC2	OEC1	OEC0			0=off, 1=drive
7F9F	UART230	230Kbaud support	0	0	0	0	0	0	UART1	UART0			1 = 230Kbaud rate
	Isochronous Control/Status Registers												
7FA0	ISOERR	ISO OUT Endpoint Error	ISO15ERR	ISO14ERR	ISO13ERR	ISO12ERR	ISO11ERR	ISO10ERR	ISO9ERR	ISO8ERR			
7FA1	ISOCTL	Isochronous Control	*	*	*	*	PPSTAT	MBZ	MBZ	ISODISAB			"MBZ" = Must Be Zero
7FA2	ZBCOUT	Zero Byte Count bits	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8			
7FA3		(reserved)											
7FA4		(reserved)											
	I^{2}C Registers												
7FA5	I2CS	Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE			
7FA6	I2DAT	Data	d7	d6	d5	d4	d3	d2	d1	d0			
7FA7	I2CMODE	I2C STOP interrupt enable	0	0	0	0	0	0	STOPIE	0			1=Enable INT3 on STOP

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0			Notes
	Interrupts												
7FA8	IVEC	Interrupt Vector	0	IV4	IV3	IV2	IV1	IV0	0	0			
7FA9	IN07IRQ	EPIN Interrupt Request	IN7IR	IN6IR	IN5IR	IN4IR	IN3IR	IN2IR	IN1IR	IN0IR			1=request
7FAA	OUT07IRQ	EPOUT Interrupt Request	OUT7IR	OUT6IR	OUT5IR	OUT4IR	OUT3IR	OUT2IR	OUT1IR	OUT0IR			1=request
7FAB	USBIRQ	USB Interrupt Request	*	*	IBNIR	URESIR	SUSPIR	SUTOKIR	SOFIR	SUDAVIR			1=request
7FAC	IN07IEN	EP0-7IN Int Enables	IN7IEN	IN6IEN	IN5IEN	IN4IEN	IN3IEN	IN2IEN	IN1IEN	IN0IEN			1=enabled
7FAD	OUT07IEN	EP0-7OUT Int Enables	OUT7IEN	OUT6IEN	OUT5IEN	OUT4IEN	OUT3IEN	OUT2IEN	OUT1IEN	OUT0IEN			1=enabled
7FAE	USBIEN	USB Int Enables	*	*	IBNIE	URESIE	SUSPIE	SUTOKIE	SOFIE	SUDAVIE			1=enabled
7FAF	USBBAV	Breakpoint & Autovector	*	*	*	*	BREAK	BPPULSE	BPEN	AVEN			1=enabled
7FB0	IBNIRQ	IBN Interrupt request		EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN			1=request
7FB1	IBNIE	IBN Interrupt Enable		EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN			1=enabled
7FB2	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8			
7FB3	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0			
	Bulk Endpoints 0-7												
7FB4	EP0CS	Control & Status	*	*	*	*	OUTBSY	INBSY	HSNAK	EP0STALL			For EP0IN and EP0OUT
7FB5	IN0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			* this bits are random
7FB6	IN1CS	Control & Status	*	*	*	*	*	*	in1bsy	in1stl			at power-on. Once
7FB7	IN1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			operational, these bits
7FB8	IN2CS	Control & Status	*	*	*	*	*	*	in2bsy	in2stl			read as zeros.
7FB9	IN2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FBA	IN3CS	Control & Status	*	*	*	*	*	*	in3bsy	in3stl			
7FBB	IN3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FBC	IN4CS	Control & Status	*	*	*	*	*	*	in4bsy	in4stl			
7FBD	IN4BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FBE	IN5CS	Control & Status	*	*	*	*	*	*	in5bsy	in5stl			
7FBF	IN5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC0	IN6CS	Control & Status	*	*	*	*	*	*	in6bsy	in6stl			
7FC1	IN6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC2	IN7CS	Control & Status	*	*	*	*	*	*	in7bsy	in7stl			
7FC3	IN7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC4		(reserved)											
7FC5	OUT0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC6	OUT1CS	Control & Status	*	*	*	*	*	*	out1bsy	out1stl			
7FC7	OUT1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FC8	OUT2CS	Control & Status	*	*	*	*	*	*	out2bsy	out2stl			
7FC9	OUT2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FCA	OUT3CS	Control & Status	*	*	*	*	*	*	out3bsy	out3stl			
7FCB	OUT3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FCC	OUT4CS	Control & Status	*	*	*	*	*	*	out4bsy	out4stl			
7FCD	OU4TBC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FCE	OUT5CS	Control & Status	*	*	*	*	*	*	out5bsy	out5stl			
7FCF	OUT5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FD0	OUT6CS	Control & Status	*	*	*	*	*	*	out6bsy	out6stl			
7FD1	OUT6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			
7FD2	OUT7CS	Control & Status	*	*	*	*	*	*	out7bsy	out7stl			
7FD3	OUT7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0			

EZ-USB Registers

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0			Notes
	Global USB Registers												
7FD4	SUDPTRH	Setup Data Ptr H	A15	A14	A13	A12	A11	A10	A9	A8			
7FD5	SUDPTRL	Setup Data Ptr L	A7	A6	A5	A4	A3	A2	A1	A0			
7FD6	USBCS	USB Control & Status	WakeSRC	*	*	*	DisCon	DiscOE	ReNum	SIGRSUME			Clear b7 by writing "1"
7FD7	TOGCTL	Toggle Control	Q	S	R	IO	0	EP2	EP1	EP0			
7FD8	USBFRAMEL	Frame Number L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0			
7FD9	USBFRAMEH	Frame Number H	0	0	0	0	0	FC10	FC9	FC8			
7FDA		(reserved)											
7FDB	FNADDR	Function Address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0			
7FDC		(reserved)											
7FDD	USBPAIR	Endpoint Control	ISOsend0	*	PR6OUT	PR4OUT	PR2OUT	PR6IN	PR4IN	PR2IN			PRx = 1 to pair EP
7FDE	IN07VAL	Input Endpoint 0-7 valid	IN7VAL	IN6VAL	IN5VAL	IN4VAL	IN3VAL	IN2VAL	IN1VAL	1			VAL =1 means valid
7FDF	OUT07VAL	Output Endpoint 0-7 valid	OUT7VAL	OUT6VAL	OUT5VAL	OUT4VAL	OUT3VAL	OUT2VAL	OUT1VAL	1			VAL =1 means valid
7FE0	INISOVAL	Input EP 8-15 valid	IN15VAL	IN14VAL	IN13VAL	IN12VAL	IN11VAL	IN10VAL	IN9VAL	IN8VAL			VAL =1 means valid
7FE1	OUTISOVAL	Output EP 8-15 valid	OUT15VAL	OUT14VAL	OUT13VAL	OUT12VAL	OUT11VAL	OUT10VAL	OUT9VAL	OUT8VAL			VAL =1 means valid
7FE2	FASTXFR	Fast Transfer Mode	FISO	FBLK	RPOL	RMOD1	RMOD0	WPOL	WMOD1	WMOD0			
7FE3	AUTOPTRH	Auto-Pointer H	A15	A14	A13	A12	A11	A10	A9	A8			
7FE4	AUTOPTRL	Auto-Pointer L	A7	A6	A5	A4	A3	A2	A1	A0			
7FE5	AUTODATA	Auto Pointer Data	D7	D6	D5	D4	D3	D2	D1	D0			
7FE6		(reserved)											
7FE7		(reserved)											
	Setup Data												
7FE8	SETUPDAT	8 bytes of SETUP data	d7	d6	d5	d4	d3	d2	d1	d0			
	Isochronous FIFO Sizes												
7FF0	OUT8ADDR	Endpt 8 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF1	OUT9ADDR	Endpt 9 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF2	OUT10ADDR	Endpt 10 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF3	OUT11ADDR	Endpt 11 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF4	OUT12ADDR	Endpt 12 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF5	OUT13ADDR	Endpt 13 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF6	OUT14ADDR	Endpt 14 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF7	OUT15ADDR	Endpt 15 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF8	IN8ADDR	Endpt 8 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FF9	IN9ADDR	Endpt 9 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFA	IN19ADDR	Endpt 10 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFB	IN11ADDR	Endpt 11 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFC	IN12ADDR	Endpt 12 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFD	IN13ADDR	Endpt 13 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFE	IN14ADDR	Endpt 14 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			
7FFF	IN15ADDR	Endpt 15 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0			

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Appendix A: 8051 Introduction

A.1 Introduction

The EZ-USB contains an 8051 core that is binary compatible with the industry standard 8051 instruction set. This appendix provides an overview of the 8051 core features. the topics are:

- New 8051 Features
- Performance Overview
- Software Compatibility
- 803x/805x Feature Comparison
- 8051/DS80C320 Differences

A.2 8051 Features

The 8051 core provides the following design features and enhancements to the standard 8051 micro-controller:

- Compatible with industry standard 803x/805x:
  - Standard 8051 instruction set
  - Two full-duplex serial ports
  - Three timers
- High speed architecture:
  - 4 clocks/instruction cycle
  - 2.5X average improvement in instruction execution time over the standard 8051
  - Runs DC to 25-MHz clock
  - Wasted bus cycles eliminated
  - Dual data pointers
- 256 Bytes internal data RAM
- High-speed external memory interface with 16-bit address bus
- Variable length `MOVX` to access fast/slow RAM peripherals
- Fully static synchronous design
- Supports industry standard compilers, assemblers, emulators, and ROM monitors

A.3 Performance Overview

The 8051 core has been designed to offer increased performance by executing instructions in a 4-clock bus cycle, as opposed to the 12-clock bus cycle in the standard 8051 (see Figure A-1.). The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures.

Some instructions require a different number of instruction cycles on the 8051 core than they do on the standard 8051. In the standard 8051, all instructions except for `MUL` and `DIV` take one or two instruction cycles to complete. In the 8051 core, instructions can take between one and five instruction cycles to complete. The average speed improvement for the entire instruction set is approximately 2.5X, calculated as follows:

Number of Opcodes	Speed Improvement
150	3.0X
51	1.5X
43	2.0X
2	2.4X
Total: 255	Average: 2.5X
Note: Comparison is for 8051 and standard 8051 running at the same clock frequency.	

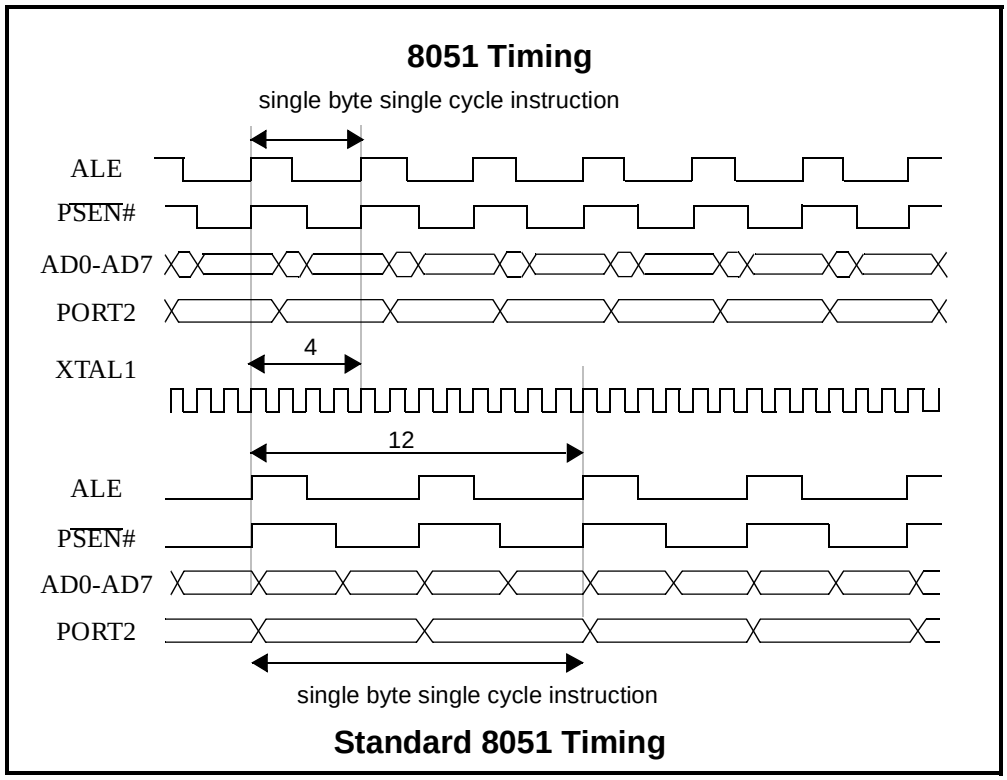

Figure A-1. Comparative Timing of 8051 and Industry Standard 8051

A.4 Software Compatibility

The 8051 core is object code compatible with the industry standard 8051 micro-controller. That is, object code compiled with an industry standard 8051 compiler or assembler will execute on the 8051 core and will be functionally equivalent. However, because the 8051 core uses a different instruction timing than the standard 8051, existing code with timing loops may require modification.

The “Instruction Set” in Table B-2 on page B-5 lists the number of instruction cycles required to perform each instruction on the 8051 core. The 8051 instruction cycle timing and number of instruction cycles required for each instruction are compatible with the Dallas Semiconductor DS80C320.

A.5 803x/805x Feature Comparison

Table A-1. provides a feature-by-feature comparison of the 8051 core and several common 803x/805x configurations.

Table A-1. Feature Summary of 8051 Core and Common 803x/805x Configurations

Feature	Intel				Dallas DS80C320	Anchor 8051
	8031	8051	80C32	80C52		
Clocks per instruction cycle	12	12	12	12	4	4
Program / Data Memory	-	4 KB ROM	-	8 KB ROM	-	8 K RAM
Internal RAM	128 bytes	128 bytes	256 bytes	256 bytes	256 bytes	256 bytes
Data Pointers	1	1	1	1	2	2
Serial Ports	1	1	1	1	2	2
16-bit Timers	2	2	3	3	3	3
Interrupt sources (total of int. and ext.)	5	5	6	6	13	13
Stretch memory cycles	no	no	no	no	yes	yes

A.6 8051 Core/DS80C320 Differences

The 8051 core is similar to the DS80C320 in terms of hardware features and instruction cycle timing. However, there are some important differences between the 8051 core and the DS80C320.

A.6.1 Serial Ports

The 8051 core does not implement serial port framing error detection and does not implement slave address comparison for multiprocessor communications. Therefore, the 8051 core also does not implement the following SFRs: SADDR0, SADDR1, SADEN0, and SADEN1.

A.6.2 Timer 2

The 8051 core does not implement Timer 2 downcounting mode or the downcount enable bit (TMOD2, bit 0). Also, the 8051 core does not implement Timer 2 output enable (T2OE) bit (TMOD2, bit 1). Therefore, the TMOD2 SFR is also not implemented in the 8051 core.

Also, the 8051 core Timer 2 overflow output is active for one clock cycle. In the DS80C320, the Timer 2 overflow output is a square wave with a 50% duty cycle.

A.6.3 Timed Access Protection

The 8051 core does not implement timed access protection and therefore, does not implement the TA SFR.

A.6.4 Watchdog Timer

The EZ-USB/8051 does not implement a watchdog timer.

Appendix B: 8051 Architectural Overview

B.1 Introduction

This appendix provides a technical overview and description of the 8051 core architecture.

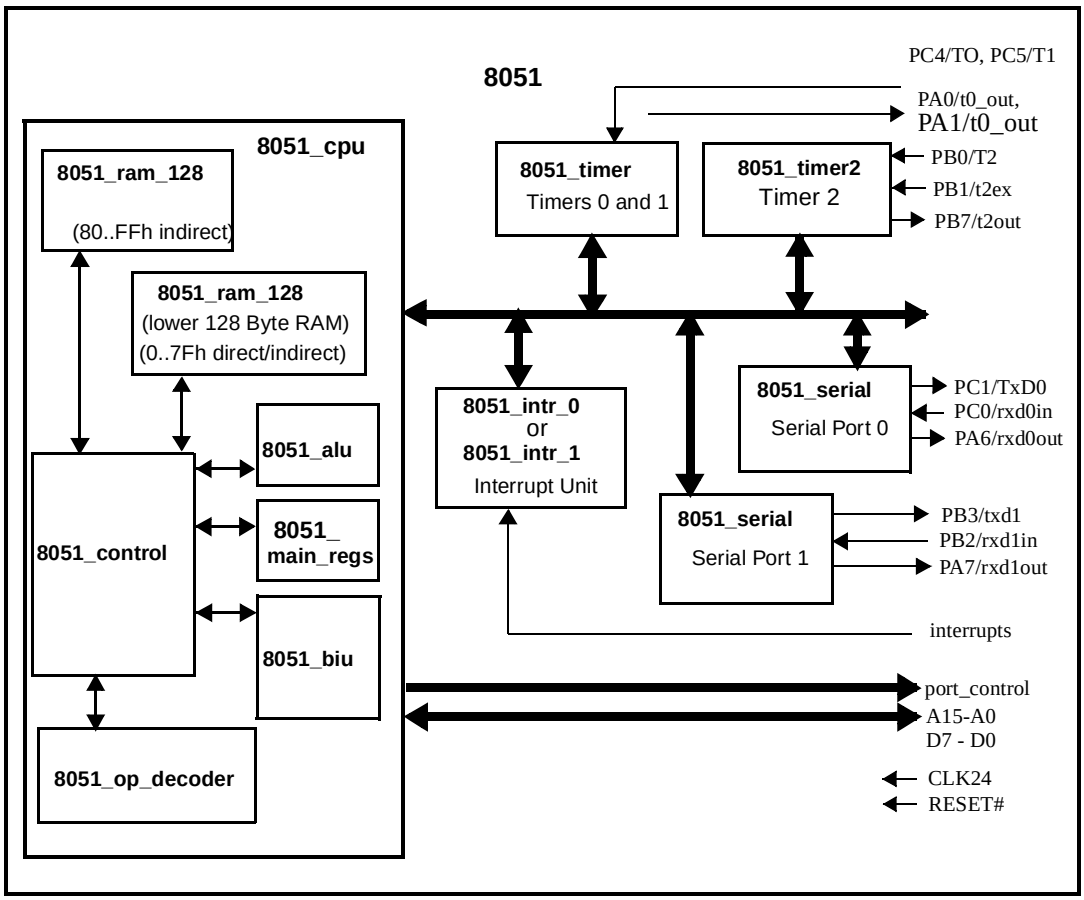

Figure B-1. 8051 Block Diagram

B.1.1 Memory Organization

Memory organization in the 8051 core is similar to that of the industry standard 8051. There are three distinct memory areas: program memory (ROM), data memory (external RAM), and registers (internal RAM).

B.1.1.1 Program Memory

The EZ-USB provides 8K of data that is mapped as both program and data memory at addresses 0x0000-0x1B3F. In addition, the bulk endpoint buffers may be used as external data memory if they are not used as endpoint buffers. See Chapter 3, "EZ-USB Memory" for more details.

B.1.1.2 External RAM

The EZ-USB chip has dedicated address and data pins, so port 2 and port 0 are not used to access the memory bus. As shown in Chapter 3, "EZ-USB Memory", the EZ-USB is expandable to over 100K of external program and data memory.

B.1.1.3 Internal RAM

The internal RAM (Figure B-2) consists of:

- 128 bytes of registers and scratch pad memory accessible through direct or indirect addressing (addresses 00h–7Fh).
- A 128 register space for special function registers (SFRs) accessible through direct addressing (addresses 80h–FFh).
- Upper 128 bytes of scratch pad memory accessible through indirect addressing (addresses 80h–FFh).

Although the SFR space and the upper 128 bytes of RAM share the same address range, the actual address space is separate and is differentiated by the type of addressing. Direct addressing accesses the SFRs, and indirect addressing accesses the upper 128 bytes of RAM.

The lower 128 bytes are organized as shown in Figure B-2. The lower 32 bytes (0x00-0xIF) form four banks of eight registers (R0–R7). Two bits on the program status word (PSW) select which bank is in use. The next 16 bytes (0x20 - 0x2F) form a block of bit-addressable memory space at *bit addresses* 0h-7Fh. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing.

The SFRs occupy addresses 80h–FFh and are only accessible through direct addressing. Most SFRs are reserved for specific functions as described in the “Special Function Registers” on page B-12.

SFR addresses ending in 0h or 8h are bit-addressable.

B.1.2 Instruction Set

All 8051 instructions are binary code compatible and perform the same functions as they do with the industry standard 8051. The effects of these instructions on bits, flags, and other status functions is identical to the industry standard 8051. However, the timing of the instructions is different, both in terms of number of clock cycles per instruction cycle and timing within the instruction cycle.

Figure B-2 lists the 8051 instruction set and the number of instruction cycles required to complete each instruction. Table B-1. defines the symbols and mnemonics used in Table B-2.

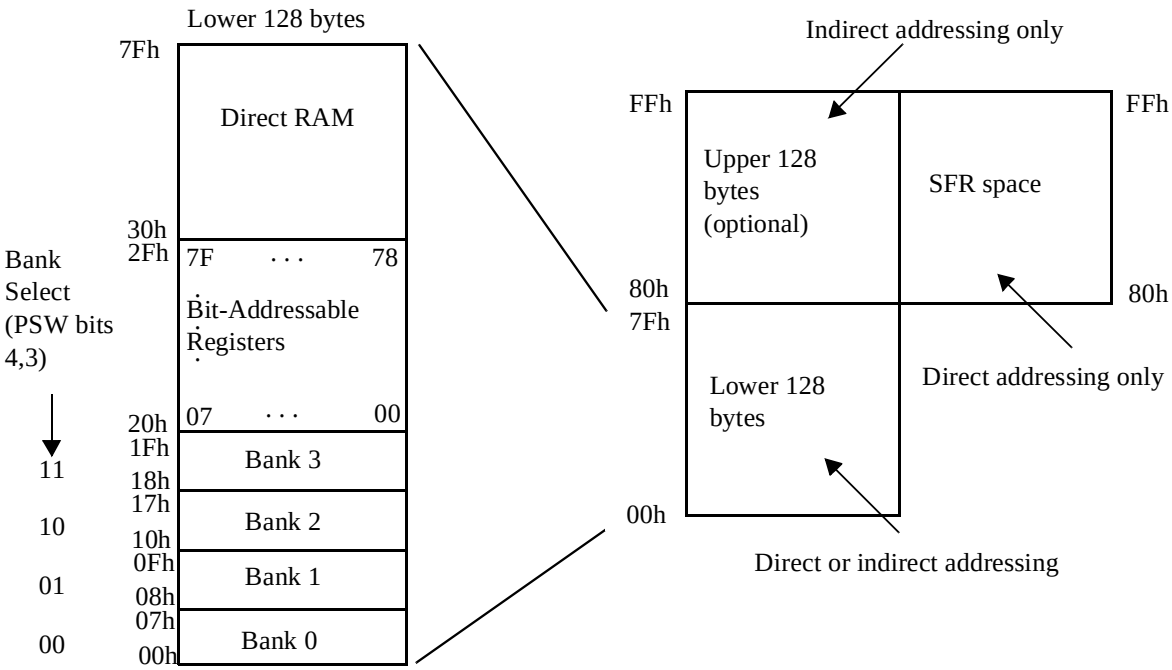

Figure B-2 Internal RAM Organization

Table B-1. Legend for Instruction Set Table

Symbol	Function
A	Accumulator
Rn	Register R7–R0
direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two’s complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

Table B-2. 8051 Instruction Set

Mnemonic	Description	Byte	Instr. Cycles	Hex Code
Arithmetic				
ADD A, Rn	Add register to A	1	1	28-2F
ADD A, direct	Add direct byte to A	2	2	25
ADD A, @Ri	Add data memory to A	1	1	26-27
ADDC A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	1	38-3F
ADDC A, direct	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add data memory to A with carry	1	1	36-37
ADDC A, #data	Add immediate to A with carry	2	2	34
SUBB A, Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A, direct	Subtract direct byte from A with borrow	2	2	95
SUBB A, @Ri	Subtract data memory from A with borrow	1	1	96-97
SUBB A, #data	Subtract immediate from A with borrow	2	2	94
INC A	increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC direct	Increment direct byte	2	2	05
INC @ Ri	Increment data memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement Register	1	1	18-1F
DEC direct	Decrement direct byte	2	2	15
DEC @Ri	Decrement data memory	1	1	16-17
INC DPTR	Increment data pointer	1	3	A3
MUL AB	Multiply A by B	1	5	A4
DIV AB	Divide A by B	1	5	84
DA A	Decimal adjust A	1	1	D4

Table B-2. 8051 Instruction Set

Mnemonic	Description	Byte	Instr. Cycles	Hex Code
Logical				
ANL, Rn	AND register to A	1	1	58-5F
ANL A, direct	AND direct byte to A	2	2	55
ANL A, @Ri	AND data memory to A	1	1	56-57
ANL A, #data	AND immediate to A	2	2	54
ANL direct, A	AND A to direct byte	2	2	52
ANL direct, #data	AND immediate data to direct byte	3	3	53
ORL A, Rn	OR register to A	1	1	48-4F
ORL A, direct	OR direct byte to A	2	2	45
ORL A, @Ri	OR data memory to A	1	1	46-47
ORL A, #data	OR immediate to A	2	2	44
ORL direct, A	OR A to direct byte	2	2	42
ORL direct, #data	OR immediate data to direct byte	3	3	43
XORL A, Rn	Exclusive-OR register to A	1	1	68-6F
XORL A, direct	Exclusive-OR direct byte to A	2	2	65
XORL A, @Ri	Exclusive-OR data memory to A	1	1	66-67
XORL A, #data	Exclusive-OR immediate to A	2	2	64
XORL direct, A	Exclusive-OR A to direct byte	2	2	62
XORL direct, #data	Exclusive-OR immediate data to direct byte	3	3	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap nibbles of a	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RRA	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table B-2. 8051 Instruction Set

Mnemonic	Description	Byte	Instr. Cycles	Hex Code
Data Transfer				
MOV A, Rn	Move register to A	1	1	E8-EF
MOV A, direct	Move direct byte to A	2	2	E5
MOV A, @Ri	Move data memory to A	1	1	E6-E7
MOV A, #data	Move immediate to A	2	2	74
MOV Rn, A	Move A to register	1	1	F8-FF
MOV Rn, direct	Move direct byte to register	2	2	A8-AF
MOV Rn, #data	Move immediate to register	2	2	78-7F
MOV direct, A	Move A to direct byte	2	2	F5
MOV direct, Rn	Move register to direct byte	2	2	88-8F
MOV direct, direct	Move direct byte to direct byte	3	3	85
MOV direct, @Ri	Move data memory to direct byte	2	2	86-87
MOV direct, #data	Move immediate to direct byte	3	3	75
MOV @Ri, A	MOV A to data memory	1	1	F6-F7
MOV @Ri, direct	Move direct byte to data memory	2	2	A6-A7
MOV @Ri, #data	Move immediate to data memory	2	2	76-77
MOV DPTR, #data	Move immediate to data pointer	3	3	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3	93
MOVC A, @A+PC	Move code byte relative PC to A	1	3	83
MOVX A, @Ri	Move external data (A8) to A	1	2-9*	E2-E3
MOVX A, @DPTR	Move external data (A16) to A	1	2-9*	E0
MOVX @Ri, A	Move A to external data (A8)	1	2-9*	F2-F3
MOVX @DPTR, A	Move A to external data (A16)	1	2-9*	F0
PUSH direct	Push direct byte onto stack	2	2	C0
POP direct	Pop direct byte from stack	2	2	D0
XCH A, Rn	Exchange A and register	1	1	C8-CF
XCH A, direct	Exchange A and direct byte	2	2	C5

Table B-2. 8051 Instruction Set

Mnemonic	Description	Byte	Instr. Cycles	Hex Code
XCH A, @Ri	Exchange A and data memory	1	1	C6-C7
XCHD A, @Ri	Exchange A and data memory nibble	1	1	D6-D7
* *Number of cycles is user-selectable. See* "Stretch Memory Cycles (Wait States)" on page B-10.				
Boolean				
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	2	B2
ANL C, bit	AND direct bit to carry	2	2	82
ANL C, /bit	AND direct bit inverse to carry	2	2	B0
ORL C, bit	OR direct bit to carry	2	2	72
ORL C, /bit	OR direct bit inverse to carry	2	2	A0
MOV C, bit	Move direct bit to carry	2	2	A2
MOV bit, C	Move carry to direct bit	2	2	92
Branching				
ACALL addr 11	Absolute call to subroutine	2	3	11-F1
LCALL addr 16	Long call to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	3	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	3	80
JC rel	Jump on carry = 1	2	3	40
JNC rel	Jump on carry = 0	2	3	50
JB bit, rel	Jump on direct bit = 1	3	4	20

Table B-2. 8051 Instruction Set

Mnemonic	Description	Byte	Instr. Cycles	Hex Code
JNB bit, rel	Jump on direct bit = 0	3	4	30
JBC bit, rel	Jump on direct bit = 1 and clear	3	4	10
JMP @ A+DPTR	Jump indirect relative DPTR	1	3	73
JZ rel	Jump on accumulator = 0	2	3	60
JNZ rel	Jump on accumulator /= 0	2	3	70
CJNE A, direct, rel	Compare A, direct JNE relative	3	4	B5
CJNE A, #d, rel	Compare A, immediate JNE relative	3	4	B4
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	4	B8-BF
CJNE @ Ri, #d, rel	Compare Ind, immediate JNE relative	3	4	B6-B7
DJNZ Rn, rel	Decrement register, JNZ relative	2	3	D8-DF
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4	D5
Miscellaneous				
NOP	No operation	1	1	00
There is an additional reserved opcode (A5) that performs the same function as NOP. All mnemonics are copyrighted. Intel Corporation 1980.				

B.1.3 Instruction Timing

Instruction cycles in the 8051 core are 4 clock cycles in length, as opposed to the 12 clock cycles per instruction cycle in the standard 8051. This translates to a 3X improvement in execution time for most instructions.

Some instructions require a different number of instruction cycles on the 8051 core than they do on the standard 8051. In the standard 8051, all instructions except for `MUL` and `DIV` take one or two instruction cycles to complete. In the 8051 core, instructions can take between one and five instruction cycles to complete.

For example, in the standard 8051, the instructions `MOVX A, @DPTR` and `MOV direct, direct` each take 2 instruction cycles (24 clock cycles) to execute. In the 8051 core, `MOVX A, @DPTR` takes two instruction cycles (8 clock cycles) and `MOV direct, direct` takes three instruction cycles (12 clock cycles). Both instructions execute faster on the 8051 core than they do on the standard 8051, but require different numbers of clock cycles.

For timing of real-time events, use the numbers of instruction cycles from Table B-1. to calculate the timing of software loops. The bytes column indicates the number of memory

accesses (bytes) needed to execute the instruction. In most cases, the number of bytes is equal to the number of instruction cycles required to complete the instruction. However, as indicated, there are some instructions (for example, `DIV` and `MUL`) that require a greater number of instruction cycles than memory accesses.

By default, the 8051 core timer/counters run at 12 clock cycles per increment so that timer-based events have the same timing as with the standard 8051. The timers can also be configured to run at 4 clock cycles per increment to take advantage of the higher speed of the 8051 core.

B.1.4 CPU Timing

As previously stated, an 8051 core instruction cycle consists of 4 *CLK24* cycles. Each *CLK24* cycle forms a CPU cycle. Therefore, an instruction cycle consists of 4 CPU cycles: C1, C2, C3, and C4, as illustrated in Figure B-3. Various events occur in each CPU cycle, depending on the type of instruction being executed. The labels C1, C2, C3, and C4 in timing descriptions refer to the 4 CPU cycles within a particular instruction cycle.

The execution for instruction *n* is performed during the fetch of instruction *n*+1. Data writes occur during fetch of instruction *n*+2. The level sensitive interrupts are sampled with the rising edge of *CLK24* at the end of C3.

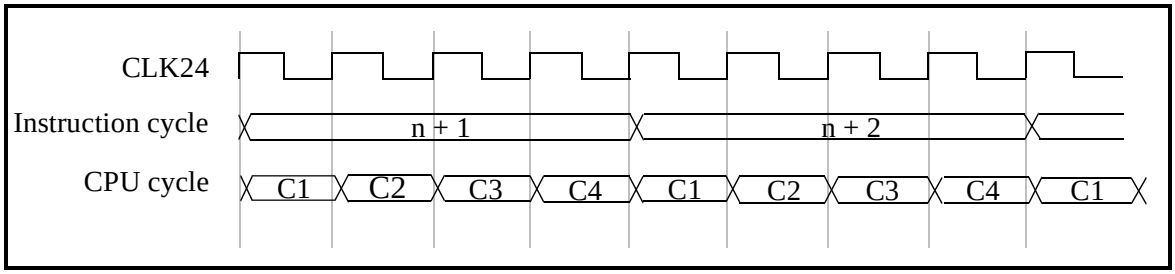

Figure B-3 CPU Timing for Single-Cycle Instruction

B.1.5 Stretch Memory Cycles (Wait States)

The stretch memory cycle feature enables application software to adjust the speed of data memory access. The 8051 core can execute the `MOVX` instruction in as few as 2 instruction cycles. However, it is sometimes desirable to stretch this value; for example to access slow memory or slow memory-mapped peripherals such as UARTs or LCDs.

The three LSBs of the Clock Control Register (at SFR location 8Eh) control the stretch value. You can use stretch values between zero and seven. A stretch value of zero adds zero instruction cycles, resulting in `MOVX` instructions executing in two instruction cycles. A stretch value of seven adds seven instruction cycles, resulting in `MOVX` instructions executing in nine instruction cycles. The stretch value can be changed dynamically under program control.

By default, the stretch value resets to one (three cycle MOVX). For full-speed data memory access, the software must set the stretch value to zero. The stretch value affects only data memory access (not program memory).

The stretch value affects the width of the read/write strobe and all related timing. Using a higher stretch value results in a wider read/write strobe, which allows the memory or peripheral more time to respond.

Table B-3. lists the data memory access speeds for stretch values zero through seven. MD2–0 are the three LSBs of the Clock Control Register (CKCON.2–0).

Table B-3. Data Memory Stretch Values

MD2	MD1	MD0	Memory Cycles	Read/Write Strobe Width (Clocks)	Strobe Width @ 24MHz
0	0	0	2	2	83.3 ns
0	0	1	3 (default)	4	166.7 ns
0	1	0	4	8	333.3 ns
0	1	1	5	12	500 ns
1	0	0	6	16	666.7 ns
1	0	1	7	20	833.3 ns
1	1	0	8	24	1000 ns
1	1	1	9	28	1166.7 ns

B.1.6 Dual Data Pointers

The 8051core employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external data RAM or peripherals. The 8051 maintains the standard data pointer as DPTR0 at SFR locations 82h (DPL0) and 83h (DPH0). It is not necessary to modify existing code to use DPTR0.

The 8051 core adds a second data pointer (DPTR1) at SFR locations 84h (DPL1) and 85h (DPH1). The SEL bit in the DPTR Select register, DPS (SFR 86h), selects the active pointer. When SEL = 0, instructions that use the DPTR will use DPL0 and DPH0. When SEL = 1, instructions that use the DPTR will use DPL1 and DPH1. SEL is the bit 0 of SFR location 86h. No other bits of SFR location 86h are used.

All DPTR-related instructions use the currently selected data pointer. To switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (`INC DPS`). This requires only one instruction to switch from a source address to a destination address, saving application code from having to save source and destination addresses when doing a block move.

Using dual data pointers provides significantly increased efficiency when moving large blocks of data.

The SFR locations related to the dual data pointers are:

82h	DPL0	DPTR0 low byte
83h	DPH0	DPTR0 high byte
84h	DPL1	DPTR1 low byte
85h	DPH1	DPTR1 high byte
86h	DPS	DPTR Select (Bit 0)

B.1.7 Special Function Registers

The Special Function Registers (SFRs) control several of the features of the 8051. Most of the 8051 core SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control features that are not available in the standard 8051.

Table B-4. lists the 8051 core SFRs and indicates which SFRs are not included in the standard 8051 SFR space.

In Table B-5., SFR bit positions that contain a 0 or a 1 cannot be written to and, when read, always return the value shown (0 or 1). SFR bit positions that contain "-" are available but not used. Table B-5. lists the reset values for the SFRs.

The following SFRs are related to CPU operation and program execution:

81h	SP	Stack Pointer
D0h	PSW	Program Status Word ()
E0h	ACC	Accumulator Register
F0h	B	B Register

Table B-6. lists the functions of the bits in the PSW SFR. Detailed descriptions of the remaining SFRs appear with the associated hardware descriptions in Appendix C of this databook.

Table B-4. Special Function Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
SP									81h
DPL0									82h
DPH0									83h
DPL1[1]									84h
DPH1[1]									85h
DPS[1]	0	0	0	0	0	0	0	SEL	86h
PCON	SMOD0	-	1	1	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/T	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON[1]	-	-	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
SPC_FNC[1]	0	0	0	0	0	0	0	WRS	8Fh
EXIF[1]	IE5	IE4	I2CINT	USBINT	1	0	0	0	91h
MPAGE[1]									92h
SCON0	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
IP	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SCON1[1]	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	C0h
SBUF1[1]									C1h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh

Table B-4. Special Function Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
EICON(1)	SMOD1	1	ERESI	RESI	INT6	0	0	0	D8h
ACC									E0H
EIE(1)	1	1	1	EWDI	EX5	EX4	EI2C	EUSB	E8h
B									F0h
EIP(1)	1	1	1	PX6	PX5	PX4	PI2C	PUSB	F8h
(1) Not part of standard 8051 architecture.									

Table B-5. Special Function Register Reset Values

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
SP	0	0	0	0	0	1	1	1	81h
DPL0	0	0	0	0	0	0	0	0	82h
DPH0	0	0	0	0	0	0	0	0	83h
DPL1(1)	0	0	0	0	0	0	0	0	84h
DPH1(1)	0	0	0	0	0	0	0	0	85h
DPS(1)	0	0	0	0	0	0	0	0	86h
PCON	0	0	1	1	0	0	0	0	87h
TCON	0	0	0	0	0	0	0	0	88h
TMOD	0	0	0	0	0	0	0	0	89h
TL0	0	0	0	0	0	0	0	0	8Ah
TL1	0	0	0	0	0	0	0	0	8Bh
TH0	0	0	0	0	0	0	0	0	8Ch
TH1	0	0	0	0	0	0	0	0	8Dh
CKCON(1)	0	0	0	0	0	0	0	1	8Eh
SPC_FNC(1)	0	0	0	0	0	0	0	0	8Fh
EXIF(1)	0	0	0	0	1	0	0	0	91h

Table B-5. Special Function Register Reset Values

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
MPAGE[1]	0	0	0	0	0	0	0	0	92h
SCON0	0	0	0	0	0	0	0	0	98h
SBUF0	0	0	0	0	0	0	0	0	99h
IE	0	0	0	0	0	0	0	0	A8h
IP	1	0	0	0	0	0	0	0	B8h
SCON1[1]	0	0	0	0	0	0	0	0	C0h
SBUF1[1]	0	0	0	0	0	0	0	0	C1h
T2CON	0	0	0	0	0	0	0	0	C8h
RCAP2L	0	0	0	0	0	0	0	0	CAh
RCAP2H	0	0	0	0	0	0	0	0	CBh
TL2	0	0	0	0	0	0	0	0	CCh
TH2	0	0	0	0	0	0	0	0	CDh
PSW	0	0	0	0	0	0	0	0	D0h
EICON[1]	0	1	0	0	0	0	0	0	D8h
ACC	0	0	0	0	0	0	0	0	E0H
EIE[1]	1	1	1	0	0	0	0	0	E8h
B	0	0	0	0	0	0	0	0	F0h
EIP[1]	1	1	1	0	0	0	0	0	F8h

[1] Not part of standard 8051 architecture.

Table B-6. PSW Register - SFR D0h

Bit	Function
PSW.7	CY - Carry flag. This is the **unsigned** carry bit. The CY flag is set when an arithmetic operation results in a carry from bit 7 to bit 8, and cleared otherwise. In other words, it acts as a virtual bit 8. The CY flag is cleared on multiplication and division.
PSW.6	AC - Auxiliary carry flag. Set to 1 when the last arithmetic operation resulted in a carry into (during addition) or borrow from (during subtraction) the high order nibble, otherwise cleared to 0 by all arithmetic operations.
PSW.5	F0 - User flag 0. Bit-addressable, general purpose flag for software control.
PSW.4	RS1 - Register bank select bit 1. used with RS0 to select a register bank in internal RAM.
PSW.3	RS0 - Register bank select bit 0, decoded as: **RS1 RS0 Banks Selected** 0 0 Register bank 0, addresses 00h-07h 0 1 Register bank 1, addresses 08h-0Fh 1 0 Register bank 2, addresses 10h-17h 1 1 Register bank 3, addresses 18h-1Fh
PSW.2	OV - Overflow flag. This is the **signed** carry bit. The OV flag is set when a positive sum exceeds 7fh, or a negative sum (in two's compliment notation) exceeds 80h. On a multiply, if OV = 1, the result of the multiply is greater than FFh. On a divide, OV = 1 on a divide by 0.
PSW.1	F1 - User flag 1. Bit-addressable, general purpose flag for software control.
PSW.0	P - Parity flag. Set to 1 when the modulo-2 sum of the 8 bits in the accumulator is 1 (odd parity), cleared to 0 on even parity.

Appendix C: 8051 Hardware Description

C.1 Introduction

This chapter provides technical data about the 8051 core hardware operation and timing. The topics are:

- Timers/Counters
- Serial Interface
- Interrupts
- Reset
- Power Saving Modes

C.2 Timers/Counters

The 8051 core includes three timer/counters (Timer 0, Timer 1, and Timer 2). Each timer/counter can operate as either a timer with a clock rate based on the *CLK24* pin, or as an event counter clocked by the *T0* pin (Timer 0), *T1* pin (Timer 1), or the *T2* pin (Timer 2).

Each timer/counter consists of a 16-bit register that is accessible to software as two SFRs:

- Timer 0 - TL0 and TH0
- Timer 1 - TL1 and TH1
- Timer 2 - TL2 and TH2

C.2.1 803x/805x Compatibility

The implementation of the timers/counters is similar to that of the Dallas Semiconductor DS80C320. Table C-1. summarizes the differences in timer/counter implementation between the Intel 8051, the Dallas Semiconductor DS80C320, and the 8051 core.

Table C-1. Timer/Counter Implementation Comparison

Feature	Intel 8051	Dallas DS80C320	8051
Number of timers	2	3	3
Timer 0/1 overflow available as output signals	not implemented	not implemented	T0OUT, T1OUT (one CLK24 pulse)
Timer 2 output enable	n/a	implemented	not implemented
Timer 2 downcount enable	n/a	implemented	not implemented
Timer 2 overflow available as output signal	n/a	implemented	T2OUT (one CLK24 pulse)

C.2.2 Timers 0 and 1

Timers 0 and 1 each operate in four modes, as controlled through the TMOD SFR (Table C-2.) and the TCON SFR (Table C-3.). The four modes are:

- 13-bit timer/counter (mode 0)
- 16-bit timer/counter (mode 1)
- 8-bit counter with auto-reload (mode 2)
- Two 8-bit counters (mode 3, Timer 0 only)

C.2.3 Mode 0

Mode 0 operation, illustrated in Figure C-1., is the same for Timer 0 and Timer 1. In mode 0, the timer is configured as a 13-bit counter that uses bits 0-4 of TL0 (or TL1) and all 8 bits of TH0 (or TH1). The timer enable bit (TR0/TR1) in the TCON SFR starts the timer. The C/$\overline{T}$ bit selects the timer/counter clock source, CLK24 or the T0/T1 pins.

The timer counts transitions from the selected source as long as the GATE bit is 0, or the GATE bit is 1 and the corresponding interrupt pin (INT0# or INT1#) is 1.

When the 13-bit count increments from 1FFFh (all ones), the counter rolls over to all zeros, the TF0 (or TF1) bit is set in the TCON SFR, and the T0OUT (or T1OUT) pin goes high for one clock cycle.

The upper 3 bits of TL0 (or TL1) are indeterminate in mode 0 and must be masked when the software evaluates the register.

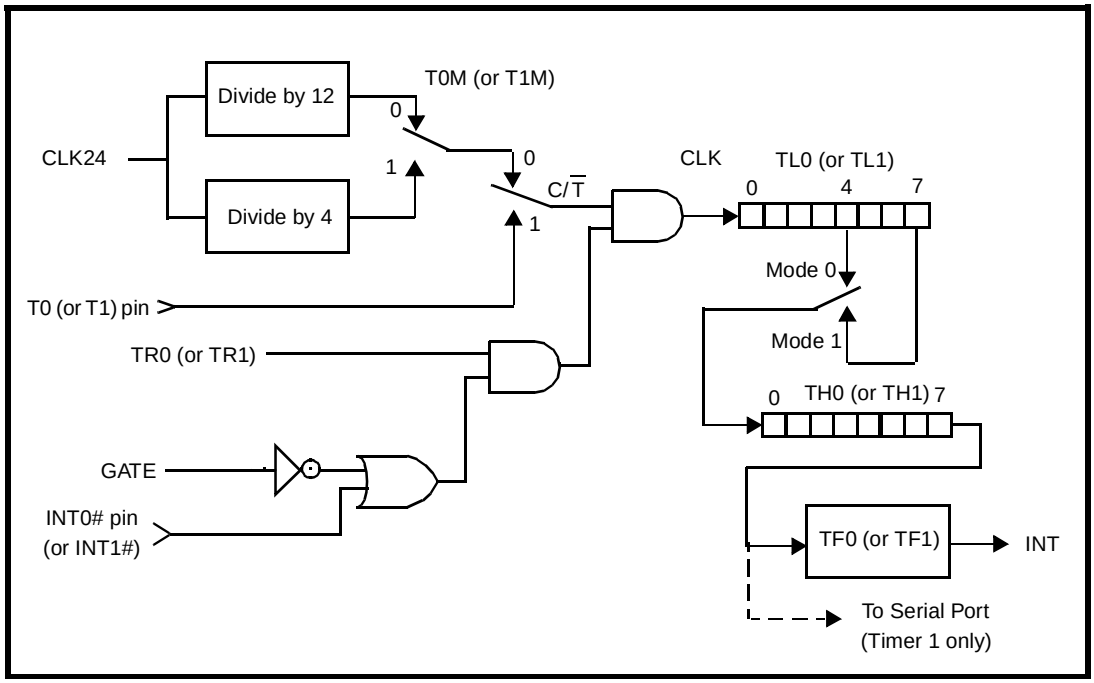

Figure C-1. Timer 0/1 - Modes 0 and 1

C.2.4 Mode 1

Mode 1 operation is the same for Timer 0 and Timer 1. In mode 1, the timer is configured as a 16-bit counter. As illustrated in Figure C-1., all 8 bits of the LSB register (TL0 or TL1) are used. The counter rolls over to all zeros when the count increments from FFFFh. Otherwise, mode 1 operation is the same as mode 0.

Table C-2. TMOD Register - SFR 89h

Bit	Function
TMOD.7	GATE - Timer 1 gate control. When GATE = 1, Timer 1 will clock only when INT1# = 1 and TR1 (TCON.6) = 1. When GATE = 0, Timer 1 will clock only when TR1 = 1, regardless of the state of INT1#.
TMOD.6	$C/\overline{T}$ - Counter/Timer select. When $C/\overline{T}$ = 0, Timer 1 is clocked by CLK24/4 or CLK24/12, depending on the state of T1M (CKCON.4). When $C/\overline{T}$ = 1, Timer 1 is clocked by the T1 pin.
TMOD.5	M1 - Timer 1 mode select bit 1.
TMOD.4	M0 - Timer 1 mode select bit 0, decoded as: **M1 M0 Mode** 0 0 Mode 0 : 13-bit counter 0 1 Mode 1 : 16-bit counter 1 0 Mode 2 : 8-bit counter with auto-reload 1 1 Mode 3 : Timer 1 stopped
TMOD.3	GATE - Timer 0 gate control, When GATE = 1, Timer 0 will clock only when INT0 = 1 and TR0 (TCON.4) = 1. When GATE = 0, Timer 0 will clock only when TR0 = 1, regardless of the state of INT0.
TMOD.2	$C/\overline{T}$ - Counter/Timer select. When $C/\overline{T}$ = 0, Timer 0 is clocked by CLK24/4 or CLK24/12, depending on the state of T0M (CKCON.3). When $C/\overline{T}$ = 1, Timer 0 is clocked by the T0 pin.
TMOD.1	M1 - Timer 0 mode select bit 1.
TMOD.0	M0 - Timer 0 mode select bit 0, decoded as: **M1 M0 Mode** 0 0 Mode 0 : 13-bit counter 0 1 Mode 1 : 16-bit counter 1 0 Mode 2 : 8-bit counter with auto-reload 1 1 Mode 3 : Two 8-bit counters

Table C-3. TCON Register - SRF 88h

Bit	Function
TCON.7	TF1 - Timer 1 overflow flag. Set to 1 when the Timer 1 count overflows and cleared when the processor vectors to the interrupt service routine.
TCON.6	TR1 - Timer 1 run control. Set to 1 to enable counting on Timer 1.
TCON.5	TF0 - Timer 0 overflow flag. Set to 1 when the Timer 0 count overflows and cleared when the processor vectors to the interrupt service routine.
TCON.4	TR0 - Timer 0 run control. Set to 1 to enable counting on Timer 0.
TCON.3	IE1 - Interrupt 1 edge detect. If external interrupt 1 is configured to be edge-sensitive (IT1 = 1), IE1 is set by hardware when a negative edge is detected on the INT1 pin and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In this case, IE1 can also be cleared by software. If external interrupt 1 is configured to be level-sensitive (IT1 = 0), IE1 is set when the INT1# pin is 0 and cleared when the INT1# pin is 1. In level-sensitive mode, software cannot write to IE1.
TCON.2	IT1 - Interrupt 1 type select. INT1 is detected on falling edge when IT1 = 1; INT1 is detected as a low level when IT1 = 0.
TCON.1	IE0 - Interrupt 0 edge detect. If external interrupt 0 is configured to be edge-sensitive (IT0 = 1), IE0 is set by hardware when a negative edge is detected on the INT0 pin and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In this case, IE0 can also be cleared by software. If external interrupt 0 is configured to be level-sensitive (IT0 = 0), IE0 is set when the INT0# pin is 0 and cleared when the INT0# pin is 1. In level-sensitive mode, software cannot write to IE0.
TCON.0	IT0 - Interrupt 0 type select. INT0 is detected on falling edge when IT0 = 1; INT0 is detected as a low level when IT0 = 0.

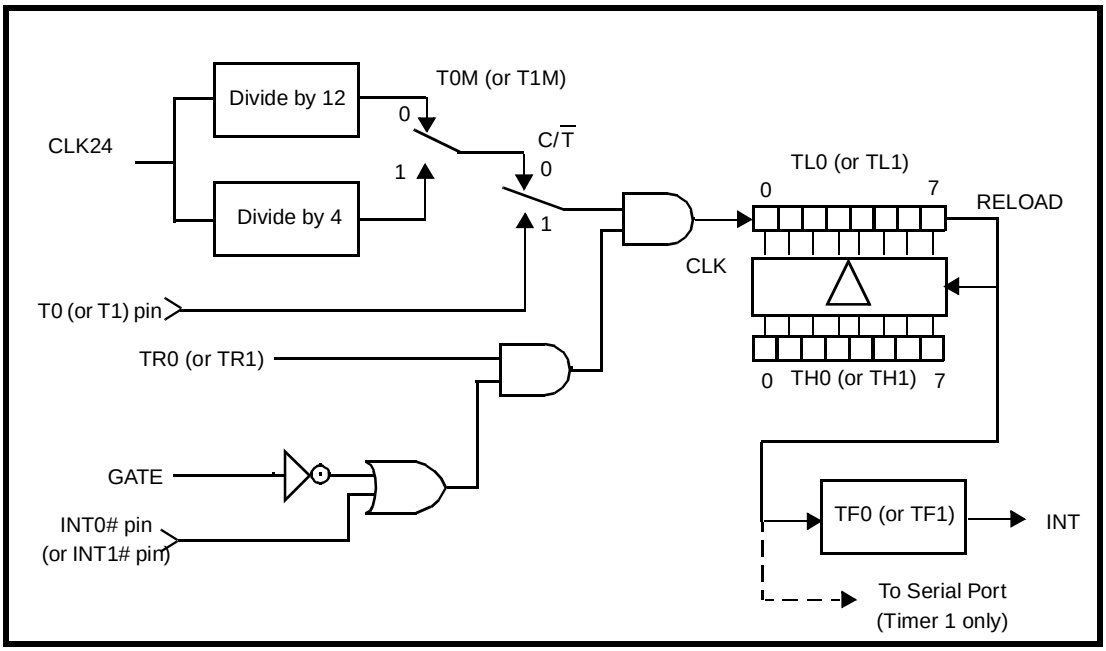

Figure C-2. Timer 0/1 - Mode 2

C.2.5 Mode 2

Mode 2 operation is the same for Timer 0 and Timer 1. In mode 2, the timer is configured as an 8-bit counter, with automatic reload of the start value. The LSB register (TL0 or TL1) is the counter and the MSB register (TH0 or TH1) stores the reload value.

As illustrated in Figure C-2., mode 2 counter control is the same as for mode 0 and mode 1. However, in mode 2, when TL*n* increments from FFh, the value stored in TH*n* is reloaded into TL*n*.

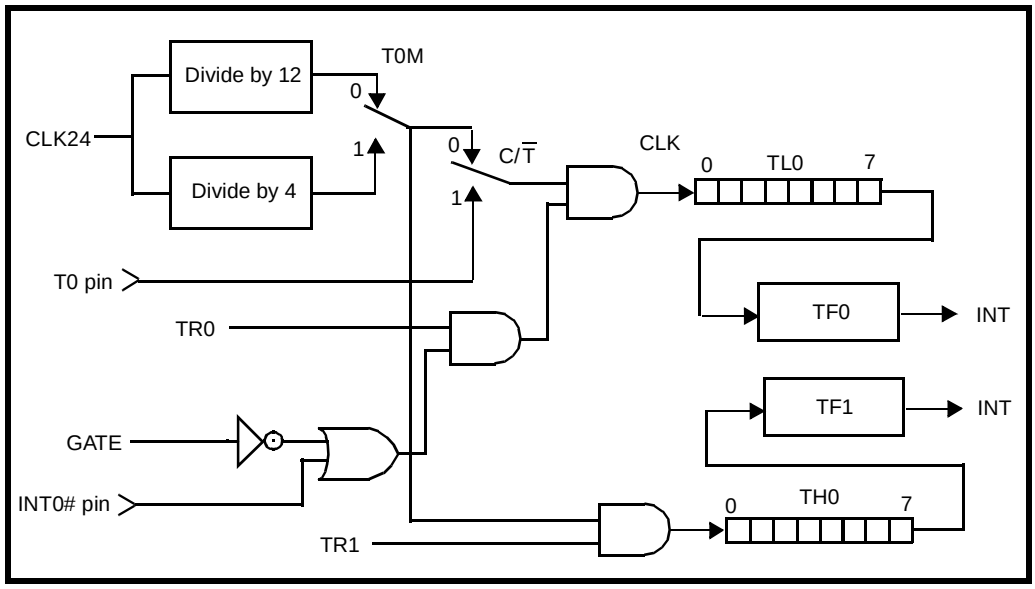

Figure C-3. Timer 0 - Mode 3

C.2.6 Mode 3

In mode 3, Timer 0 operates as two 8-bit counters and Timer 1 stops counting and holds its value.

As shown in Figure C-3., TL0 is configured as an 8-bit counter controlled by the normal Timer 0 control bits. TL0 can either count CLK24 cycles (divided by 4 or by 12) or high-to-low transitions on *T0*, as determined by the C/$\overline{T}$ bit. The GATE function can be used to give counter enable control to the INT0# pin.

TH0 functions as an independent 8-bit counter. However, TH0 can only count CLK24 cycles (divided by 4 or by 12). The Timer 1 control and flag bits (TR1 and TF1) are used as the control and flag bits for TH0.

When Timer 0 is in mode 3, Timer 1 has limited usage because Timer 0 uses the Timer 1 control bit (TR1) and interrupt flag (TF1). Timer 1 can still be used for baud rate generation and the Timer 1 count values are still available in the TL1 and TH1 registers.

Control of Timer 1 when Timer 0 is in mode 3 is through the Timer 1 mode bits. To turn Timer 1 on, set Timer 1 to mode 0, 1, or 2. To turn Timer 1 off, set it to mode 3. The Timer 1 C/$\overline{T}$ bit and T1M bit are still available to Timer 1. Therefore, Timer 1 can count CLK24/4, CLK24/12, or high-to-low transitions on the T1 pin. The Timer 1 GATE function is also available when Timer 0 is in mode 3.

C.2.7 Timer Rate Control

The default timer clock scheme for the 8051 timers is 12 CLK24 cycles per increment, the same as in the standard 8051. However, in the 8051, the instruction cycle is 4 CLK24 cycles.

Using the default rate (12 clocks per timer increment) allows existing application code with real-time dependencies, such as baud rate, to operate properly. However, applications that require fast timing can set the timers to increment every 4 CLK24 cycles by setting bits in the Clock Control register (CKCON) at SFR location 8Eh (see Table C-4.).

The CKCON bits that control the timer clock rates are:

CKCON Bit	Counter/Timer
5	Timer 2
4	Timer 1
3	Timer 0

When a CKCON register bit is set to 1, the associated counter increments at 4-CLK24 intervals. When a CKCON bit is cleared, the associated counter increments at 12-CLK24 intervals. The timer controls are independent of each other. The default setting for all three timers is 0 (12-CLK24 intervals). These bits have no effect in counter mode.

Table C-4. CKCON Register - SRF 8Eh

Bit	Function
CKCON.7,6	Reserved
CKCON.5	T2M - Timer 2 clock select. When T2M = 0, Timer 2 uses CLK24/12 (for compatibility with 80C32); when T2M = 1, Timer 2 uses CLK24/4. This bit has no effect when Timer 2 is configured for baud rate generation.
CKCON.4	T1M - Timer 1 clock select. When T1M = 0, Timer 1 uses CLK24/12 (for compatibility with 80C32); when T1M = 1, Timer 1 uses CLK24/4.
CKCON.3	T0M - Timer 0 clock select. When T0M = 0, Timer 0 uses CLK24/12 (for compatibility with 80C32); when T0M = 1, Timer 0 uses CLK24/4.
CKCON.2-0	MD2, MD1, MD0 - Control the number of cycles to be used for external MOVX instructions.

C.2.8 Timer 2

Timer 2 runs only in 16-bit mode and offers several capabilities not available with Timers 0 and 1. The modes available with Timer 2 are:

- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter
- Baud rate generator

The SFRs associated with Timer 2 are:

- T2CON - SFR C8h (Table C-6.)
- RCAP2L - SFR CAh - Used to capture the TL2 value when Timer 2 is configured for capture mode, or as the LSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.
- RCAP2H - SFR CBh - Used to capture the TH2 value when Timer 2 is configured for capture mode, or as the MSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.
- TL2 - SFR CCh - Lower 8 bits of the 16-bit count.
- TH2 - SFR CDh - Upper 8 bits of the 16-bit count.

C.2.8.1 Timer 2 Mode Control

Table C-5. summarizes how the SFR bits determine the Timer 2 mode.

Table C-5. Timer 2 Mode Control Summary

RCLK	TCLK	CP/$\overline{\text{RL2}}$	TR2	Mode
0	0	1	1	16-bit timer/counter with capture
0	0	0	1	16-bit timer/counter with auto-reload
1	X	X	1	Baud rate generator
X	1	X	1	Baud rate generator
X	X	X	0	Off
X = Don’t care.				

C.2.8.2 16-Bit Timer/Counter Mode

Figure C-4. illustrates how Timer 2 operates in timer/counter mode with the optional capture feature. The C/$\overline{T2}$ bit determines whether the 16-bit counter counts CLK24 cycles (divided by 4 or 12), or high-to-low transitions on the T2 pin. The TR2 bit enables the counter. When the count increments from FFFFh, the TF2 flag is set, and the T2OUT pin goes high for one CLK24 cycle.

Table C-6. T2CON Register - SFR C8h

Bit	Function
T2CON.7	TF2 - Timer 2 overflow flag. Hardware will set TF2 when the Timer 2 overflows from FFFFh. TF2 must be cleared to 0 by the software. TF2 will only be set to a 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
T2CON.6	EXF2 - Timer 2 external flag. Hardware will set EXF2 when a reload or capture is caused by a high-to-low transition on the T2EX pin, and EXEN2 is set. EXF2 must be cleared to 0 by the software. Writing a 1 to EXF2 forces a Timer 2 interrupt if enabled.
T2CON.5	RCLK - Receive clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of received data in serial mode 1 or 3. RCLK =1 selects Timer 2 overflow as the receive clock. RCLK =0 selects Timer 1 overflow as the receive clock.
T2CON.4	TCLK - Transmit clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of transmit data in serial mode 1 or 3. RCLK =1 selects Timer 2 overflow as the transmit clock. RCLK =0 selects Timer 1 overflow as the transmit clock.
T2CON.3	EXEN2 - Timer 2 external enable. EXEN2 = 1 enables capture or reload to occur as a result of a high-to-low transition on the T2EX pin, if Timer 2 is not generating baud rates for the serial port. EXEN2 = 0 causes Timer 2 to ignore all external events on the T2EX pin.
T2CON.2	TR2 - Timer 2 run control flag. TR2 = 1 starts Timer 2. TR2 = 0 stops Timer 2.
T2CON.1	C/$\overline{T2}$ - Counter/timer select. C/$\overline{T2}$ = 0 selects a timer function for Timer 2. C/$\overline{T2}$ = 1 selects a counter of falling transitions on the T2 pin. When used as a timer, Timer 2 runs at 4 clocks per tick or 12 clocks per tick as programmed by CKCON.5, in all modes except baud rate generator mode. When used in baud rate generator mode, Timer 2 runs at 2 clocks per tick, independent of the state of CKCON.5.

Table C-6. T2CON Register - SFR C8h

Bit	Function
T2CON.0	CP/$\overline{RL2}$ - Capture/reload flag. When CP/$\overline{RL2}$ = 1, Timer 2 captures occur on high-to-low transitions of the T2EX pin, if EXEN2 = 1. When CP/$\overline{RL2}$ = 0, auto-reloads occur when Timer 2 overflows or when high-to-low transitions occur on the T2EX pin, if EXEN2 = 1. If either RCLK or TCLK is set to 1, CP/$\overline{RL2}$ will not function and Timer 2 will operate in auto-reload mode following each overflow.

C.2.8.3 6-Bit Timer/Counter Mode with Capture

The Timer 2 capture mode (Figure C-4.) is the same as the 16-bit timer/counter mode, with the addition of the capture registers and control signals.

The CP/$\overline{RL2}$ bit in the T2CON SFR enables the capture feature. When CP/$\overline{RL2}$ = 1, a high-to-low transition on the T2EX pin when EXEN2 = 1 causes the Timer 2 value to be loaded into the capture registers RCAP2L and RCAP2H.

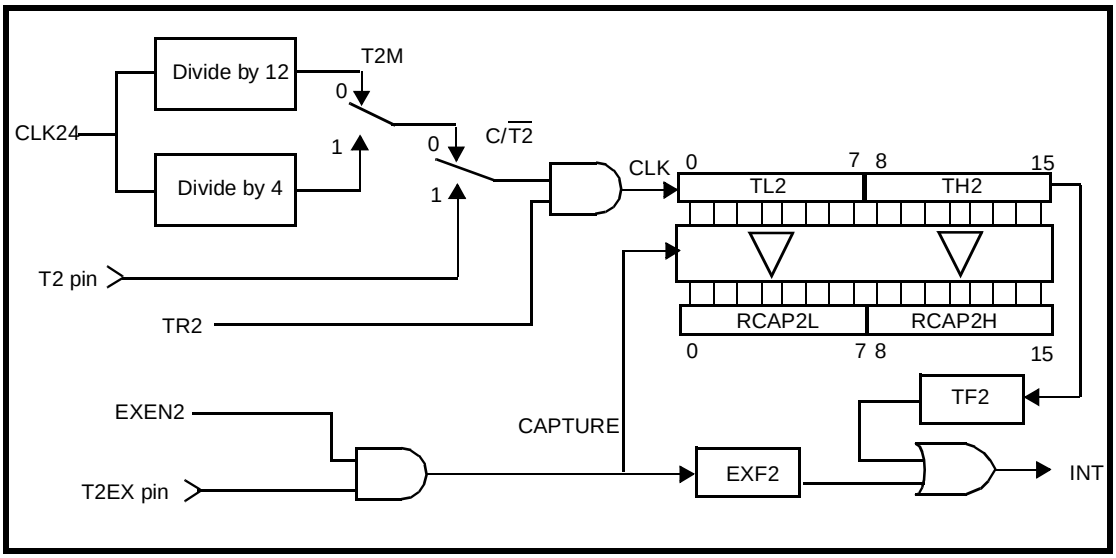

Figure C-4. Timer 2 - Timer/Counter with Capture

C.2.8.4 16-Bit Timer/Counter Mode with Auto-Reload

When CP/$\overline{RL2}$ = 0, Timer 2 is configured for the auto-reload mode illustrated in Figure C-5.. Control of counter input is the same as for the other 16-bit counter modes. When the count increments from FFFFh, Timer 2 sets the TF2 flag and the starting value is reloaded into TL2 and TH2. The software must preload the starting value into the RCAP2L and RCAP2H registers.

When Timer 2 is in auto-reload mode, a reload can be forced by a high-to-low transition on the T2EX pin, if enabled by EXEN2 = 1.

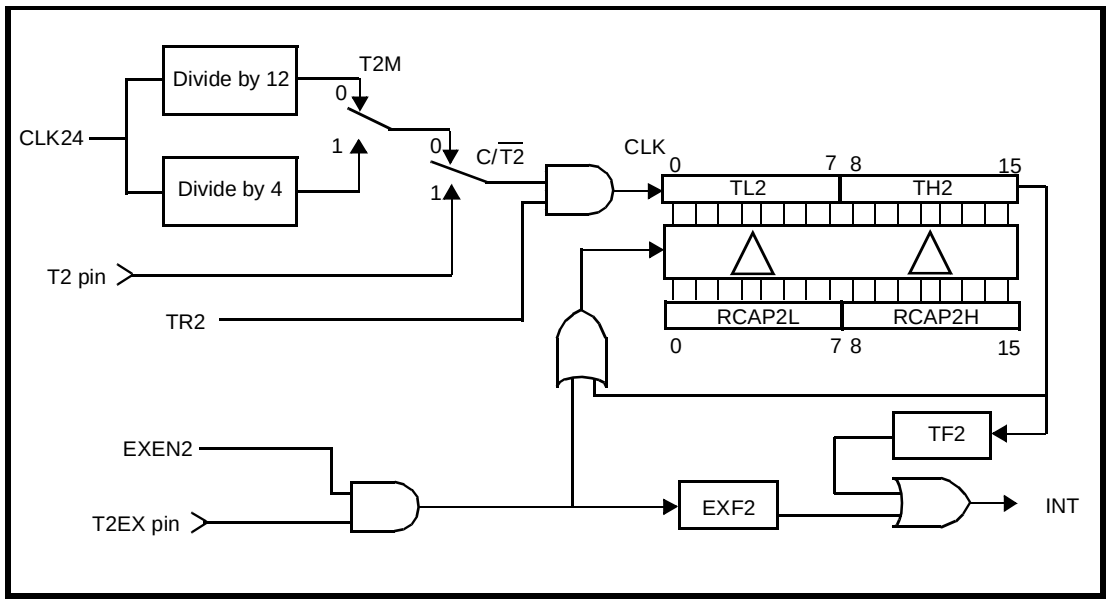

Figure C-5. Timer 2 - Timer/Counter with Auto Reload

C.2.8.5 Baud Rate Generator Mode

Setting either RCLK or TCLK to 1 configures Timer 2 to generate baud rates for Serial Port 0 in serial mode 1 or 3. In baud rate generator mode, Timer 2 functions in auto-reload mode. However, instead of setting the TF2 flag, the counter overflow is used to generate a shift clock for the serial port function. As in normal auto-reload mode, the overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers.

When either TCLK = 1 or RCLK = 1, Timer 2 is forced into auto-reload operation, regardless of the state of the CP/$\overline{RL2}$ bit.

When operating as a baud rate generator, Timer 2 does not set the TF2 bit. In this mode, a Timer 2 interrupt can only be generated by a high-to-low transition on the T2EX pin setting the EXF2 bit, and only if enabled by EXEN2 = 1.

The counter time base in baud rate generator mode is CLK24/2. To use an external clock source, set C/$\overline{T2}$ to 1 and apply the desired clock source to the T2 pin.

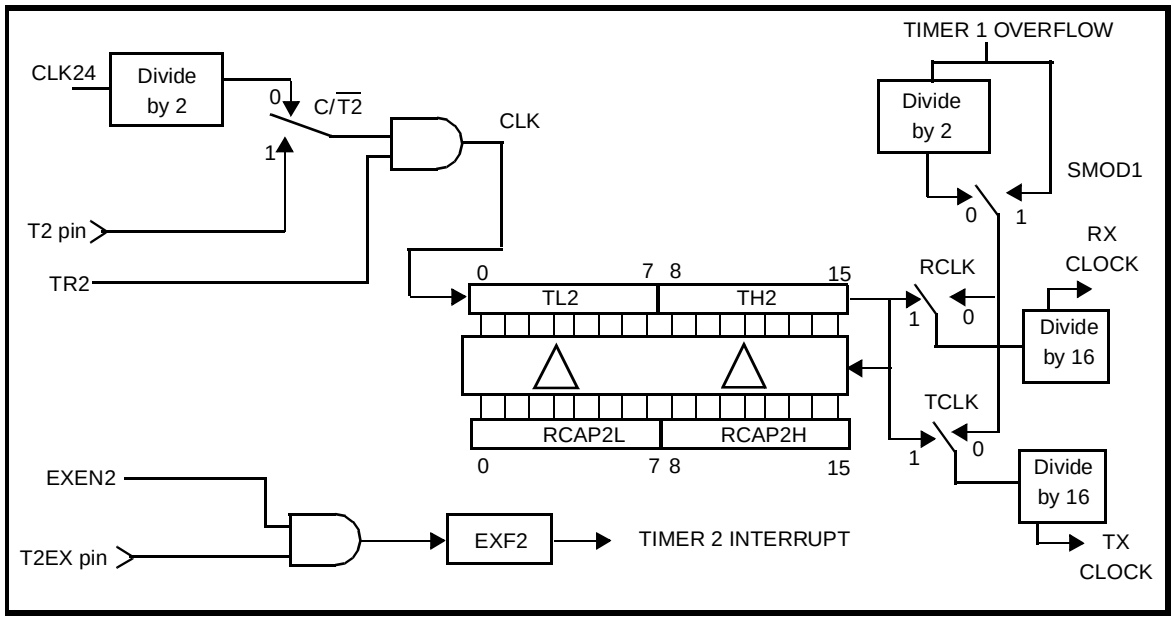

Figure C-6. Timer 2 - Baud Rate Generator Mode

C.3 Serial Interface

The 8051 core provides two serial ports. Serial Port 0 is identical in operation to the standard 8051 serial port. Serial Port 1 is identical to Serial Port 0, except that Timer 2 cannot be used as the baud rate generator for Serial Port 1.

Each serial port can operate in synchronous or asynchronous mode. In synchronous mode, 8051 generates the serial clock and the serial port operates in half-duplex mode. In asynchronous mode, the serial port operates in full-duplex mode. In all modes, 8051 buffers received data in a holding register, enabling the UART to receive an incoming byte before the software has read the previous value.

Each serial port can operate in one of four modes, as outlined in Table C-7..

Table C-7. Serial Port Modes

Mode	Sync/ Async	Baud Clock	Data Bits	Start/Stop	9th Bit Function
0	Sync	CLK24/4 or CLK24/12	8	None	None
1	Async	Timer 1 or Timer 2[1]	8	1 start, 1 stop	None
2	Async	CLK24/32 or CLK24/64	9	1 start, 1 stop	0, 1, parity
3	Async	Timer 1 or Timer 2[1]	9	1 start, 1 stop	0, 1, parity
(1) Timer 2 available for Serial Port 0 only.					

The SFRs associated with the serial ports are:

- SCON0 - SFR 98h - Serial Port 0 control (Table C-8.).
- SBUF0 - SFR 99h - Serial Port 0 buffer.
- SCON1 - SFR C0h - Serial Port 1 control (Table C-9.).
- SBUF1 - SFR C1h - Serial Port 1 buffer.

C.3.1 803x/805x Compatibility

The implementation of the serial interface is similar to that of the Intel 8052.

C.3.2 Mode 0

Serial mode 0 provides synchronous, half-duplex serial communication. For Serial Port 0, serial data output occurs on the RXD0OUT pin, serial data is received on the RXD0 pin, and the TXD0 pin provides the shift clock for both transmit and receive. For Serial Port 1, the corresponding pins are RXD1OUT, RXD1, and TXD1.

The serial mode 0 baud rate is either CLK24/12 or CLK24/4, depending on the state of the SM2_0 bit (or SM2_1 for Serial Port 1). When SM2_0 = 0, the baud rate is CLK24/12, when SM2_0 = 1, the baud rate is CLK24/4.

Mode 0 operation is identical to the standard 8051. Data transmission begins when an instruction writes to the SBUF0 (or SBUF1) SFR. The UART shifts the data, LSB first, at the selected baud rate, until the 8-bit value has been shifted out.

Mode 0 data reception begins when the REN_0 (or REN_1) bit is set and the RI_0 (or RI_1) bit is cleared in the corresponding SCON SFR. The shift clock is activated and the UART shifts data in on each rising edge of the shift clock until 8 bits have been received. One

machine cycle after the 8th bit is shifted in, the RI_0 (or RI_1) bit is set and reception stops until the software clears the RI bit.

Figure C-7.through Figure C-10.illustrate Serial Port Mode 0 transmit and receive timing for both low-speed (CLK24/12) and high-speed (CLK24/4) operation.

Table C-8. SCON0 Register - SFR 98h

Bit	Function
SCON0.7	SM0_0 - Serial Port 0 mode bit 0.
SCON0.6	SM1_0 - Serial Port 0 mode bit 1, decoded as: SM0_0 SM1_0 Mode 0 0 0 0 1 1 1 0 2 1 1 3
SCON0.5	SM2_0 - Multiprocessor communication enable. In modes 2 and 3, this bit enables the multiprocessor communication feature. If SM2_0 = 1 in mode 2 or 3, then RI_0 will not be activated if the received 9th bit is 0. If SM2_0=1 in mode 1, then RI_0 will only be activated if a valid stop is received. In mode 0, SM2_0 establishes the baud rate: when SM2_0=0, the baud rate is CLK24/12; when SM2_0=1, the baud rate is CLK24/4.
SCON0.4	REN_0 - Receive enable. When REN_0=1, reception is enabled.
SCON0.3	TB8_0 - Defines the state of the 9th data bit transmitted in modes 2 and 3.
SCON0.2	RB8_0 - In modes 2 and 3, RB8_0 indicates the state of the 9th bit received. In mode 1, RB8_0 indicates the state of the received stop bit. In mode 0, RB8_0 is not used.
SCON0.1	TI_0 - Transmit interrupt flag. indicates that the transmit data word has been shifted out. In mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, TI_0 is set when the stop bit is placed on the TXD0 pin. **TI_0 must be cleared by firmware.**
SCON0.0	RI_0 - Receive interrupt flag. Indicates that serial data word has been received. In mode 0, RI_0 is set at the end of the 8th data bit. In mode 1, RI_0 is set after the last sample of the incoming stop bit, subject to the state of SM2_0. In modes 2 and 3, RI_0 is set at the end of the last sample of RB8_0. **RI_0 must be cleared by firmware.**

Table C-9. SCON1 Register - SFR C0h

Bit	Function
SCON1.7	SM0_1 - Serial Port 1 mode bit 0.
SCON1.6	SM1_1 - Serial Port 1 mode bit 1, decoded as: SM0_1 SM1_1 Mode 0 0 0 0 1 1 1 0 2 1 1 3
SCON1.5	SM2_1 - Multiprocessor communication enable. In modes 2 and 3, this bit enables the multiprocessor communication feature. If SM2_1 = 1 in mode 2 or 3, then RI_1 will not be activated if the received 9th bit is 0. If SM2_1=1 in mode 1, then RI_1 will only be activated if a valid stop is received. In mode 0, SM2_1 establishes the baud rate: when SM2_1=0, the baud rate is CLK24/12; when SM2_1=1, the baud rate is CLK24/4.
SCON1.4	REN_1 - Receive enable. When REN_1=1, reception is enabled.
SCON1.3	TB8_1 - Defines the state of the 9th data bit transmitted in modes 2 and 3.
SCON1.2	RB8_1 - In modes 2 and 3, RB8_0 indicates the state of the 9th bit received. In mode 1, RB8_1 indicates the state of the received stop bit. In mode 0, RB8_1 is not used.
SCON1.1	TI_1 - Transmit interrupt flag. indicates that the transmit data word has been shifted out. In mode 0, TI_1 is set at the end of the 8th data bit. In all other modes, TI_1 is set when the stop bit is placed on the TXD0 pin. TI_1 must be cleared by the software.
SCON1.0	RI_1 - Receive interrupt flag. Indicates that serial data word has been received. In mode 0, RI_1 is set at the end of the 8th data bit. In mode 1, RI_1 is set after the last sample of the incoming stop bit, subject to the state of SM2_1. In modes 2 and 3, RI_1 is set at the end of the last sample of RB8_1. RI_1 must be cleared by the software.

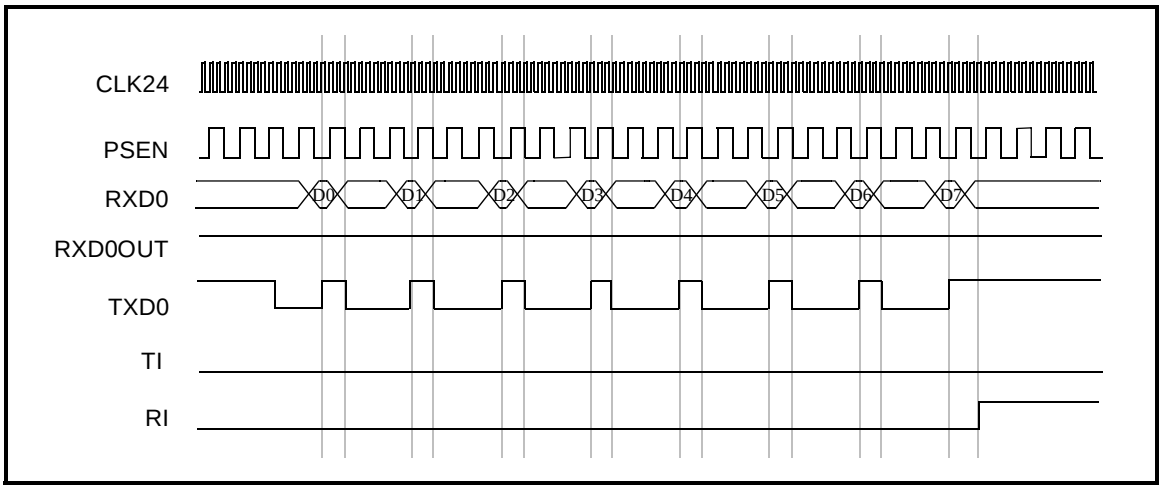

Figure C-7. Serial Port Mode 0 Receive Timing - Low Speed Operation

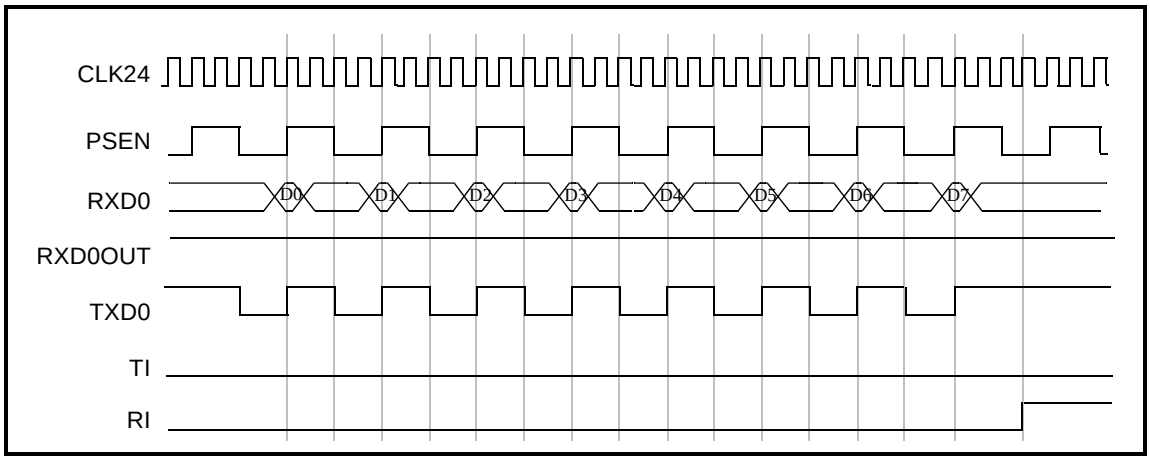

Figure C-8. Serial Port Mode 0 Receive Timing - High Speed Operation

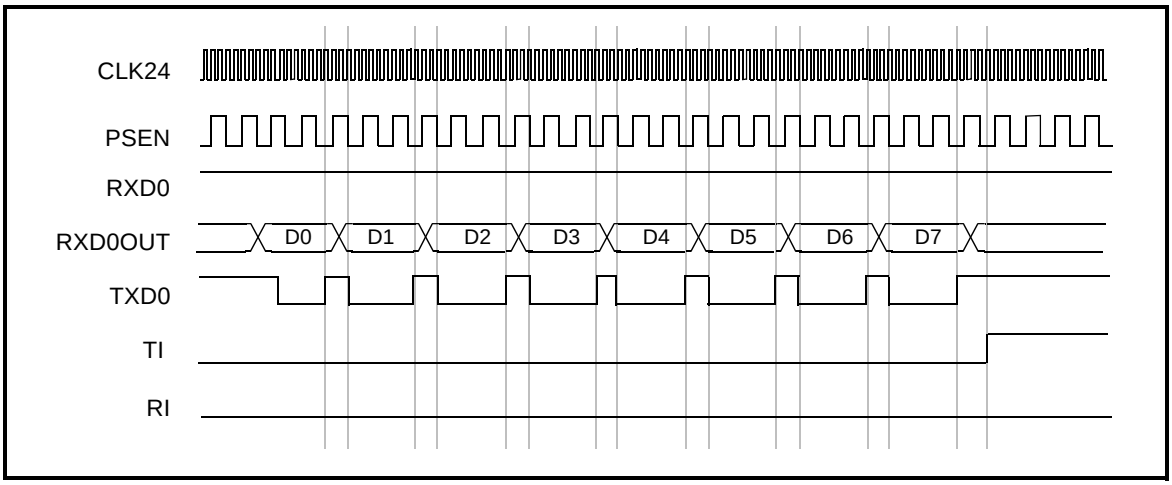

Figure C-9. Serial Port Mode 0 Transmit Timing - Low Speed Operation

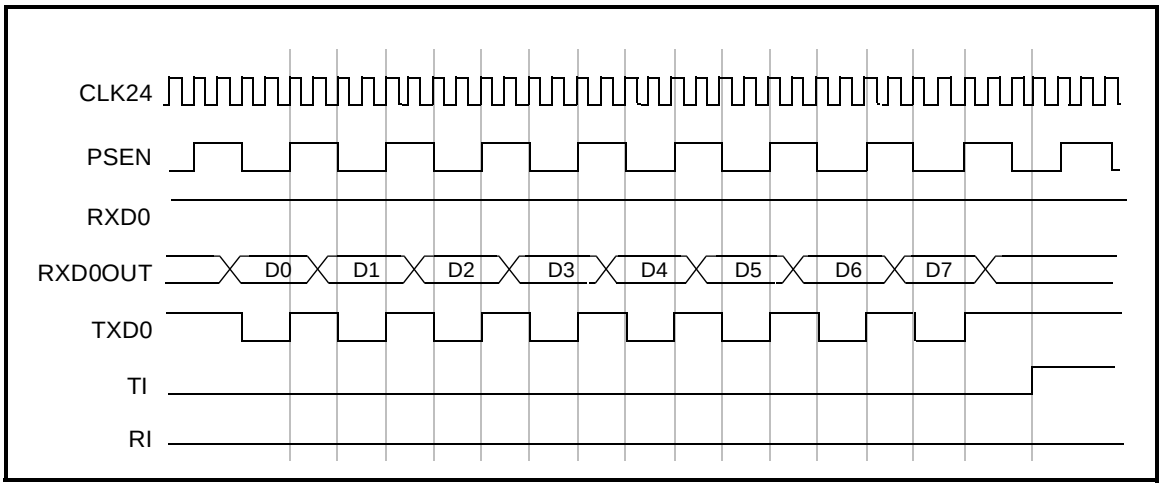

Figure C-10. Serial Port Mode 0 Transmit Timing - High Speed Operation

C.3.3 Mode 1

Mode 1 provides standard asynchronous, full-duplex communication, using a total of 10 bits: 1 start bit, 8 data bits, and 1 stop bit. For receive operations, the stop bit is stored in RB8_0 (or RB8_1). Data bits are received and transmitted LSB first.

C.3.3.1 Mode 1 Baud Rate

The mode 1 baud rate is a function of timer overflow. Serial Port 0 can use either Timer 1 or Timer 2 to generate baud rates. Serial Port 1 can only use Timer 1. The two serial ports can run at the same baud rate if they both use Timer 1, or different baud rates if Serial Port 0 uses Timer 2 and Serial Port 1 uses Timer 1.

Each time the timer increments from its maximum count (FFh for Timer 1 or FFFFh for Timer 2), a clock is sent to the baud rate circuit. The clock is then divided by 16 to generate the baud rate.

When using Timer 1, the SMOD0 (or SMOD1) bit selects whether or not to divide the Timer 1 rollover rate by 2. Therefore, when using Timer 1, the baud rate is determined by the equation:

$$\text{Baud Rate} = \frac{2^{\text{SMODx}}}{32} \times \text{Timer 1 Overflow}$$

SMOD0 is SFR bit PCON.7; SMOD1 is SFR bit EICON.7.

When using Timer 2, the baud rate is determined by the equation:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow}}{16}$$

To use Timer 1 as the baud rate generator, it is best to use Timer 1 mode 2 (8-bit counter with auto-reload), although any counter mode can be used. The Timer 1 reload is stored in the TH1 register, which makes the complete formula for Timer 1:

$$\text{Baud Rate} = \frac{2^{\text{SMODx}}}{32} \times \frac{\text{CLK24}}{12 \times (256 - \text{TH1})}$$

The 12 in the denominator in the above equation can be changed to 4 by setting the T1M bit in the CKCON SFR. To derive the required TH1 value from a known baud rate (when TM1 = 0), use the equation:

$$TH1 = 256 - \frac{2^{SMODx} \times CLK24}{384 \times \text{Baud Rate}}$$

You can also achieve very low serial port baud rates from Timer 1 by enabling the Timer 1 interrupt, configuring Timer 1 to mode 1, and using the Timer 1 interrupt to initiate a 16-bit software reload. Table C-10. lists sample reload values for a variety of common serial port baud rates.

Note that more accurate baud rates are achieved by using Timer 2 as the baud rate generator (next section).

Table C-10. Timer 1 Reload Values for Common Serial Port Mode 1 Baud Rates

Nominal Rate	24 MHz Divisor	Reload Value	Actual Rate	Error
57600	6	FA	62500	8.5%
38400	10	F6	37500	-2.3%
28800	13	F3	28846	+0.16%
19200	20	EC	18750	-2.3%
9600	39	D9	9615	+0.16%
4800	78	B2	4807	+0.15%
2400	156	64	2403	+.13%
Settings: SMOD =1, C/$\overline{T}$=0, Timer1 mode=2, TIM=1 Note: Using rates that are off by 2.3% or more will not work in all systems.				

To use Timer 2 as the baud rate generator, configure Timer 2 in auto-reload mode and set the TCLK and/or RCLK bits in the T2CON SFR. TCLK selects Timer 2 as the baud rate generator for the transmitter; RCLK selects Timer 2 as the baud rate generator for the receiver. The 16-bit reload value for Timer 2 is stored in the RCAP2L and RCA2H SFRs, which makes the equation for the Timer 2 baud rate:

$$\text{Baud Rate} = \frac{\text{CLK24}}{32 \times (65536 - \text{RCAP2H,RCAP2L})}$$

where RCAP2H,RCAP2L is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned number.

The 32 in the denominator is the result of CLK24 being divided by 2 and the Timer 2 overflow being divided by 16. Setting TCLK or RCLK to 1 automatically causes CLK24 to be divided by 2, as shown in Figure C-6., instead of the 4 or 12 determined by the T2M bit in the CKCON SFR.

To derive the required RCAP2H and RCAP2L values from a known baud rate, use the equation:

$$\text{RCAP2H,RCAP2L} = 65536 - \frac{\text{CLK24}}{32 \times \text{Baud Rate}}$$

When either RCLK or TCLK is set, the TF2 flag will not be set on a Timer 2 roll over, and the T2EX reload trigger is disabled.

Table C-11. Timer 2 Reload Values for Common Serial port Mode 1 Baud Rates

Nominal Rate	C/T2	Divisor	Reload Val	Actual Rate	Error
57600	0	13	F3	57692.31	0.16%
38400	0	20	EC	37500	-2.34%
28800	0	26	E6	28846.15	0.16%
19200	0	39	D9	19230.77	0.16%
9600	0	78	B2	9615.385	0.16%
4800	0	156	64	4807.692	0.16%
2400	0	312	FEC8	2403.846	0.16%
Note: using rates that are off by 2.3% or more will not work in all systems.					

C.3.3.2 Mode 1 Transmit

Figure C-11. illustrates the mode 1 transmit timing. In mode 1, the UART begins transmitting after the first roll over of the divide-by-16 counter after the software writes to the SBUF0 (or SBUF1) register. The UART transmits data on the TXD0 (or TXD1) pin in the following order: start bit, 8 data bits (LSB first), stop bit. The TI_0 (or TI_1) bit is set 2 CLK24 cycles after the stop bit is transmitted.

C.3.3.3 Mode 1 Receive

Figure C-12. illustrates the mode 1 receive timing. Reception begins at the falling edge of a start bit received on the RXD0 (or RXD1) pin, when enabled by the REN_0 (or REN_1) bit. For this purpose, the RXD0 (or RXD1) pin is sampled 16 times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter roll over to the bit boundaries.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on the RXD0 (or RXD1) pin is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on the RXD0 (or RXD1) pin.

At the middle of the stop bit time, the serial port checks for the following conditions:

- RI_0 (or RI_1) = 0, and
- If SM2_0 (or SM2_1) = 1, the state of the stop bit is 1.
  (If SM2_0 (or SM2_1) = 0, the state of the stop bit doesn't matter.)

If the above conditions are met, the serial port then writes the received byte to the SBUF0 (or SBUF1) register, loads the stop bit into RB8_0 (or RB8_1), and sets the RI_0 (or RI_1) bit. If the above conditions are not met, the received data is lost, the SBUF register and RB8 bit are not loaded, and the RI bit is not set.

After the middle of the stop bit time, the serial port waits for another high-to-low transition on the (RXD0 or RXD1) pin.

Mode 1 operation is identical to that of the standard 8051 when Timers 1 and 2 use CLK24/12 (the default).

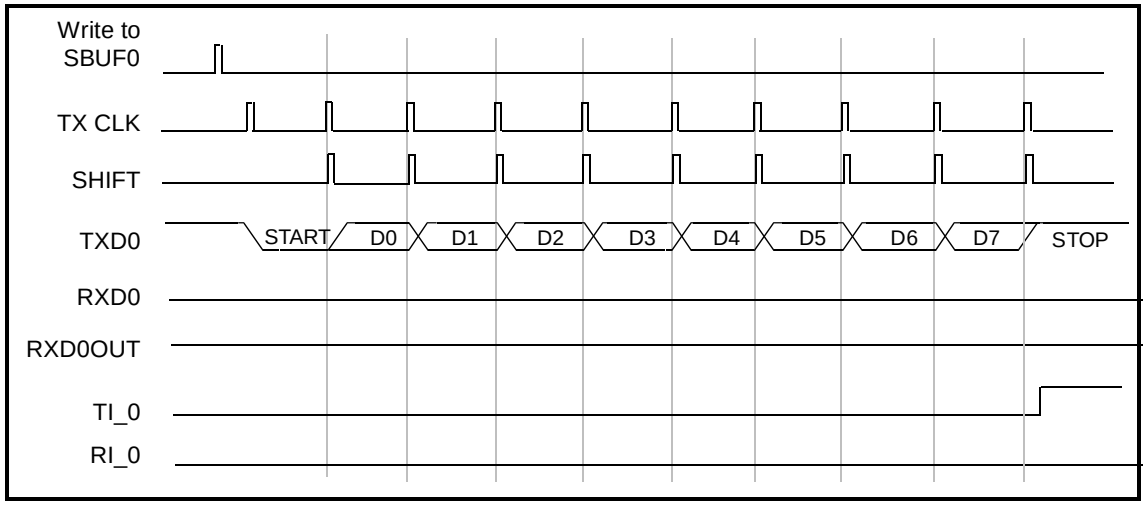

Figure C-11. Serial Port 0 Mode 1 Transmit Timing

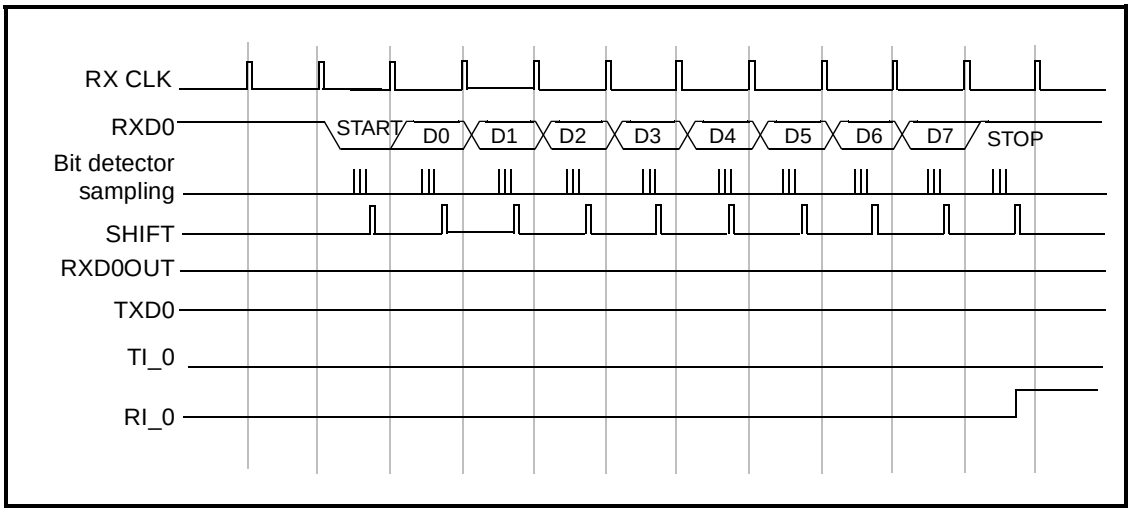

Figure C-12. Serial Port 0 Mode 1 Receive Timing

C.3.4 Mode 2

Mode 2 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first. For transmission, the 9th bit is determined by the value in TB8_0 (or TB8_1). To use the 9th bit as a parity bit, move the value of the P bit (SFR PSW.0) to TB8_0 (or TB8_1).

The mode 2 baud rate is either CLK24/32 or CLK24/64, as determined by the SMOD0 (or SMOD1) bit. The formula for the mode 2 baud rate is:

$$\text{Baud Rate} = \frac{2^{\text{SMODx}} \times \text{CLK24}}{64}$$

Mode 2 operation is identical to the standard 8051.

C.3.4.1 Mode 2 Transmit

Figure C-13. illustrates the mode 2 transmit timing. Transmission begins after the first roll over of the divide-by-16 counter following a software write to SBUF0 (or SBUF1). The UART shifts data out on the TXD0 (or TXD1) pin in the following order: start bit, data bits (LSB first), 9th bit, stop bit. The TI_0 (or TI_1) bit is set when the stop bit is placed on the TXD0 (or TXD1) pin.

C.3.4.2 Mode 2 Receive

Figure C-14. illustrates the mode 2 receive timing. Reception begins at the falling edge of a start bit received on the RXD0 (or RXD1) pin, when enabled by the REN_0 (or REN_1) bit. For this purpose, the RXD0 (or RXD1) pin is sampled 16 times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter roll over to the bit boundaries.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on the RXD0 (or RXD1) pin is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on the RXD0 (or RXD1) pin.

At the middle of the stop bit time, the serial port checks for the following conditions:

- RI_0 (or RI_1) = 0, and
- If SM2_0 (or SM2_1) = 1, the state of the stop bit is 1.
  (If SM2_0 (or SM2_1) = 0, the state of the stop bit doesn't matter.)

If the above conditions are met, the serial port then writes the received byte to the SBUF0 (or SBUF1) register, loads the stop bit into RB8_0 (or RB8_1), and sets the RI_0 (or RI_1) bit. If the above conditions are not met, the received data is lost, the SBUF register and RB8 bit are not loaded, and the RI bit is not set. After the middle of the stop bit time, the serial port waits for another high-to-low transition on the RXD0 *(*or RXD1) pin.

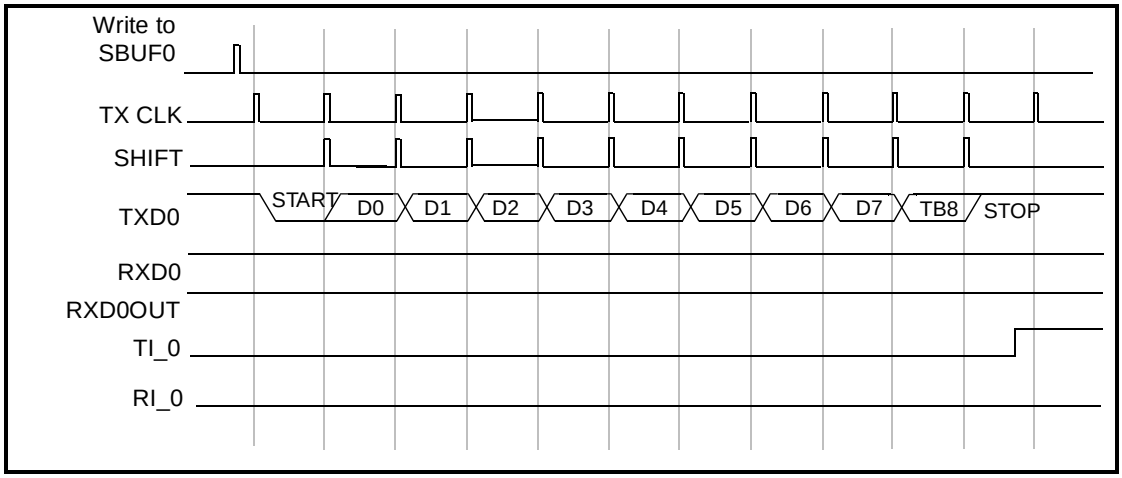

Figure C-13. Serial Port 0 Mode 2 Transmit Timing

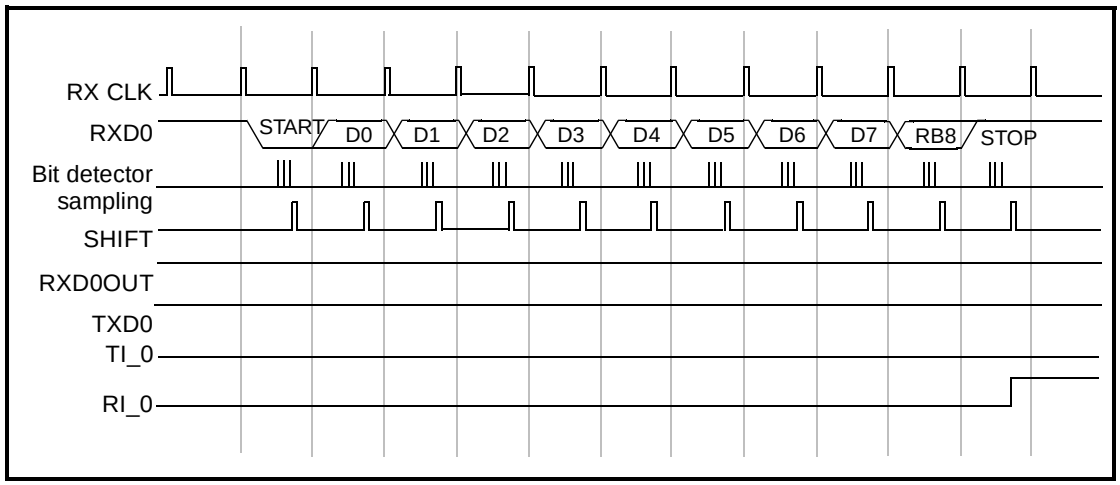

Figure C-14. Serial Port 0 Mode 2 Receive Timing

C.3.5 Mode 3

Mode 3 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first.

The mode 3 transmit and operations are identical to mode 2. The mode 3 baud rate generation is identical to mode 1. That is, mode 3 is a combination of mode 2 protocol and mode 1 baud rate. Figure C-15.illustrates the mode 3 transmit timing. Figure C-16.illustrates the mode 3 receive timing.

Mode 3 operation is identical to that of the standard 8051 when Timers 1 and 2 use CLK24/12 (the default).

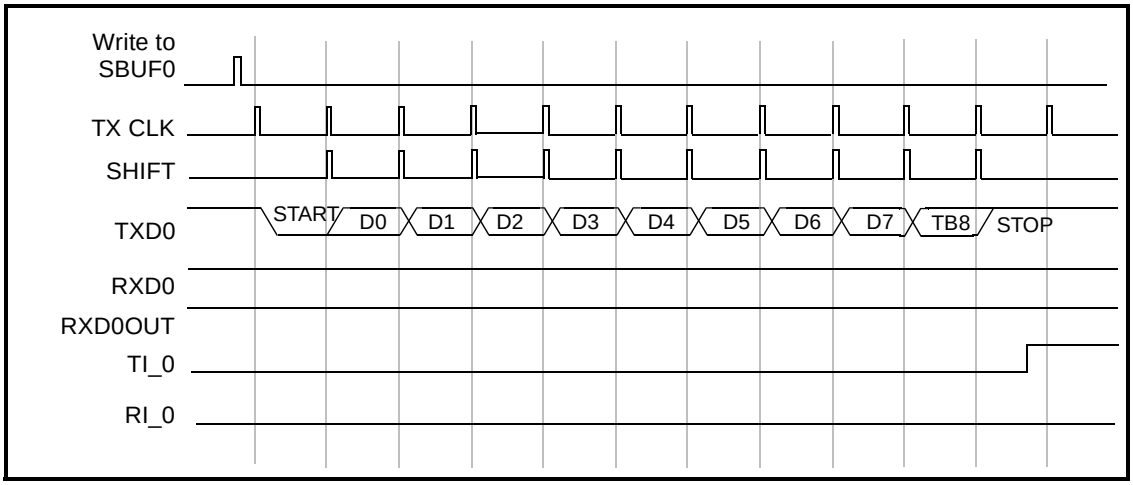

Figure C-15. Serial Port 0 Mode 3 Transmit Timing

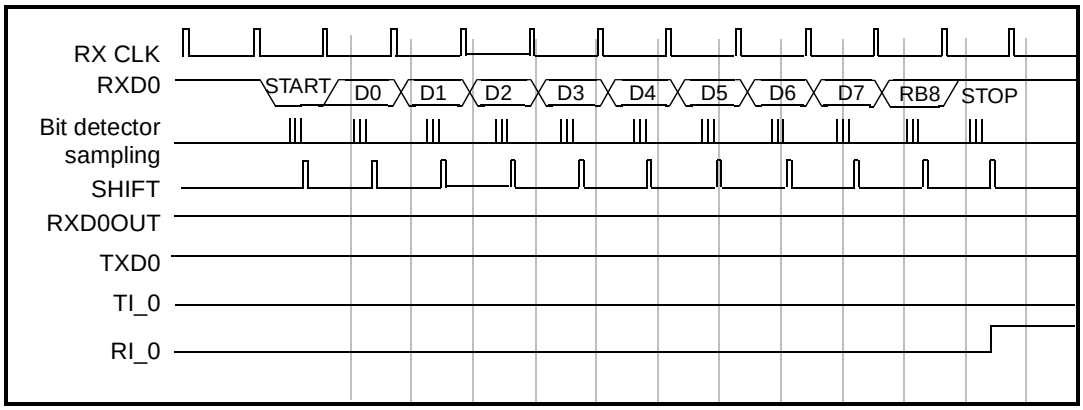

Figure C-16. Serial Port 0 Mode 3 Receive Timing

C.3.6 Multiprocessor Communications

The multiprocessor communication feature is enabled in modes 2 and 3 when the SM2 bit is set in the SCON SFR for a serial port (SM2_0 for Serial Port 0, SM2_1 for Serial Port 1). In multiprocessor communication mode, the 9th bit received is stored in RB8_0 (or RB8_1) and, after the stop bit is received, the serial port interrupt is activated only if RB8_0 (or RB8_1) = 1.

A typical use for the multiprocessor communication feature is when a master wants to send a block of data to one of several slaves. The master first transmits an address byte that identifies the target slave. When transmitting an address byte, the master sets the 9th bit to 1; for data bytes, the 9th bit is 0.

With SM2_0 (or SM2_1) = 1, no slave will be interrupted by a data byte. However, an address byte interrupts all slaves so that each slave can examine the received address byte to determine whether that slave is being addressed. Address decoding must be done by software during the interrupt service routine. The addressed slave clears its SM2_0 (or SM2_1) bit and prepares to receive the data bytes. The slaves that are not being addressed leave the SM2_0 (or SM2_1) bit set and ignore the incoming data bytes.

C.3.7 Interrupt SFRs

The following SFRs are associated with interrupt control:

- IE - SFR A8h (Table C-12.)
- IP - SFR B8h (Table C-13.)
- EXIF - SFR 91h (Table C-14.)
- EICON - SFR D8h (Table C-15.)
- EIE - SFR E8h (Table C-16.)
- EIP - SFR F8h (Table C-17.)

The IE and IP SFRs provide interrupt enable and priority control for the standard interrupt unit, as with the standard 8051. Additionally, these SFRs provide control bits for the Serial Port 1 interrupt. These bits (ES1 and PS1) are available only when the extended interrupt unit is implemented (ext_intr=1). Otherwise, they are read as 0.

Bits ES0, ES1, ET2, PS0, PS1, and PT2 are present, but not used, when the corresponding module is not implemented.

The EXIF, EICON, EIE and EIP registers provide flags, enable control, and priority control for the optional extended interrupt unit.

Table C-12. IE Register - SFR A8h

Bit	Function
IE.7	EA - Global interrupt enable. Controls masking of all interrupts except USB wakeup (resume). EA = 0 disables all interrupts except USB wakeup. When EA = 1, interrupts are enabled or masked by their individual enable bits.
IE.6	ES1 - Enable Serial Port 1 interrupt. ES1 = 0 disables Serial port 1 interrupts (TI_1 and RI_1). ES1 = 1 enables interrupts generated by the TI_1 or TI_1 flag.
IE.5	ET2 - Enable Timer 2 interrupt. ET2 = 0 disables Timer 2 interrupt (TF2). ET2=1 enables interrupts generated by the TF2 or EXF2 flag.
IE.4	ES0 - Enable Serial Port 0 interrupt. ES0 = 0 disables Serial Port 0 interrupts (TI_0 and RI_0). ES0=1 enables interrupts generated by the TI_0 or RI_0 flag.
IE.3	ET1 - Enable Timer 1 interrupt. ET1 = 0 disables Timer 1 interrupt (TF1). ET1=1 enables interrupts generated by the TF1 flag.
IE.2	EX1 - Enable external interrupt 1. EX1 = 0 disables external interrupt 1 (INT1). EX1=1 enables interrupts generated by the INT1# pin.
IE.1	ET0 - Enable Timer 0 interrupt. ET0 = 0 disables Timer 0 interrupt (TF0). ET0=1 enables interrupts generated by the TF0 flag.
IE.0	EX0 - Enable external interrupt 0. EX0 = 0 disables external interrupt 0 (INT0). EX0=1 enables interrupts generated by the INT0# pin.

Table C-13. IP Register - SFR B8h

Bit	Function
IP.7	Reserved. Read as 1.
IP.6	PS1 - Serial Port 1 interrupt priority control. PS1=0 sets Serial Port 1 interrupt (TI_1 or RI_1) to low priority. PS1=1 sets Serial port 1 interrupt to high priority.
IP.5	PT2 - Timer 2 interrupt priority control. PT2=0 sets Timer 2 interrupt (TF2) to low priority. PT2=1 sets Timer 2 interrupt to high priority.
IP.4	PS0 - Serial Port 0 interrupt priority control. PS0=0 sets Serial Port 0 interrupt (TI_0 or RI_0) to low priority. PS0=1 sets Serial Port 0 interrupt to high priority.
IP.3	PT2 - Timer 1 interrupt priority control. PT1 = 0 sets Timer 1 interrupt (TF1) to low priority. PT1=1 sets Timer 1 interrupt to high priority.
IP.2	PX1 - External interrupt 1 priority control. PX 1= 0 sets external interrupt 1 (INT1) to low priority. PT1 = 1 sets external interrupt 1 to high priority.
IP.1	PT0 - Timer 0 interrupt priority control. PT0 = 0 sets Timer 0 interrupt (TF0) to low priority. PT0=1 sets Timer 0 interrupt to high priority.
IP.0	PX0 - External interrupt 0 priority control. PX0 = 0 sets external interrupt 0 (INT0) to low priority. PX0=1 sets external interrupt 0 to high priority.

Table C-14. EXIF Register - SFR 91h

Bit	Function
EXIF.7	IE5 - External interrupt 5 flag. IE 5= 1 indicates a falling edge was detected at the INT5# pin. IE5 must be cleared by software. Setting IE5 in software generates an interrupt, if enabled.
EXIF.6	IE4 - External interrupt 4 flag. IE4 indicates a rising edge was detected at the INT4 pin. IE4 must be cleared by software. Setting IE4 in software generates an interrupt, if enabled.
EXIF.5	I2CINT - External interrupt 3 flag. The “INT3” interrupt is internally connected to the EZ-USB I^2C controller and renamed “I2CINT”. I2CINT = 1 indicates an I^2C interrupt. I2CINT must be cleared by software. Setting I2CINT in software generates an interrupt, if enabled.
EXIF.4	USBINT - External interrupt 2 flag. The “INT2” interrupt is internally connected to the EZ-USB interrupt and renamed “USBINT”. USBINT = 1 indicates an USB interrupt. USBINT must be cleared by software. Setting USBINT in software generates an interrupt, if enabled.
EXIF.3	Reserved. Read as 1.
EXIF.2-0	Reserved. Read as 0.

Table C-15. EICON Register - SFR D8h

Bit	Function
EICON.7	SMOD1 - Serial Port 1 baud rate doubler enable. When SMOD1 = 1 the baud rate for Serial Port is doubled.
EICON.6	Reserved. Read as 1.
EICON.5	ERESI - Enable resume interrupt. ERESI = 0 disables resume interrupt (RESI). ERESI = 1 enables interrupts generated by the resume event.
EICON.4	RESI - Wakeup interrupt flag. EICON.4 = 1 indicates a negative transition was detected at the WAKEUP# pin, or that USB has activity resumed from the suspended state. EICON.4 = 1 must be cleared by software before exiting the interrupt service routine, otherwise the interrupt occurs again. Setting EICON.4=1 in software generates a wakeup interrupt, if enabled.
EICON.3	INT6 - External interrupt 6. When INT6 = 1, the INT6 pin has detected a low to high transition. INT6 will remain active until cleared by writing a 0 to this bit. Setting this bit in software generates an INT6 interrupt in enabled.
EICON.2-0	Reserved. Read as 0.

Table C-16. EIE Register - SFR E8h

Bit	Function
EIE.7-5	Reserved. Read as 1.
EIE.4	EX6 - Enable external interrupt 6. EX6 = 0 disables external interrupt 6 (INT6). EX6 = 1 enables interrupts generated by the INT6 pin.
EIE.3	EX5 - Enable external interrupt 5. EX5 = 0 disables external interrupt 5 (INT5). EX5 = 1 enables interrupts generated by the INT5# pin.
EIE.2	EX4 - Enable external interrupt 4. EX4 = 0 disables external interrupt 4 (INT4). EX4 = 1 enables interrupts generated by the INT4 pin.
EIE.1	EI2C - Enable external interrupt 3. EI2C = 0 disables external interrupt 3 (INT3). EI2C = 1 enables interrupts generated by the I^2C interface.
EIE.0	EUSB - Enable USB interrupt. EUSB = 0 disables USB interrupts. EUSB = 1 enables interrupts generated by the USB Interface.

Table C-17. EIP Register - SFR F8h

Bit	Function
EIP.7-5	Reserved. Read as 1.
EIP.4	PX6 - External interrupt 6 priority control. PX6 = 0 sets external interrupt 6 (INT6) to low priority. PX6 = 1 sets external interrupt 6 to high priority.
EIP.3	PX5 - External interrupt 5 priority control. PX5 = 0 sets external interrupt 5 (INT5#) to low priority. PX5=1 sets external interrupt 5 to high priority.
EIP.2	PX4 - External interrupt 4 priority control. PX4 = 0 sets external interrupt 4 (INT4) to low priority. PX4=1 sets external interrupt 4 to high priority.
EIP.1	PI2C - External interrupt 3 priority control. PI2C = 0 sets I^2C interrupt to low priority. PI2C=1 sets I^2C interrupt to high priority.
EIP.0	PUSB - External interrupt 2 priority control. PUSB = 0 sets USB interrupt to low priority. PUSB=1 sets USB interrupt to high priority.

C.4 Interrupt Processing

When an enabled interrupt occurs, the 8051 core vectors to the address of the interrupt service routine (ISR) associated with that interrupt, as listed in Table C-18.. The 8051 core executes the ISR to completion unless another interrupt of higher priority occurs. Each ISR ends with a `RETI` (return from interrupt) instruction. After executing the `RETI`, the CPU returns to the next instruction that would have been executed if the interrupt had not occurred.

An ISR can only be interrupted by a higher priority interrupt. That is, an ISR for a low-level interrupt can only be interrupted by high-level interrupt. An ISR for a high-level interrupt can only be interrupted by the resume interrupt.

The 8051 core always completes the instruction in progress before servicing an interrupt. If the instruction in progress is `RETI`, or a write access to any of the IP, IE, EIP, or EIE SFRs, the 8051 core completes one additional instruction before servicing the interrupt.

C.4.1 Interrupt Masking

The EA bit in the IE SFR (IE.7) is a global enable for all interrupts except the USB wakeup (resume) interrupt. When EA = 1, each interrupt is enabled or masked by its individual enable bit. When EA = 0, all interrupts are masked, except the USB wakeup interrupt.

Table C-19. provides a summary of interrupt sources, flags, enables, and priorities.

Table C-18. Interrupt Natural Vectors and Priorities

Interrupt	Description	Natural Priority	Interrupt Vector
RESUME	USB Wakeup (resume) interrupt	0	33h
INT0	External interrupt 0	1	03h
TF0	Timer 0 interrupt	2	0Bh
INT1	External interrupt 1	3	13h
TF1	Timer 1 interrupt	4	1Bh
TI_0 or RI_0	Serial port 0 interrupt	5	23h
TF2 or EXF2	Timer 2 interrupt	6	2Bh
TI_1 or RI_1	Serial port 1 interrupt	7	3Bh
INT2	USB interrupt	8	43h
INT3	I^2C interrupt	9	4Bh
INT4	External interrupt 4	4	53h
INT5	External interrupt 5	11	5Bh
INT6	External interrupt 6	12	63H

C.4.2 Interrupt Priorities

There are two stages of interrupt priority assignment, interrupt level and natural priority. The interrupt level (highest, high, or low) takes precedence over natural priority. The USB wakeup interrupt, if enabled, always has highest priority and is the only interrupt that can have highest priority. All other interrupts can be assigned either high or low priority.

In addition to an assigned priority level (high or low), each interrupt also has a natural priority, as listed in Table C-18.. Simultaneous interrupts with the same priority level (for example, both high) are resolved according to their natural priority. For example, if INT0 and INT2 are both programmed as high priority, INT0 takes precedence due to its higher natural priority.

Once an interrupt is being serviced, only an interrupt of higher priority level can interrupt the service routine of the interrupt currently being serviced.

Table C-19. Interrupt Flags, Enables, and Priority Control

Interrupt	Description	Flag	Enable	Priority Control
RESUME	Resume interrupt	EICON.4	EICON.5	N/A
INT0	External interrupt 0	TCON.1	IE.0	IP.0
TF0	Timer 0 interrupt	TCON.5	IE.1	IP.1
INT1	External interrupt 1	TCON.3	IE.2	IP.2
TF1	Timer 1 interrupt	TCON.7	IE.3	IP.3
TI_0 or RI_0	Serial port 0 transmit or receive	SCON0.0 (RI.0), SCON0.1 (Ti_0)	IE.4	IP.4
TF2 or EXF2	Timer 2 interrupt	T2CON.7 (TF2), T2CON.6 (EXF2)	IE.5	IP.5
TI_1 or RI_1	Serial port 1 transmit or receive	SCON1.0 (RI_1), SCON1.1 (TI_1)	IE.6	IP.6
USB	USB interrupt	EXIF.4	EIE.0	EIP.0
I^2C	I^2C interrupt	EXIT.5	EIE.1	EIP.1
INT4	External interrupt 4	EXIF.6	EIE.2	EIP.2
INT5	External interrupt 5	EXIF.7	EIE.3	EIP.3
INT6	External INT 6	EICON.3	EIE.4	EIP.4

C.4.3 Interrupt Sampling

The internal timers and serial ports generate interrupts by setting their respective SFR interrupt flag bits. External interrupts are sampled once per instruction cycle.

INT0 and INT1 are both active low and can be programmed to be either edge-sensitive or level-sensitive, through the IT0 and IT1 bits in the TCON SFR. For example, when IT0 = 0, INT0 is level-sensitive and the 8051 core sets the IE0 flag when the INT0# pin is sampled low. When IT0 = 1, INT0 is edge-sensitive and the 8051 sets the IE0 flag when the INT0# pin is sampled high then low on consecutive samples.

The remaining five interrupts (INT 4-6, USB & I^2C Interrupts) are edge-sensitive only. INT6 and INT4 are active high and INT5 is active low.

To ensure that edge-sensitive interrupts are detected, the corresponding ports should be held high for 4 CLK24 cycles and then low for 4 CLK24 cycles. Level-sensitive interrupts are not

latched and must remain active until serviced.

C.4.4 Interrupt Latency

Interrupt response time depends on the current state of the 8051. The fastest response time is 5 instruction cycles: 1 to detect the interrupt, and 4 to perform the `LCALL` to the ISR.

The maximum latency (13 instruction cycles) occurs when the 8051 is currently executing a `RETI` instruction followed by a `MUL` or `DIV` instruction. The 13 instruction cycles in this case are: 1 to detect the interrupt, 3 to complete the `RETI`, 5 to execute the `DIV` or `MUL`, and 4 to execute the `LCALL` to the ISR. For the maximum latency case, the response time is 13 x 4 = 52 CLK24 cycles.

C.4.5 Single-Step Operation

The 8051 interrupt structure provides a way to perform single-step program execution. When exiting an ISR with an `RETI` instruction, the 8051 will always execute at least one instruction of the task program. Therefore, once an ISR is entered, it cannot be re-entered until at least one program instruction is executed.

To perform single-step execution, program one of the external interrupts (for example,INT0) to be level-sensitive and write an ISR for that interrupt the terminates as follows:

```
JNB  TCON.1,$   ; wait for high on INT0# pin
JB   TCON.1,$   ; wait for low on INT0# pin
RETI            ; return for ISR
```

The CPU enters the ISR when the INT0# pin goes low, then waits for a pulse on INT0#. Each time INT0# is pulsed, the CPU exits the ISR, executes one program instruction, then re-enters the ISR.

C.5 Reset

The 8051 RESET pin is internally connected to an EZ-USB register bit that is controllable through the USB host. See Chapter 10, "EZ-USB Resets" for details.

C.6 Power Saving Modes

C.6.1 Idle Mode

An instruction that sets the IDLE bit (PCON.0) causes the 8051 to enter idle mode when that instruction completes. In idle mode, CPU processing is suspended, and internal registers maintain their current data. When the 8051 core is in idle, the EZ-USB core enters suspend

mode and shuts down the 24 MHz oscillator. See Chapter 11, "EZ-USB Power Management" for a full description of the Suspend/Resume process.

Table C-20. PCON Register - SFR 87h

Bit	Function
PCON.7	SMOD0 - Serial Port 0 baud rate double enable. When SMOD0 = 1, the baud rate for Serial Port 0 is doubled.
PCON.6-4	Reserved.
PCON.3	GF1 - General purpose flag 1. Bit-addressable, general purpose flag for software control.
PCON.2	GF0 - General purpose flag 0. Bit-addressable, general purpose flag for software control.
PCON.1	This bit should always be set to 0.
PCON.0	IDLE - Idle mode select. Setting the IDLE bit places the 8051 in idle mode.