G-LINK Technology

□□□□□□

GLT725608/08L

Ultra High Performance 32K x 8 Bit CMOS Static RAM

Features

- 32K x 8-bit organization
- Very high speed -10,12,15, 20 ns.
- Low standby power
  - Maximum 100 μA for GLT725608L
  - GLT725608L also provides minimum 2 V data retention.
- Fully static operation
- 5 V ±10% power supply
- TTL compatible I/O
- Three state output
- Chip enable for simple memory expansion.
- Available in 28-Pin 600 mil plastic DIP, 300 mil plastic DIP, 300 mil SOJ, 28-Pin TSOP and 330 mil SOP Packages

General Description

GLT725608 and GLT725608L are high performance 256K bit static random access memory organized as 32K by 8 bits and operate at a single 5 volt supply. Fabricated with G-Link Technology's very advanced CMOS sub-micron technology, GLT725608, GLT725608L offer a combination of features: very high speed and very low stand-by current. In addition, this device also supports easy memory expansion with an active LOW chip enable ($\overline{CE}$) as well as an active LOW output enable ($\overline{OE}$) and three state outputs.

The lower power version, GLT725608L also provides typical 1 μA data retention current at minimum 2 V data retention voltage.

Functional Block Diagram

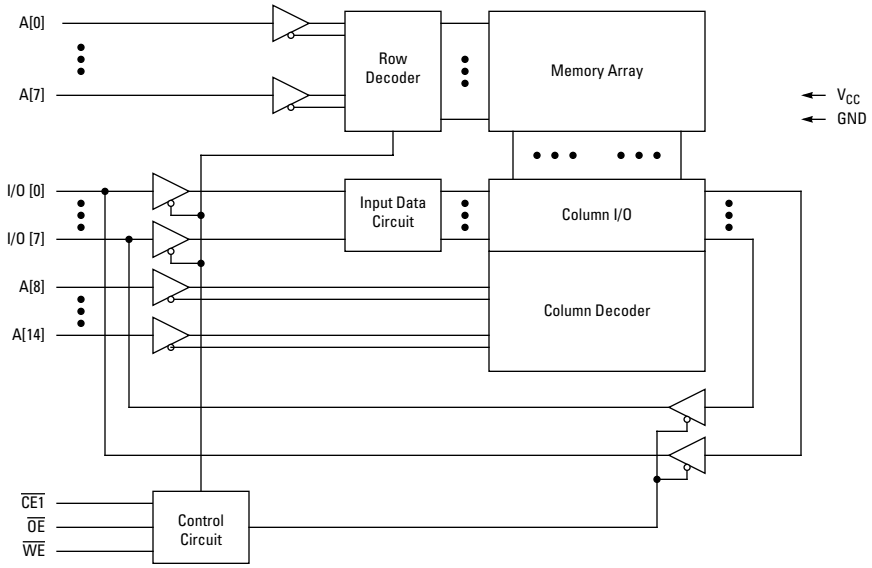


Figure 1. GLT725608 Block Diagram

Signal Descriptions

Symbol	Description
A[14:0]	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O[7:0]	Data Input and Data Output
V_{CC}	+5 V Power Supply
GND	Ground

Truth Table

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{CC} Current
Not Selected (Power Down)	X	H	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Parameter	Ratings	Unit
Ambient Temperature Under Bias	-10°C to +80	°C
Storage Temperature (plastic)	-55°C to +125	°C
Voltage Relative to GND	-0.5 V to +7.0	V
Data Output Current	50	mA
Power Dissipation	1.0	W

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATING may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance (T_A = 25°C,f = 1.0 MHZ)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0 V	10	pF

DC Characteristics [1]

Symbol	Parameter	Test Conditions	-10		-12		-15		-20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{IL}	Guaranteed Input Low Voltage [2]		-0.3	+0.8	-0.3	+0.8	-0.3	+0.8	-0.3	+0.8	V
V_{IH}	Guaranteed Input High Voltage [2]		2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0 V to V_{CC}	-5	5	-5	5	-5	5	-5	5	µA
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE} \geq V_{IH}$	-5	5	-5	5	-5	5	-5	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -4 mA	2.4	–	2.4	–	2.4	–	2.4	–	V
ICC	Operating Power Supply Current	V_{CC} = Max, $\overline{CE} \leq V_{IL}$, $I_{I/O}$ = 0 mA, F = F_{max} [3]	–	190	–	160	–	150	–	120	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{CE} \geq V_{IH}$, $I_{I/O}$ = 0 mA, F = F_{max} [3]	–	70	–	40	–	30	–	20	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{CE} \geq V_{CC}$-0.2 V, $V_{IN} \geq V_{CC}$ -0.2 V or $V_{IN} \leq$ 0.2 V	–	20	–	10	–	10	–	10	mA
	L version only			–		100		100		100	µA

1. Typical characteristics are at V_{CC} = 5 V, TA = 25
2. These are absolute values with reject to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

Data Retention (L version only)

Symbol	Parameter	Test Conditions	Min	Typ [1])	Max	Unit
V_{DR}	V_{CC} for Data retention	$\overline{CE} \geq V_{CC}$ -0.2 V, $V_{IN} \geq V_{CC}$ -0.2 V or $V_{IN} \leq 0.2$ V	2.0	-	5.5	V
I_{CCDR} [1]	Data Retention Current	V_{DR} = 2.0 V		-	30	µA
		V_{DR} = 3.0 V			50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operating Recovery Time		t_{RC} [2]	-	-	ns

1. $\overline{CE} \geq V_{DR}$ -0.2 V, $V_{IN} \geq V_{DR}$ -0.2 V or $V_{IN} \leq 0.2$ V.
2. t_{RC} = Read Cycle Time.

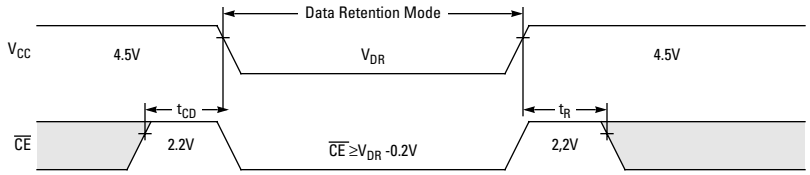


Figure 2. Low V_{CC} Data Retention Waveform (CE Controlled)

AC Test Conditions

Parameter	Rating
Input pulse levels	0V to 3.0V
Input rise and fall times	3 ns
Input and Output Timing Reference level	1.5 V

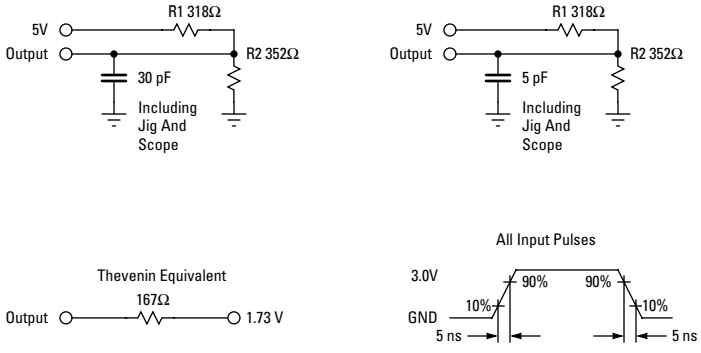


Figure 3. AC Test Loads and Waveforms

AC Characteristics - Read Cycle (over the commercial operating range)

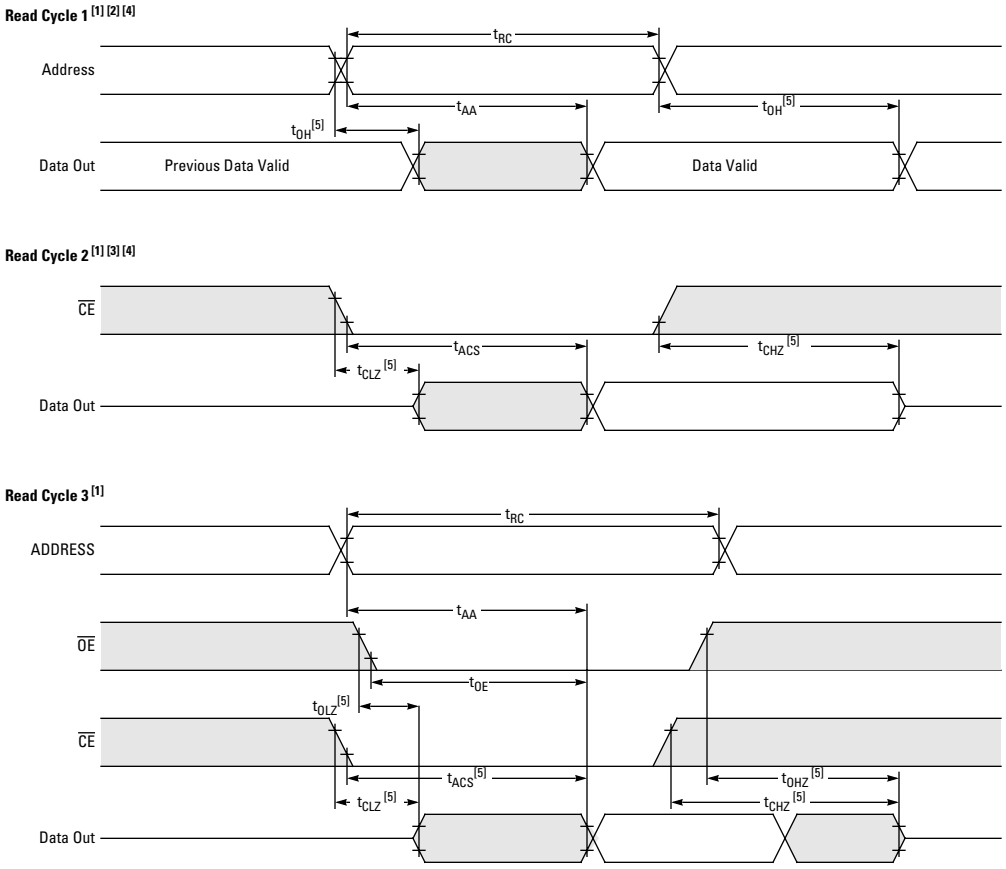
JEDEC Symbol	Symbol	Parameter	-10 [1]		-12		-15		-20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAX}	t_{RC}	Read Cycle Time	10	–	12	–	15	–	20	–	ns
t_{AVQV}	t_{AA}	Address Access Time	–	10	–	12	–	15	–	20	ns
t_{E1LQV}	t_{ACS}	Chip Select Access Time, $\overline{CE}$	–	10	–	12	–	15	–	20	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	–	5	–	5	–	6	–	8	ns
t_{E1LQX}	t_{CLZ}	Chip Select to Output Low Z, $\overline{CE}$	3	–	3	–	3	–	3	–	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	0	–	3	–	3	–	3	–	ns
t_{E1HQZ}	t_{CHZ}	Chip Deselect to Output in High Z, $\overline{CE}$	–	7	–	7	–	8	–	10	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	–	6	–	6	–	6	–	– 8	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	3	–	3	–	3	–	3	–	ns

1. GLT725609 Standard power only.

AC Characteristics - Write Cycle (over the commercial operating range)

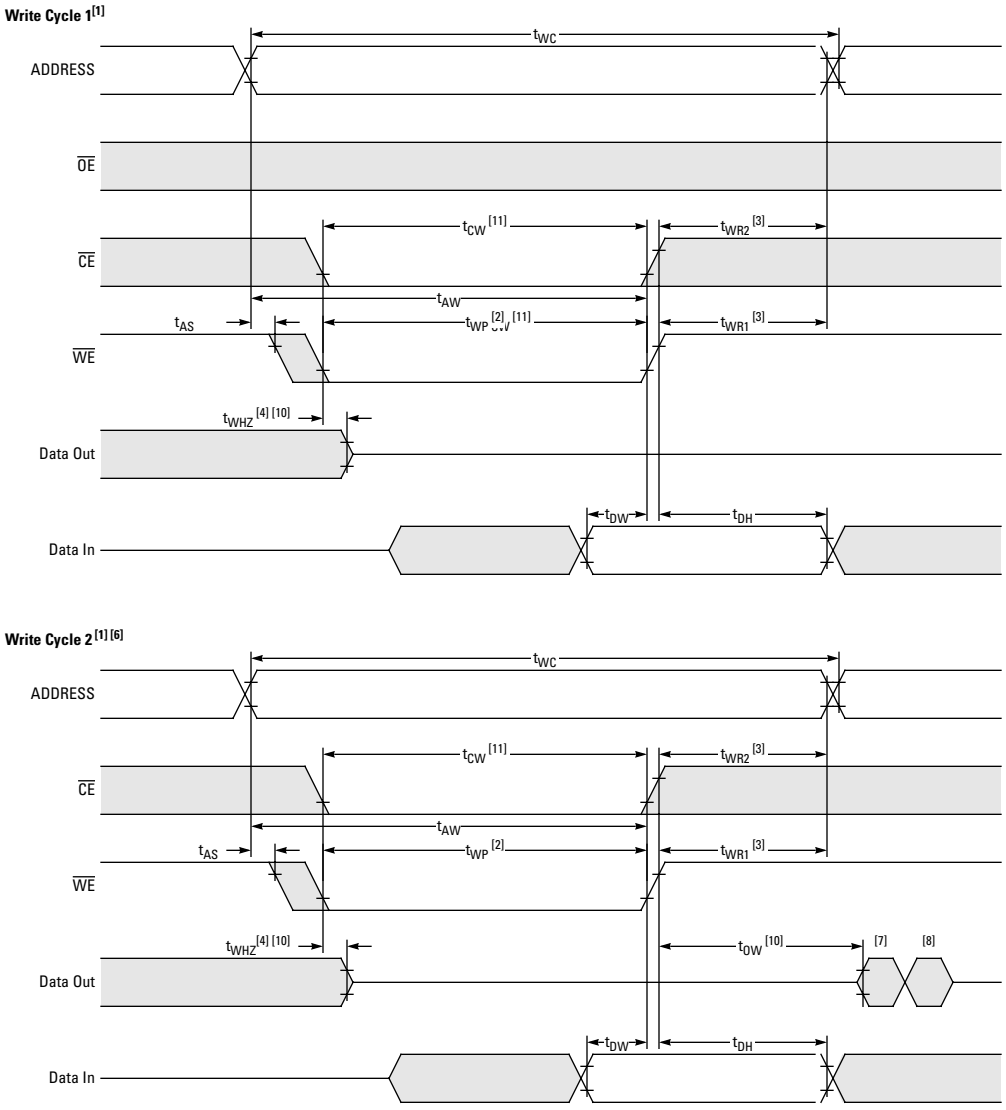
JEDEC Symbol	Symbol	Parameter	-10 [1]		-12		-15		-20		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAX}	t_{WC}	Write Cycle Time	10	–	12	–	15	–	20	–	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	10	–	10	–	12	–	15	–	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	–	0	–	0	–	0	–	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	10	–	10	–	12	–	15	–	ns
t_{WLWH}	t_{WP}	Write Pulse Width	8	–	10	–	12	–	15	–	ns
t_{WHAX}	t_{WR1}	Write Recovery Time, $\overline{WE}$	0	–	0	–	0	–	0	–	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time, $\overline{CE}$	0	–	0	–	0	–	0	–	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	–	6	–	7	–	8	–	10	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	6	–	6	–	7	–	8	–	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	0	–	3	–	3	–	3	–	ns

1. GLT725609 Standard power only.



1. $\overline{WE}$ is high for READ Cycle.
2. Device is continuously selected $\overline{CE} \leq V_{IL}$ and CE 2 $\geq V_{IH}$.
3. Address valid prior to or coincident with CE 1 transition low and/or $\overline{CE}$ transition high.
4. $\overline{OE} \leq V_{IL}$.
5. Transition is measured ± 200 mV from steady state with C_L = 5 pF.

Figure 4. Read Cycle Timing



1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{CE}$ 1and $\overline{CE}$ 2 active and WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE}$ 1 or $\overline{WE}$ going high or $\overline{CE}$ 2 going low at the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ 1 low transition or the $\overline{CE}$ 2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ 1 is low and $\overline{CE}$ 2 is high during this period, I/O pins are in the output state. Then the data input signals of the opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 200 mV from steady state with C_L = 5 pF.
11. t_{CW} is measured from the later of $\overline{CE}$ 1 going low or $\overline{CE}$ 2 going high to the end of write.

Figure 5. Write Cycle Timing

Packaging Information

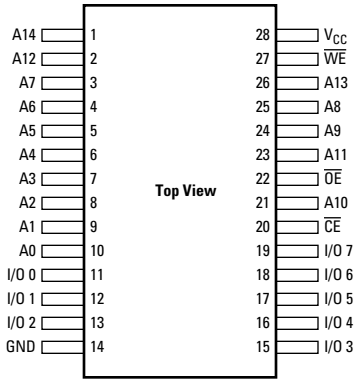


Figure 6. 28-Pin PDIP, SOJ and SOP Pin Assignment

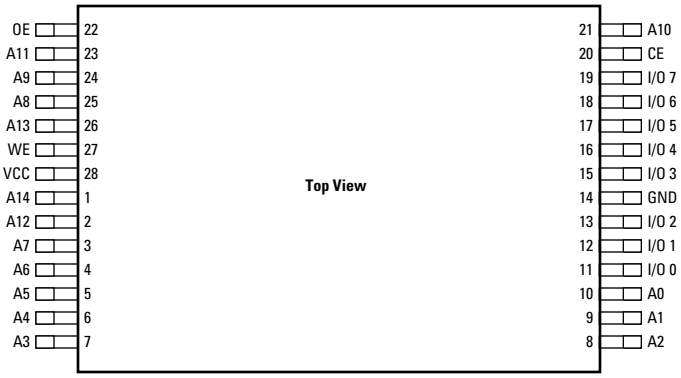
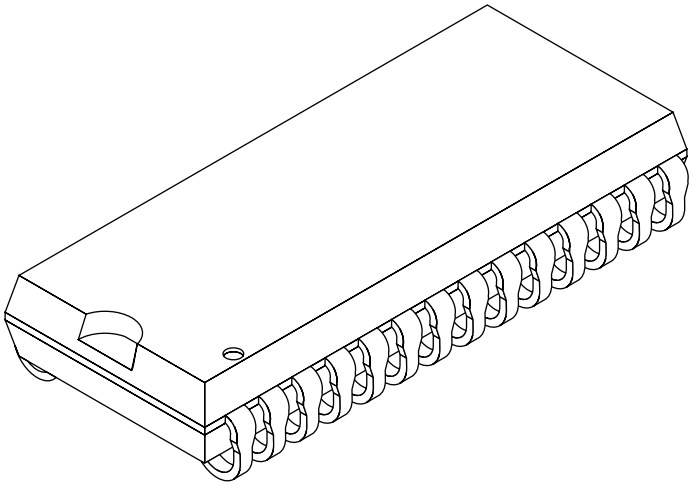


Figure 7. 28-Pin TSOP Pin Assignment



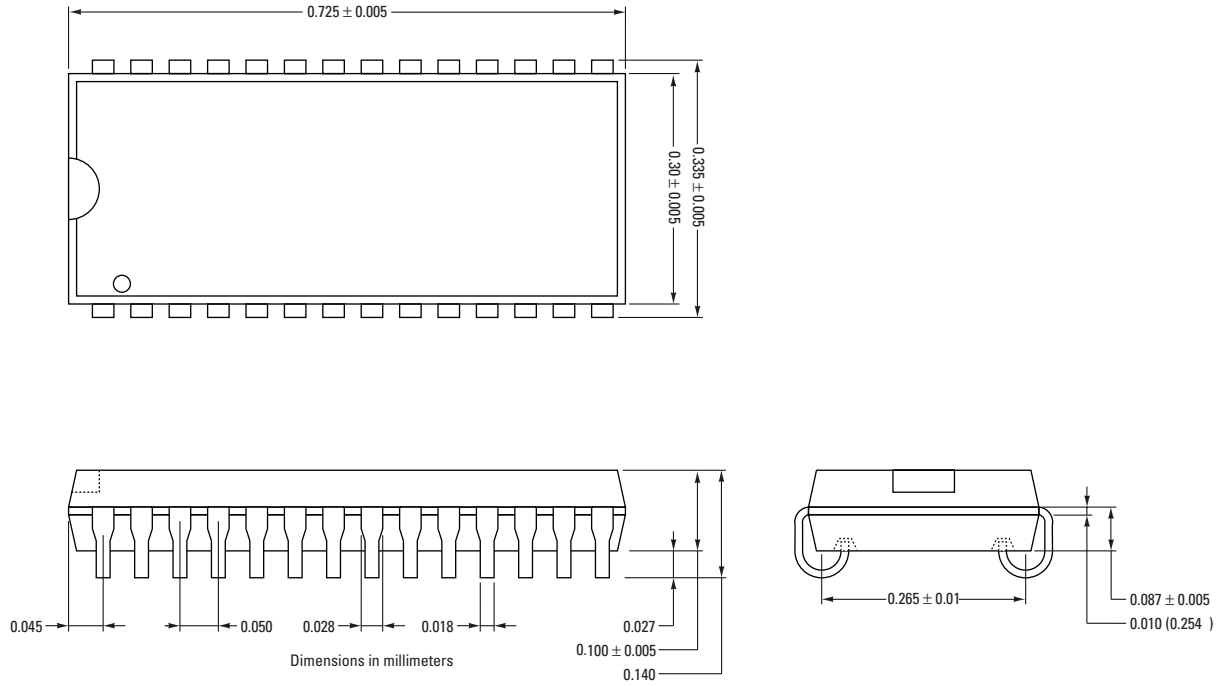
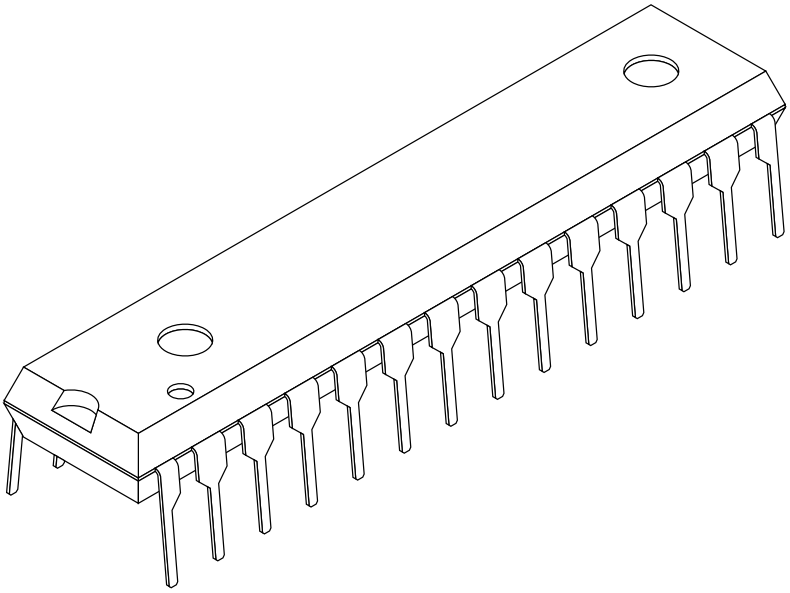


Figure 8. 28-Pin 300 mil SOJ Package Dimensions



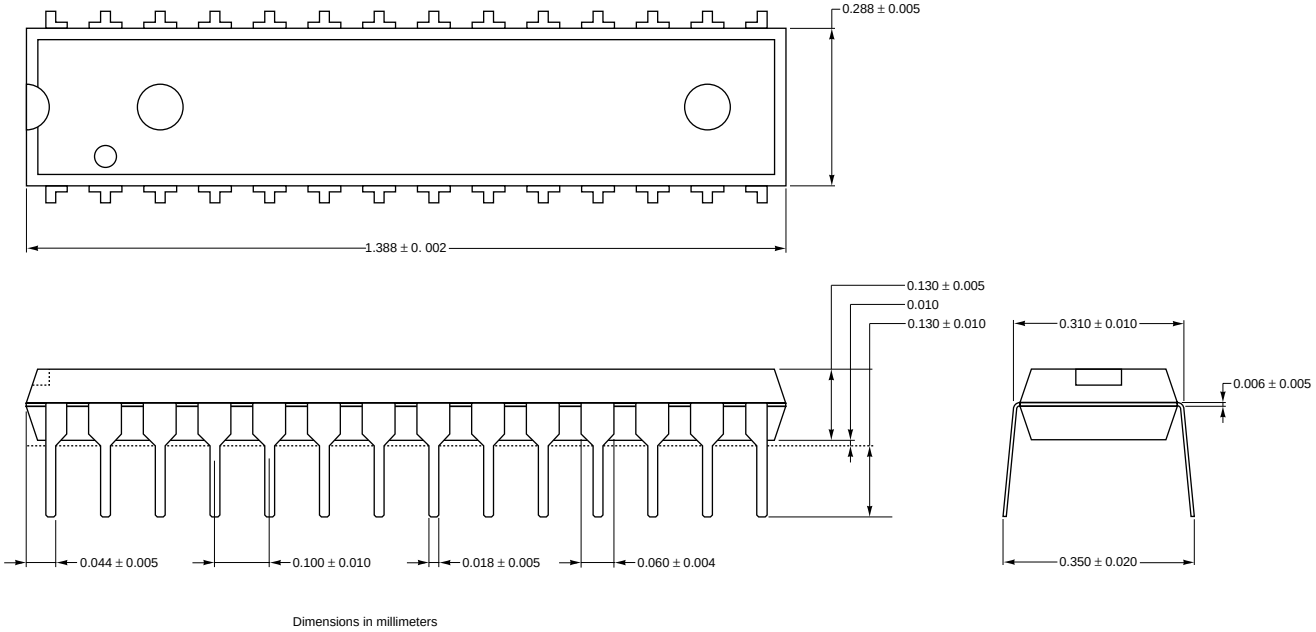
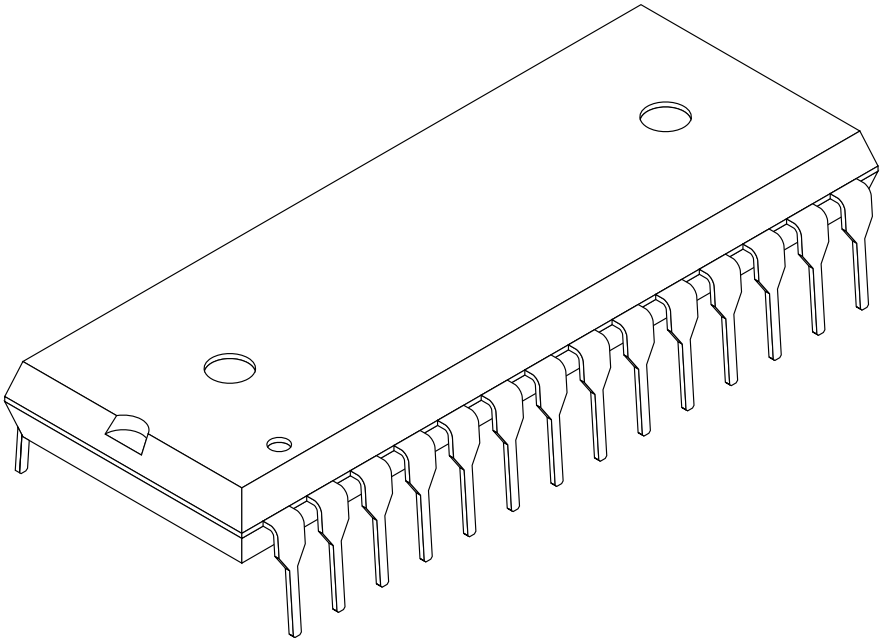


Figure 9. 28-Pin 300 mil PDIP Package Dimensions



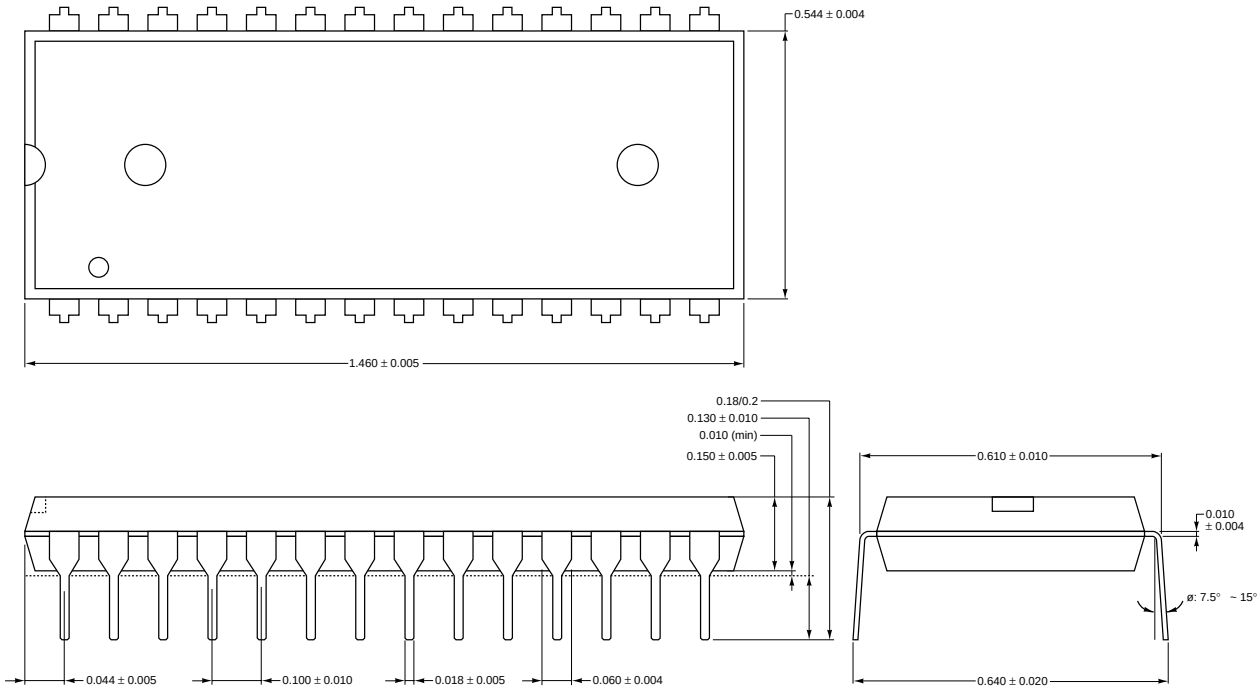
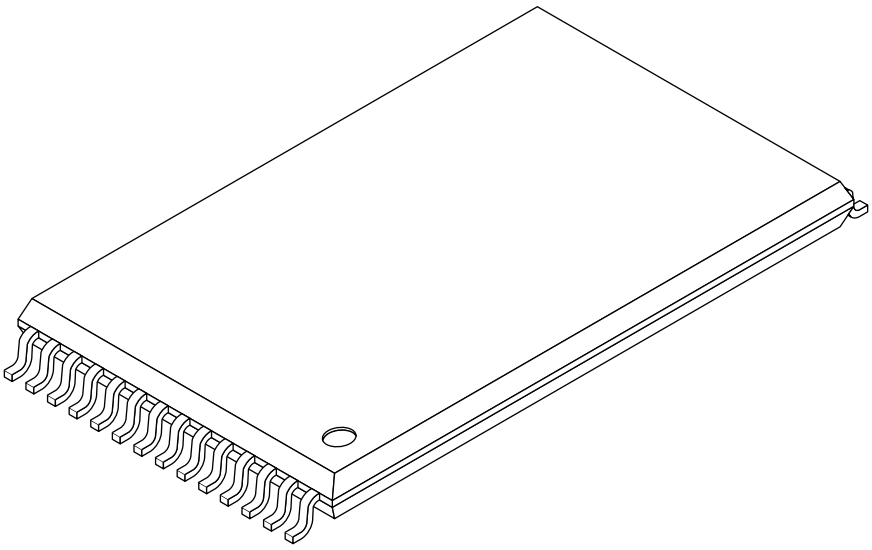


Figure 10. 28-Pin 600 mil PDIP Package Dimensions



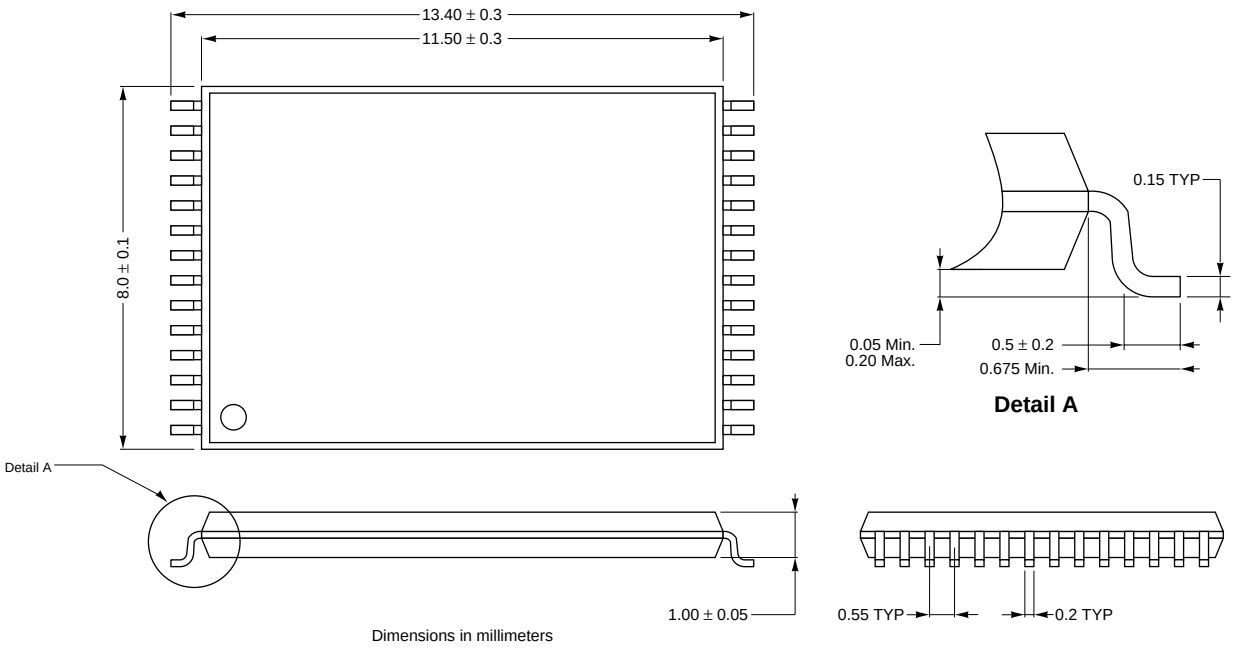


Figure 11. 28-Pin (8 x 13.4 mm) TSOP (Type I) Package Dimensions

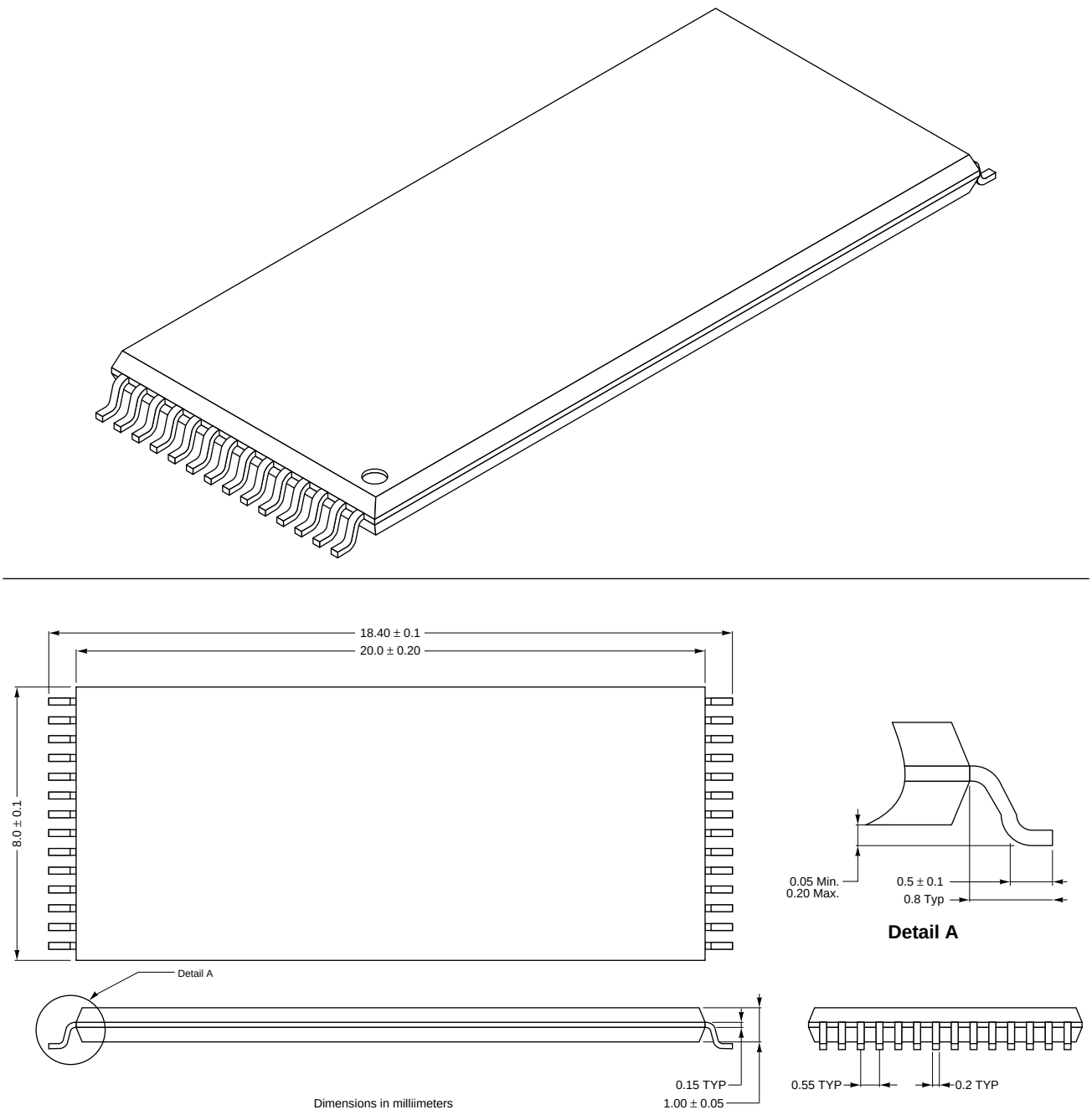


Figure 12. 28-Pin (8 x 20 mm) TSOP (Type I) Package Dimensions

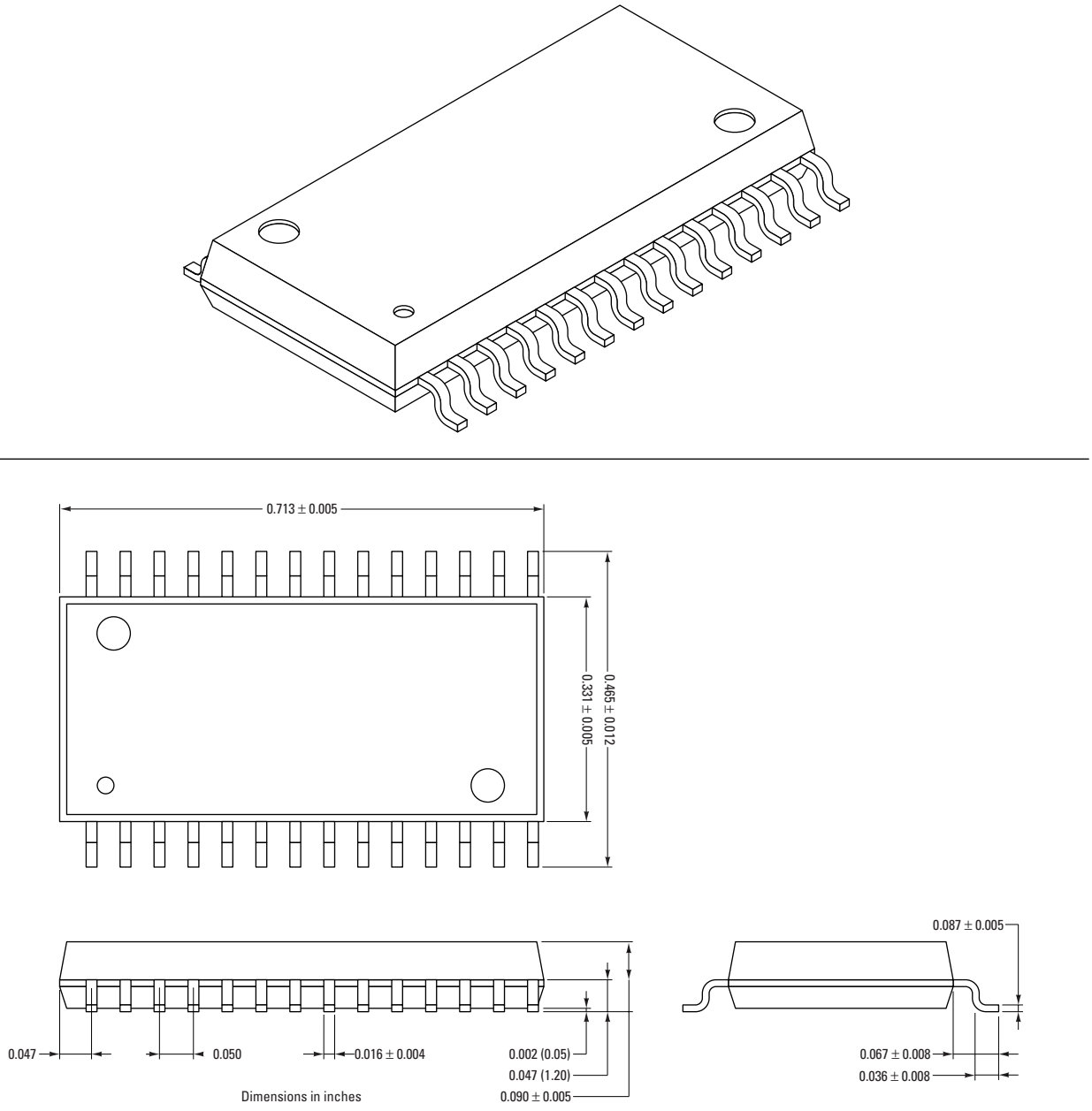


Figure 13. 28-Pin 330 mil SOP Package Outline

Ordering Information

Part Number	Speed	Power	Package
GLT725608-12T	12 ns	Normal	28-Pin SDIP
GLT725608-15T	15 ns	Normal	28-Pin SDIP
GLT725608-20T	20 ns	Normal	28-Pin SDIP
GLT725608-12J3	12 ns	Normal	28-Pin 300 mil SOJ
GLT725608-15J3	15 ns	Normal	28-Pin 300 mil SOJ
GLT725608-20J3	20 ns	Normal	28-Pin 300 mil SOJ
GLT725608-10TS	10 ns	Normal	28-Pin TSOP (Type I)
GLT725608-12T	12 ns	Mix Voltage	28-Pin SDIP
GLT725608-15T	15 ns	Mix Voltage	28-Pin SDIP
GLT725608-20T	20 ns	Mix Voltage	28-Pin SDIP
GLT725608-12J3	12 ns	Mix Voltage	28-Pin 300 mil SOJ
GLT725608-15J3	15 ns	Mix Voltage	28-Pin 300 mil SOJ
GLT725608-20J3	20n s	Mix Voltage	28-Pin 300 mil SOJ

www.glinktech.com

G-LINK Technology

1753 South Main Street
Milpitas, California, 95035, USA
TEL: 408-240-1380 • FAX: 408-240-1385

G-LINK Technology Corporation, Taiwan

6F, No. 24-2, Industry E. Rd. IV
Science-Based Industrial Park
Hsin Chu, Taiwan, R.O.C.
TEL: 03-578-2833 • FAX: 03-578-5820

Printed in USA