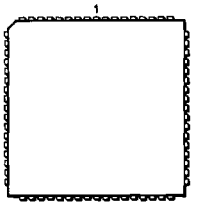
FEATURES

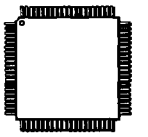
- ☐ Supports MNP2–5 and CCITT V.42bis (SC11091), CCITT V.42 (SC11091/SC11095)
- ☐ Supports SDLC, HDLC, Bisync, Monosync & Async protocols in software
- ☐ Internal Serial Synchronous Communication Circuit
- ☐ Can address 64K ROM, 32K RAM
- ☐ Selectable Clock Frequency
- ☐ 16x16 multiply in 2μs
- ☐ Low Power Power-down (Standby) Mode
- ☐ Supports asymmetric protocols
- ☐ Reverse compatible with SC11011, 21, 61
- ☐ Direct interface to SC11006, SC11024, SC11026, SC11044, SC11046, SC11054 Modems
- ☐ 384 Byte internal RAM
- ☐ 256 byte Internal ROM
- ☐ Power Down mode indicator on $\overline{PD}$ pin
- ☐ Built-in UART with 80ns data access time in parallel mode
- ☐ Direct IBM PC bus interface
- ☐ Selectable IORDY Interface
- ☐ CMOS technology

68-PIN PLCC PACKAGE



SC11091CV
SC11095CV

80-PIN QFP PACKAGE (14 mm)



SC11091CQ
SC11095CQ

GENERAL DESCRIPTION

The UMAC is a high-speed MAC designed to perform the DSP and control functions for modems operating under data compression modes. The SC11091 is capable of supporting V.42bis, V.42, MNP2–5, as well as V.22bis. The SC11095 is functionally similar to the SC11091 except that it does not support V.42bis. (Complete firmware package and licensing information are available from Sierra.) The UMAC supports all of Sierra's V.22bis modem devices: SC11044, SC11046 and SC11054 for Sendfax™ modems; SC11006 and SC11024 for standard modems; SC11026 for Quatro modems; and SK9698 for S/R Fax modems.

Besides preserving the MAC (Modem Advanced Controller—SC11011) and Big MAC (SC11021 series) structure, the UMAC includes a one bit Serial Synchronous Communication Circuit (SSCC) which, with firmware support, eliminates the need for an external SSCC to support HDLC and other synchronous protocols.

BLOCK DIAGRAM
(Parallel Mode Callout)

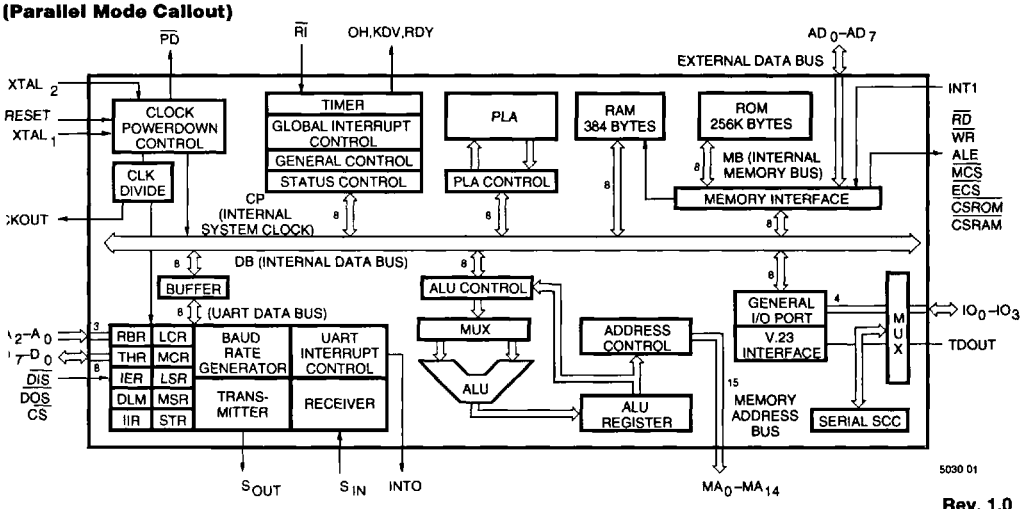


Figure 1.

DESCRIPTION (continued)

The SSCC is implemented as a 1 bit input, 1 bit output, 1 receive clock and 1 transmit clock. This SSCC can interrupt the CPU each time a bit is received or when a bit has been transmitted.

The SC11091/SC11095 contains a 16C450 compatible UART which can be configured to provide a serial or parallel DTE interface. In the RDY mode, the UMAC provides an I/O channel ready (RDY) signal to insert wait states in the PC bus read/write cycle to allow reliable data transfer with any speed bus. This can be changed by a register setting to a no-wait-state-mode. This provides a high speed UART interface, with a minimum read time of 80 ns. On original power up reset, the default mode is active RDY mode. When RDY is deselected, the IORDY pin is tristated and the parallel interface timing is speeded up.

APPLICATIONS

- ☐ V.22bis modem with V.42bis compression(SC11091)
- ☐ MNP2–5 modems
- ☐ Class 2 Fax & Data modems
- ☐ Feature rich International modems
- ☐ Upgrade from SC11011, 11021, 11061
- ☐ Synchronous data links

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER PLCC	PIN NUMBER QFP	DESCRIPTION
I. Parallel Systems Interface (to PC bus)			
A_0–A_2	57, 55, 53	57, 55, 53	Address lines for UART register select, input, TTL.
$\overline{CS}$	63	64	Chip select, active low, input, TTL.
D_0–D_7	50, 48, 46, 43, 41, 40, 39, 37	50, 48, 46, 39, 37, 36, 35, 33	8-bit data port, input-output, TTL.
$\overline{DIS}$	64	65	Data in strobe (PC reads from UART registers), active low, input, TTL.
$\overline{DOS}$	59	59	Data out strobe (PC writes into UART registers), active low, input, TTL.
INTO	66	67	Interrupt, output, CMOS/TTL. Tristate™
RDY	60	61	Output, ready signal for high speed PC-AT interface.
II. RS-232 (Data Set Mode) and Display Interface			
$\overline{AA}$	55	55	Automatic answer enable indicator (low), output, TTL/CMOS.
$\overline{CTS}$	59	59	Clear to send, output, TTL/CMOS.
$\overline{DSR}$	63	64	Data set ready, output, TTL/CMOS.
$\overline{DTR}$	64	65	Data terminal ready, input, TTL.
$\overline{HS}$	53	53	High speed indicator, output, TTL/CMOS. Low when operating at 2400 bps rate. High otherwise.
$\overline{MRDY}$	66	67	Modem ready.
$\overline{RLSD}$	57	57	Carrier detect, output, TTL/CMOS.
$\overline{RTS}$	37	33	Request to send, input, TTL.
III. MAP Interface			
AD_0–AD_7	31–33, 21, 20, 17, 15, 13	27–29, 14, 13, 10, 8, 6	8-bit bidirectional multiplexed address/databus, CMOS.
ALE	8	78	Address Latch Enable, output, CMOS/TTL, the address on ECS, MCS, AD_7–AD_0 are valid at the falling edge of this normally low pulse.
$\overline{ECS}$	36	32	External EERAM chip select or for second MAP chip select, output, TTL/CMOS, addressing space is from 1100H to 11FFH. When used for ROM expanded mode, the ECS functions as the second chip select.

Tristate is a trademark of National Semiconductor.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER PLCC	PIN NUMBER QFP	DESCRIPTION
INTI	5	75	Interrupt input, TTL; interrupt received from the MAP at 600 Hz. Interrupt is detected when this pin has a low to high transition. The line has to stay high for at least 200 ns.
$\overline{MCS}$	24	17	Map chip select for MAP interface, output, TTL/CMOS, addressing space is from 1000H to 10FFH and 1200H to 12FFH
$\overline{RD}$	29	25	RAM read, output, CMOS/TTL, normally high, data on AD_7–AD_0 must be valid at the rising edge of this pulse.
S_{IN}	9	80	Received data, input; TTL. Serial data received from the MAP.
S_{OUT}	3	72	Transmit data, output, CMOS/TTL. Serial data to be transmitted by the modem.
$\overline{WR}$	25	18	RAM write, output, CMOS/TTL, normally high, data on AD_7–AD0 is valid at the rising edge of this pulse.
			IV. Switch Port Pins (RS-232 Mode)
KDV	2	71	Data/voice Relay Control, output, TTL/CMOS. When high, indicates the voice (telephone set) relay is closed and the modem is in the voice mode.
OH	65	66	Off-hook, output, TTL/CMOS, when high, indicates the DAA should go off-hook.
S_0–S_6	50, 48, 46, 43, 41–39	50, 48, 46, 39, 37–35	7-bit input port for sensing switch setting inputs. Weak internal pull-ups (30 kΩ) are provided on these inputs.
			V. DAA Interface
$\overline{RI}$	61	62	Ring indicator, input, Schmitt, when low, indicates the modem is receiving a ringing signal.
			VI. External ROM/RAM Interface
$\overline{CSRAM}$	23	16	Output, TTL/CMOS, chip select for external RAM, address from 4000H to 7FFFH.
$\overline{CSROM}$	19	12	Output, TTL/CMOS, chip select for external ROM, address from 8000H to FFFFH.
MA_0–MA_{14}	30, 35, 38, 47, 49, 51, 54, 56, 58, 67, 1, 4, 12, 14, 16	26, 31, 34, 47, 49, 51, 54, 56, 58, 68, 70, 74, 5, 7, 9	Output, TTL/CMOS, 15 bit address bus for external program/data access.
$\overline{PD}$	27	20	Output, CMOS open drain, indicates power down mode by active low.
			VII. Other Pins
CKOUT	7	77	Clock output pin, TTL/CMOS, from UMAC (9.8304 MHz).
RESET	44	44	Master reset Schmitt input, TTL, active high. When RESET is high, UMAC program counter resets to location 2000H. It resumes counting after RESET goes low.
V_{CCI}	68	69	+5 V
V_{CCP}	18	11	Second V_{CC} pin.
$XTAL_1$	10	2	Together with $XTAL_2$ for crystal input (19.6608 MHz or 29.4912MHz).
$XTAL_2$	11	3	Crystal output pin (19.6608 MHz or 29.4912 MHz).
GNDI	6	76	Ground.
GNDI	34	30	Fourth Ground pin.
GNDP	22	15	Second Ground pin.
GNDP	52	52	Third Ground pin.

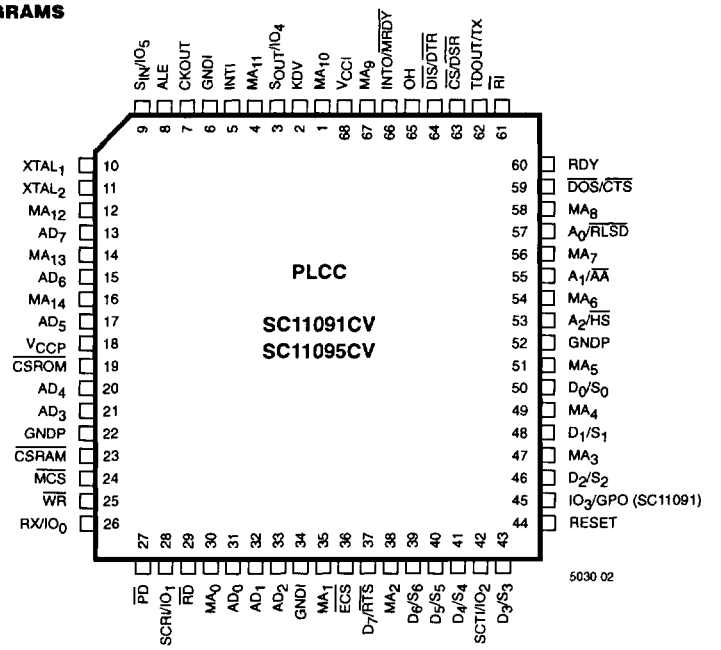
PIN DESCRIPTIONS (continued)

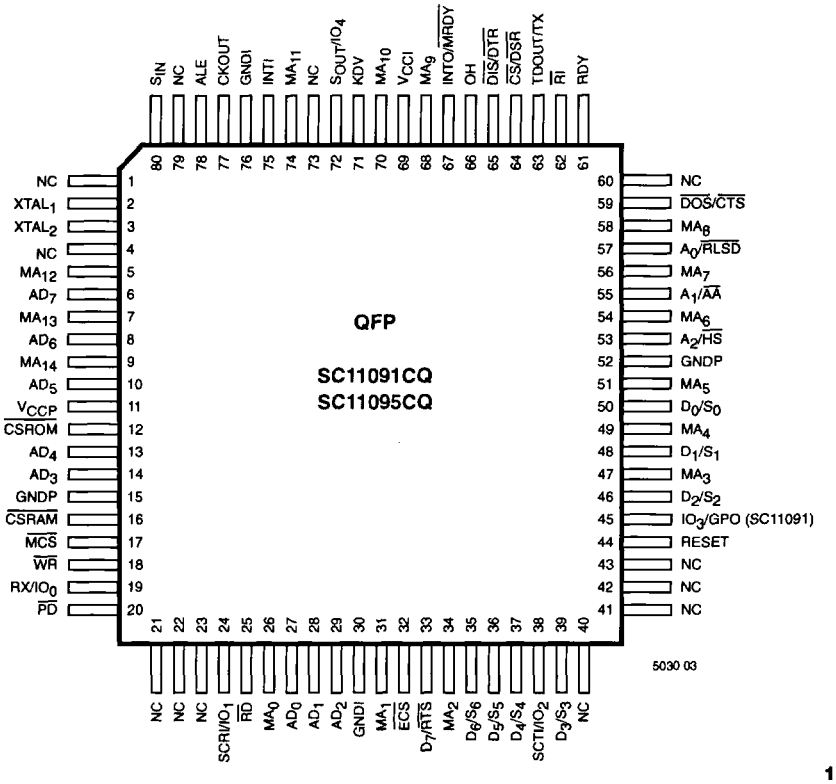
PIN NAME	PIN NUMBER PLCC	PIN NUMBER QFP	DESCRIPTION
VIII. Special Pin Functions			
The UMAC can be configured to emulate the BigMAC (SC11021) which has four IO pins and a TDOUT pin added. For the UMAC, the functions of these 5 pins are preserved on power up or reset. When the SSCC mode is selected, the functions of these 5 pins will conform to the requirements for a firmware SSCC. (See Figure 3.)			
IX. In SSCC Mode			
SCRI	28	24	Synchronous clock receive. TTL input. Data from the MAP is valid on the rising edge of the clock.
SCTI	42	38	Synchronous clock transmit. TTL input. Data to the MAP is strobed in on the rising edge of this clock.
RX	26	19	Receive data from MAP. TTL input.
TDOUT	62	63	Transmit data to MAP. TTL output.
GPO	45	45	General purpose output. TTL/CMOS compatible. RAM bank select. (SC11091 only).[1]
S_{IN}	9	80	Input bit 7 of Data Register. Serial input to UART when XUART set low.
S_{OUT}	3	72	UART serial output when XUART set low.
IO_4	3	72	General purpose output when XUART set high. Output follows the state of Bit 6 of Data Register.
X. In Big MAC mode			
IO_0-IO_3	26, 28, 42, 45	19, 24, 38, 45	General I/O Port, TTL/CMOS, tri-state. Each I/O can be configured as input or output under the control of GIO register. Not available on the SC11095.[2]
IO_5	9	80	General purpose input when XUART is set high. Readable on bit 7 of the data register.

NOTE 1: The UMAC can be configured to emulate the BigMAC (SC11021) which has four IO pins and a TDOUT pin added. For the UMAC, the functions of these 5 pins are preserved on power up or reset. When the SSCC mode (GCRI:B0 = 1) is selected, the functions of these 5 pins will conform to the requirements for a firmware SSCC. (See Figure 3.)

NOTE 2: IO_3/GPO pin is at ground on SC11095.

CONNECTION DIAGRAMS





INTERFACE BLOCK DIAGRAMS

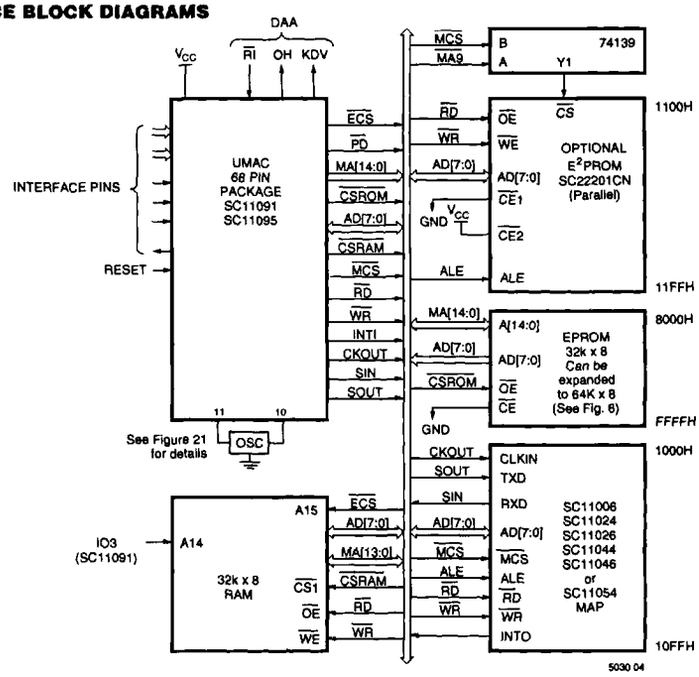


Figure 2a. UMAC 68 Pin Package Interfaces to MUX E²PROM, ROM Map

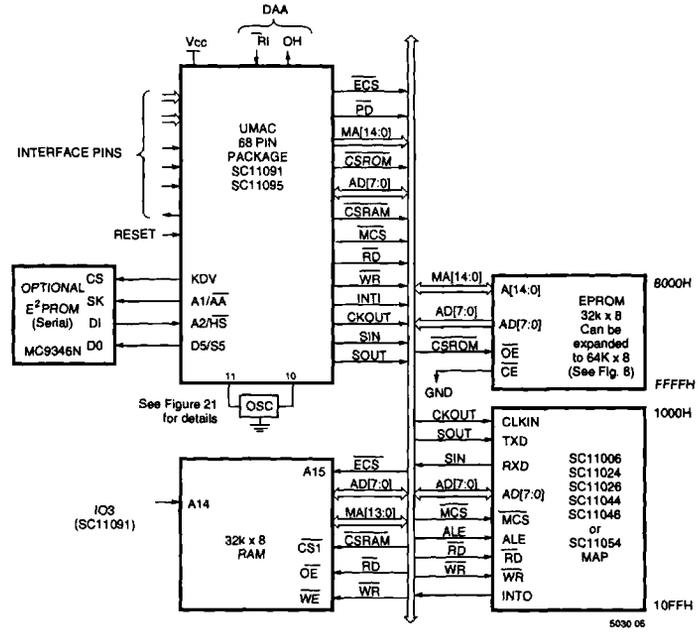


Figure 2b. UMAC 68 Pin Package Interfaces to Serial E²PROM, ROM Map for Serial Interface Configurations

INTERFACE BLOCK DIAGRAMS (continued)

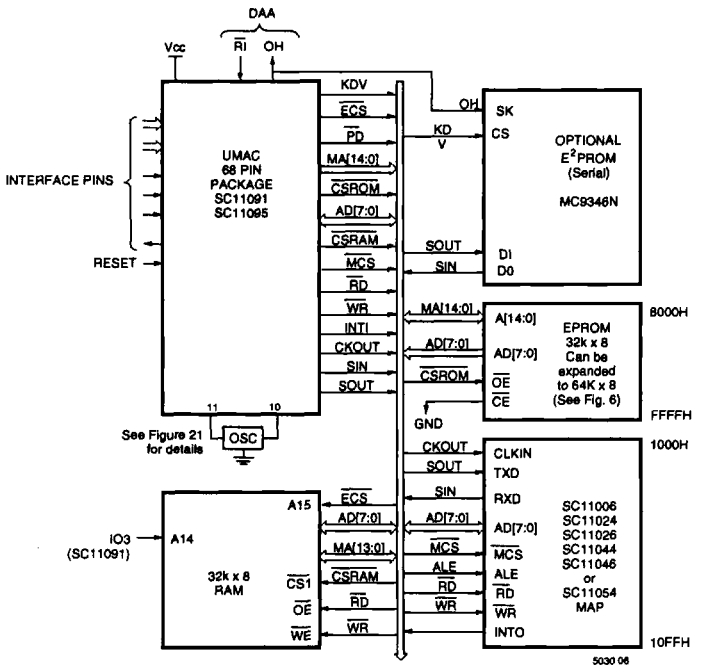


Figure 2c. UMAC 68 Pin Package Interfaces to Serial E^2PROM, ROM Map for Parallel Interface Configurations

FUNCTIONAL DESCRIPTION

The UMAC (Universal MAC) incorporates all the features of MAC (SC11011), BIGMAC (SC11021) and FastMAC (SC11061) plus other enhancements for greater capability and added value.

New Features (compared to SC11011, SC1021, SC11061)

The UMAC has External ROM address space of 64K. On power up the original 32K ROM is selected. A register select is provided to switch over to the expanded 32K ROM using the ECS pin. Bank switching is simplified through the use of instruction activated address synchronization.

Whereas the other controllers are built with 8 or 16K of internal ROM, the UMAC is designed to always use external ROM. Its internal ROM is just 256 bytes. This is for the purpose of program execution at startup and execution during power down mode. Expanded internal RAM of 384 bytes allows for more features including buffering for Fax and asymmetrical modem protocols such as V.23.

The external RAM space of the SC11091 is doubled to 32K. The original 16K address space is allocated to RAM but provision is made for bank switching to select 32K as required for full V.42bis implementation. The SC11095 will access 16K RAM space only, due to the fact that the IO_3 pin (used for bank switching) is disabled. This prohibits the use of this part in V.42bis implementations.

In Power Down (or Standby) mode, the internal CPU clock is divided by 32 to reduce power while still remaining active and ready to respond to any input. The chip is placed in this mode by the external ROM firmware which will set the power-down bit when it determines there is no activity. The power-down bit is reset by hardware when DTR, CS, SIN or RI signals go true. An internal program loop monitors this bit and returns to normal modem operations when it is reset. By using the internal ROM for this loop, the external ROM may be de-selected so its power dissipation is minimized. A power-down mode indication is available from the $\overline{PD}$ pin to control external power switches.

In normal operation, the $\overline{PD}$ pin behaves as a tristate pin. When power down is activated, the $\overline{PD}$ pin becomes output active low. It can be used to drive an LED indicator.

By means of register selection, the RDY interface for the parallel PC can be de-activated. This is to cater to certain LAP TOP applications where the RDY line is not supported.

When the UMAC is first powered up or reset, it defaults to Big MAC mode, which is also the mode for MAC (11011). All programs written for ROMless Big MAC (11021) and MAC (11011) or the FastMAC (11061) should run with no or minimal modifications.

Weak pullups are provided on switch inputs so that external pullup resistors are not needed when option switches are employed.

Internal multiplexing for asymmetrical protocols such as V.23 (1200/75 bps) is provided to allow both answer and originate modes without additional chips.

The former EA pin of MAC and Big MAC (pin 27) is redefined on the SC11091 to indicate power down status and re-named $\overline{PD}$. (Since the SC11091 always requires external ROM, the External Access option is not used.) On power down activation $\overline{PD}$ pin becomes output low. Otherwise it is tristated.

The SC11011 requires a 19.6608 MHz crystal. The SC11061 (Fast MAC) requires a 29.4912MHz crystal. The UMAC has a selectable internal clock divider so it can be used with either crystal. Start-up assumes a 19.6608 MHz crystal for compatibility with SC11011 or SC11021.

Functions in common with SC11011

The SC11091 interfaces to a parallel system bus, such as that in the IBM PC, or by changing one bit in a register it interfaces to an RS232 port.

The UMAC receives 4-bit signal samples from the MAP and performs adaptive equalization, carrier phase recovery, data decode, and descrambling.

The UMAC is interrupted once every 1.667 msec (600 Hz). It reads two I channel samples and two Q channel samples (T/2 sampling) within 100 µsec of receiving the interrupt.

After the samples are processed, a quad-bit (4 bits) of descrambled data is written back to the MAP. The MAP performs the synchronous to asynchronous conversion function, if operating in asynchronous mode, and outputs the received data on the RXD pin.

The UMAC uses a bit slice core processor to perform the digital signal processing (DSP) and the control functions. Its instruction set is a subset of the Intel 8096 instruction set but operates faster than the 8096. For instance, a signed (2's complement) 16 bit x 16 bit multiply with 32 bit result takes 3.5 µsec when operating with 19.6608 MHz crystal or 2µs with a 29.4912 MHz crystal. (Intel 8096 takes 6.5 µsec with a 12 MHz clock.)

When a 29.4912 MHz crystal is used, the ROM code must select a divide by 3 internal clock divider for compatibility with SC11061.

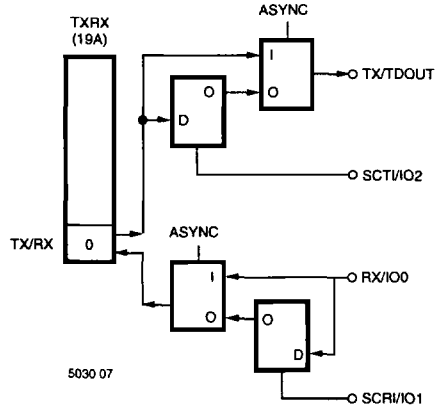


Figure 3a. Simplified Schematic of 1 bit SSCC

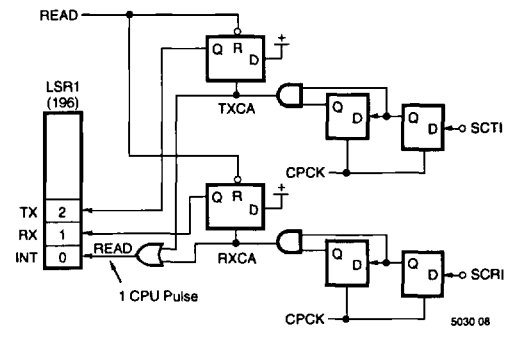


Figure 3b. SSCC Interrupt Circuit (Simplified)

FIRMWARE ARCHITECTURE

The SC11091/SC11095 uses a subset of 8096 instructions and can be compiled with an 8096 cross assembler such as AD2500. Rev 4.0x of this assembler is strongly recommended.

Operand Types

1. Short Integers: Short integers are 8-bit signed 2's complement variables. Results outside the range –128 and +127 will set the overflow bit in the Program Status Byte (PSB). There are no alignment restrictions on short integers.

2. Integers: Integers are 16-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –32768 and +32767 will set the overflow bit in the PSB. The least significant byte of the integers is in the even byte address and the next most significant byte is in the next higher (odd) address. Therefore, the integers must be aligned at even byte boundaries in the address space. The address of a word is the address of its least significant byte (always an even address).

3. Bits: The bits within the bytes of the register file are numbered from 0 to 7 with 0 referring to the LSB. The only instructions that use bit addressing are JBC and JBS.

4. Long Integers: Long integers are 32-bit signed 2's complement variables. The result of a 16 x 16-bit multiply will be stored in a long integer. Only SHRL and SHLL manipulate this data type. Long integers are addressed by the address of their least significant byte in the register file. They must be aligned such that their address is evenly divisible by 4. The most significant byte of a long integer resides on "address" +3, where "address" is the long integer's address.

Operand Addressing

Three types of addressing are allowed:

1. Immediate Addressing: This is a direct field within the instruction. For short integers, this is an 8-bit field, whereas, for the integers this is a 16-bit field. Only one operand within an instruction can be an immediate reference type. This operand must always be the last (right most) operand within an instruction.

   e.g. ADD AX, #340H is allowed
   ADD AX, #340H, BX is NOT allowed
   ADD AX, BX, #340H is allowed

2. Register Direct Addressing: In this mode, an 8-bit field is used to access a register from the 384 byte register file. The register address must conform to the alignment rules. Only register addresses 0–255 may use direct addressing.

   e.g. ADD AX, BX :AX, BX must be "even" numbers
   ADDB AX, BX :AX, BX can be "odd" or "even"

3. Indirect Addressing: A memory location can be addressed indirectly by placing its 16-bit address in the register file. Only one operand (the right most operand) within an instruction can be indirect.

   e.g. ADDB AL, BL, [CX] is allowed
   ADDB AL, [CX], BL is NOT allowed

Software Considerations for SSCC Implementation

The one bit SSCC approach saves a significant portion of hardware needed to implement the SSCC. The drawback is that the workload of the CPU is increased to emulate the SSCC. When operated at 1200 baud, the time window between data bits is 833 µs and at 2400 baud, it is 417 µS. The CPU must juggle between UART communication and DSP execution.

The following items should be considered:

SDLC:

1. Send flags (01111110) for start, stop or idle operation. (SC11054 Sendfax MAP included hardware flag detectors)
2. For data and CRC result, a zero must be inserted after five ones has been transmitted.
3. If five ones have been received and the next bit is zero, this zero bit is deleted
4. Detection of flag (01111110) or abort (11111111) sequence.
5. Generation and checking of CRC-CCITT or the newer CRC-32 for 32 bit CRC.
6. Interpret, transmit and receive error conditions and make corrective actions for data integrity.

BISYNC & MONOSYNC:

1. Generation and detection of SYNC character.
2. Selectable character length.
3. Parity may be included.
4. 6 or 8 bit (12 or 16 for bisync) sync character.
5. Detect escape sequence to prevent false sync detection and exclusion from CRC-16 calculation and checking.
6. Go into hunt mode to detect sync characters.
7. Interpret transmit and receive error conditions and make corrective actions for data integrity.

ASYNC:

1. Generation and detection of start and stop bits.
2. Selectable character length.
3. Parity may be included.
4. Selectable baud rates. Autobauding may be required. Independent baud rates for transmit and receive may be needed.
5. In MNP operation, CRC-16 generation and checking are required.
6. In MNP operation, detect escape sequence to prevent false sync detection and exclusion from CRC-16 calculation and checking.
7. Intepret transmit and receive error conditions and make corrective actions for data integrity.

Interrupt Structure

Five interrupt sources exist in the UMAC, namely the external interrupt, timer interrupt, ring leading edge interrupt, SSCC and UART interrupt. The interupt service routine address is 2004H.

1. External interrupt: A low to high transition on the INTI pin initiates this interrupt.
2. Timer interrupt: Timer overflow interrupt—frequency set by PSB bit 6 or GCR2 bits 2 and 3.
3. Ring leading edge: Interrupt generated by leading edge of ring input.
4. UART interrupt: Interrupt from UART.
   a. Parallel version: From UMR register. Any one of the following can generate this interrupt:
      - RBR was read by external processor
      - Data was transferred from THR to TSR
      - LCR was changed
      - MCR was changed
      - DLL or DLM was changed
   b. Serial version: In this configuration the interrupt signal from 16C450 compatible UART is brought in as an interrupt source to the internal CPU.
5. SSCC Interrupt.

INSTRUCTION SET

The UMAC instruction set is a subset of Intel 8096 instruction set. The object codes, formats and the flags they effect are identical to those of 8096. The differences are:

- No VT or ST flags exist in the UMAC.
- Register locations in the UART section can only be accessed by using indirect addressing.
- The operands refer to one or more bytes of the register file. ROM locations can only be addressed using indirect addressing.
- If a memory location is addressed between 1000H and 12FFH, an external six clock multiplexed bus operation is initiated. The multiplexed address/data will use AD_7–AD_0 bus.
- When using ST or STB operations, the destinations are always considered to be indirect addresses.

  e.g. ST, AX, [BX] is allowed

  ST, AX, BX is NOT allowed

Location	Name	PC address	7	6	5	4	3	2	1	0
180H	RBR	0 (DLAB=0)	DATA.7	DATA.6	DATA.5	DATA.4	DATA.3	DATA.2	DATA.1	DATA.0
181H	IER	1 (DLAB=0)	0	0	0	0	EDSSI	ELSI	ETBEI	ERBFI
182H	IIR	2	0	0	0	0	0	ID.1	ID.0	PENDING
183H	LCR	3	DLAB	SB	PARITY	EPS	PEN	STB	WLS1	WLS0
184H	MCR	4	0	0	0	LOOP	OUT2	OUT1	RTS	DTR
185H	LSR	5	0	TEMT	THRE	BI	FE	PE	OE	DR
186H	MSR	6	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
187H	STR	7	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
188H	DLL	0 (DLAB=1)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
189H	DLM	1 (DLAB=1)	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
18BH	UMR		RTRST	CM	RDI	DLF	LCF	TXF	RXF	MCF

Table 2a. SC11091 UART Registers

Location	Name	7	6	5	4	3	2	1	0
18DH	SWP	—	S6	S5	S4	S3	S2	S1	S0
18EH	DIR	—	—	—	—	DIR3	DIR2	DIR1	DIR0
18FH	DAR	DAR7	DAR6	DAR5	DAR4	DAR3	DAR2	DAR1	DAR0
190H	GCR	CONF	OH	KDV	MRDY	AA	HS	PAGE	PD
191H	TIM	TFF7	TFF6	TFF5	TFF4	TFF3	TFF2	TFF1	TFF0
192H	PSB	$\overline{PD}$	ROBK/TM	IP	IE	Z	N	C	V
193H	ICR	EXT_ENA	TIMER_ENA	RING_ENA	UART_ENA	EXTERNAL	TIMER	RING	UART
194H	GCR1	SSCC_GPD	SSCC_SC	SSCC_AEE	SSCC_LLB	SDLC	USART	USART	SSCC
195H	GCR2	OSC0	OSC1	TIMER0	TIMER1	ROM64K	BANKSW_ENA	—	NORDY
196H	LSR1	—	—	—	—	—	SSCC_INT	RX_AVA	TX_EMPTY
199H	ITEN	—	—	—	—	—	—	RX_INT_ENA	TX_INT_ENA
19AH	TX/RX	—	—	—	—	—	—	—	—

Table 2b. SC11091 Internal Registers

ACCESSIBLE UART REGISTERS

UART Interrupt Enable Register (IER, location 181H)

The 8-bit register enables the four types of interrupts of the UART to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 1 and are described below. **NOTE:** IIR and IER should be used as Read Only in Parallel Configuration.

Bit Number	Bit Name	Description
0	ERBFI	This bit enables the Received Data Available Interrupt when set to logic 1.
1	ETBEI	This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.
2	ELSI	This bit enables the Receiver Line Status Interrupt when set to logic 1.
3	EDSSI	This bit enables the MODEM Status Interrupt when set to logic 1.
4–7		These four bits are always logic 0.

Interrupt Identification Register (IIR, location 182H)

The UART has on-chip interrupt capability that allows for flexibility in interfacing popular micro-processors presently available. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identifi-cation Register (IIR). When ad-dressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts change the IIR, even though they are recorded, until the particular interrupt is serviced by the CPU. The contents of the IIR are described below.

Bit Number	Bit Name	Description
0		This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.
1–2		Interrupt ID bits.These two bits of the IIR are used to identify the highest priority interrupt pending as indicated below.
3–7		These five bits of the IIR are always logic 0.

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

ACCESSIBLE UART REGISTERS (continued)

Line Control Register (LCR), location 183H

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in the following table.

Bit Number	Bit Name	Description
0–1	WLS0–WLS1	Word Length Select Bits. These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows: BIT 1 / BIT 0 / WORD LENGTH 0 0 5 Bits 0 1 6 Bits 1 0 7 Bits 1 1 8 Bits
2	STB	Number of Stop Bits. This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the programmed number of Stop-bits selected.
3	PEN	Parity Enable. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)
4	EPS	Even Parity Select. This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.
5		Stick Parity. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0, then the Parity bit is transmitted as a 1.
6	SB	Set Break. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has not effect on the transmitter logic. **Note:** This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break. 1. Load an all 0s, pad character, in response to THRE. 2. Set break after the next THRE. 3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored. During the break, the Transmitter can be used as a character timer to accurately establish the break duration.
7	DLAB	Divisor Latch Access Bit. It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

ACCESSIBLE UART REGISTERS (continued)

Modem Control Register (MCR), location 184H

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 6 and are described below.

Bit Number	Bit Name	Description
0	DTR	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
1	RTS	This bit controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.
2	OUT1	Auxiliary user-designated bit. It is connected to MSR[6] (RI) during local loopback.
3	OUT2	Auxiliary user-designated bit. It is connected to MSR[7] (DCD) during local loopback. When Out2 = 0, INTO pin is Hi-Z.
4	LOOP	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input: the four MODEM Status Register bits CTS, DSR, DCD and RI are disconnected internally; and the four MODEM Control Register bits DTR, RTS, OUT1 and OUT2 are internally connected to the four MODEM Status Register inputs, and the MODEM Control output pins RLSD, CTS, DSR are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART.
	In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.	
5–7	These bits are permanently set to logic 0.	

Line Status Register (LSR), location 185H

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are described below.

Bit Number	Bit Name	Description
0	DR	Data Ready indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.
1	OE	Overrun Error indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.
2	PE	Parity Error indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.
3	FE	Framing Error indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

ACCESSIBLE UART REGISTERS (continued)

4	BI	Break Interrupt indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word trans-mission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator. **Note:** Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.
5	THRE	Transmitter Holding Register Empty indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.
6	TEMT	Transmitter Empty indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.
7		This bit is permanently set to logic 0. **Note:** The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Modem Status Register (MSR), location 186H

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU in addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are described below.

Bit Number	Bit Name	Description
0	DCTS	This bit is the Delta Clear to Send indicator. Bit 0 indicates that the CTS input to the chip has changed state since the last time it was read by the CPU.
1	DDSR	This bit is the Delta Data Set Read indicator. Bit 1 indicates that the DSR input to the chip has changed state since the last time it was read by the CPU.
2	TERI	This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the chip has changed from a low to a high state.
3	DDCD	This is the Delta Data Carrier Detect indicator. Bit 3 indicates that the DCD input to the chip has changed state. **NOTE:** Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.
4	CTS	This bit is the complement of the Clear to Send input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR. Read/Write inparallel mode.
5	DSR	This bit is the complement of the Data Set Ready input. If bit 4 of the MCR is set to a 1, this bit is equivalent of DTR in the MCR. Read/Write inparallel mode.
6	RI	This bit is the complement of the Ring Indicator input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR. Read only.
7	DCD	This bit is the complement of the Data Carrier Detect (DCD) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR. Read/Write is in parallel mode. Always = 1 in serial mode.

Scratchpad Register (STR), location 187H

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

ACCESSIBLE UART REGISTERS (continued)

UART Monitor (UMR), location 18BH

The UART Monitor register allows the processor to monitor UART operations. A read operation to the UART Monitor register will clear Bit 0 to Bit 4. UMR should be used instead of IIR in parallel configurations.

Bit Number	Bit Name	Description
0	MCF	Modem Control Flag. This bit indicates if the modem control register has been written.
1	RXF	Receive Buffer Empty Flag. This bit indicates if the last character has been read from the receive buffer.
2	TXF	Transmit Buffer Full Flag. This bit indicates if a new character is in the transmit shadow register.
3	LCF	Line Control Flag. This bit indicates if the line control register has been written.
4	DLF	Divisor Latch Flag. This bit indicates if a new baud rate count has been written to the Divisor Latch.
5	RDI	Receive Data Input. This bit monitors the RXD input of the UART.
6	CM	UART Command/Modem Output. When set HIGH the UART is placed in modem mode. At reset it is low in command mode. This bit together with BI in LCR are used for bit by bit echoing. In serial version the user can set BI = 1 and CM = $\overline{RDI}$ to echo a bit. When CONF = 1 for normal operation set CM = 1.
7	RTRST	Reset receiver and transmitter. When set high, both receiver and transmitter will be put into reset state.

INTERNAL REGISTERS

Switch Port (SWP), location 18DH—for serial version only

The Switch Port is a 7-bit input port used only in the serial version of the MAC. It allows for reading of the external switches of a stand-alone modem. Only S0–S2 are available on the 44 pin SC11020CV.

Bit Number	Bit Name	Description
0–6	S 0–6	Switch Input. These bits monitor external switches.
7		Unused.

Direction Register (DIR), location 018EH

Bit Number	Bit Name	Description
0	DIR0	When HIGH, IO0 is an output. When LOW, IO0 is an input.
1	DIR1	When HIGH, IO1 is an output. When LOW, IO1 is an input.
2	DIR2	When HIGH, IO2 is an output. When LOW, IO2 is an input.
3	DIR3	When HIGH, GPO/IO3 is an output. When LOW, GPO/IO3 is an input. (N/A if GCR1 bit 0=1).
4–7		Unused.

Data Register (DAR), location 018FH

Bit Number	Bit Name	Description
0–3	DAR0–3	Output to IO0–3.
4	DAR4	When set HIGH, DAR5 is output to TDOUT pin. When set LOW, SOUT or SIN is output to TDOUT pin when GCR bit 7 (CONF) is set LOW or HIGH respectively. See Figure 11.
5	DAR5	This bit is routed to TDOUT pin when DAR4 is set HIGH.
6	DAR6	Write Only to SOUT (pin 3) if XUART = 1.
7	DAR7	Read Only from SIN (pin 9).

General Control Register (GCR), location 0190H

GCR contains a miscellaneous set of control and status bits.

Bit Number	Bit Name	Description
0	$\overline{PD}$	Power Down Mode. Read Only. Can be used as input when not using Power Down Function.
1	PAGE	Register Page Bit. This bit selects the active register page. When LOW, the lower 256 registers are accessed during register operations and when HIGH, the upper page is active.
2	HS	Active HIGH HS indicator. When high this bit sets the $\overline{HS}$ pin low.
3	AA	Active HIGH AA indicator. When high this bit sets the $\overline{AA}$ pin low.
4	MRDY	Modem ready.
5	KDV	KDV Output. Data/Voice Relay Control. When high, the modem is in the voice mode.
6	OH	Off Hook Output. When set HIGH, the phone will be placed off hook.
7	CONF	Configuration output. This bit controls the state of the MAC configuration. When HIGH, the MAC is configured with the SERIAL interface. It is configured with the PARALLEL interface after a reset.

INTERNAL REGISTERS (continued)

Timer (TIM), location 191H

The Timer includes an 11 bit counter and a timer flip-flop. It is used to aid software timing functions. The counter is readable only in autobaud mech (GCR2.6 = 1. See Hardware Autobaud section). It can only be reset by a write. The timer flip-flop can be read to test if it is already set.

The counter and flip-flop will be reset on a write (value is don't care). After that the counter sends out a pulse train at 4.8 kHz rate to set the timer flip-flop. The flip-flop can be cleared on a read. The Timer is constantly counting by the internal clock (9.8304 MHz).

Bit Number	Bit Name	Description
0	TFF0	Timer flip-flop bit.
1–7	TFF1–7	Seven bit autobaud timer result if GCR2.6 = 1.Program Status Byte (PSB), location 0192H

This is an 8-bit register storing the condition flags of arithmetic, shift, and compare instructions. The programmer can access these bits by using address 0192H. Only bits 4, 6 and 7 are writeable by software.

Bit Number	Bit Name	Description
0	V	Overflow bit; indicates the last arithmetic operation produced an overflow.
1	C	Carry bit; indicates the state of the arithmetic carry from the most significant bit of the ALU for an arithmetic operation or the state of the last bit shifted out of the operand for a shift. Arithmetic "Borrow" after a subtract is the complement of the C flag (i.e. if borrow generated then C = 0).
2	N	Negative bit; indicates the last arithmetic or compare instruction produced a negative result.
3	Z	Zero bit; indicates the last arithmetic or compare instruction produced a zero result.
4	IE	Global interrupt enable bit; when zero, all interrupts are disabled.
5	IP	Global interrupt pending bit. Set upon receipt of interrupt. Cleared when interrupt service begins. (Read only.)
6	ROBK/TM	ROM bank switch when GCR2.5 = 1 else set TIMER rate TIM, location 191H, 0 = 4.8 kHz, 1 = 19.2 kHz.
7	$\overline{PD}$	Power-Down enable bit. Set HIGH to power down. Set LOW to power-up. Hardware reset on RI, DTR on in serial mode or RI, CS true in parallel mode.

Interrupt Control Register (ICR), location 0193H

This is an 8 bit register to enable or disable four of the five interrupt sources and to record the interrupt sources. The upper four bits are read/write registers while the lower four bits are read only registers. A read operation to the register will automatically clear the lower four bits.

Any one of these four interrupts will drive the processor to address 2004H. From there the software can check interrupt sources and do priority control to branch to different service routines.

The SSCC Interrupt enable bits are located in Interrupt Enables, ITEN, address 199H. The transmit bit and receive bit interrupts may be independently enabled/disabled. The interrupt pending bits are located in Line Status 1, LSR1, address 196H. Bit zero = 1 indicates an SSCC interrupt occurred. If either Bit 0 or Bit 1 of ITEN are set, the processor will be forced to address 2004H on each SSCC interrupt. LSR1 Bit 1 = 1 for RX bit interrupt and LSR1 Bit 2 = 1 for TX bit interrupt. A Read to LSR1 resets all bits.

Bit Number	Bit Name	Description
0		"1" indicates UART requested an interrupt.
1		"1" indicates RING leading edge requested an interrupt.
2		"1" indicates TIMER overflow requested an interrupt.
3		"1" indicates EXTERNAL source requested an interrupt.

INTERNAL REGISTERS (continued)

Bit Number	Bit Name	Description
4		"1" to enable UART interrupt.
5		"1" to enable RING leading edge interrupt.
6		"1" to enable TIMER overflow interrupt.
7		"1" to enable EXTERNAL interrupt.

General Control 1 (GCR1), location 0194H

This register controls the switching between the SSCC and the UART (in MAC or Big MAC), and selects the SSCC modes.

Bit Number	Bit Name	Description
0		SSCC select. When high, the SSCC is connected to the MAP for MNP operation. Default is low after reset.
1–2		SSCC modes: The SSCC defaults to synchronous mode if B1 and B2 are not set to high. The program can use this as a flag when performing the function of the software SSCC by reading the status of these 2 bits. For async mode B1 and B2 must be set high. 0 0 Indicate SDLC mode select. 1 0 Indicate BISYNC mode select. 0 1 Indicate MONOSYNC mode select. 1 1 ASYNC.
3		XUART. When high, the UART is disconnected from the SIN and SOUT pin. These 2 pins can then be used for general purpose IO.
4		SSCC LOCAL LOOPBACK. When high, the internal trans-mitted data is routed back to the receiver as well as to the Tx output pin. Default is low after reset.
5		SSCC AUTO ECHO ENABLE. When high, signal into the Rx pin is routed to the Tx pin but the receiver still listens to the Rx input. Transmitted data from the SSCC is not routed to the Tx pin. Default is low after reset.
6		SCTI SCRI CONNECT . When high, the transmit clock input SCTI drives the receive clock internally. The SCRI serves as a general purpose input and its state is readable in DAR1 (Bit 2, reg 18FH in Big MAC).Default is low after reset.
7		GPO. The state of this bit sets the general purpose output port at pin GPO. This bit can be used to indicate SSCC operation or bank switching of the external RAM. Default is low after reset.

General Control 2 (GCR2), location 0195H

Clock divide for crystal oscillator, timer frequency, and SSCC modes are selected in this register.

Bit Number	Bit Name	Description
0–1		OSCILLATOR DIVIDE 0 0 OSC DIV 3. For 29.4912 MHz crystal. 0 1 OSC DIV 2. For 19.6608 MHz crystal. This is the default after reset. 1 0 reserved 1 1 reserved
2–3		TIMER FREQUENCIES 0 0 4800 Hz TIMER. Timer interrupts once every 208.33uS. This is the default state. 1 0 9600 Hz TIMER. Timer interrupts once every 104.16uS. 0 1 19200 Hz TIMER. Timer interrupts once every 52.08 uS. 1 1 38400 Hz TIMER. Timer interrupts once every 26.04 uS.
4		ROM CONFIG. This bit determines the configuration for the extended ROM. If this bit is 0, two 32K x 8 ROMS are used. If this bit is 1, a single 64K x 8 ROM is used. Refer to Figure 7 for clarification. Default is low after reset.

INTERNAL REGISTERS (continued)

Bit Number	Bit Name	Description
5		ROM EXTENSION ACTI-VATE. This bit should be set high to activate bank switching. Default is low after reset.
6		Unused.
7		NORDY. When set high, the parallel interface operates without the need of the RDY pin.

Line Status 1 (LSR1), location 196H

This register contains the status of the transmit and receive buffers. It also includes the interrupt status.

Bit Number	Bit Name	Description
0		SSCC request interrupt. A high indicates that any of the SSCC enabled interrupt sources request-ed an interrupt. This bit is cleared after this register is read.
1		Rx bit available. A high indicates that a bit is available in the receive buffer. If the receive interrupt is enabled, an interrupt will be requested. This bit is cleared after this register is read.
2		Tx Buffer Empty. This bit is set to a "1" when a bit is shifted out of the transmit buffer. If the transmit interrupt is enabled, an interrupt will be requested. It is reset when a character is loaded into the transmit buffer. This bit is set to "1" after a reset.
3–7		Unused.

SSCC Interrupt Enable Register (ITEN location 199H)

Bit Number	Bit Name	Description
0		Transmit Interrupt Enable. When set high, the transmitter request an interrupt whenever the transmit buffer becomes empty. Default is low after reset.
1		Receive Interrupt Enable. When set high, the receiver request an interrupt when the Rx Buffer indicates character available. Default is low after reset.
2–7		Unused.
		The present architecture allows interrupt to the CPU (if enabled) each time the SCR or SCT clocks change to a 1. Asynchronous receive data can also interrupt the CPU. This relieves the CPU from having to scan the status continously.

TX/RX Buffer (TX/RX), location19AH

Transmit and receive bit are communicated through the LSB (B0) of the read and write register.

MNEMONIC	NO. OF OPERANDS	OPERATION	BYTES[1]	TIME[2]
ADD/ADDB	2	B ← A + B	3	10
ADD/ADDB	3	D ← A + B	4	10
AND/ANDB	2	B ← A AND B	3	10
AND/ANDB	3	D ← A AND B	4	10
CMP/CMPB	2	D – A	3	10
DJNZ	1	Decrement & JNZ	3	9/12
EXTB	1	Sign Extend Byte	2	7
JBC	0	Jump if bit clear	3	10/13
JBS	0	Jump if bit set	3	10/13
JC	0	Jump if Carry Set	2	5/8
JNC	0	Jump if no carry	2	5/8
JE	0	Jump if =	2	5/8
JNE	0	Jump if not =	2	5/8
JGT	0	Jump if >	2	5/8
JGE	0	Jump if >=	2	5/8
JLE	0	Jump if < or =	2	5/8
JLT	0	Jump if <	2	5/8
JV	0	Jump if Overflow	2	5/8
JNV	0	Jump if no overflow	2	5/8
JH	0	Jump if higher	2	5/8
JNH	0	Jump if not higher	2	5/8
LCALL	0	Long Call	3	11
LD/LDB	2	Load	3	10
MUL	3	D ← A * B	5	33
NOP	0	NO Operation	1	2
OR/ORB	2	D ← D OR A	3	10
XOR/XORB	2	D ← D XOR A	3	10
PUSHF	0	Push PSB	1	5
POPF	0	Pop PSB	1	5
RET	0	Return	1	10
SHL/SHLB	1	Shift Left	3	$11 + N^3$
SHLL	1	Shift Left Long	3	$15 + N^3$
SHR/SHRB	1	Shift Right	3	$11 + N^3$
SHRL	1	Shift Right Long	3	$15 + N^3$
SHRA	1	Arith. Right Shift	3	$10 + N^3$
SHRAL	1	Arith. Right Long	3	$15 + N^3$
SJMP	0	Short Jump	2	7
LJMP	0	Long Jump	3	9
ST/STB	2	Store to Memory	3	13[4]
SUB/SUBB	2	B ← B – A	3	10
SUB/SUBB	3	D ← B – A	4	10

NOTE 1: Add one for immediate words.

NOTE 2: Add 9 for indirect mode and 2 or 0 for immediate mode—see table. (Cycle times @ 1.02 ns) for 19.6608 MHz crystal or 68 ns for 29.4916 MHz crystal)

NOTE 3: N is number of bit shifts.

NOTE 4: Indirect Mode.

Table 2. Instruction Set

HARDWARE ARCHITECTURE

The UMAC device is organized with two buses that interconnect four main logic sections. The two buses are the internal data bus (DB) and address bus (Y). The four sections of the device are the internal processor, registers, memory, and dual port UART.

The two bus architecture was chosen to allow the UMAC to execute the 8096 instruction set as fast or faster than the 8096 itself. The device is intended to run at 9.8304 MHz or 14.745MHz. (The internal divider provides these clock speeds from an external 19.6608 MHz or 29.4912 MHz crystal.) A typical three operand instruction effectively executes in 10 clock cycles. The signed 16 x 16 multiply operation requires 34 clock cycles.

The internal data bus (DB) is the main bus of the device. It is an 8-bit bus that interconnects all four sections of the device. All internal data travels on DB. The Y bus is a 16-bit output only bus fromthe internal processor that provides addresses to the memory and register sections of the device. This bus allows memory control to be resident inside the internal processor without degrading performance.

The internal processor controls UMAC operations and performs all of the required computation functions. The internal processor consists of a microcontrol PLA and a 16-bit registered arithmetic/logic unit (RALU). The microcontrol PLA accepts as input 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU performs instruction execution, operand address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. The RALU is implemented with the 2901 silicon compiler.

The register section of the UMAC includes RAM and the ports of the device. Code can't be executed from registers; however, it can be executed from external RAM or ROM. The UART registers are functionally, but not physically, part of the register section. The UART registers are accessed via indirect addressing mode only. There are 384 bytes of RAM to support DSP functions and the command set. The memory section of the UMAC includes the program ROM and the external memory interface. The device contains 256 bytes of program ROM. The external memory interface allows the UMAC to access program storage or data storage from external memory.

The UART section of the device implements, in hardware, the industry standard 16C450 UART. In its parallel version the UMAC appears as a 16C450 to the user. The UART contains true dual-port capability to allow the user and the internal processor access to its internal registers.

Hardware Definition of the SSCC

Figure 3a shows a simplified diagram of the single bit Serial Synchronous Communication Circuit. In synchronous operation, the internally generated transmit signal is clocked out by the SCT clock and the received signal is clocked in by the SCR clock. In asynchronous, mode the latches are bypassed.Figure 3b shows how the SSCC interrupts are generated. Figure 4 shows the timing relation between the MAP to SSCC interface and the internal synchronization for clock and data.

The SSCC can be operated either in the synchronous or asynchronous modes. In synchronous mode, SCR and SCT clocks are supplied by the MAP. To operate in asynchronous mode, the CPU must generate the neccessary timing for the transmit and receive.

Synchronous Operation

If SSCC is selected and the SSCC mode select bits are both low, the SSCC operates in synchronous mode.

Receiver Operation—When SCR is low, the d_latch is enabled to pass in Rx input. When the SCR goes high, it latches the Rx input, generates a pulse of 1 cp period to interrupt the processor and sets the Rx available flip flop. When the CPU reads the Rx data, the Rx flip flop is reset. If the interrupt mode is disabled, the CPU can scan the Rx available flip flop to determine if data is available.

Transmitter Operation—To transmit a bit, the CPU writes the bit data into the transmit buffer. This resets the transmit buffer empty flip flop. When the SCT is low, this data bit passes through to the Tx (transmit) pin. When the SCT goes high, this data bit is latched. The SCT also causes an interrupt pulse and also sets the Tx Buffer Empty flip flop. If the interrupt mode is disabled, the CPU can scan the Tx Buffer Empty flip flop to determine if data has been strobed out.

Asynchronous Operation

If SSCC is selected and the SSCC mode select bits are both high, the SSCC operates in asynchronous mode.

Receiver Operation—The d_latch is always open. If the interrupt is enabled, a high to low transistion will generate an interrupt pulse and latch the Rx available flip flop. This interrupt should then be disabled until the character is fully assembled. The CPU must internally synchronize with the incoming data stream.

Transmitter Operation—The d_latch is always open. To transmit a bit, the CPU writes the bit into th

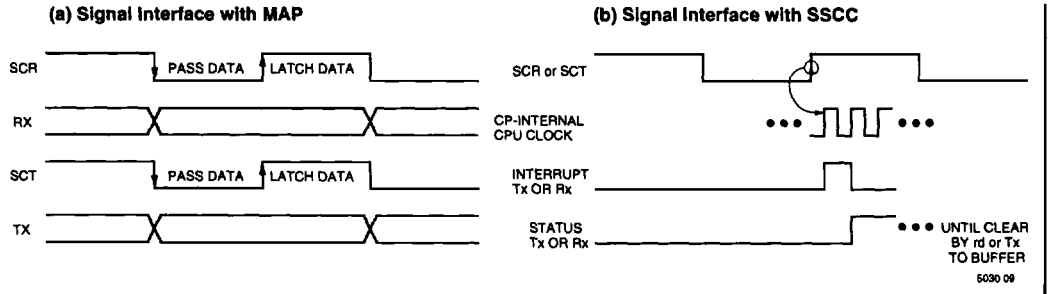


Figure 4. Synchronous Mode Timing

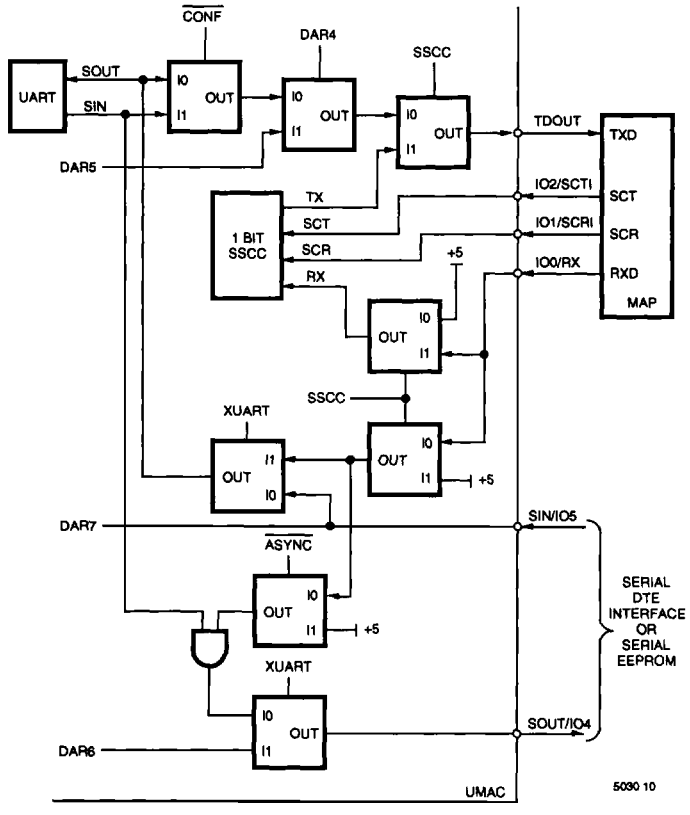


Figure 5a. UMAC Internal Data Path

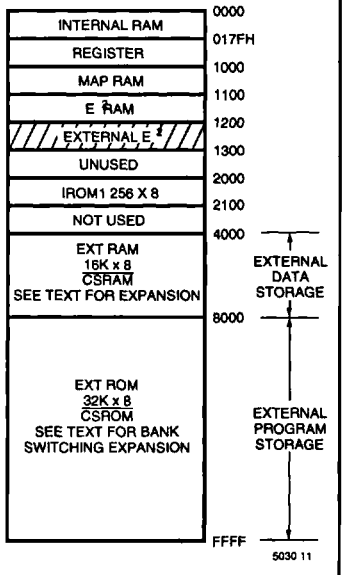


Figure 5b. UMAC Address Map

care of start stop bits and the timing to strobe the data out to the TX pin.

Other Modes of Operation

If the SSCC local loopback is set to 1, the transmitted data is routed back to the receive buffer.

If the Auto echo is set to 1, received signal is echoed back to the transmitter. The receiver will still receive the data.

If the SCTI SCRI is set to 1, the transmit clock provides clock input to the receiver.

Datapath & Description

Figure 5a shows the data path portion of UMAC. The function of the I/O pins affected by the UMAC is described. The rest of the I/O functions remains the same as SC11021. See GIO register information on page 27.

The control signals are described in Table 3 to aid analysis of the data path.

SIGNAL NAME	DESCRIPTION
SCC(B0 in GCR1)	When high, the firmware SSCC is selected for communication. Default is low after reset.
CONF	Refers to GCR bit 7 in MAC. When high, the configuration is serial. Default is low after reset.
DIR0-3	Direction registers as in GPIO of Big MAC (SC11021).
	When high, the IOs are defined as outputs. When low, they become inputs.
DAR0-5	Data registers as defined in Big MAC (SC11021).
DAR6-7	2 Additional registers utilizing the SIN and SOUT pins when UMAC is configured in parallel mode. DAR6 is output only and DAR7is input only.
XUART	Exclude UART. When high, signal from SIN and SOUT will not be communicated to the UART. When the UMAC has the SSCC selected and configured for parallel operation, this control enables the SIN pin to be used as an IO pin and SOUT to be used for an output pin. Default is low after reset.
$\overline{\text{ASYNC}}$	When bit B1 and B2 of general control register 1 (GCR1) are high, $\overline{\text{ASYNC}}$ will be low. The signal from the RX/IO0 can be directed to the SOUT/IO4 pin. This control enables full V.23 implementation of originate and answer mode without having to add external components to the route.

Table 3.

The following operating modes are allowed:

MODE	DESCRIPTION
Stand-alone	UART communicates with MAP and RS232. Conditions: SCC=0, DAR4=1, CONF=1, XUART=0, $\overline{\text{ASYNC}}$=0. This configuration is used to establish handshake.
Stand-alone	SSCC communicates with MAP. UART communicates with RS232. Conditions: SCC=1, DAR4=X, CONF=1, XUART=0, $\overline{\text{ASYNC}}$=1. This configuration is used for MNP and V.42bis operation.
Parallel	UART communicates with MAP andPC interface. Conditions: SCC=0, DAR4=0, CONF=0, XUART=1, $\overline{\text{ASYNC}}$=0. This configuration is used to establish handshake.
Parallel	UART communicates with PC interface. SSCC communicates with MAP. Conditions: SCC=1, DAR4=X, CONF=0, XUART=1. $\overline{\text{ASYNC}}$=1. This configuration is used for MNP and V.42 bis operation.
Stand-alone	UMAC operating as replacement for MAC (SC11011, 61) or Big MAC (SC11021). Conditions: SCC=0, DAR4=0, CONF=1, XUART=0, $\overline{\text{ASYNC}}$=0.
Parallel	UMAC operating as replacement for MAC or Big Mac. Conditions: SCC=0, DAR4=X, CONF=0, XUART=0, $\overline{\text{ASYNC}}$=1.

Clock Generation and Powerdown

The UMAC runs on either a 19.6608 MHz or 29.4912 MHz crystal. This frequency is divided by two and the 9.8304 MHz is used for internal hardware timing and for the CKOUT clock. When the UMAC is operated at 29.4912MHz (1.5X) the internal CPU clock remains at half the crystal oscillator speed. However, the UART baud rate, the timers and the CKOUT to the MAP are kept at the normal speed to maintain compatibility. This is done by setting the clock selection to divide by 3.

CKOUT—is maintained at 9.8304 MHz out. When the divide by 3 is selected, the CKOUT will be out of phase to the internal divide by 2 clock at certain cycles. When divide by 2 is selected, the CKOUT will be synchronized with the internal clock.

UART—Maintains the same base clock into the baud rate generator. This is achieved by modulating the counter input.

Clock selection. Register refers to bits B0 and B1 in GCR2.

REGISTER B0	B1	SELECT	CRYSTAL USED
0	0	divide by 3	29.4912 MHz
0	1	divide by 2	19.6608 MHz - default
1	x	reserved	

When switching from one frequency to another, the transitions are glitch free. The CKOUT is phase synchronized with the internal CPU clock when the divide by 2 is selected.

Power down mode is activated in the same manner as in BigMAC when bit 7 of the PSB byte is set high and inputs RI, CS, DTR and SIN are all high. The UMAC comes out of power down mode when any of the inputs or bit 7 of PSB is set low. A short subroutine loop is included in the UMAC ROM which examines bit 7 of the PSB byte. When it goes low, a return is executed and the external code execution resumes. By using the internal ROM for this function, there is no need to select the external ROM so that it can be in a low power state.

RDY Interface

The RDY pin is used to inject wait states to synchronize the UMAC with the PC's parallel access. Some Laptops do not incorporate this wait mechanism. By setting bit 7 in GCR2 high, the UMAC operates in the NO-RDY mode that interfaces to the PC without the need for the RDY pin.

MEMORY DESCRIPTION

Internal ROM:

The 256 bytes of internal ROM are located at 2000H to 20FFH.

The SC11091 controller is built with the same basic architecture as the SC11019/20/21/22/23 so that firmware will be upward compatible.

External Read/Write:

Three different types of external memory operations are defined.

A) For addresses from 1000H to 12FFH:

These external operations occur through the AD bus. These operations take six clock cycles, four more than internal operations. These are mainly for MAP & EEROM interfaces, however, instructions and data can also be fetched from these memory spaces.

B) For addresses from 4000H to 7FFFH:

These memory spaces are reserved for external DATA storage. The UMAC can access external RAM through MA address bus and AD data bus. There are six clock memory cycles for each access.

C) For addresses from 8000H to FFFFH:

The chip fetches instructions from external program storage by MA_0–MA_{14} and AD_0–AD_7. These operations are exactly the same as internal ROM fetch and they take 2 clock cycles.

Extended ROM bank switching and addressing

With increased code needed to service MNP and V.42bis classes of communication, the usual 32K ROM may not be sufficient to hold all the code. An improved method of hardware switching and software selection of the desired 32K ROM bank is implemented in the UMAC. No external Hardware decoder is needed to select the 2 ROM banks. However, one extra gate is needed to select the MAP when the 64k mode is used. The extended ROM can be two 32K x 8 ROMs (27256) or one 64Kx8 ROM (27512). Fig 6a and 6b show the two configurations. If two 32K x 8 ROMs are used, the ROM CONFIG bit in B4 of GCR2 must be set to 0 (default state). If one 64K x 8 ROM is used, then the ROM CONFIG bit is set to 1.

The ECS pin is used for the ROM extension. This is normally used for the EEPROM selection. If used for ROM extension, then the EEPROM must be addressed differently. The memory locations 1100H to 11FFH must not be accessed if extended ROM is used. Instead, the EEPROM access will be mapped at 1200H to 12FFH using the MCS pin as the chip select. External decoding is needed. Fig 6c shows how it is done.

If multiplexed EEPROM is not used, there is no need for this extra decoding.

The original ROM bank is called bank 0 and the extended bank is called bank 1. Bank 0 is the power-on or reset default when two 32K x 8 ROMs are used. However when one 64K x 8 ROM is used, the external ROM access starts at Bank 1 as the ECS pin is high by default. Switching from bank 0 to bank 1 is done using a method known as instruction activated bank switching. The 3 instructions LCALL, LJMP and RET will activate the ROM bank selection at the appropriate moment when a new address is strobed onto the memory bus. The advantage of this method is that interbank access can take place even when the program is executing from the external ROMs. Interrupts must be disabled in conjunction with changing the ROM bank so as to guard against erroneous bank changes due to the interrupt service routines.

The ROM selection bit is bit 6 of PSB (0192H). However this is currently used by Fast MAC (SC11061) for switching the timer from 4800Hz to 19.2kHz which presents a compatibility issue. The UMAC design satisfies both demands. On power up or reset, the PSB bit 6 is used for the timer selection. By setting bit 5 of GCR2 to 1, the function of the PSB bit 6 is changed to ROM select bit as defined. The timer frequencies can be selected from bits 2 and 3 in the GCR2.

The selection of the ROM banks during interrupt servicing is further enhanced by a modified PUSHF instruction. If bit 5 in the GCR2 is set to 1 to activate the ROM bank mode, the PUSHF instruction will set the PSB bit 6 to 0 after the PSB status is saved onto the stack. Thus, no additional software is needed to set this bit. The POPF instruction will restore the correct bank status on return from interrupt. The PUSHF and POPF are included in the interrupt servicing routine in the internal ROM. It need not be repeated externally.

Table 4a illustrates how an LCALL can be done into the other bank. Table 4b illustrates how LJMP can be done into the other bank. Table 4c illustrates how the interrupt is serviced.

RD Indication During External ROM Access

The SC11011, 21 & 61 do not provide an indication when the ROM contents are read into the CPU. In the SC11091, the RD pin goes low for 1 clock cycle when the ROM contents are being read into the UMAC CPU. Figure 9 shows the timing. The RD function is the same for extended ROM operation.

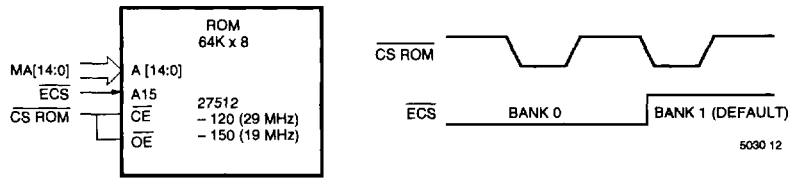


Figure 6a. OE Could be Grounded, But Above Connection Saves Power In $\overline{PD}$ Mode.

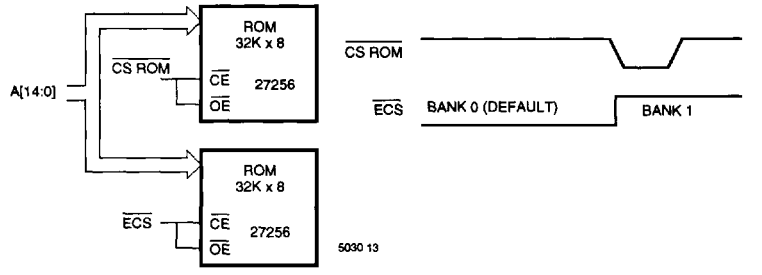
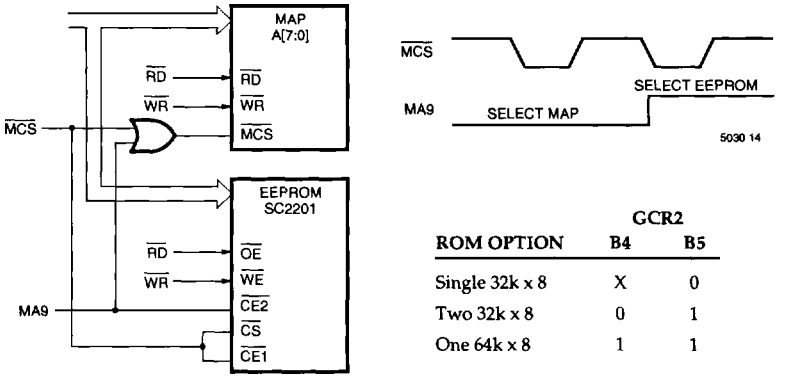


Figure 6b. Alternative Use of Two 27256 ROMs



ROM OPTION	GCR2 B4	GCR2 B5
Single 32k x 8	X	0
Two 32k x 8	0	1
One 64k x 8	1	1

Figure 6c. If EEPROM is Used and If $\overline{ECS}$ is Used for Expanded ROM Options then Additional Decoding is Required

Figure 6. Interface Block Diagrams for Optional Modes

Bank 0

```
.
. LD AX, #0192H
. LDB BL, [AX]
. ANDB BL, #11101111B
. ORB BL, #01000000B  ;disable interrupts
. STB BL, [AX]        ;set bank bit
LCALL  MODX
.
. ; must enable interrupts on return
.
```

Bank 1

```
.
MODX:
;enable interrupts if necessary
.
. LCALL within the bank allowed
.
. LD AX, #0192H
. LDB BL, [AX]
. ANDB BL, #10101111B
. STB BL, [AX]        ;disable interrupts
. RET ;TO BANK 0      ;clear bank bit
```

Table 4a. LCALL Across Bank

Bank 0

```
.
. LD AX, #0192H
. LDB BL, [AX]
. ANDB BL, #11101111B ;disable interrupts
. ORB BL, #01000000B  ;set bank bit
. STB BL, [AX]
LJMP XX
```

Bank 1

```
.
.
.
XX:
.
. program execution continues from XX.
.
.
```

Table 4b. LJMP Across Bank

When an interrupt occurs, the program vectors to internal address 2004H. Here the internal firmware performs a PUSHF instruction. If the ROM extension mode is enabled, the PSB bit 6 will be set to 0 to point to external bank 0. The firmware then does an LCALL to external address 8004H. The user interrupt service routine begins here. The last instruction must be "RET" to return the execution to the internal ROM. The firmware executes a "POPF" instruction to restore the flags and bank pointer. A "RET" instruction returns the execution to the last address before the interrupt.

```
2004          ORG     INTV
2004                  EINT:
2004  F2              PUSHF                ; SAVE PSB,
                                           ; SET BANK
2005  EF FC 5F        LCALL   INTE         ; BIT TO 0
2008  F3              POPF                 ; JLCALL 8004H
2009  F0              RET                  ; RESTORE PSB
                                           ; RETURN FROM
                                           ; INTERRUPT
```

Table 4c. Interrupt Servicing

ADDRESS	FUNCTION	R/W	BYTES	COMMENTS
0000H-017FH	Internal RAM *	R/W	384	(a)
0180H-019AH	Internal REG*	R/W	24	(b)
1000H-10FFH	External MAP	R/W	256	(c)
1100H-11FFH	External EEPROM	R/W	256	(c)
2000H-20FFH	Internal ROM	RO	256	(d)
4000H-7FFFH	External RAM	R/W	16K	(e)
8000H-FFFFH	External ROM	RO	32K	(f)
1200H-12FFH	External EEPROM	R/W	256	(g)

* 0000H – 00FFH may be accessed using direct addressing mode. 0100 – 0194H may only be accessed as memory locations (16-bit address) in an indirect mode. For direct addressing a 9th bit (GCR [1], called Page Bit) must be set to switch from the first 256 bytes to the rest of the RAM.

(a) The SC11011,61 have 304 bytes and SC11021 has 320 bytes

(b) The internal register is compatible with the MAC and Big MAC. Registers 194H to 19AH controls the selection of SSCC mode. The SSCC function is completed in firmware.

(c) In the normal mode of operation, the MCS and ECS chip select for MAP and EERAM remain the same as in MAC or Big MAC. A provision is made to extend the ROM capacity by another 32K bytes. If selected, the ECS pin becomes a chip select to address a 32K ROM from 8000H to FFFFH. If extended ROM is used, the address 1100 to 11FF must not be accessed. The EEPROM will be selected using the MCS pin and an external memory decode will select either the MAP or the EEPROM.

(d) Internal ROM size is 256 bytes.

(e) The external RAM address remains the same as the SC11011. It has a maximum addressable space of 16K bytes. With multiplexing using the IO_3 pin (pin 45), it can address 32K bytes. (Not available with SC11095.)

(f) The 32K bytes ROM address remains the same as in MAC or Big MAC. With the ECS pin, the ROM address is expanded to a total of 64K bytes.

(g) If extended ROM is used, The EEPROM will be addressed from 1200H to 12FFH. See the hardware configuration section.

(h) SC11011, 1102X, 11061 stack is reset to 302 on power up. SC11091 stack is reset to 320.

REGISTER DESCRIPTION

This section contains a description of each of the registers in the UMAC device. All of the registers of the device are 8-bits with 16-bit addresses. The registers are made up of bits that are either inputs or outputs. Input bits are read-only (RO). Output bits are read/write (R/W). The state of an output may be read back by the processor.

Serial Mode

In parallel mode (CONF = 0) the functions of the UART registers are exactly the same as those in 16C450 UART. However in serial mode, (CONF = 1), the UART is turned around and controlled by the internal processor and it becomes a data set UART. The DTR, RTS, and OUT1 in MCR register becomes DSR, CTS, and RLSD outputs. The CTS, DSR in MSR register become RTS, DTR input status from RTS, DTR pins.

Note:
In serial version to echo SIN to SOUT after RESET and then go back to normal operation.

1. Set SB in LCR to "1".
2. Sample RDI in UART monitor register.
3. Set CM = RDI in the same register.
4. SOUT will be the same state as CM.
5. Receiver is functioning, ignoring it.
6. After finishing all echoing, reset SB in LCR.
7. Update DLL, DLM, and set CM = 1 for normal operation.
8. Do a SET then RESET to RTRST bit to RESET RCV and TMR. Do a READ to LSR to clear LSR.
9. The UART is ready for normal operation.

Bit No	Register Address										
	0(DLAB=0)	0(DLAB=0)	1(DLAB=0)	2	3	4	5	6	7	0(DLAB=1)	1(DLAB=1)
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Iden. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	STR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2 INT0 is High-Z when out2=0	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break (SB)	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Table 6. Summary of Accessible UART Registers

Programmable Baud Generator

The UART contains a programmable Baud Generator that takes an internal clock of (3/32)(XTAL1) = 1.8432 MHz and divides it by any divisor from 1 to (2^{16}–1). The output frequency of the Baud Generator is 16 x the Baud [(divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on the initial load.

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3) forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bit 3–7 are permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bits 0–3 Low, Bits 4–7— Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read BRR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read RBR/MR	Low

Table 7. Summary of Accessible UART Registers

Table 8 illustrates the use of the Baud Generator with a crystal frequency of 19.6608 MHz. The accuracy of the desired baud rate is dependent on the crystal accuracy. Communicaiton software writing values to the divisor latches typically expects the input to the UART to be 1.8432 MHz. They will work correctly only if the UMAC input clock is maintained at 19.6608 MHz.

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Error Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.4	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
57600	2	—

Table 8. Baud Rate Generator Divisors

SC11091/SC11095 SPECIFICATIONS

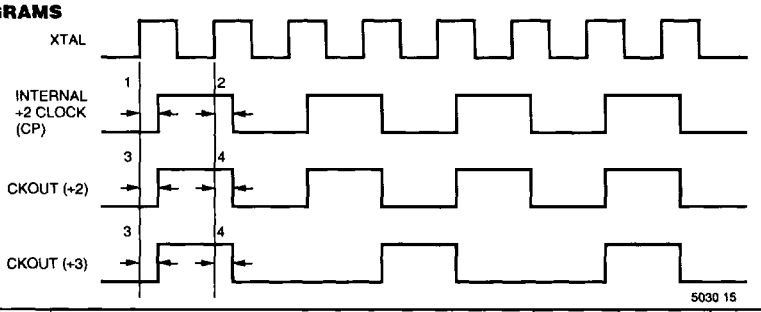
ABSOLUTE MAXIMUM RATINGS:

V_{CC} Supply Voltage	+6 V
Input Voltage	–0.6 V to V_{CC} +0.6 V
Storage Temperature Range	–65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS: (T_A = 0 to 70°C, V_{CC} = +5 V +10%)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.5 V		40	75	mA
I_{CCPD}	Power Down Current @ V_{CC} = 5.5 V		25	35	mA
V_{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	 2 0.8 V_{CC}			 V V
V_{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			 0.8 0.2 V_{CC}	 V V
VT+	Positive Hysteresis Threshold for RESET & $\overline{RI}$ input pins		2.8		V
VT–	Negative Hysteresis Threshold for RESET & $\overline{RI}$ input pins		2.3		V
V_{OH}	High Level Output Voltage for D7–D0, INT0 @ I_{OH} = 8 mA for RDY—open collector for other output @ I_{OH} = 2 mA	 0.7 V_{CC} +0.5			 V
V_{OL}	Low Level Output Voltage for D7–D0, INT0 pins @ I_{OL} = 8 mA for RDY @ I_{OL} = 8 mA for other output pins @ I_{OL} = 2 mA			 0.3 V_{CC} –0.5	 V
I_I	Leakage Current		±1	±20	µA
F_{CLK}	Crystal Clock Frequency (GCR2:0, 1 - 01)		19.6608		MHz
F_{CLK}	Crystal Clock Frequency (GCR2:0, 1 - 00)		29.4912		MHz

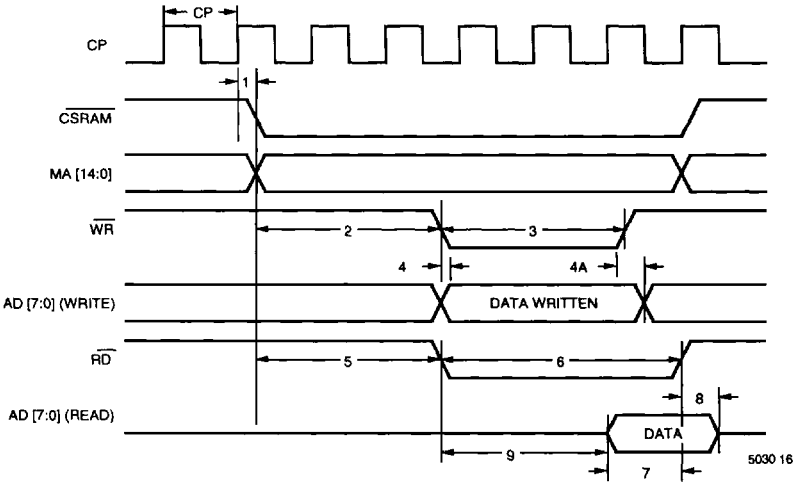
TIMING DIAGRAMS



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TXTCPH	XTAL high to internal +2 clock high			20	ns
2	TXTERL	XTAL high to internal +2 clock low			20	ns
3	TXTCKH	XTAL high toCKOUT high			30	ns
4	TXTCKL	XTAL high toCKOUT low			30	ns

NOTE: CP is the internal +2 clock. CP = 102 ns for 19.6608 MHz crystal or 68 ns for 29.4912 MHz crystal.

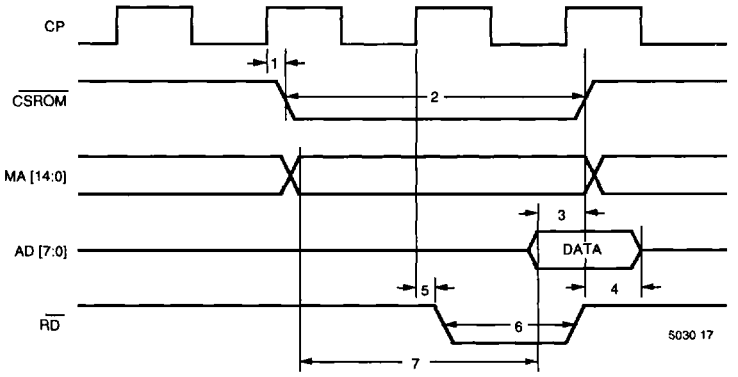
Figure 7. Oscillator, Internal (+2) Clock and CKOUT Timing



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCPCSR	CP to $\overline{CSRAM}$ low			20	ns
2	TCSRWR	$\overline{CSRAM}$ low to $\overline{WR}$ low		2.5		cp
3	TRW	$\overline{WR}$ width		2.5		cp
4	TWRADV	$\overline{WR}$ low to data valid			5	ns
4a	TWRADI	$\overline{WR}$ high to data invalid		.5		cp
5	TCSRRD	$\overline{CSRAM}$ low to $\overline{RD}$ low		2.5		cp
6	TRD	$\overline{RD}$ width		3.5		cp
7	TADVCL	Read set up time	20			ns
8	TCLADI	Read hold time	0			ns
9	TRLDV	Read low to data valid 29.4912 MHz 19.6608 MHz			170 320	ns ns

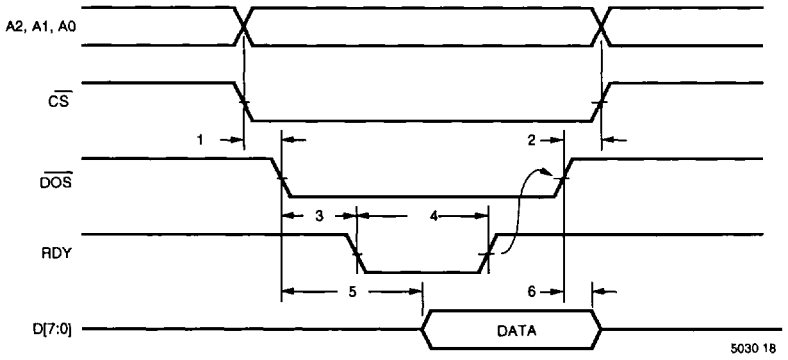
NOTE: CP = 102 ns for 19.6608 MHz XTAL & 68 ns for 29.4912 MHz crystal.

Figure 8. RAM Read or Write Cycle



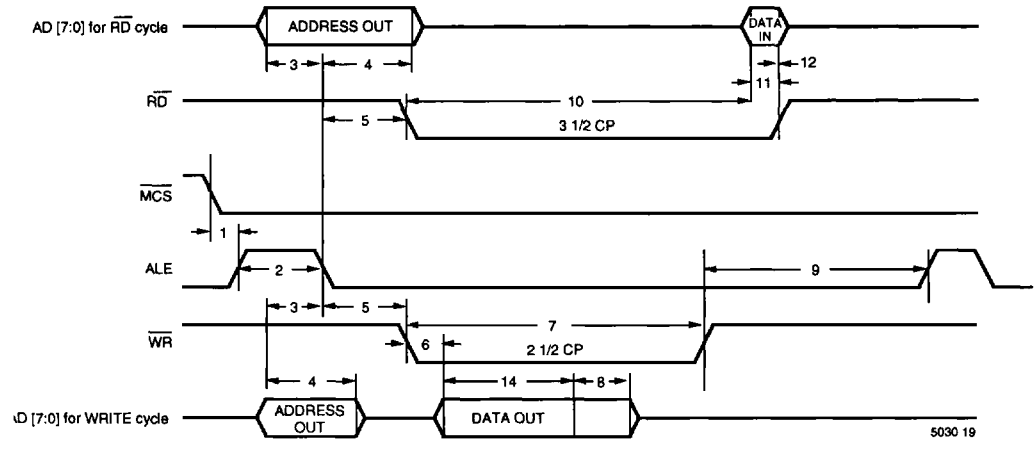
NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCPCRM	CP to $\overline{\text{CSROM}}$ low			20	ns
2	TCSROM	$\overline{\text{CSROM}}$ width		2		cp
3	TCSRAD	Read setup time	10			ns
4	TCSRDH	Read hold time	0			ns
5	TCPRD	CP to $\overline{\text{RD}}$ low			20	ns
6	TRD	$\overline{\text{RD}}$ width		1		cp
7	TADDV	Address valid to data valid 29.4912 MHz 19.6608 MHz			120 170	ns ns

Figure 9. External Program Storage Read Bus Cycle



NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDOL	$\overline{\text{CS}}$ low to $\overline{\text{DOS}}$ low				0	ns
2	TDOHCSH	$\overline{\text{DOS}}$ high to $\overline{\text{CS}}$ high				0	ns
3	TDOLRDL	$\overline{\text{DOS}}$ low to RDY low				26	ns
4	TRDL	RDY low time (~5–6CP)		330		400	ns
5	TDOLDV	$\overline{\text{DOS}}$ low to D valid				200	ns
6	TDOHDZ	$\overline{\text{DOS}}$ high to D high-Z		0			ns

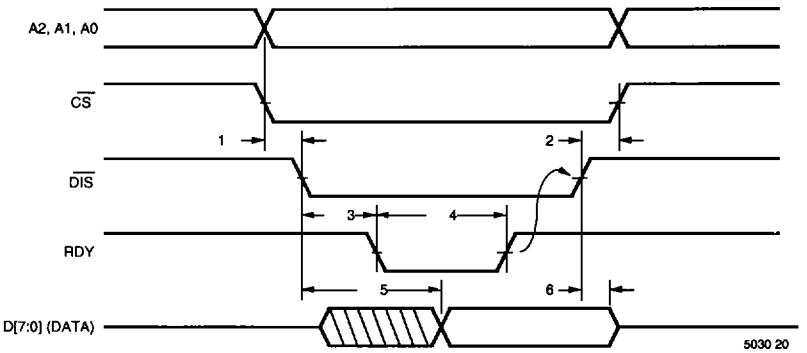
Figure 10. Write Cycle (PC Bus Write Into UART Register)



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high	10		20	ns
2	TALE	ALE pulse width	45			ns
3	TAVLE	Address valid to ALE low	30			ns
4	THAD	Hold address after ALE low	48			ns
5	TALRD	Delay from ALE low to $\overline{RD}/\overline{WR}$ low	45			ns
6	TDURL	Data valid after $\overline{WR}$ low			20	ns
7	TWR	Write pulse width	160			ns
8	TDHWR	Data hold after $\overline{WR}$ high	30			ns
9	TWHLH	End of $\overline{WR}$ to next ALE	120			ns
10	TDVRL	Data valid after $\overline{RD}$ low			185	ns
11	TDVRH	Data valid setup to $\overline{RD}$ high	15			ns
12	TDH	Data hold after $\overline{RD}$ high	0			ns
13	TRD	Read pulse width	220			ns
14	TDHWR	Data setup before $\overline{WR}$ high	70			ns

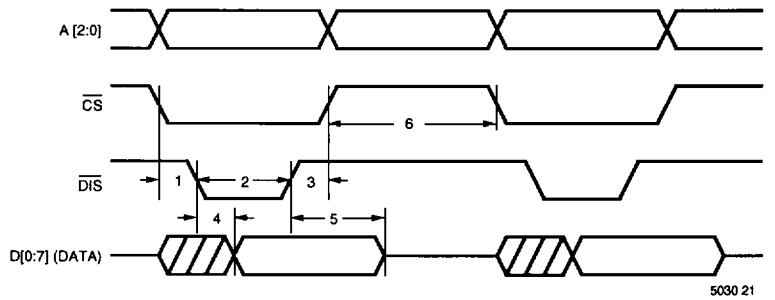
NOTE: CP = 68 ns using 29.4912 MHz crystal

Figure 11. MAP EERAM Read and Write Cycles



NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDIL	$\overline{CS}$ low to $\overline{DIS}$ low				0	ns
2	TDIHCSH	$\overline{DIS}$ high to $\overline{CS}$ high				0	ns
3	TDILRDL	$\overline{DIS}$ low to RDY low				26	ns
4	TRDL	RDY low time (~5–6CP)		330		400	ns
5	TDILDV	$\overline{DIS}$ low to D valid				180	ns
6	TDIHDZ	$\overline{DIS}$ high to D high-Z				12	ns

Figure 12. Read Cycle (PC Bus Read From UART Register)

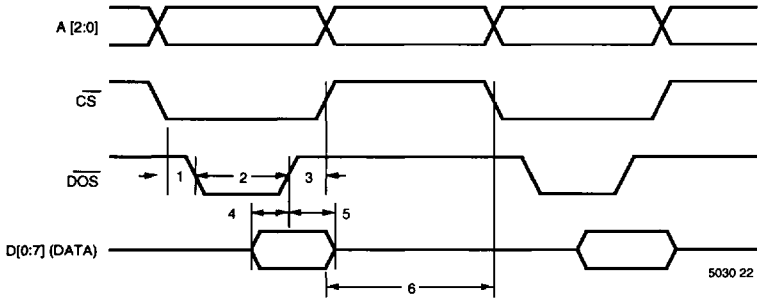


NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCSLDIL	$\overline{CS}$ low to $\overline{DIS}$ low			0	ns
2	TDIS	$\overline{DIS}$ width	3			cp
3	TDIHCSH	$\overline{DIS}$ high to $\overline{CS}$ high			0	ns
4	TDILDV	$\overline{DIS}$ low to D valid		2		cp
5	TDIHDZ	$\overline{DIS}$ high to high-Z			20	ns
6	TCYCRD	Wait time before next access	2			cp

NOTE 1: CP is +2 clock

NOTE 2: User does not need to write into No Ready Bit Register

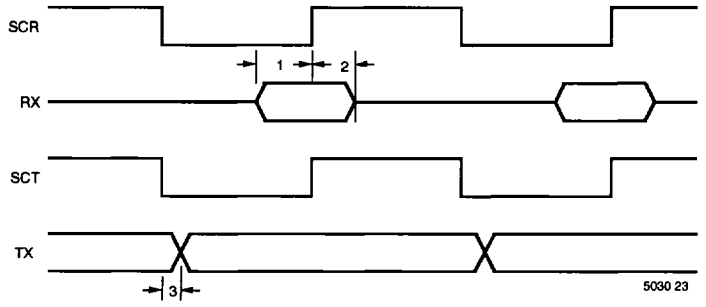
Figure 13. Read Cycle (No Ready Mode) (PC Bus Read From UART Register)



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCSLDOL	$\overline{CS}$ low to $\overline{DOS}$ low			0	ns
2	TDOS	$\overline{DOS}$ width	4			cp
3	TDOHCSH	$\overline{DOS}$ high to $\overline{CS}$ high			0	ns
4	TDSUP	Data set up time	20			ns
5	TDHLD	Data hold time	10			ns
6	TCYCWRD	Wait time before next access	2			cp

NOTE: CP is internal ÷2 clock

Figure 14. Write Cycle (No Ready Mode) (PC Bus Read Into UART Register)



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TRXSH	Bit set up time	20			ns
2	TRXHD	Bit hold time	0			ns
3	TTXBIT	XCT low to bit out			30	ns

Figure 15. Single Bit USART Read and Write Timing