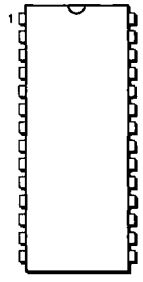
FEATURES

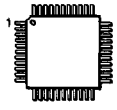
- ☐ Complete 2400 bit/s modem and 9600/7200/4800/2400 bit/s Sendfax (SC11055), 4800/2400 bit/s Sendfax (SC11045)
- ☐ Single 5V supply with 10 mW power down mode
- ☐ Pin compatible with Sierra SC11024, SC11054 2400 bit/s modem (not compatible in PQFP packages)
- ☐ Compatible with CCITT V.29 (SC11055), V.27ter, V.23, V.22 bis, V.22, V.21, and Bell 212A and 103 standards
- ☐ Synchronous & Asynchronous modes
- ☐ Integrated DTMF/Guard tone generator, call progress monitor
- ☐ 2225/2100/1650/1300/390 Hz tone detector
- ☐ Contains an on-chip hybrid
- ☐ Analog, digital, and remote digital loopback
- ☐ Compatible with SC11021, SC11091, and SC1104X Series controllers
- ☐ Programmable audio output
- ☐ CMOS technology
- ☐ Flag detector in V.21 mode
- ☐ Relay driver in 44 pin QFP version

28-PIN DIP PACKAGE



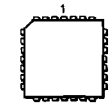
SC11045CN, SC11055CN

44-PIN QFP (10mm) PACKAGE



SC11045CQ, SC11055CQ

28-PIN PLCC PACKAGE



SC11045CV, SC11055CV

BLOCK DIAGRAM

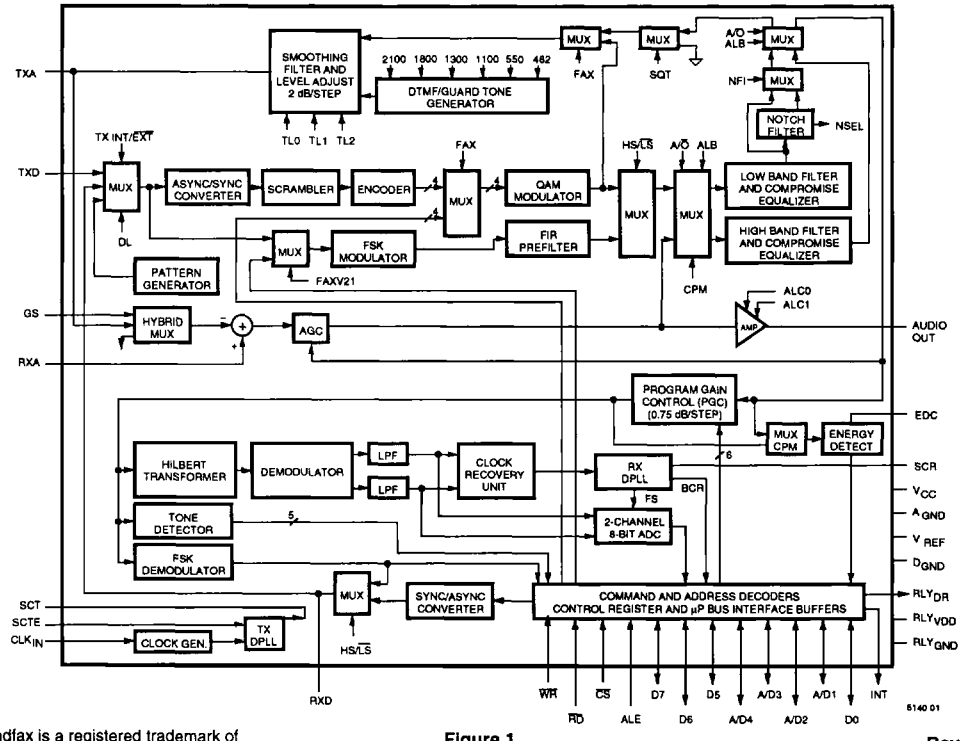


Figure 1.

Sendfax is a registered trademark of Sierra Semiconductor Corporation.

GENERAL DESCRIPTION

The SC11045/SC11055 are complete V.23, V.22bis, V.22, V.21 5V only modem ICs including a Sendfax capability up to 9600 bit/s. The ICs contain all modem functions except the adaptive equalizer. Each is used in conjunction with an external controller, such as the Sierra SC11021 for RS-232 interface or parallel bus applications to implement a 2400 bit/s full duplex modem, having Sendfax capability at up to 9600 bit/s (SC11055) or 4800 bit/s (SC11045). The controller performs all modem control and handshaking functions including the Sendfax call set-up in accordance with T.30 recommendation as well as the adaptive equalization.

The SC11045 and SC11055 operate in 2400 bit/s QPSK/QAM and 1200 bit/s PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22, V.22 bis and V.23 standards. In addition the SC11055 can transmit 9600 bit/s QAM with fall back to 7200 bit/s per V.29 standard or 4800 bit/s PSK with fall back to 2400 bit/s compatible with V.27ter recommendation. The SC11045 can transmit 4800 bit/s PSK with fallback to 2400 bit/s compatible with V.27ter recommendation. The two chip set of modem and controller comprise the smallest modem with fax capability in the industry.

The SC11045/55 may be used with several Sierra controllers. Currently they are:

CONTROLLER	APPLICATION
SC11021	General purpose – Low Power.
SC11041	< 30 mW standby. Address up to 1Mb ROM, 32k x 8 RAM.

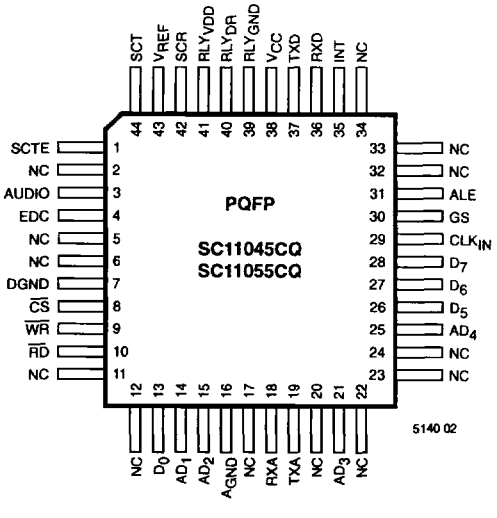
PIN DESCRIPTIONS

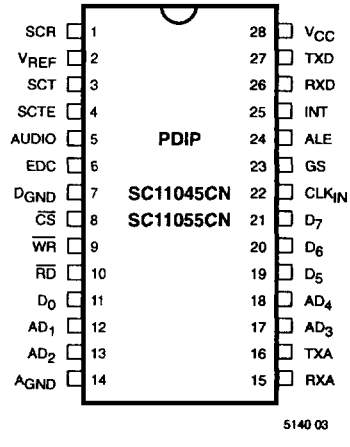
PIN NAME	PIN NUMBER		DESCRIPTION
	DIP, PLCC	QFP	
AD_1–AD_4	12, 13, 17, 18	14, 15, 21, 25	**INPUT/OUTPUT (TTL).** Multiplexed address/data bus (8-bits); AD_4–AD_1 (4-bits) are used for multiplexed addressing of internal registers.
A_{GND}	14	16	**ANALOG GROUND.**
ALE	24	31	**INPUT (TTL).** Address Latch Enable; The address on AD_4–AD_1 is latched into the SC11045/55 Address decoder at the falling edge of this normally low pulse.
AUDIO	5	3	**OUTPUT (ANALOG).** The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the AUDIO register as specified under AUDIO register description.
CLK_{IN}	22	29	**INPUT (TTL). CLOCK.** 9.8304 MHz clock input from the controller.
$\overline{CS}$	8	8	**INPUT (TTL).** Chip Select; active low.
D_0, D_5–D_7	11, 19–21	13, 26–28	**INPUT/OUTPUT (TTL).** Bits 0, 5, 6 and 7 are don't cares as far as address is concerned.
D_{GND}	7	7	**DIGITAL GROUND.**
EDC	6	4	**INPUT.** Capacitor for energy detect; A 1.0 µF capacitor should be connected between this pin and A_{GND}.
GS	23	30	**INPUT (THREE-LEVEL).** Gain Select to compensate for loss in line coupling transformer. When left open or tied to A_{GND}, the compensation is 0 dB; connected to V_{REF}, +2 dB compensation is provided; And when tied to V_{CC}, the compensation is +3 dB.
INT	25	35	**OUTPUT (TTL). INTERRUPT.** Normally low; A short (13 µs typical) positive pulse is generated after all A to D conversions are completed.
$\overline{RD}$	10	10	**INPUT (TTL). READ.** Normally high; Data on AD_7–AD_0 is to be read by the processor at the rising edge of this pulse.
RLY_{GND}	—	39	Ground for the Relay Driver.
RLY_{DR}	—	40	**OUTPUT (OPEN DRAIN).** Relay Driver.

PIN DESCRIPTIONS (continued)

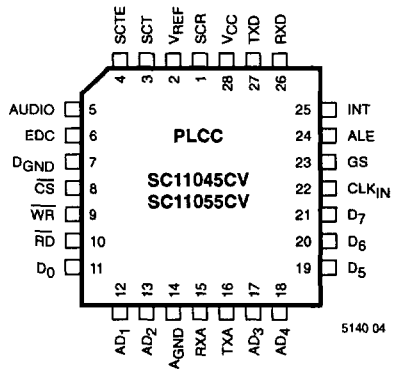
PIN NAME	PIN NUMBER		DESCRIPTION
	DIP, PLCC	QFP	
RLY_{VDD}	—	41	+5V supply for the Relay Driver.
RXA	15	18	**INPUT (ANALOG).** Received signal.
RXD	26	36	**OUTPUT (TTL).** Received Data.
SCR	1	42	**OUTPUT (TTL).** Synchronous Clock Receive (Data set source); Used only in bit synchronous mode; Recovered by the Receiver Phase Locked Loop from the far end modem. Data on RXD is valid at the rising edge of this clock.
SCT	3	44	**OUTPUT (TTL).** Synchronous Clock Transmit (Data set source); Used only in bit synchronous mode; Generated internally by the SC11045/55 Clock Generator; Rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
SCTE	4	1	**INPUT (TTL).** Synchronous Clock Transmit External (DTE source);Used only in bit synchronous mode; Data on TXD line is latched by the SC11045/55 at the rising edge of this clock. Clock rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
TXA	16	19	**OUTPUT (ANALOG).** Transmit signal.
TXD	27	37	**INPUT (TTL).** Transmit Data.
V_{CC}	28	38	+5 V supply.
V_{REF}	2	43	**REFERENCE GROUND.** Generated inside the chip and is equal to $V_{CC}/2$.
$\overline{WR}$	9	9	**INPUT (TTL). WRITE.** Normally high; Data on AD_7–AD_0 is written into the SC11045/55 registers at the rising edge of this pulse.

CONNECTION DIAGRAMS





CONNECTION DIAGRAMS (continued)



FUNCTIONAL DESCRIPTION OF THE SC11055 MODEM

The SC11045/SC11055 includes the following:

- ☐ Full transmitter consisting of
  - Async to Sync converter
  - Scrambler
  - Data encoder
  - 75% square root of raised cosine pulse shaper in V.22 mode, 50/90% square root of raised cosine shaping in V.27ter 4800/2400 bit/s modes (SC11045/SC11055) and 20% square root of raised cosine shaping in V.29 9600/7200 bit/s modes (SC11055)
  - Quadrature amplitude and phase modulators
  - FSK (Bell 103, CCITT V.21 and V.23) modulator
  - Hybrid
- ☐ High band and low band filters
- ☐ High band and low band compromise equalizers
- ☐ V.22 notch filter (selectable at 550 or 1800 Hz)
- ☐ Transmit smoothing filter
- ☐ Programmable attenuator for transmit level adjust
- ☐ DTMF, 462 Hz, 550 Hz, 1100 Hz, 1300 Hz, 1800 Hz, and 2100 Hz tone generator
- ☐ Tone detector for 390/1300/1650/2100/2225 Hz frequencies
- ☐ Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- ☐ Pattern generator for generating fixed digital patterns in handshaking mode
- ☐ Receive section consisting of
  - 64-step programmable gain controller (PGC)
  - Energy detector at the output of the PGC
  - Hilbert transformer
  - Quadrature amplitude and phase demodulators (free running carrier) with low pass filters
  - Baud timing recovery circuit (sampling clock of 600 Hz)
  - FSK demodulator
  - Sync to Async converter
- ☐ Two channel 8-bit analog to digital converter (ADC)
- ☐ Control and Status registers
- ☐ 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- ☐ Audio output with level adjust

Transmitter (V.22bis, V.22, 212A, V.23 and V.21 and 103)

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bit/s transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 2400/1200 Hz +2.3%, –2.5%. It outputs serial data at a fixed rate of 2400/1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band, centered at 2400 Hz, or the low band, centered at 1200 Hz. In the 2400 bit/s mode, the modem actually sends four bits at a time, called a quadbit. The actual rate of transmission for a quadbit is 600 baud. This is the optimum rate of transmission over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bit/s data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit are encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits define one of the four signaling elements associated with the new quadrant.

In the 1200 bit/s data rate, the data stream is divided into groups of two consecutive bits (dibits). The dibits are used to determine the phase quadrant change relative to the quadrant occupied by the pre-

ceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through baseband filters with a square root of raised cosine shape. The filtered signals subsequently modulate sine and cosine carriers, and add to form the QAM/QPSK signal. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second-order low-pass switched-capacitor filter that adds the modem transmit signal to the V.22 guard tones. It also provides a 2 dB per step programmable gain function to set the output level.

Transmitter (V.29 and V.27ter)

In these modes the functions required to convert the transmit data to transmit analog signal are partitioned between the analog and controller chips. The firmware implemented in the controller chip performs the scrambling and also generates the training sequences as required by the V.29 and V.27ter specifications. Next, it carries out the encoding function based on the selected mode and bit rate (9600/7200/4800/2400 bit/s) and determines the new location of the constellation point. A 4-bit word (a_3 a_2 a_1 a_0) has been assigned to each constellation point to facilitate the quadrature modulation by the analog chip. (See Figures 2a and b).

Every two baud periods (2400/1600/1200 baud), the analog chip sends an interrupt to the controller, within 250 µs, the controller has to write an 8-bit word into the FAXR register of the analog chip, that conveys the constellation point locations for two consecutive bauds (8-bit word corresponds to 8-bits of Tx data in 9600 bit/s mode, 6 bits in 7200 bit/s mode, 6 bits in 4800 bit/s mode and 4 bits in 2400 bit/s mode).

The analog chip will perform quadrature modulation on the 4 LSB's first and 4 MSB's on the next baud period. It also carries out square root of raised cosine shaping based on the selected baud rate. In fax mode (V.29, V.27ter) the modulated signal will directly feed the transmit smoothing filter, bypassing the band pass filter and equalizer.

Transmitter (V.21 FAX)

In FAX mode (BR3 =1 or BR2 =1) the operation of V.21 modem, referred to as V.21FAX, is half-duplex and uses the high channel.

The input/output data will be handled through the controller interface instead of the TXD/RXD pins.When transmitting in V.21 mode, the analog chip sends inter-

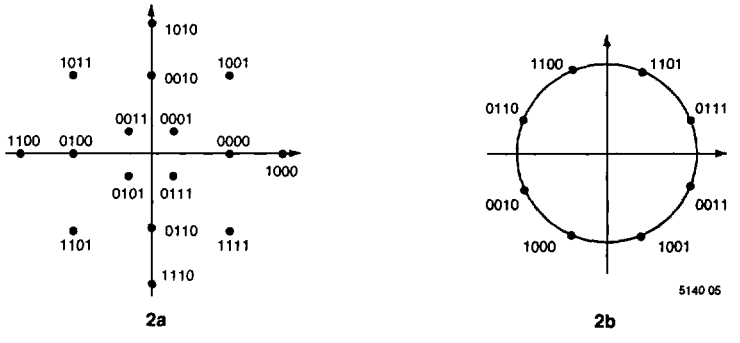


Figure 2. 4-Bit Words ($a_3a_2a_1a_0$) Identifying Constellation Points in V.29 (2a) and V.27ter (2b)

rupts to the controller at a 300 Hz ±.01% rate which serves as a timing base. Within 2 ms after every eight interrupts, the controller has to write an 8-bit word into the FAXR register that corresponds to eight consecutive transmit data bits with the LSB to be sent first.

The analog chip will perform a parallel-to serial conversion on the 8-bit word and feed the result into the FSK modulator block. The signal path from FSK modulator input to TXA pin will be similar to the normal V.21 mode.

Receiver (V.22 bis, V.22, 212A, V.23, V.21 and 103)

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8-bit ADC and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides detection within 17 to 24 msec. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode, the energy detector is connected to the output of the PGC to allow detection level adjustment.

The output of the receive filter is applied to the programmable gain control (PGC). This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also provides auto-zeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a Hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by a free-running carrier. The baseband components are low-pass filtered to produce I and Q (Inphase and Quadrature) channel outputs. The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period, allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 µs from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is transferred from the SC11045/55 during each baud period.

In the asynchronous mode, data received from the processor is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are re-inserted. Underspeed data is passed essentially unchanged. The sync/async converter has two modes of operation. In the basic signaling mode, the buffer can accept an overspeed which corresponds to one missing stop bit in eight characters. The length of the start bit and data elements will be the same, and the stop bit will be reduced by 12.5%. In the extended-signaling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/async converter, along with the output of the FSK demodulator, is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed and output data received on the RXD pin.

For low-speed operation, the FSK demodulator is used. The output of the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

To improve the performance of the receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to the band-pass filter. The decision thresholds of this AGC are controlled by the AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB further apart than when AGCVT = 0, so that the probability of gain change will be reduced. The status of the AGC gain is available through the AGCO bit. AGC will have 8 dB more gain when AGCO = 1. Status of AGCO should be monitored at every baud timing period and when it makes a transition (causing a gain-hit) the PGC's gain shouldbe modified accordingly to prevent divergence of the adaptive equalizer.

Receiver (V.21 FAX)

When receiving in V.21FAX mode, which is half-duplex, the serial output data from FSK demodulator will be loaded into a serial-to-parallel register. The timing for serial shift as well as interrupt is derived from the received data through a resettable counter. The counter divides an input clock of 9.6 kHz by 32 to generate a 300 Hz signal. On every high to low transition of data the counter is reset and resynchronized to data timing. Assuming a received bit rate of 300 bit/s ±0.01%, the interrupt should have an average frequency of 300 Hz ±.01%. The controller should count

the interrupt pulses and read the contents of FAXV21R register within 1.5 ms after every eighth pulse. The LSB corresponds to FSK demodulator output that has been received first in time.

A flag detector is implemented on the chip to facilitate detection of flag sequences (Hex 7E) in V.21 FAX mode. The decoder, detects the flag itself or possible rotations of it; i.e. it detects 01111110, 00111111, 1001111, 11001111, 11100111, 11110011, 11111100. If any of these combinations is detected, then FLAGDET bit of the status register will go high and stay high until the condition goes away. The flag detector output is updated on every interrupt pulse in the V.21FAX receive mode. To ensure that the flag detector is not triggered by false data, it is recommended that the FLAGDET bit be checked for at least 16 consectutive interrupts after this bit gets set. If it does not stay high continuously the received data may not be a true flag sequence. Flag detector should be used in V.21FAX receive mode only.

Caller ID Mode

The V.23 1200 bps can be used for the 202 caller ID mode.

Monitor Call Waiting Mode

The RNGX/TRITX bit can be used to tri-state the transmit output pin to prevent the 600 ohm resistance from terminating the line in this mode.

Tone Detector

A digital tone detector has been implemented in the SC11045/SC11055 to facilitate detection of 390/1300/1650/2100/2225 Hz tones. The output of the PGC is passed through a zero crossing detector which in turn feeds a digital timer that verifies the period of the tone. If four consecutive periods of input tone pass the requirements, then, the appropriate tone detector output (TD390, TD1300, TD1650, TD2100 or TD2225 bit in status register) goes high. To detect these tones user must insert the highband filter in the receive path to allow their passage, also, PGC gain must be set properly to amplify the input to the tone detector. It will be a good practice to monitor ED bit when reading TD to ensure that the signal energy is within acceptable limits.

With the PGC gain word (PGCR) set to 011111 the tone detector threshold will be typically -43dBm.

Tone Detector Operation

The following circuit description clarifies the operation of Tone Detector, how it can be set up and how its output should be interpreted.

The Tone Detector works very differently from energy/carrier detect as follows:

a) Carrier energy detect looks for the presence of energy and does not check the frequency.

b) Tone Detector is a digital timer. The input signal is passed through a Schmitt trigger with ±50mV hysteresis and the period of the output signal is checked by a digital timer to see if it falls within allowed limits. This block does not care about the energy of the signal unless it becomes so weak that it affects the period of the Schmitt-trigger output (i.e. close to hysteresis levels). The Tone Detector verifies 4 consecutive periods of signal before turning the corresponding bit "on." After this time, if one of the zero-crossings of the signal is corrupted (say, due to noise) it will not pass the period-check and the output bit will return "low" and wait for four new consecutive cycles of the tone with clean zero-crossings.

From the above explanation we see that:

1) Tone Detector and carrier/energy detect complement each other and for reliable tone detection, the output of both has to be monitored to check frequency and energy simultaneously.

2) Weak signals are more vulnerable to corruption by noise; consequently, the tone detector output may not stay steadily high, so its output should be integrated in software. In other words, if a given "tone bit" stays on at least 70% of the time within a time frame (say, within 40 msec), it should be considered present. Note that since the output of this block is updated at every 4 cycles of tone, then reading the output at shorter intervals just provides the same result.

As Figure 3 shows, for tone detect to function properly, its preceding block has to be set up properly; i.e. Filter has to be in the right band to allow passage of the tone, and the PGC gain has to be set up correctly to provide proper signal level to

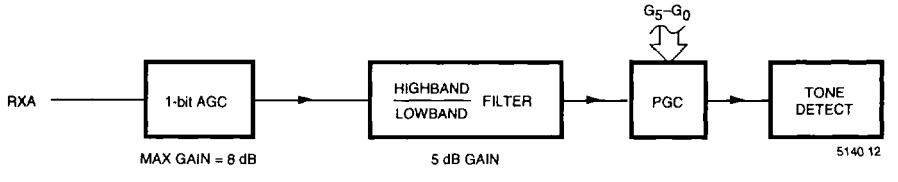


Figure 3. Tone Detector Signal Path

tone detect, which has ±50mV hysteresis at its input. Assuming that PGC gain code is "1F," the PGC gain will be 13.25 dB. If input level at RXA is -40 dBm, the 1-bit AGC will be at its max gain and the overall gain from input pin (RXA) to tone detector input will be:

G = 8+5+13.25 = 26.25 dB
Tone Detector input = -40+26.25 = -13.75 dBm = 425mV_{P-P}

This is 4 times the hysteresis of Tone Detector!

So, the part should not have problems detecting -40 dBm and even weaker signals if Filter and PGC are set up correctly. Reliability of detection in presence of noise can be improved by implementing the above recommendations.

Relay Driver

An internal relay driver is provided in the 44 pin QFP package. It can be used to drive a 390Ω with a maximum turn on voltage of 4V. The relay may be used for offhook relay or caller ID supplementary relay. A protective diode is required across the relay coil.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by turning the "Hybrid" bit on through the interface, this matching is provided by an external resistor connected between the TXA and RXA pins on the SC11055. The filter section provides sufficient attenuation of the out-of-band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter. The hybrid can be deactivated by the controller.

The SC11045/SC11055 internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. By tying the GS pin to A_{GND}, V_{REF} or V_{CC}, compensation levels of 0, +2, +3 dB, respectively are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 4, can be used to overcome these losses and achieve maximum performance. In this case, the internal hybrid must be turned off by setting bit 6 of the TXCR register to 0.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11045/SC11055 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under

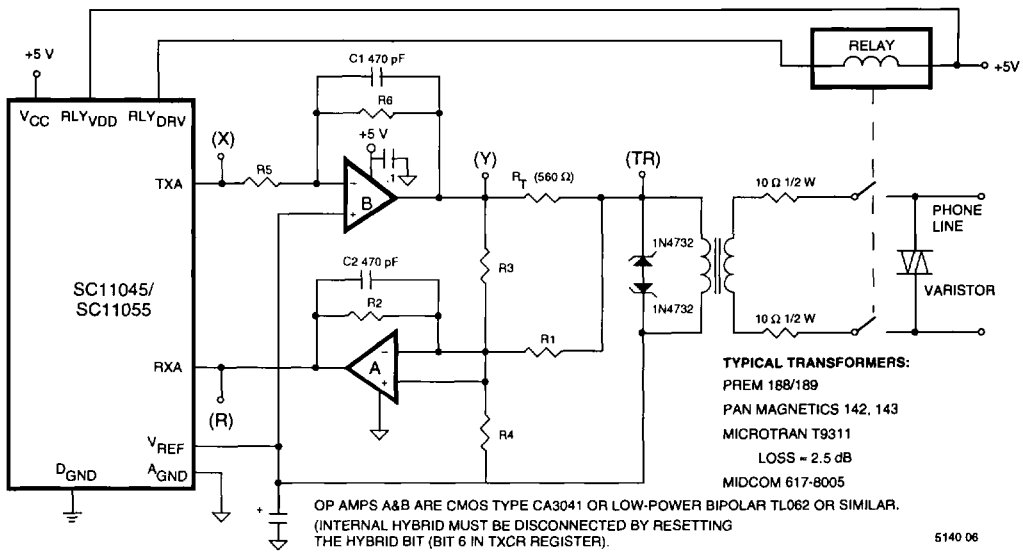


Figure 4. Using an External Hybrid with the SC11045/SC11055

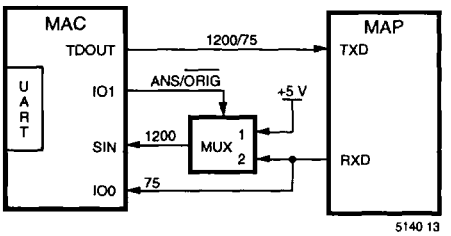


Figure 5a. Parallel Mode

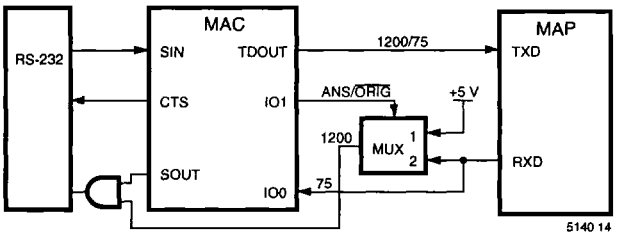


Figure 5b. Serial Mode

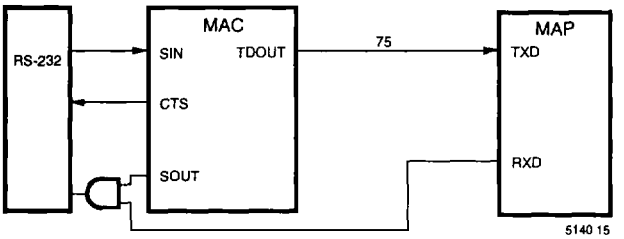


Figure 5c. Serial Mode—V.23 Originate Only

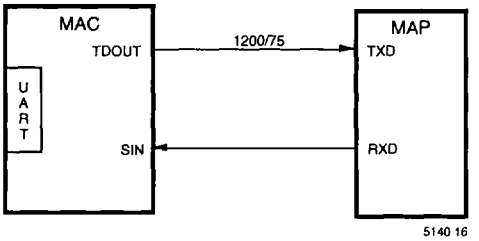


Figure 5d. Parallel Mode—V.23 Originate Only with SC11021

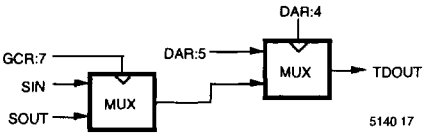


Figure 5e. TDOUT Function

Figure 5. V.23 Interface to SC11021

ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore, it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain (G_R) and transmit gain (G_T) are set by the ratios of resistors R2, R1 and R6, R5, respectively (Figure 4).

The circuit can be analyzed as follows:

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_y = 2V_{TX}$,

$$V_R = -\frac{R2}{R1}(V_{TX} + V_{RX}) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$
$$= -\frac{R2}{R1}V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) = \frac{R2}{R1}$$

Solving for R3/R4:

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:

R1 = 20KΩ, R2 = 27KΩ, R3 = 13KΩ, R4 = 5.1KΩ, R5 = 20KΩ, and R6 = 27KΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated, and point X can be connected to point Y in the circuit of Figure 4 to achieve a more cost effective external hybrid arrangement.

The SC11045/SC11055 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, the "Hybrid" bit must be turned off. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator, V.22 guard-tone, and 1300 and 2100 Hz tone generators. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and A, B, C, D, *, and # keys. The V.22 guard-tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the tone control register. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300, 1100, 464 and 2100 Hz and the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50K Ohms is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB attenuation, 12 dB attenuation, and squelch are provided through the ALC1 and ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Clock Input

CLK_{IN} should be connected to a 9.8304 MHz clock source with an accuracy of ±50 ppm.

Address $A_4A_3A_2A_1$	Name	Bit 7	6	5	4	3	2	1	0
0000	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
0001	I1	I17	I16	I15	I14	I13	I12	I11	I10
0010	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20
0011	I2	I27	I26	I25	I24	I23	I22	I21	I20
0100	STATUS	TD1300	TD1650	FLGDT/TD390	AGC0	TD2100	TD2225	FSKD	ED
0101	FAXV21R	R7	R6	R5	R4	R3	R2	R1	R0
0110	UNUSED	—	—	—	—	—	—	—	—
0111	UNUSED	—	—	—	—	—	—	—	—

Internal Status Register (Read Only)

Address $A_4A_3A_2A_1$	Name	Bit 7	6	5	4	3	2	1	0
1000	TXCR	BR2	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1001	MCRA	SLAVE	LCR/$\overline{INT}$	RNGX/TRITX	SYNC	WLS1	WLS0	A/$\overline{O}$	RXMRR
1010	MCRB	BR3	PD	TONEDETE	CPM	ALB	TL2	TL1	TL0
1011	TONE	CIDRLY	HNDSHK	TONEON	DTMF	D3	D2	D1	D0
1100	PGCR	TL3	AGCVT	G5	G4	G3	G2	G1	G0
1101	DATA	GDFLAT	PLLJAM	PLLFRZ	PLLFAST	RD3	RD2	RD1	RD0
1110	AUDIO	ANS/$\overline{ANS}$	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC0
1111	FAXR	B7	B6	B5	B4	B3	B2	B1	B0

Internal Control Register (Write Only)

INTERNAL STATUS REGISTERS

NOTE: All samples are represented in two's complement form.

Read Register (Q1), Address (A4–A1) 0000

Bit Number	Bit Name	Description
7–0	Q17–Q10	Stores midbaud inphase sample output of ADC.

Read Register (I1), Address (A4–A1) 0001

Bit Number	Bit Name	Description
7–0	I17–I10	Stores midband quadrature sample output of ADC.

Read Register (Q2), Address (A4–A1) 0010

Bit Number	Bit Name	Description
7–0	Q27–Q20	Stores endband inphase sample output of ADC.

Read Register (I2), Address (A4–A1) 0011

Bit Number	Bit Name	Description
7–0	I27–I20	Stores endband quadrature sample output of ADC.

Status Register, Address (A4–A1) 0100

Bit Number	Bit Name	Description
7	TD1300	1300 Hz tone detector output. TD1300 = 1 when this tone is present.
6	TD1650	1650 Hz tone detector output. TD1650 = 1 when this tone is present.
5	FLAGDET/ TD390	In FAX mode: Flag Sequence detector output. When set, flag sequence is present in V.21FAX mode. In V.23 mode: 390 Hz tone detector output. TD390 = 1 when this tone is present.
4	AGCO	Status of internal 1-bit AGC. When this bit is set, RXA signal is amplified by 8 dB before entering the bandpass filters.
3	TD2100	2100 Hz tone detector output. TD2100=1 when this tone is present.
2	TD2225	2225 Hz tone detector output. TD2225=1 when this tone is present.
1	FSKD	Received FSK data. FSKD = 1 when mark is received.
0	ED	Energy detect circuit output. ED = 1 when energy detected.

FAXV21R Register, Address (A4–A1) 0101

Bit Number	Bit Name	Description
7–0	R7–R0	In V.21 FAX receive mode this register will be loaded by received data and should be read every eighth interrupt pulse. LSB (R0) corresponds to the data bit received first in time.

INTERNAL CONTROL REGISTERS

Transmit Control Register (TXCR), Address (A4–A1) 1000

When writing into these registers, the bus lines corresponding to the unused bits are ignored by the SC11045/SC11055.

Bit Number	Bit Name	Description
7	BR2	This bit, in conjunction with BR3, BR1 and BR0, selects bit rate.
6	HYBRID	When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2 to 4 wire conversion.
5–3	TXSEL2–0	Transmit Select bits. These 3 bits determine the data transmitted by the transmitter according to the following table:

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loop back mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

NOTE 1: S1 is a pattern of 0011 transmitted at 1200 bit/s rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bit/s rate.

NOTE 2: In this mode, the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the Synchronous mode.

NOTE 3: Reversals are continuous streams of 01.

NOTE 4: When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

2	SQT	When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see Figure 1) to analog ground.

INTERNAL CONTROL REGISTERS (continued)

1–0 BR1–BR0

Bit Rate Selection bits based on the following tables:

SC11045 (BR3 is internally forced to zero)

BR2	BR1	BR0	BIT RATE (bits/sec)		MODE	MODULATION SCHEME
0	0	0	2400	V.22 bis	Modem	16-pt QAM
0	0	1	0–300	Bell 103	Modem	FSK
0	1	0	1200	V.22	Modem	4-pt DPSK
0	1	1	0–300	V.21	Modem	FSK
1	0	0	4800	V.27	Fax	8-pt DPSK
1	0	1	75/1200	V.23	Modem	FSK
1	1	0	2400	V.27 FB	Fax	4-pt DPSK
1	1	1	0–300	V.21 FAX	Fax	FSK

SC11055

BR3	BR2	BR1	BR0	BIT RATE (bits/sec)		MODE	MODULATION SCHEME
0	0	0	0	2400	V.22 bis	Modem	16-pt QAM
0	0	0	1	0–300	Bell 103	Modem	FSK
0	0	1	0	1200	V.22	Modem	4-pt DPSK
0	0	1	1	0–300	V.21	Modem	FSK
0	1	0	0	4800	V.27	Fax	8-pt DPSK
0	1	0	1	75/1200	V.23	Modem	FSK
0	1	1	0	2400	V.27 FB	Fax	4-pt DPSK
0	1	1	1	0-300	V.21 FAX	Fax	FSK
1	0	0	0	9600	V.29	Fax	16-pt QAM
1	0	0	1	N/A		N/A	
1	0	1	0	7200	V.29 FB	Fax	8-pt QAM
1	0	1	1	0-300	V.21 FAX	Fax	FSK
1	1	0	0	N/A		N/A	
1	1	0	1	N/A		N/A	
1	1	1	0	N/A		N/A	
1	1	1	1	0-300	V.21 FAX	Fax	FSK

Mode Control Register A (MCRA), Address (A4–A1) 1001

Bit Number	Bit Name	Description
7	SLAVE	When set, receiver timing will be used as clock source for transmitter. LCK/INTB and SYNC bits must be high for slave mode.
6	LCK/$\overline{\text{INT}}$	Determines the clock source for the transmitter. When this bit is set, the clock source is externally provided on SCTE (pin 4), and when cleared, it is internally generated (SCT). This bit can select the clock source independent of Sync/Async mode selection (see below). When in Digital Loop-Back mode, the clock source will be forced to the Slave mode (SCR).
5	RNGX/TRITX	Range extender for the receiver Sync/Async converter. When set, the receiver Sync/Async can insert up to one stop bit per four (8, 9, 10 or 11-bit) characters to compensate for a far end DTE being up to 2.3% over speed. The transmitter Async/Sync always handles this overspeed condition regardless of this bit's condition.In V.23/CID mode, setting RNGX/TRITX = 1 tri-states the transmit output; setting RNGX/TRITX = 0, enables the transmit output.
4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in Digital Loop-Back mode, the SC11045/55 will be forced to the Synchronous mode. In V.23 1200 bps mode, setting this signal to 1 enables synchronous clock recovery circuit.

INTERNAL CONTROL REGISTERS (continued)

3–2	WLS1–WLS0	Word length select bits in asynchronous mode, according to the following table:

WLS1	WLS0	NUMBER OF BITS PER CHARACTER
1	0	8
1	1	9
0	0	10
0	1	11

1	A/$\overline{O}$	When set, operate in answer mode; when clear, operate in originate mode.
0	RXMRR	When set, the RXD pin is clamped to the high logical level.

Mode Control Register B (MCRB), Address (A4–A1) 1010

Bit Number	Bit Name	Description
7	BR3	This bit in conjunction with BR2–BR0 selects the bit rate in SC11055. This bit is forced low (BR3 = 0) in SC11045 mode.
6	PD	When this bit is set, chip will be powered down. When cleared normal operation is restored.
5	TONDETE	When this bit is set, 2100/2225 Hz tone detector will be enabled. However, for proper functioning, highband filter must be set in the receive path to pass these tones. Tone amplification before detection can be set by PGC.
4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high band filter to detect answer tone (ALB=0) or to the low band filter scaled down 2.5 times (ALB=1) to listen for the call progress tones during auto dialing.
3	ALB	Analog Loop Back. When set, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.
2–0	TL2–TL0	Transmit level adjust bits based. In FAX modes (V.21 FAX, V.27, V.29) maximum transmit level will be 2 dB lower than modem modes (V.21, V.22, V.23, Bell 103, Bell 212).

				TRANSMIT LEVEL AT TXA PIN (dBm)	
TL2	TL1	TL0	TL3	MODEM MODE	FAX MODE
0	0	0	0	-3	-5
0	0	0	1	-4	-5
0	0	1	0	-5	-5
0	0	1	1	-6	-6
0	1	0	0	-7	-7
0	1	0	1	-8	-8
0	1	1	0	-9	-9
0	1	1	1	-10	-10
1	0	0	0	-11	-11
1	0	0	1	-12	-12
1	0	1	0	-13	-13
1	0	1	1	-14	-14
1	1	0	0	-15	-15
1	1	0	1	-16	-16
1	1	1	0	-17	-17
1	1	1	1	-18	-18

TONE Register, Address (A4–A1) 1011

Bit Number	Bit Name	Description
7	CIDRLY	Setting CIDRLY = 1 activates the relay driver; setting CIDRLY = 0 deactivates the relay driver.
6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, FSK demodulator is disabled when in high speed mode.
5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.

INTERNAL CONTROL REGISTERS (continued)

Bit Number	Bit Name	Description
4	DTMF	When set, the DTMF generator is turned on. When cleared, the DTMF generator is turned off, but other tones can be generated. NOTE: TONEON must also be set to generate DTMF signals.
3–0	D3–D0	Specify the desired tone (see the following table):

DTMF	D3	D2	D1	D0	DIGIT DIALED	TONE OUTPUT FREQUENCIES (Hz)	
1	0	0	0	0	0	941	1336
1	0	0	0	1	1	697	1209
1	0	0	1	0	2	697	1336
1	0	0	1	1	3	697	1477
1	0	1	0	0	4	770	1209
1	0	1	0	1	5	770	1336
1	0	1	1	0	6	770	1477
1	0	1	1	1	7	852	1209
1	1	0	0	0	8	852	1336
1	1	0	0	1	9	852	1477
1	1	0	1	0	*	941	1209
1	1	0	1	1	(A)	697	1633
1	1	1	0	0	(B)	770	1633
1	1	1	0	1	(C)	852	1633
1	1	1	1	0	#	941	1477
1	1	1	1	1	(D)	941	1633
0	0	0	0	0		No tone; tone generator turned off	
0	0	0	0	1		550	
0	0	0	1	0		1800	
0	0	0	1	1		2100	
0	0	1	0	0		1300	
0	0	1	0	1		1100	
0	0	1	1	x		462	
0	1	x	x	x		No tone; tone generator turned off	

Programmable Gain Controller Register (PGCR), Address (A4–A1) 1100

Bit Number	Bit Name	Description
7	TL3	When set, the transmit level id further attenuated by 1 dB. (See TL2-TL0.)
6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16-way decision making.
5–0	G5–G0	Control the gain of the PGC within a range from –10 to +37.5 dB in 0.75 dB steps. (See the following table.) NOTE: Signal level is adjusted by an internal AGC with +8 dB or 0 dB gain, plus a fixed gain of 5 dB in the filter.

G5	G4	G3	G2	G1	G0	PGC GAIN (dB)
0	0	0	0	0	0	–10.0
0	0	0	0	0	1	–9.25
0	0	0	0	1	0	–8.5
0	0	0	1	0	0	–7.0
0	0	1	0	0	0	–4.0
0	1	0	0	0	0	+2.0
1	0	0	0	0	0	+14.0
1	1	1	1	1	1	+37.25

INTERNAL CONTROL REGISTERS (continued)

DATA Register, Address (A4–A1) 1101

Bit Number	Bit Name	Description
7	GDFLAT	When set, the group delay of the transmit band split filters will be flat. When clear, the filter group delay response is compromise delay.
6	PLLJAM	When this bit is set, the DPLL will be reset by the next rising edge of the received baud clock. This bit must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ (see below) overrides PLLJAM when both are enabled.
5	PLLFRZ	Phase locked loop freeze. When this bit is set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
4	PLLFAST	When set, the DPLL operates in "fast" locking mode. In this mode, the DPLL is updated on every baud period by 13 µs steps. When this bit is cleared (default mode), the DPLL operates in "normal" locking mode and is updated once every 8 baud periods by 6.5 µs steps.
3–0	RD3–RD0	Four-bit Received Data. Used only in high speed (1200 or 2400 bit/s) mode, they are descrambled by the processor and shifted out by the SC11045/55. Sync to Async is also done by the SC11045/55, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2 and RD3. In the 1200 bit/s mode, only RD0 and RD1 are shifted out during one baud period.

AUDIO Register, Address (A4–A1) 1110

Bit Number	Bit Name	Description
7	ANS/$\overline{\text{ANS}}$	Switching this bit from 0 to 1 or 1 to 0 will reverse the phase of the 2100 Hz Answer Tone.
6	DISS	When this bit is set, the scrambler is disabled, when cleared, it is enabled. Transmit select bits (TXSEL0–2) override this bit when in "transmit internal mode".
5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and canceled by the controller.
4–2	TEST	Test bits used for factory testing. For normal chip operation, these bits must be cleared.
1	ALC1	Audio level control bit 1.
0	ALC0	Audio level control bit 0. These two bits are used to control the audio level at AUDIO pin according to the following table:

ALC1	ALC0	AUDIO ATTENUATION (dB)
0	0	Audio off
0	1	12
1	0	6
1	1	0 (no attenuation)

NOTE: The audio signal may be amplified by 8 dB by the line receiver AGC before being fed to the audio attenuator.

FAX Register, Address (A4–A1) 1111

Bit Number	Bit Name	Description
7–0	B7–B0	In V.27 or V.29 modes, this register has to be loaded at every interrupt with an 8-bit word that identifies constellation points for two consecutive baud periods. 4 LSB's correspond to first baud in time. In V.21FAX mode, when transmitting, the register should be loaded every eighth interrupt pulse. In V.21FAX, LSB is the data bit which is first in time.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1—SC11045/55 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 6.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11045/55 in the synchronous mode. This provides a 2400/1200 Hz clock on the SCT pin that can be used as a clock source for the DTE. The Transmit Phase-Locked-Loop (TX PLL) of the SC11045/55 will be in free-running mode.

Case 2—SC11045/55 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode, also select "Locked" mode.

The TX PLL of SC11045/55 will then synchronize itself to the clock provided on its "SCTE" pin.

If TX timing should be slaved to the receiver recovered clock, select synchronous and "Locked" mode and set SLAVE bit.

In either case, the SC11045/55 will sample the data on the rising edge of the clock.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock. Data is valid on the rising edge of the clock.

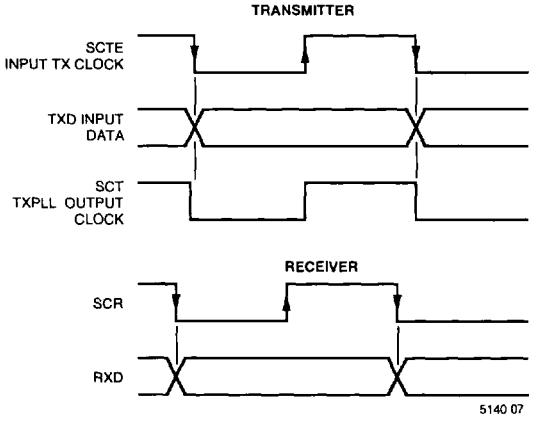


Figure 6. SC11045/SC11055 Synchronous Mode Timing Diagrams

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} – GND	7 V
DC Input Voltage (Analog Signals)	A_{GND} – 0.6 to V_{CC} +0.6 V
DC Input Voltage (Digital Signals)	D_{GND} – 0.6 to V_{CC} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Unless otherwise specified, all voltages are referenced to ground.

NOTE 3: Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

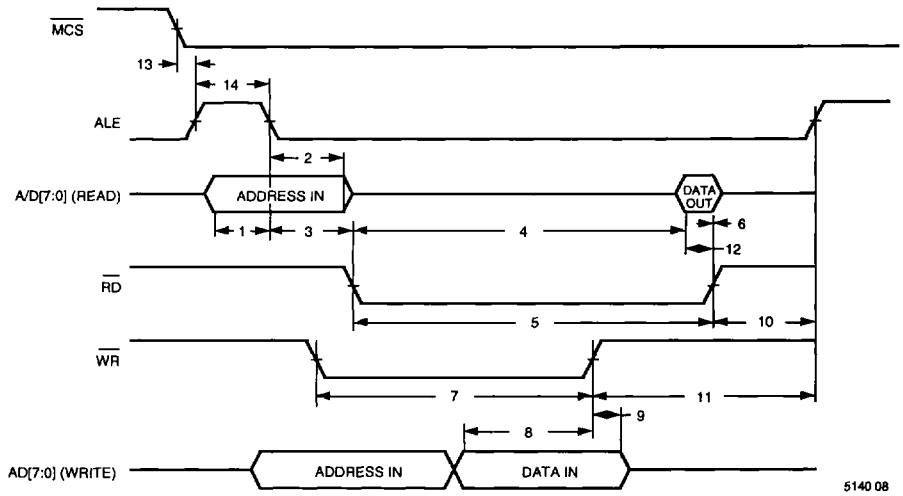
OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
A_{GND}, D_{GND}	Ground			0		V
F_C	Clock Frequency		9.8300	9.8304	9.8309	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLK_{IN}			500	ns
T_R, T_F	Input Rise or Fall Time	CLK_{IN}			20	ns

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal Power Down Mode		17 1.0	25 4	mA mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Ouput (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Ouput (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V	3			V_{PP}
RLYOL	Relay output low	RL = 390Ω		0.7	1	V

PROCESSOR BUS TIMING



	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	t_{AVEL}	Address Valid to ALE low		30			ns
2	t_{HAD}	Hold address after ALE low		40			ns
3	t_{ALRD}	Delay from ALE low to $\overline{RD}$ low		45			ns
4	t_{DVRL}	Data valid after $\overline{RD}$ low				180	ns
5	t_{RD}	Read pulse width		200			ns
6	t_{DHRD}	Data hold after $\overline{RD}$ high		0			ns
7	t_{WR}	Write pulse width		150			ns
8	t_{DVWR}	Data setup before $\overline{WR}$ high		70			ns
9	t_{DHWR}	Data hold after $\overline{WR}$ high		15			ns
10	t_{RHLH}	End of read to next ALE		55			ns
11	t_{WHLH}	End of write to next ALE		120			ns
12	t_{DVRH}	Data valid set-up to $\overline{RD}$ high		15			ns
13	t_{MCAL}	$\overline{MCS}$ low to ALE high		10			ns
14	t_{ALE}	ALE Pulse width		40			ns

Figure 7. Processor Bus Timing

MODEM TRANSMIT SIGNALS – Hz (CLK_{IN} = 9.8304 MHz)

PARAMETER	CONDITIONS	NOM.	ACT.	UNITS
Bell 103				
Answer Mark		2225	2226	Hz
Answer Space		2025	2024.4	Hz
Originate Mark		1270	1269.4	Hz
Originate Space		1070	1070.4	Hz
CCITT V.21				
Answer Mark		1650	1649.4	Hz
Answer Space		1850	1850.6	Hz
Originate Mark		980	978.3	Hz
Originate Space		1180	1181.5	Hz
CCITT V.23				
Answer Mark		1300	1300.3	Hz
Answer Space		2100	2100.5	Hz
Originate Mark		390	389.4	Hz
Originate Space		450	450.1	Hz

Call progress monitor mode:		MIN	TYP	MAX	
Center frequency	ALB = 1, G5–G0 = 101111		480		Hz
Detect level (ED high) measured at RXA		–43			dBm
Reject level (ED low) measured at RXA				–48	dBm
Hysterisis measured at RXA		2			dB
Delay time (ED low to high)	EDC = 1.0 µF	10	15	24	ms
Hold time (ED high to low)	EDC = 1.0 µF	10	15	24	ms

DTMF GENERATOR (CLK_{IN} = 9.8304 MHz)

PARAMETER	NOMINAL FREQUENCY	ALLOWABLE ERROR (Note 1)	ACTUAL ERROR
Row 1	697 Hz	±1%	–0.23%
Row 2	770 Hz	±1%	–0.01%
Row 3	852 Hz	±1%	–0.12%
Row 4	941 Hz	±1%	–0.39%
Column 1	1209 Hz	±1%	–0.35%
Column 2	1336 Hz	±1%	–0.93%
Column 3	1477 Hz	±1%	–0.48%
Column 4	1633 Hz	±1%	–0.91%
Guard Tones	550 Hz 1800 Hz	±20 Hz ±20 Hz	–2 Hz –2 Hz
Calling Tone	1300 Hz		–6 Hz
Answer Tone	2100 Hz	±15 Hz	+3.2 Hz
Calling Tone	1100 Hz	±38 Hz	–3.8 Hz
PIS Tone	462 Hz	±1.5 Hz	–0.05 Hz

NOTE 1: CCITT Specification

DTMF GENERATOR (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion	V_{CC} = +5 V TL2 = TL1 = TL0 = 0 Measured at TXA Pin		–40		dB
Row Output Level			–2		dBm
Column Ouput Level			0		dBm
550 Hz Guard Tone			–3		dB (Note 1)
1800 Hz Guard Tone			–6		dB (Note 1)
1300 Hz Calling Tone			–3		dBm
2100 Hz Answer Tone			–3		dBm
1100 Hz Calling Tone			–3		dBm
462 Hz PIS Tone			–3		dBm
Transmit level measured at TXA	Load = 1200 Ohms TL2 = TL1 = TL0 = 0 Squelched		–3	 –50	dBm dBm

NOTE 1: These levels are referenced to the TX signal level. When guard tones are added, the TXA level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 1.0 µF; measured at RXA PGC = 0				
Energy detect level (ED low to high)				–43	dBm
Loss of energy detect level (ED high to low)		–48			dBm
Hysterisis		2			dB

Programmable Gain Controller (PGC)

Gain step size			0.75		dB
Dynamic range			47.25		dB
Response time (from change in PGC register to output of A to D converter)			1.0		ms

Filter Characteristics

Crosstalk rejection			70		dB
Power supply rejection			0		dB
DPLL Response times JAM or FRZ Fast			20 200		µs µs

TYPICAL APPLICATIONS

The SC11045/55 with an external control microprocessor, a telephone line interface and a suitable computer interface, can implement a complete 2400 bit/s Sendfax modem with a minimum of components and cost.

The only external components required by the SC11045/SC11055 are a 600 Ω line matching resistor and a 1.0 µF capacitor from the EDC pin to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11045/SC11055 can directly drive a high impedance (50 kΩ) earphone-type transducer.

Figures 8 and 9 show the standalone and PC bus integral modems implemented with Sierra's SC11074/75 MACs.

The SC11045/SC11055 may also be controlled by SC11074 or SC11075 internal ROM controllers. See the SC11019 series data sheet.

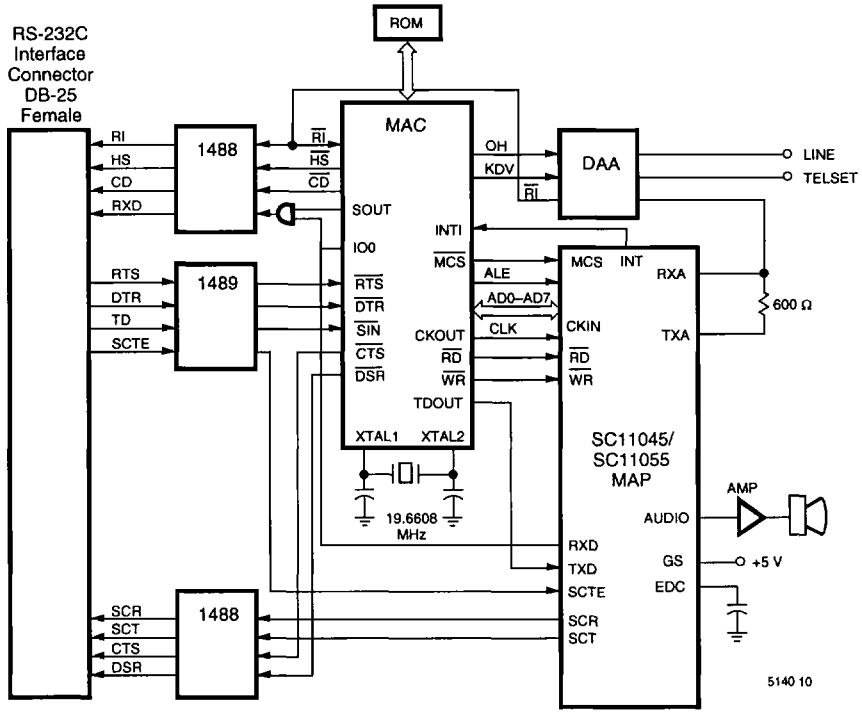


Figure 8. V.22bis Standalone Sendfax & Data Modem

TYPICAL APPLICATIONS (continued)

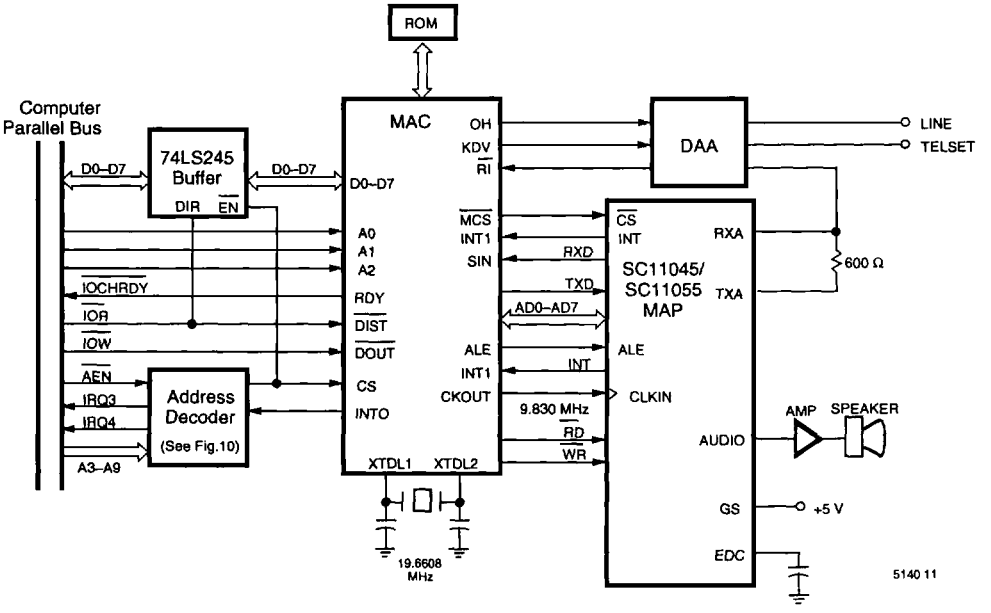


Figure 9. Internal Sendfax & Data Modem for PC Bus Applications

Detailed schematics for these and other combinations are available on the Sierra BBS.