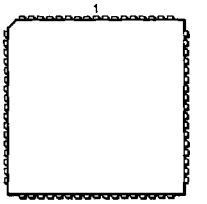
FEATURES

- ☐ Supports MNP2–5 and CCITT V.42bis, CCITT V.42
- ☐ Supports SDLC, HDLC, Bisync, Monosync & Async protocols in software
- ☐ Serial Transmit Bit
- ☐ Can address 128Kx8 ROM, 31.25Kx8 RAM
- ☐ Selectable Clock Frequency
- ☐ 16x16 multiply in 2μs
- ☐ Low Power Power-down (Stop) Mode
- ☐ Supports asymmetric protocols
- ☐ Sleepmode
- ☐ Pin compatible with SC11011, 21, 61, 91, 95
- ☐ Direct interface to Sierra Modems & Datapumps
- ☐ 384 Byte internal RAM
- ☐ Power Down mode indicator on $\overline{PD}$ pin
- ☐ CMOS technology
- ☐ 16C450 compatible UART

APPLICATIONS

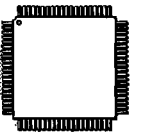
- ☐ V.22bis modem with V.42bis compression (11043)
- ☐ MNP2–5 modems
- ☐ Class 1 and 2 Fax & Data modems
- ☐ Feature rich International modems
- ☐ Upgrade from SC11011, 11021, 11061, 11091, 11095
- ☐ Synchronous data links
- ☐ Voice, Fax and Data modems

68-PIN PLCC PACKAGE



SC11031CV, SC11040CV, SC11041CV, SC11042CV, SC11043CV

80-PIN QFP PACKAGE (14 mm)



SC11031CQ, SC11040CQ, SC11041CQ, SC11042CQ, SC11043CQ

GENERAL DESCRIPTION

The SC11031/SC11040 series are application-specific Modem Controllers that perform DSP and control functions for a variety of modems operating up to 9600 bps. Various members of the family can perform error control and compression algorithms according to MNP2–5, V.42bis and other specifications. They can also be used for combination Voice, Fax and Data modems.

These second generation devices offer expanded addressing capability for feature-rich products. They also consume substantially less power compared to earlier devices and offer very low power standby modes.

The SC11031 is ROMless and is used for general applications. It can be used in place of SC11011,

BLOCK DIAGRAM
(Parallel Mode Callout)

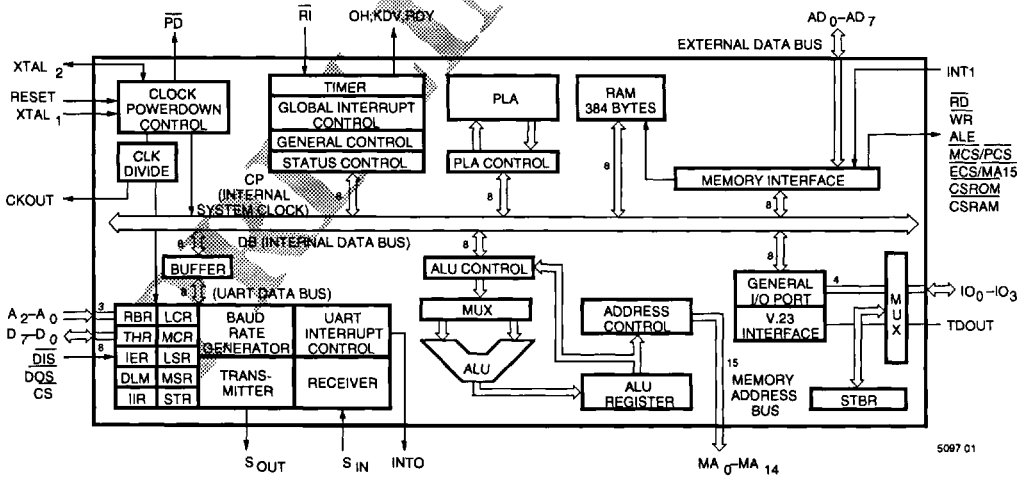


Figure 1.

GENERAL DESCRIPTION (continued)

SC11021, or SC11061. SC11040 series devices have internal ROM programmed for specific applications. See Table 1 for a summary of these devices.

These devices contain a 16C450 compatible UART which can be configured to provide a serial or parallel DTE interface. In the RDY mode, the MAC II provides an I/O channel ready (RDY) signal to insert wait states in the PC bus read/write cycle to allow reliable data transfer with any speed bus.

	SC11031	SC11040	SC11041	SC11042	SC11043
V.21, V.22, V.22 bis Bell 212A/103	✓	✓	✓	✓	✓
Fax Class	1, 2		1, 2	1, 2	1, 2
MNP2–5			✓	✓	✓
V.42				✓	✓
V.42bis					✓
Caller I.D.	optional	optional	optional	optional	optional
Voice		optional	optional	optional	optional

Table 1. SC1104X Series Function

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER PLCC	PIN NUMBER QFP	DESCRIPTION
I. Parallel Systems Interface (to PC bus)			
A_0–A_2	57, 55, 53	57, 55, 53	**INPUT, TTL.** Address lines for UART register select.
$\overline{CS}$	63	64	**INPUT, TTL.** Chip select, active low.
D_0–D_7	50, 48, 46, 43, 41, 40, 39, 37	50, 48, 46, 39, 37, 36, 35, 33	**INPUT-OUTPUT, TTL.** 8-bit data port.
$\overline{DIS}$	64	65	**INPUT, TTL.** Data in strobe (PC reads from UART registers), active low.
$\overline{DOS}$	59	59	**INPUT, TTL.** Data out strobe (PC writes into UART registers), active low.
INTO	66	67	**OUTPUT, CMOS/TTL.** Tristate™. Interrupt.
RDY	60	61	**OUTPUT.** Open Drain. Ready signal for high speed PC-AT interface.
II. RS-232 (Data Set Mode) and Display Interface			
$\overline{AA}$	55	55	**OUTPUT, CMOS/TTL.** Automatic answer enable indicator (low).
$\overline{CTS}$	59	59	**OUTPUT, CMOS/TTL.** Clear to send.
$\overline{DSR}$	63	64	**OUTPUT, CMOS/TTL.** Data set ready.
$\overline{DTR}$	64	65	**INPUT, TTL.** Data terminal ready.
$\overline{HS}$	53	53	**OUTPUT, CMOS/TTL.** High speed indicator. Low when operating at 2400 bps rate. High otherwise.
$\overline{MRDY}$	66	67	Modem ready.
$\overline{RLSD}$	57	57	**OUTPUT, CMOS/TTL.** Carrier detect.
$\overline{RTS}$	37	33	**INPUT, TTL.** Request to send, input, TTL.

Tristate is a trademark of National Semiconductor.

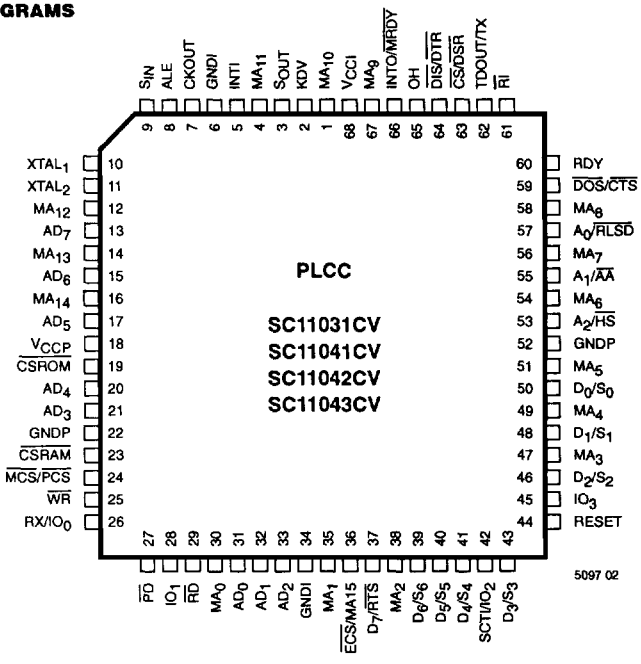
PIN DESCRIPTIONS (continued)

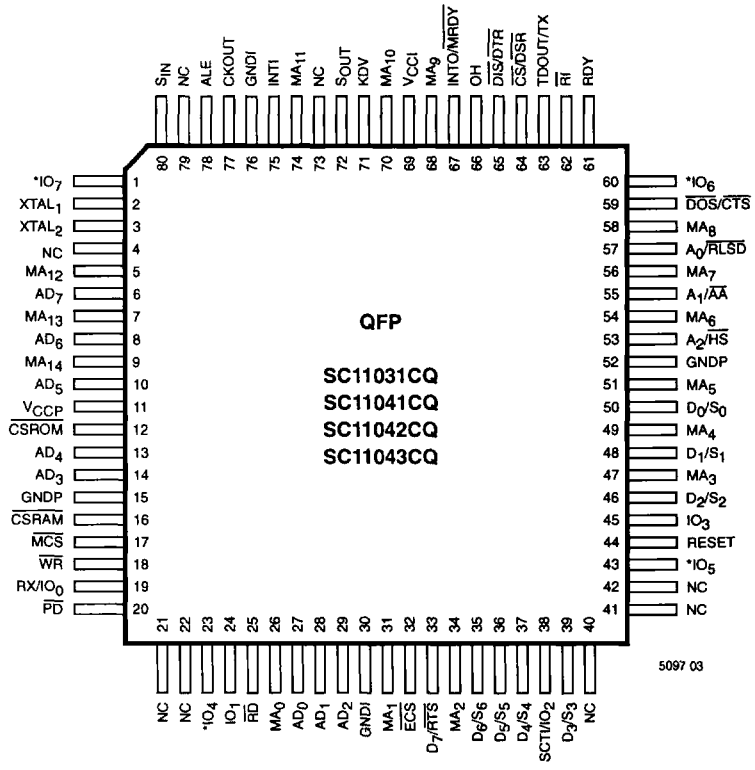
PIN NAME	PIN NUMBER PLCC	PIN NUMBER QFP	DESCRIPTION
			III. MAP Interface
AD_0–AD_7	31–33, 21, 20, 17, 15, 13	27–29, 14, 13, 10, 8, 6	**INPUT–OUTPUT, CMOS.** 8-bit bidirectional multiplexed address/databus. Weak internal pull-ups (30kΩ) are provided on these inputs.
ALE	8	78	**OUTPUT, CMOS/TTL.** Address Latch Enable. The address on ECS, MCS, AD_7 – AD_0 are valid at the falling edge of this normally low pulse.
$\overline{ECS}$/MA15	36	32	**OUTPUT, CMOS/TTL.** External EERAM chip select. Addressing space is from 280H to 2FFH. When used for expanded ROM mode, the ECS functions as MA15.
INTI	5	75	**INPUT, TTL.** Interrupt received from the MAP. Interrupt is detected when this pin has a low to high transition. The line has to stay high for at least 200 ns.
$\overline{MCS}$/$\overline{PCS}$	24	17	**OUTPUT, CMOS/TTL.** Map chip select for MAP interface. Addressing space is from 200H to 27FH. When used in expanded ROM mode, the Addressing space expands from 200H to 2FFH. This function is known as PCS, Peripheral Chip Select.
$\overline{RD}$	29	25	**OUTPUT, CMOS/TTL.** RAM read. Normally high, data on AD_7 – AD_0 must be valid at the rising edge of this pulse.
S_{IN}	9	80	**INPUT, TTL.** Received data. Serial data received from the DTE.
S_{OUT}	3	72	**OUTPUT, CMOS/TTL.** Transmit data. Serial data to be transmitted to the modem.
$\overline{WR}$	25	18	**OUTPUT, CMOS/TTL.** Peripheral write. Normally high, data on AD_7 – AD0 is valid at the rising edge of this pulse.
			IV. Switch Port Pins (RS-232 Mode)
KDV	2	71	**OUTPUT, CMOS/TTL.** Data/voice Relay Control. When high, indicates the voice (telephone set) relay is closed and the modem is in the voice mode.
OH	65	66	**OUTPUT, CMOS/TTL.** Off-hook. When high, indicates the DAA should go off-hook.
S_0–S_6	50, 48, 46, 43, 41–39	50, 48, 46, 39, 37–35	**INPUT, TTL.** 7-bit input port for sensing switch setting inputs. Weak internal pull-ups (30 kΩ) are provided on these inputs. These only work in serial mode.
			V. DAA Interface
$\overline{RI}$	61	62	**SCHMITT INPUT.** Ring indicator. When low, indicates the modem is receiving a ringing signal.
			VI. External ROM/RAM Interface
$\overline{CSRAM}$	23	16	**OUTPUT, CMOS/TTL.** Chip select for external RAM, address from 300H to 7FFFH.
$\overline{CSROM}$	19	12	**OUTPUT, CMOS/TTL.** Chip select for external ROM, address from 8000H to FFFFH.
MA_0–MA_{14}	30, 35, 38, 47, 49, 51, 54, 56, 58, 67, 1, 4, 12, 14, 16	26, 31, 34, 47, 49, 51, 54, 56, 58, 68, 70, 74, 5, 7, 9	**OUTPUT, CMOS/TTL.** 15 bit address bus for external program/data access.
$\overline{PD}$	27	20	**OUTPUT, OPEN DRAIN.** Indicates power down mode by active low.
TDOUT/TX	62	63	**OUTPUT, TTL/CMOS.** Transmit DATA. Serial data to be transmitted by the modem.
RX	26	19	**INPUT, TTL.** Serial Data received by the modem.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER PLCC	PIN NUMBER QFP	DESCRIPTION
VII. Other Pins			
CKOUT	7	77	**CLOCK OUTPUT PIN, TTL/CMOS.** From MAC II (9.8304 MHz).
RESET	44	44	**INPUT, TTL, ACTIVE HIGH.** Master reset schmitt. When RESET is high, MAC II program counter resets to location 2000H. It resumes counting after RESET goes low.
V_{CCI}	68	69	+5 V.
V_{CCP}	18	11	Second V_{CC} pin.
$XTAL_1$	10	2	Together with $XTAL_2$ for crystal input (19.6608 MHz or 29.4912MHz).
$XTAL_2$	11	3	Crystal output pin (19.6608 MHz or 29.4912 MHz).
GNDI	6	76	Ground.
GNDI	34	30	Fourth Ground pin.
GNDP	22	15	Second Ground pin.
GNDP	52	52	Third Ground pin.
VIII. Special Pin Functions			
The MAC II can be configured to emulate the BigMAC (SC11021) which has four IO pins and a TDOUT pin added. For the MAC II, the functions of these 5 pins are preserved on power up or reset. When the STBR (Serial Transmit Bit Register) mode is selected, IO2 becomes SCTI, IO0 becomes RX, and TDOUT becomes TX.			
IX. In STBR Mode			
SCTI	42	38	**INPUT, TTL.** Synchronous clock transmit. TData to the MAP is strobed in on the rising edge of this clock.
TX	62	63	**OUTPUT, TTL/CMOS.**
X. In Big MAC mode			
IO_0-IO_7	26, 28, 42, 45	19, 24, 38, 45, 23, 43, 60, 1	**GENERAL I/O PORT, TTL/CMOS, TRI-STATE.** Each I/O can be configured as input or output under the control of GIO register. Weak internal pull-ups are provided on these inputs. IO_4 through IO_7 is only available in QFP for the SC11031.

CONNECTION DIAGRAMS





* SC11031 only

FUNCTIONAL DESCRIPTION

The MAC II has External ROM address space of 64K. On power up the original 32K ROM is selected. A register select is provided to switch over to the expanded 32K ROM using the ECS pin.

Expanded internal RAM of 384 bytes allows for more features including buffering for Fax and asymmetrical modem protocols such as V.23.

The original 16K RAM address is expanded to 31.25K as required for full V.42bis implementation.

In Power Down (or Stop) mode, the internal CPU clock is turned off. The power-down circuitry is kept alive and ready to respond to any valid power up input. The power-down bit is reset by hardware when DTR or SIN becomes active on a negative edge trigger, when RI becomes level active, or a valid CS is generated by the PC Bus, (level active low).

In the RC Mode an internal oscillator is used instead of the XTAL oscillator. If one enters power-down mode while in RC mode, the XTAL oscillator is turned off, thereby reducing the powerdown current by more than 50%. When coming out of powerdown while in RC mode, the firmware must wait 20 msec before switching back to XTAL mode because the XTAL oscillator needs time to start-up and stabilize. A power-down mode indication is available from the $\overline{PD}$ pin to control external power switches.

In normal operation, the $\overline{PD}$ pin behaves as a tristate pin. When power down is activated, the $\overline{PD}$ pin becomes output active low. It can be used to drive an LED indicator or control power to other devices.

The active power can be reduced by using the sleep mode. The system clock can be divided down by 5 different divisors. Please refer to the GCR2 register description. CKOUT is unaffected, but the UART base clock of the baud rate generator is affected. If the UART is used in sleep mode, then the divisor numbers need to be compensated for by the same divisor.

When the MAC II is first powered up or reset, it defaults to Big MAC mode, which is also the mode for the MAC (11011). All programs written for ROMless Big MAC (11021) and MAC (11011) or the FastMAC (11061) should run with minor modifications.

Weak pullups are provided on switch inputs so that external pullup resistors are not needed when option switches are employed.

Internal multiplexing for asymmetrical protocols such as V.23 (1200/75 bps) is provided to allow both answer and originate modes without additional chips.

The former EA pin of MAC and Big MAC (pin 27) is redefined on the MAC II to indicate power down status and renamed $\overline{PD}$. On power down activation the $\overline{PD}$ pin becomes output low. Otherwise it is tristated.

The MAC II has a selectable internal clock divider so it can be used with either a 19.6608 MHz or 29.412 MHz crystal. Start-up assumes a 19.6608 MHz crystal for compatibility with SC11011 or SC11021.

The MAC II interfaces to a parallel system bus, such as that in the IBM PC, or by changing one bit in a register it interfaces to an RS-232 port. The power on/reset default is parallel configuration.

The MAC II is interrupted once every 1.667 msec (600 Hz). It must read two I channel samples and two Q channel samples (T/2 sampling) within 100 µsec of receiving the interrupt.

After the samples are processed a quad-bit (4 bits) of descrambled data is written back to the MAP. The MAP performs the synchronous to asynchronous conversion function, if operating in asynchronous mode, and outputs the received data on the RXD pin.

The MAC II uses a bit slice core processor to perform the digital signal processing (DSP) and the control functions. Its instruction set is a subset of the Intel 8096 instruction set but operates faster than the 8096. For instance, a signed (2's complement) 16 bit by 16 bit multiply with 32 bit result takes 3.5 µsec when operating with 19.6608 MHz crystal or 2µs with a 29.4912 MHz crystal. (Intel 8096 takes 6.5 µsec with a 12 MHz clock.)

A wait state generator has been added for applications that do not require fast ROMS. This adds one clock cycle to each ROM access.

Hardware Echo has been added to assist in high Speed Autobauds.

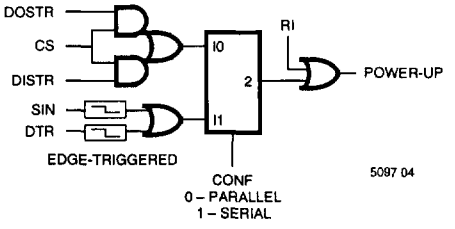


Figure 3. VALID Power-up Inputs

HARDWARE ARCHITECTURE

The MAC II device is organized with two buses that interconnect four main logic sections. The two buses are the internal data bus (DB) and address bus (Y). The four sections of the device are the internal processor, registers, memory, and dual port UART.

The two bus architecture was chosen to allow the MAC II to execute the 8096 instruction set as fast or faster than the 8096 itself. The device is intended to run at 9.8304 MHz or 14.745MHz. (The internal divider provides these clock speeds from an external 19.6608 MHz or 29.4912 MHz crystal.) A typical three operand instruction effectively executes in 10 clock cycles. The signed 16 x 16 multiply operation requires 34 clock cycles.

The internal data bus (DB) is the main bus of the device. It is an 8-bit bus that interconnects all four sections of the device. All internal data travels on DB. The Y bus is a 16-bit output only bus fromthe internal processor that provides addresses to the memory and register sections of the device. This bus allows memory control to be resident inside the internal processor without degrading performance.

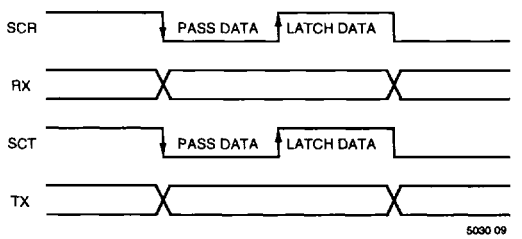
The internal processor controls MAC II operations and performs all of the required computation functions. The internal processor consists of a microcontrol PLA and a 16-bit registered arithmetic/logic unit (RALU). The microcontrol PLA accepts as input 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU performs instruction exe-cution, operand address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. The RALU is implemented with the 2901 silicon compiler.

The register section of the MAC II includes RAM and the ports of the device. Code can't be executed from registers; however, it can be executed from external RAM or ROM. The UART registers are functionally, but not physically, part of the register section. The UART registers are accessed via indirect addressing mode only. There are 384 bytes of internal RAM to support DSP functions and the command set. The memory section of the MAC II includes the program ROM and the external memory interface. The device contains 16K bytes (except 11031) of program ROM. The external memory interface allows the MAC II to access program storage or data storage from external memory.

The UART section of the device implements, in hardware, the industry standard 16C450 UART. In its parallel version the MAC II appears as a 16C450 to the user. The UART contains true dual-port capability to allow the user and the internal processor access to its internal registers.

Datapath & Description

Figure 5a shows the data path portion of MAC II. The function of the I/O pins affected by the MAC II is described. The rest of the I/O functions remains the same as SC11021. See GIO register information.



(a) Signal Interface with MAP, (Synchronous mode)

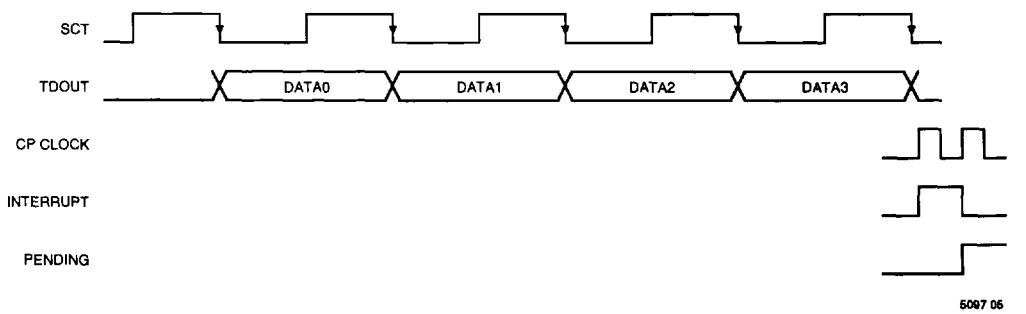


Figure 4. TX Timing Diagram

Hardware Description of the STBR

The serial transmit bit word consists of a 4-bit shift register which is clocked by SCT. Data 0 is shifted out first, and Data 3 is the last bit shifted out. An interrupt is generated on the last shift if the enable bit is set. The pending bit remains high until it is cleared by reading the STBR register. Data 3 remains on the TX output until the next 4-bit data is loaded.

Clock Generation and Powerdown

The MAC II runs on either a 19.6608 MHz or 29.4912 MHz crystal. This frequency is divided by two and the 9.8304 MHz is used for internal hardware timing and for the CKOUT clock. When the MAC II is operated at 29.4912MHz (1.5X) the internal CPU clock remains at half the crystal oscillator speed. However, the UART baud rate, the timers and the CKOUT to the MAP are kept at the normal speed to maintain compatibility. This is done by setting GCR1.B0 to a 1.

CKOUT—is maintained at 9.8304 MHz. When the MAC II is running at 19.6608 MHz and GCR1.B0 is set to a zero, a divide by 2 circuit will enable CKOUT to maintain 9.8304 MHz. When it is running at 29.4912 MHz and GCR1.B1 is set to a one, a divide by 3 circuit will enable CKOUT to maintain 9.8304 MHz. The CKOUT is phase synchronized with the internal CPU clock when the divide by 2 is selected.

UART—Maintains the same base clock into the baud rate generator.

Power down mode is activated in the same manner as in BigMAC when bit 7 of the PSB byte is set high and inputs RI, CS, DTR and SIN are all high. In this mode, the internal CPU clock is turned off. The MAC II comes out of power down mode when any of the inputs are set low.

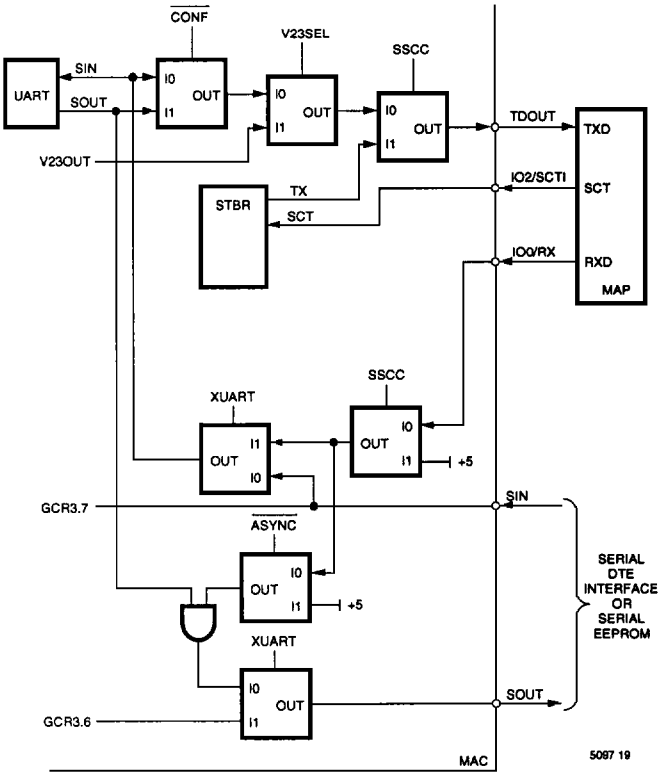


Figure 5a. MAC II Internal Data Path

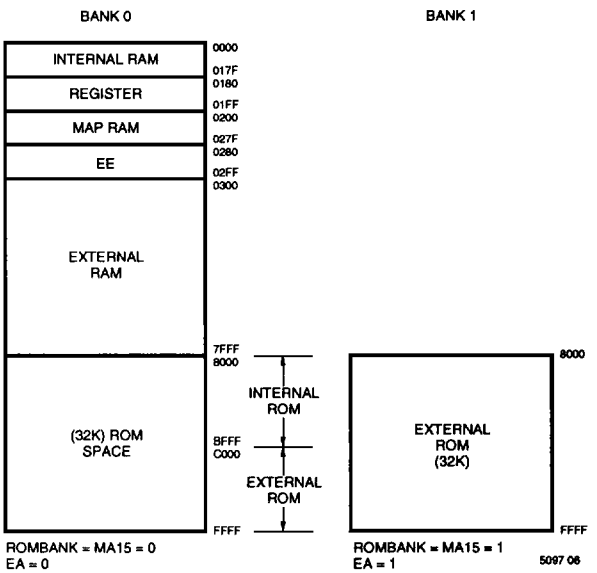


Figure 5b. MAC II Address Map

RDY Interface

The RDY pin is used to inject wait states to synchronize the MAC II with the PC's parallel access. Some Laptops do not incorporate this wait mechanism. MAC II will still be able to interface to these laptops without having to use the RDY pin.

MEMORY DESCRIPTION

Internal ROM:

The MAC II controller is built with the same basic architecture as the SC11019/20/21/22/23 so that firmware will be upward compatible.

External Read/Write:

Three different types of external memory operations are defined.

A) For address from 0200H to 02FFH:

These external operations occur through the AD bus. These operations take six clock cycles, four more than internal operations. These are mainly for MAP & EEROM interfaces, however, instructions and data can also be fetched from these memory spaces.

B) For address from 0300H to 7FFFH:

These memory spaces are reserved for external DATA storage. The MAC II can access external RAM through MA address bus and AD data bus. There are three clock cycles for each access.

C) For address from 8000H to FFFFH:

The chip fetches instructions from external program storage by MA_0–MA_{14} and AD_0–AD_7. These operations are exactly the same as internal ROM fetch and they take three clock cycles.

Extended ROM bank switching and addressing

With increased code needed to service MNP and V.42bis classes of communication, the usual 32K ROM may not be sufficient to hold all the code. However, one extra gate is needed to select the MAP when the 64k mode is used. The extended ROM is one 64Kx8 ROM (27512).

The external ROM access starts at Bank 1 as the ECS pin is high by default. To select extended ROM mode, set GCR1:B4 and GTCR1:B6. The rombank configuration bit, GCR1.B4, must be set to reconfigure ECS as MA15 and MCS as PCS. The Rombank bit, GCR1.B6, must be set to bank 1, the same as the ECS default. Switching between bank 1 and bank 0 is done by setting or resetting GCR1.B6. More than 64K can be accessed by using an additional I/O pin, such as IO3, as MA16.

RD Indication During External ROM Access

The SC11011, 21 & 61 do not provide an indication when the ROM contents are read into the CPU. In the MAC II, the RD pin goes low for 2 clock cycle when the ROM contents are being read into the MAC II CPU. The RD function is the same for extended ROM operation.

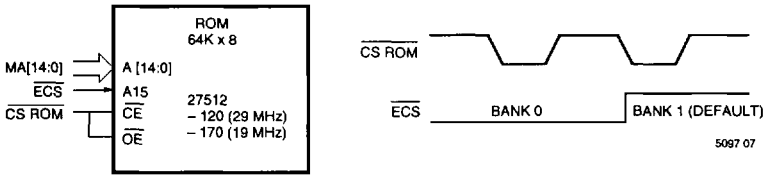


Figure 6a. OE Could be Grounded, But Above Connection Saves Power in PD Mode.

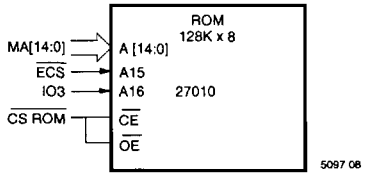


Figure 6b. 128K ROM Connections

Figure 6. Interface Block Diagrams for Optional Modes

Code at line 1 must start at the same address in both banks. And code alignment must be maintained in the bank switching routines.

Here GCR1.6 and DAR.3 are used as A15 and A16, respectively (see Figure 6b). Thus by changing their values in a similar way, it is possible to switch from any bank to any other bank.

LJMP across banks is accomplished by simply changing the bank bit in either GCR1 or DAR, such as line 1 to line 4 in Table 4a. Code execution from the other bank begins immediately after the STB instruction.

When an interrupt happens, the program pointer always points to 8004H of the current bank it is in. There is two ways to handle interrupts. One is to copy the same interrupt handling routine to all banks. The second way is to use bank switching routines to switch to bank 0 to handle the interrupt, and then return to the original bank. To save code space, the second way is recommended. The implementation is similar to Table 4a, except that a PUSHF has to precede line 1 to disable interrupts, and a POPF has to be put between line 9 and 10 to re-enable interrupts.

Bank 0

```
BANK_0_ROUTINE:

 1 LD    AX,  #GCR1
 2 LDB   BL,  [AX]
 3 ORB   BL,  #01000000B   ;select bank 1
 4 STB   BL,  [AX]
 5 LCALL BANK_0_ROUTINE    ;alignment
 6 LD    AX,  #GCR1        ;alignment
 7 LDB   BL,  [AX]         ;alignment
 8 AND   BL,  #10111111B   ;alignment
 9 STB   BL,  [AX]         ;alignment
10 RET                     ;return to caller

.
.  LCALL BANK_0_ROUTINE:   ;caller calls bank switching
                           ;routine in bank 0
```

Bank 1

```
 1 LD    AX,  #GCR1        ;alignment
 2 LDB   BL,  [AX]         ;alignment
 3 ORB   BL,  #01000000B   ;alignment
 4 STB   BL,  [AX]         ;alignment
 5 LCALL BANK_1_ROUTINE    ;call actual routine
 6 LD    AX,  #GCR1
 7 LDB   BL,  [AX]
 8 AND   BL,  #10111111B   ;select bank 0
 9 STB   BL,  [AX]
10 RET                     ;alignment

.
.  BANK_1_ROUTINE:         ;actual routine
.  .....
.  RET                     ;return to bank switching
                           ;routine in bank 1
```

Table 4a. LCALL Across Bank

Bank 0

```
.
. LD AX, #0192H
. LDB BL, [AX]
. ANDB BL, #11101111B ;disable interrupts
. ORB BL, #01000000B  ;set bank bit
. STB BL, [AX]
LJMP XX
```

Bank 1

```
.
.
.
XX:
.
. program execution continues from XX.
.
.
```

Table 4b. LJMP Across Bank

FIRMWARE ARCHITECTURE

The MAC II uses a subset of 8096 instructions and can be compiled with an 8096 cross assembler such as AD2500. Rev 4.0x of this assembler is strongly recommended.

Operand Types

1. Short Integers: Short integers are 8-bit signed 2's complement variables. Results outside the range –128 and +127 will set the overflow bit in the Program Status Byte (PSB). There are no alignment restrictions on short integers.
2. Integers: Integers are 16-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –32768 and +32767 will set the overflow bit in the PSB. The least significant byte of the integers is in the even byte address and the next most significant byte is in the next higher (odd) address. Therefore, the integers must be aligned at even byte boundaries in the address space. The address of a word is the address of its least significant byte (always an even address).
3. Bits: The bits within the bytes of the register file are numbered from 0 to 7 with 0 referring to the LSB. The only instructions that use bit addressing are JBC and JBS.
4. Long Integers: Long integers are 32-bit signed 2's complement variables. The result of a 16 x 16-bit multiply will be stored in a long integer. Only SHRL and SHLL manipulate this data type. Long integers are addressed by the address of their least significant byte in the register file. They must be aligned such that their address is evenly divisible by 4. The most significant byte of a long integer resides on "address" +3, where "address" is the long integer's address.

Operand Addressing

Three types of addressing are allowed:

1. Immediate Addressing: This is a direct field within the instruction. For short integers, this is an 8-bit field, whereas, for the integers this is a 16-bit field. Only one operand within an instruction can be an immediate reference type. This operand must always be the last (right most) operand within an instruction.
   e.g. ADD AX, #340H is allowed
   ADD AX, #340H, BX is NOT allowed
   ADD AX, BX, #340H is allowed
2. Register Direct Addressing: In this mode an 8-bit field is used to access a register from the 384 byte register file. The register address must conform to the alignment rules. Registers 256-383 can use direct addressing only if the page bit, GCR bit 1, is set.
   e.g. ADD AX, BX :AX, BX must be "even" numbers
   ADDB AX, BX :AX, BX can be "odd" or "even"
3. Indirect Addressing: A memory location can be addressed indirectly by placing its 16-bit address in the register file. Only one operand (the right most operand) within an instruction can be indirect.
   e.g. ADDB AL, BL, [CX] is allowed
   ADDB AL, [CX], BL is NOT allowed
4. Indexed addressing is NOT allowed.

Interrupt Structure

Five interrupt sources exist in the MAC II, namely the external interrupt, timer interrupt, ring leading edge interrupt, STBR transmit and UART interrupt. The interupt service routine address is 8004H.

1. External interrupt: A low to high transition on the INTI pin initiates this interrupt.
2. Timer interrupt: Timer overflow interrupt—frequency set by GCR bits 0.
3. Ring leading edge: Interrupt generated by leading edge of ring input.
4. UART interrupt: Interrupt from UART.
   a. Parallel version: From UMR register. Any one of the following can generate this interrupt:
      - RBR was read by external processor
      - Data was transferred from THR to TSR
      - LCR was changed
      - MCR was changed
      - SHDLL or SHDLM was changed

   b. Serial version: In this configuration the interrupt signal, IIR from the 16C450 compatible UART is brought in as an interrupt source to the internal CPU.
5. TX Interrupt. Interrupt initiated when 4-bit data has finished shifting.

INSTRUCTION SET

The MAC II instruction set is a subset of Intel 8096 instruction set. The object codes, formats and the flags they effect are identical to those of 8096. The differences are:

- No VT or ST flags exist in the MAC II.
- Register locations in the UART section can only be accessed by using indirect addressing.
- The operands refer to one or more bytes of the register file. ROM locations can only be addressed using indirect addressing.
- If a memory location is addressed between 200H and 2FFH, an external six clock multiplexed bus operation is initiated. The multiplexed address/data will use AD_7–AD_0 bus.
- When using ST or STB operations, the destinations are always considered to be indirect addresses.
  e.g. ST, AX, [BX] is allowed
  ST, AX, BX is NOT allowed

MNEMONIC	NO. OF OPERANDS	OPERATION	BYTES[1]	TIME[2]
ADD/ADDB	2	B ← A + B	3	10
ADD/ADDB	3	D ← A + B	4	10
AND/ANDB	2	B ← A AND B	3	10
AND/ANDB	3	D ← A AND B	4	10
CMP/CMPB	2	D - A	3	10
DJNZ	1	Decrement & JNZ	3	9/12
EXTB	1	Sign Extend Byte	2	7
JBC	0	Jump if bit clear	3	10/13
JBS	0	Jump if bit set	3	10/13
JC	0	Jump if Carry Set	2	5/8
JNC	0	Jump if no carry	2	5/8
JE	0	Jump if =	2	5/8
JNE	0	Jump if not =	2	5/8
JGT	0	Jump if >	2	5/8
JGE	0	Jump if >=	2	5/8
JLE	0	Jump if < or =	2	5/8
JLT	0	Jump if <	2	5/8
JV	0	Jump if Overflow	2	5/8
JNV	0	Jump if no overflow	2	5/8
JH	0	Jump if higher	2	5/8
JNH	0	Jump if not higher	2	5/8
LCALL	0	Long Call	3	11
LD/LDB	2	Load	3	10
MUL	3	D ← A * B	5	33
NOP	0	NO Operation	1	2
OR/ORB	2	D ← D OR A	3	10
XOR/XORB	2	D ← D XOR A	3	10
PUSHF	0	Push PSB	1	5
POPF	0	Pop PSB	1	5
RET	0	Return	1	10
SHL/SHLB	1	Shift Left	3	11 + N[3]
SHLL	1	Shift Left Long	3	15 + N[3]
SHR/SHRB	1	Shift Right	3	11 + N[3]
SHRL	1	Shift Right Long	3	15 + N[3]
SHRA	1	Arith. Right Shift	3	10 + N[3]
SHRAL	1	Arith. Right Long	3	15 + N[3]
SJMP	0	Short Jump	2	7
LJMP	0	Long Jump	3	9
ST/STB	2	Store to Memory	3	13[4]
SUB/SUBB	2	B ← B - A	3	10
SUB/SUBB	3	D ← B - A	4	10

NOTE 1: Add one for immediate words.

NOTE 2: Add 9 for indirect mode and 2 or 0 for immediate mode—see table. (Cycle times @ 1.02 ns) for 19.6608 MHz crystal or 68 ns for 29.4916 MHz crystal)

NOTE 3: N is number of bit shifts.

NOTE 4: Indirect Mode.

Table 4. Instruction Set

REGISTER DESCRIPTION

This section contains a description of each of the registers in the MAC II device. All of the registers of the device are 8-bits with 16-bit addresses. The registers are made up of bits that are either inputs or outputs. Input bits are read-only (RO). Output bits are read/write (R/W). The state of an output may be read back by the processor.

Serial Mode

In parallel mode (CONF = 0) the functions of the UART registers are exactly the same as those in 16C450 UART. However in serial mode, (CONF = 1), the UART is turned around and controlled by the internal processor and it becomes a data set UART. The DTR, RTS, and OUT1 in MCR register becomes DSR, CTS, and RLSD outputs. The CTS, DSR in MSR register become RTS, DTR input status from RTS, DTR pins.

Note:
In serial version to echo SIN to SOUT after RESET and then go back to normal operation.

1. Set SB in LCR to "1".
2. Sample RDI in UART monitor register.
3. Set CM = RDI in the same register.
4. SOUT will be the same state as CM.
5. Receiver is functioning, ignoring it.
6. After finishing all echoing, reset SB in LCR.
7. Update DLL, DLM, and set CM = 1 for normal operation.
8. Do a SET then RESET to RTRST bit to RESET RCV and TMR. Do a READ to LSR to clear LSR.
9. The UART is ready for normal operation.

Echo can be hardware selected by setting GCR1 bit 2. If selected omit step 3.

ADDRESS	FUNCTION	R/W	BYTES	COMMENTS
0000H-017FH	Internal RAM *	R/W	384	(a)
0180H-019AH	Internal REG*	R/W	24	(b)
0200H-027FH	External MAP	R/W	128	(c)
0280H-02FFH	External EEPROM	R/W	128	(c)
0300H-7FFFH	External RAM	R/W	31.25K	(d)
8000H-FFFFH	External ROM	RO	32K	(e)

* 0000H – 00FFH may be accessed using direct addressing mode. 0100 – 01A9H may only be accessed as memory locations (16-bit address) in an indirect mode. For direct addressing a 9th bit (GCR [1], called Page Bit) must be set to switch from the first 256 bytes to the rest of the RAM.

(a) The SC11011,61 have 304 bytes and SC11021 has 320 bytes

(b) The internal register is compatible with the SC11011 and SC11021.

(c) In the normal mode of operation, the MCS and ECS chip select for MAP and EERAM remain the same as in MAC or Big MAC. A provision is made to extend the ROM capacity by another 32K bytes. If selected, the ECS pin becomes a chip select to address another 32K ROM bank from 8000H to FFFFH. MCS pin and an external memory decoder with MA7 must be used to select either the MAP or the EEPROM.

(d) The external RAM address has a maximum addressable space of 31.25K.

(e) The 32K bytes ROM address remains the same as in SC11011 and SC11021. With the ECS pin, the ROM address is expanded to a total of 64K bytes.

(f) SC11011, 1102X, 11061 stack is reset to 302 on power up. MAC II stack is reset to 320.

Location	Name	PC address	7	6	5	4	3	2	1	0
180H	RBR	0 (DLAB=0)	DATA.7	DATA.6	DATA.5	DATA.4	DATA.3	DATA.2	DATA.1	DATA.0
18AH	THR	0 (DLAB=0)	DATA.7	DATA.6	DATA.5	DATA.4	DATA.3	DATA.2	DATA.1	DATA.0
181H	IER	1 (DLAB=0)	0	0	0	0	EDSSI	ELSI	ETBEI	ERBFI
182H	IIR	2	0	0	0	0	0	ID.1	ID.0	PENDING
183H	LCR	3	DLAB	SET BRK	PARITY	EPS	PEN	STB	WLS1	WLS0
184H	MCR	4	0	0	0	LOOP	OUT2	OUT1	RTS	DTR
185H	LSR	5	0	TEMT	THRE	BI	FE	PE	OE	DR
186H	MSR	6	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
187H	STR	7	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
188H	DLL	—	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
189H	DLM	—	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
18BH	UMR	—	RTRST	CM	RDI	DLF	LCF	TXF	RXF	MCF
1A8H	SHDLL	0 (DLAB=1)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1A9H	SHDLM	1 (DLAB=1)	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8

Table 2a. SC11031 UART Registers

Location	Name	7	6	5	4	3	2	1	0
18CH	STBR	DATA.3	DATA.2	DATA.1	DATA.0	ASYNC	SSCC	ENABLE	PENDING
18DH	SWP	—	S6	S5	S4	S3	2S	S1	S0
18EH	DIR	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
18FH	DAR	DAR7	DAR6	DAR5	DAR4	DAR3	DAR2	DAR1	DAR0
190H	GCR	CONF	OH	KDV	MRDY	AA	HS	PAGE	TIMER
191H	TIM	RAM 32K	—	—	—	—	—	—	TFF0
192H	PSB	PD	—	IP	IE	Z	N	C	V
193H	ICR	EXT ENABLE	TIMER ENABLE	RING ENABLE	UART ENABLE	EXT INT	TIMER INT	RING INT	UART INT
194H	GCR1	TEST	ROMBANK	EA	ROMBANK CONF	XUART	HW ECHO	FAST ROM	FREQ SEL
195H	GCR2	RI	CKOUT	RC CAL	RC SEL	RC	DIV.2	DIV.1	DIV.0
196H	GCR3	SIN	SOUT	V.23 OUT	V.23 SEL	—	—	—	—

Table 2b. SC11031 Internal Registers

Location	Name	PC address	7	6	5	4	3	2	1	0
180H	RBR	0 (DLAB=0)	DATA.7	DATA.6	DATA.5	DATA.4	DATA.3	DATA.2	DATA.1	DATA.0
18AH	THR	0 (DLAB=0)	DATA.7	DATA.6	DATA.5	DATA.4	DATA.3	DATA.2	DATA.1	DATA.0
181H	IER	1 (DLAB=0)	0	0	0	0	EDSSI	ELSI	ETBEI	ERBFI
182H	IIR	2	0	0	0	0	0	ID.1	ID.0	PENDING
183H	LCR	3	DLAB	SET BRK	PARITY	EPS	PEN	STB	WLS1	WLS0
184H	MCR	4	0	0	0	LOOP	OUT2	OUT1	RTS	DTR
185H	LSR	5	0	TEMT	THRE	BI	FE	PE	OE	DR
186H	MSR	6	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
187H	STR	7	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
188H	DLL	0 (DLAB=1)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
189H	DLM	1 (DLAB=1)	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
18BH	UMR	—	RTRST	CM	RDI	DLF	LCF	TXF	RXF	MCF

Table 3a. SC11040 UART Registers

Location	Name	7	6	5	4	3	2	1	0
18CH	STBR	DATA.3	DATA.2	DATA.1	DATA.0	ASYNC	SSCC	ENABLE	PENDING
18DH	SWP	—	S6	S5	S4	S3	S2	S1	S0
18EH	DIR	—	—	RC CAL	RC SEL	DIR3	DIR2	DIR1	DIR0
18FH	DAR	SIN	SOUT	V23 OUT	V23 SEL	DAR3	DAR2	DAR1	DAR0
190H	GCR	CONF	OH	KDV	MRDY	AA	HS	PAGE	TIMER
191H	TIM	RAM 32K	—	—	—	—	—	—	TFF0
192H	PSB	PD	—	IP	IE	Z	N	C	V
193H	ICR	EXT ENABLE	TIMER ENABLE	RING ENABLE	UART ENABLE	EXT INT	TIMER INT	RING INT	UART INT
194H	GCR1	TEST	ROMBANK	EA	ROMBANK CONF	XUART	HW ECHO	FAST ROM	FREQ SEL

Table 3b. SC11040 Internal Registers

UART REGISTERS

UART Interrupt Enable Register (IER), location 181H

The 8-bit register enables the four types of interrupts of the UART to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 9 and are described below. IER and IIR should be used as Read Only in Parallel Configuration.

Bit Number	Bit Name	Description
4–7		These four bits are always logic 0.
3	EDSSI	This bit enables the MODEM Status Interrupt when set to logic 1.
2	ELSI	This bit enables the Receiver Line Status Interrupt when set to logic 1.
1	ETBEI	This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.
0	ERBFI	This bit enables the Received Data Available Interrupt when set to logic 1.

Interrupt Identification Register (IIR, location 182H)

The UART has on-chip interrupt capability that allows for flexibility in interfacing popular micro-processors presently available. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts change the IIR, even though they are recorded, until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 9 and are described on the next page.

Bit Number	Bit Name	Description
3–7		These five bits of the IIR are always logic 0.
1–2	ID0–ID1	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 9.
0	PENDING	This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Line Control Register (LCR), location 183H

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 6 and are described in the following table.

Bit Number	Bit Name	Description
7	DLAB	This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

UART REGISTERS (continued)

6	SET BRK	This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. **Note:** This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break. 1. You must wait for TEMT. 2. Set SETBRK bit. 3. Wait for predetermined time and then clear SETBRK bit. During the break, the Transmitter can be used as a character timer to accurately establish the break duration.
5	PARITY	This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0, then the Parity bit is transmitted as a 1.
4	EPS	This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.
3	PEN	This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)
2	STB	This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, two Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the programmed number of Stop-bits selected.
0 and 1	WLS0, WLS1	These two bits specify the number of bits in each trans-mitted or received serial character. The encoding of bits 0 and 1 is as follows: **Bit 1** / **Bit 0** / **Word Length** 0 / 0 / 5 Bits 0 / 1 / 6 Bits 1 / 0 / 7 Bits 1 / 1 / 8 Bits

Modem Control Register (MCR), location 184H

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 6 and are described below.

Bit Number	Bit Name	Description
5–7		These bits are permanently set to logic 0.

UART REGISTERS (continued)

4	LOOP	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input: the four MODEM Status Register bits CTS, DSR, DCD and RI are disconnected internally; and the four MODEM Control Register bits DTR, RTS, OUT1 and OUT2 are internally connected to the four MODEM Status Register inputs, and the MODEM Control output pins RLSD, CTS, DSR are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
3	OUT2	Auxiliary user-designated bit. It is connect to MSR[7] (DCD) during local loopback. When Out2 = 0, INTO pin is Hi-Z.
2	OUT1	Auxiliary user-designated bit. It is connected to MSR[6] (RI) during local loopback.
1	RTS	This bit controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.
0	DTR	This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

Line Status Register (LSR), location 185H

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 5 and are described below.

Bit Number	Bit Name	Description
7		This bit is permanently set to logic 0. **Note:** The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.
6	TEMT	This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.
5	THRE	The bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the THR is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.
4	BI	This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word trans-mission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator. **Note:** Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.
3	FE	This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

UART REGISTERS (continued)

2	PE	This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.
1	OE	This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.
0	DR	This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Modem Status Register (MSR), location 186H

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU in addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 1 and are described below.

Bit Number	Bit Name	Description
7	DCD	This bit is the complement of the Data Carrier Detect (DCD) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR. Read/Write in parallel mode.
6	RL	On the SC11031 this bit is the Ring Latch. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR. RI has moved to GCR2:B7. The firmware must read the contents of the RI and write it to this bit.
	RI	Except the SC11031, this bit is RIng Idicator.
5	DSR	This bit is the complement of the Data Set Ready (DSR) input. If bit 4 of the MCR is set to a 1, this bit is equivalent of DTR in the MCR.
4	CTS	This bit is the complement of the Clear to Send (CTS) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
3	DDCD	This is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the DCD input to the chip has changed state. Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.
2	TERI	This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the chip has changed from a low to a high state. The firmware must detect the trailing edge and update this bit.
1	DDSR	This bit is the Delta Data Set Read (DDSR) indicator. Bit 1 indicates that the DSR input to the chip has changed state since the last time it was read by the CPU.
0	DCTS	This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the chip has changed state since the last time it was read by the CPU.

Scratchpad Register (STR), location 187H

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

UART REGISTERS (continued)

UART Monitor (UMR), location 18BH

The UART Monitor register allows the processor to monitor UART operations. A read operation to the UART Monitor register will clear Bit 0 to Bit 4. UMR should be used instead of IIR in parallel configurations.

Bit Number	Bit Name	Description
7	RTRST	Reset receiver and transmitter. When set high both receiver and transmitter will be put into reset state.
6	CM	UART Command/Modem Output. When set HIGH the UART is placed in modem mode. At reset it is low, in command mode. This bit together with SB in LCR are used for bit by bit echoing. In serial version the user can set BI = 1 and CM = $\overline{RDI}$ to echo a bit. When CONF = 1 for normal operation set SB = 1.
5	RDI	Receive Data Input. This bit monitors the RXD input of the UART.
4	DLF	Divisor Latch Flag. This bit indicates if a new baud rate count has been written to the Divisor Latch.
3	LCF	Line Control Flag. This bit indicates if the line control register has been written.
2	TXF	Transmit Buffer Full Flag. This bit indicates if a new character is in the transmit shadow register.
1	RXF	Receive Buffer Empty Flag. This bit indicates if the last character has been read from the receive buffer.
0	MCF	Modem Control Flag. This bit indicates if the modem control register MCR has been written.

INTERNAL REGISTERS

SERIAL TRANSMIT BIT (STBR), location 18CH

This register controls the serial transmit bit circuitry.

Bit Number	Bit Name	Description
7	DATA.3	
6	DATA.2	
5	DATA.1	
4	DATA.0	4-bit data is shifted out through TDOUT on the falling clock edge of SCT.
3	ASYNC	This bit going high turns on asynchronous mode.
2	SSCC	This bit going high turns on serial synchronous transmit circuitry.
1	ENABLE	Interrupt enable. A "1" enables the STBR interrupt. A"0" disables the STBR interrupt.
0	PENDING	Interrupt pending. Set when 4-bit data has finished shifting.

Switch Port (SWP), location 18DH - for serial version only

The Switch Port is a 7-bit input port used only in the serial version of the MAC. It allows for reading of the external switches of a stand-alone modem.

Bit Number	Bit Name	Description
6-0	S6-0	Switch Input. These bits monitor external switches.

DIR, location 18EH

DIR controls the input/output direction of the IO port.

Bit Number	Bit Name	Description
7	DIR7	When HIGH, IO_7 is an output. When LOW, IO_7 is an input.
6	DIR6	When HIGH, IO_6 is an output. When LOW, IO_6 is an input.
5	DIR5	When HIGH, IO_5 is an output. When LOW, IO_5 is an input.
4	DIR4	When HIGH, IO_4 is an output. When LOW, IO_4 is an input.
3	DIR3	When HIGH, IO_3 is an output. When LOW, IO_3 is an input.
2	DIR2	When HIGH, IO_2 is an output. When LOW, IO_2 is an input.
1	DIR1	When HIGH, IO_1 is an output. When LOW, IO_1 is an input.
0	DIR0	When HIGH, IO_0 is an output. When LOW, IO_0 is an input.

DAR, location 18FH

DAR is the data register for the IO port.

Bit Number	Bit Name	Description
7	DAR7	Output to IO_7.
6	DAR6	Output to IO_6.
5	DAR5	Output to IO_5.
4	DAR4	Output to IO_4.
3	DAR3	Output to IO_3.
2	DAR2	Output to IO_2.
1	DAR1	Output to IO_1.
0	DAR0	Output to IO_0.

INTERNAL REGISTERS (continued)

General Control Register (GCR), location 190H

GCR contains a miscellaneous set of control and status bits.

Bit Number	Bit Name	Description
7	CONF	Configuration output. This bit controls the state of the MAC configuration. When HIGH, the MAC is configured with the SERIAL interface. It is configured with the PARALLEL interface after a reset.
6	OH	Off Hook Output. When set HIGH, the phone will be placed off hook.
5	KDV	KDV Output. Data/Voice Relay Control. When high, the modem is in the voice mode.
4	MRDY	Modem ready.
3	AA	Active HIGH AA indicator. When high this bit sets the $\overline{AA}$ pin low.
2	HS	Active HIGH HS indicator. When high this bit sets the $\overline{HS}$ pin low.
1	PAGE	Register Page Bit. This bit selects the active register page. When LOW, the lower 256 registers are accessed during register operations and when HIGH, the upper page is active.
0	TIMER	Set timer rate (TIM, location 191H) 0 = 4.8 KHz; 1 = 19.2 KHz

Timer (TIM), location 191H

The Timer includes an 11 bit counter and a timer flip-flop. It is used to aid software timing functions. The counter is not readable. It can only be reset by a write. The timer flip-flop can be read to test if it is already set.

The counter and flip-flop will be reset on a write (value is don't care).

Bit 0 is set according to the selected rate (4.8KHz, 19.2KHz). The flip-flop can be cleared on a read. The Timer is constantly counting by the internal clock (9.8304 MHz).

Bit Number	Bit Name	Description
7	7	Read status of RAM 32K 0 = 16K; 1 = 31.25K
0	TFF0	Timer flip-flop bit.

Program Status Byte (PSB), location 192H

This is an 8-bit register storing the condition flags of arithmetic, shift, and compare instructions. The programmer can access these bits by using address 0192H. Only bits 4, 6 and 7 are writeable by software.

Bit Number	Bit Name	Description
7	PD	Power-Down enable bit. Set HIGH to power down. Hardware reset on RI, DTR on in serial mode or RI, CS true anded with read or write in parallel mode. If RC mode is selected, this bit will also shut down the xtal oscillator.
5	IP	Global interrupt pending bit. Set upon receipt of interrupt. Cleared when interrupt service begins. (Read only.)
4	IE	Global interrupt enable bit; when zero, all interrupts are disabled.
3	Z	Zero bit; indicates the last arithmetic or compare instruction produced a zero result.
2	N	Negative bit; indicates the last arithmetic or compare instruction produced a negative result.
1	C	Carry bit; indicates the state of the arithmetic carry from the most significant bit of the ALU for an arithmetic operation or the state of the last bit shifted out of the operand for a shift. Arithmetic "Borrow" after a subtract is the complement of the C flag (i.e. if borrow generated then C = 0).
0	V	Overflow bit; indicates the last arithmetic operation produced an overflow.

INTERNAL REGISTERS (continued)

Interrupt Control Register (ICR), location 193H

This is an 8 bit register to enable or disable four of the five interrupt sources and to record the interrupt sources. The upper four bits are read/write registers while the lower four bits are read only registers. A read operation to the register will automatically clear the lower four bits. Any one of the four interrupts will drive the processor to address 8004H. From there the software can check interrupt sources and do priority control to branch to different service routines.

Bit Number	Bit Name	Description
7	UART Int	"1" to enable EXTERNAL interrupt.
6	Ring Int	"1" to enable TIMER overflow interrupt.
5	Timer Int	"1" to enable RING leading edge interrupt.
4	Ext Int	"1" to enable UART interrupt.
3	UART Enable	"1" indicates EXTERNAL source requested an interrupt.
2	Ring Enable	"1" indicates TIMER overflow requested an interrupt.
1	Timer Enable	"1" indicates RING leading edge requested an interrupt.
0	Ext Enable	"1" indicates UART requested an interrupt.

General Control Register 1 (GCR1), location 194H

GCR1 contains a miscellaneous set of control bits. All bits are default low at reset.

Bit Number	Bit Name	Description
7	TEST	A test mode used for factory testing.
6	ROMBANK	This bit selects which ROM bank is to be accessed in extended ROM mode. A "0" selects Bank 0. A "1" selects Bank 1. Bank 0 is address decoded as MA15=0, and Bank 1 is address decoded as MA15=1.
5	EA	External ROM access. This bit determines whether memory addresses 8000H to BFFFH access either internal or external ROM. A "0" selects the 16K internal ROM. A "1" selects the external ROM. This function is disabled on the 11031 since there is no internal ROM.
4	ROMBANK CONF	ROMbank configuration. This bit determines the pin configuration of the MCS and the ECS pin for either normal MAP & EEPROM operation or extended ROM operation. A "0" selects pin 24 as MCS & pin 36 as ECS. A "1" selects pin 24 as PCS & pin 36 as MA15. PCS is the combination of MCS and ECS.
3	XUART	When high, the UART is disconnected from the SIN and SOUT pin. SIN and SOUT can then be accessed through GCR3 bits 7 and 6 respectively.
2	HWECHO	SIN is internally connected to SOUT, allowing hardware echo.
1	FASTROM	This bit determines the configuration of the rom access interface. a "0" selects the slow rom access with wait state. A "1" selects the fast rom access without wait state.
0	FREQ SEL	19 MHz/29MHz frequency select. This bit maintains CKOUT at 9.8304 MHz and the base clock of the baud rate generator at 1.8432 MHz, provided the correct crystal frequency is chosen. A "0" selects 19.6608 MHz xtal operation. A "1"selects 29.4912 MHz xtal operation.

General Control Register 2 (GCR2), location 195H (SC11031 only)

GCR2 contains all the control bits to manage power consumption. Bits 6-0 are default low at reset.

Bit Number	Bit Name	Description
7	RI	Ring indicator. Read only. This bit is the complement of the Ring Indicator (RI) input.
6	CKOUT	This bit determines the state of the CKOUT clock. A "0" turns CKOUT on. A "1" turns CKOUT off.

INTERNAL REGISTERS (continued)

5	RC CAL	RC calibrate. This bit going high turns on the RC calibration circuitry to determine the RC frequency. The RC oscillator clocks only the hardware timer, while the rest of the chip is running from the crystal oscillator. A firmware timer is compared against the hardware timer to deduce the RC frequency.
4	RC SEL	This bit selects the source for the clock circuitry. A "0" selects the external XTAL mode. The crystal oscillator drives the chip. A "1" selects the internal RC mode. The internal RC oscillator drives the chip and the crystal oscillator is turned off.
3	RC	This bit determines the state of the RC oscillator. A "0" turns RC oscillator on. A "1" turns the RC oscillator off.
2-0	DIV.2 DIV.1 DIV.0	Clock divisor. These bits determines the rate at which the system clock slows down. A range of 1 to 6 clock pulses can be chosen where there are normally 6 clock pulses.

Bit 210	Description	Frequency of CP (19/29 MHz)	
000	full speed	9.83 MHz	14.75 MHz
001	1/6 of CP	1.638 MHz	2.458 MHz
010	2/6 of CP	3.277 MHz	4.915 MHz
011	3/6 of CP	4.915 MHz	7.373 MHz
100	4/6 of CP	6.554 MHz	9.83 MHz
101	5/6 of CP	8.192 MHz	12.29 MHz

Note: Firmware must use the same divisor on the values located in the baud rate table, Table 8.

General Control Register (GCR3), location 196H (SC11031 only)

GCR3 contain functions needed for a firmware SSCC.

Bit Number	Bit Name	Description
7	SIN	Read only from SIN pin.
6	SOUT	Write only to SOUT pin.
5	V23 OUT	This bit is routed to TDOUT pin when V23 SEL is high.
4	V23 SEL	When set high, V23 OUT is output to TDOUT pin. when set low, SOUT, SIN or STBR is output to TDOUT pin.

Bit No	Register Address									
	0(DLAB=0)	0(DLAB=0)	(DLAB=0)	2	3	4	5	6	7	(DLAB=1)	(DLAB=1)
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Iden. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	STR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSi)	0	Parity Enable (PEN)	Out 2 INT0 is High-Z when out2=0	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)**	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

** On the SC11031 this bit is Ring Latch. Rin Indicator has moved to GCR2 bit 7.

Table 5. Summary of Accessible UART Registers

Table 6. Register Address MAP

NAME	ABV	INTERNAL[1] DIRECT ADDRESS[2]	INTERNAL[1] INDIRECT ADDRESS[3]	INTERNAL[1] R/W	EXTERNAL[4] ADDRESS A [2:0]	EXTERNAL[4] R/W
UART Registers:						
Receive Buffer	RBR		180H	R/W	00H, DLAB=0	RO
Transmit Holding	THR		18AH	R/W	00H, DLAB=0	WO
Interrupt Enable	IER		181H	R/W	01H, DLAB=0	R/W
Interrupt ID	IIR		182H	RO	02H	RO
Line Control	LCR		183H	R/W	03H	R/W
Modem Control	MCR		184H	R/W	04H	R/W
Line Status	LSR		185H	R/W	05H	R/W
Modem Status	MSR		186H	R/W	06H	R/W[5]
Scratch Pad (8 bit)	STR		187H	R/W	07H	R/W
Divisor Latch LSB	DLL		188H	R/W		
Divisor Latch MSB	DLM		189H	R/W		
UART Monitor	UMR		18BH	R/W		
Shadow Divisor Latch LSB	SHDLL		1A8H	R/W	00H, DLAB=1	R/W
Shadow Divisor Latch MSB	SHDLM		1A9H	R/W	01H, DLAB=1	R/W
Internal Registers:						
4-bit shift	TX	8CH	18CH	R/W		
Switch Port	SWP		18DH	RO		
General I/O Port						
Direction Register	DIR	8EH	18EH	WO		
Data Register	DAR	8FH	18FH	R/W		
General Control	GCR	90H	190H	R/W		
TIMER	TIM	91H	191H	R/W		
Processor Status Byte	PSB	92H	192H	R/W		
Interrupt Control	ICR	93H	193H	R/W		
General Control 1	GCR1	94H	194H	R/W		
General Control 2	GCR2	95H	195H	R/W		
General Control 3	GCR3	96H	196H	R/W		

NOTE 1: Register access through MA bus.
NOTE 2: 8-bit addresses for direct addressing only, or with Page bit (GCR [1]) used.
NOTE 3: 16-bit addresses for indirect addressing only.
NOTE 4: UART register access through PC parallel system bus.
NOTE 5: PC parallel systems bus can only write to MSR bits 3-0

Programmable Baud Generator

The UART contains a programmable Baud Generator that takes an internal clock of (3/32)(XTAL1) for 19.668 MHz (2/32)(XTAL) for 29.4912 MHz = 1.8432 MHz and divides it by any divisor from 1 to (2^{16}–1). The output frequency of the Baud Generator is 16 x the Baud [(divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on the initial load.

The SHDLL and SHDLM are now accessed through the PC interface instead of DLL, DLM. Writing to the SHDLL or SHDLM will set the DLF bit in the UMR register.

The firmware must now read the contents of the SHDLL and SHDLM and transfer the data to DLL and DLM. If the clock divisor function has been selected, the firmware must adjust the values in Table 8 by the same clock divisor value. Example: If 5/6 clock divide is selected and 9600 Baud is desired, the 16 x clock value (column 2) must be reduced by 5/6 as well. 12 times 5/6=10. Writing 10 to the DLL will then select 9600 Baud in 5/6 clock mode.

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3) forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bit 3–7 are permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bits 0–3 Low, Bits 4–7— Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read BRR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read RBR/MR	Low

Table 7. Reset Diagram of UART Registers

Table 8 illustrates the use of the Baud Generator. The values in column 2 must be written into DLL and DLM as a 16 bit number to select the desired Baud Rate at SIN and SOUT.

Desired Baud Rate	Divisor* Used to Generate 16 x Clock	Error Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.4	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
57600	2	—

Table 8. Baud Rate Generator Divisors

*Note: When using the clock divisor mode, these values must be reduced by the divisor value. ex: DLL for 9600=12 for 5/6 mode DLL=5/6 x 12=10

IIR

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Table 9. Interrupt Identification Register

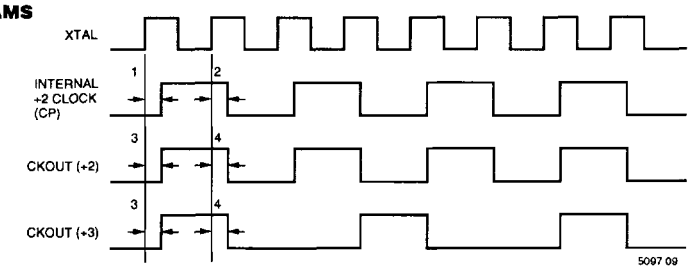
ABSOLUTE MAXIMUM RATINGS:

V_{CC} Supply Voltage	+6 V
Input Voltage	–0.6 V to V_{CC} +0.6 V
Storage Temperature Range	–65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS: (T_A = 0 to 70°C, V_{CC} = +5 V ±10%)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC29}	Nominal Operating Current @ V_{CC} = 5.0 V, F_{CLK} = 29 MHz		36	60	mA
I_{CCPD29}	Power Down Current @ V_{CC} = 5.0 V, F_{CLK} = 29 MHz		13	15	mA
I_{CC19}	Nominal Operating Current @ V_{CC} = 5.0 V, F_{CLK} = 19 MHz		26	40	mA
I_{CCPD19}	Power Down Current @ V_{CC} = 5.0 V, F_{CLK} = 19 MHz		8	15	mA
I_{CCPDRC}	Power Down Current in RC mode @ V_{CC} = 5.0		3	6	mA
V_{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	 2 0.8 V_{CC}			 V V
V_{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			 0.7 0.2 V_{CC}	 V V
VT+	Positive Hysteresis Threshold for RESET & $\overline{RI}$ input pins	2.6	2.8	3.4	V
VT–	Negative Hysteresis Threshold for RESET & $\overline{RI}$ input pins	1.8	2.2	2.5	V
V_{OH}	High Level Output Voltage for D7–D0, INT0 @ I_{OH} = 8 mA for RDY—open collector for other output @ I_{OH} = 2 mA	0.7 V_{CC} +0.5			V
V_{OL}	Low Level Output Voltage for D7–D0, INT0 pins @ I_{OL} = 8 mA for RDY @ I_{OL} = 8 mA for other output pins @ I_{OL} = 2 mA			0.3 V_{CC} –0.5	V
I_I	Leakage Current		±1	±20	µA
F_{CLK}	Crystal Clock Frequency (GCR2:0, 1 - 01)		19.6608		MHz
F_{CLK}	Crystal Clock Frequency (GCR2:0, 1 - 00) (Not SC11031)		29.4912		MHz

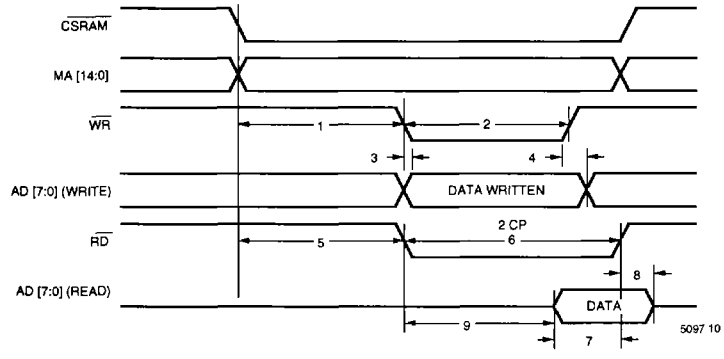
TIMING DIAGRAMS



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{XTCPH}	XTAL high to internal ÷2 clock high			20	ns
2	t_{XTERL}	XTAL high to internal ÷2 clock low			20	ns
3	t_{XTCKH}	XTAL high to CKOUT high			30	ns
4	t_{XTCKL}	XTAL high to CKOUT low			30	ns

NOTE: CP is the internal ÷2 clock. CP = 102 ns for 19.6608 MHz crystal or 68 ns for 29.4912 MHz crystal.

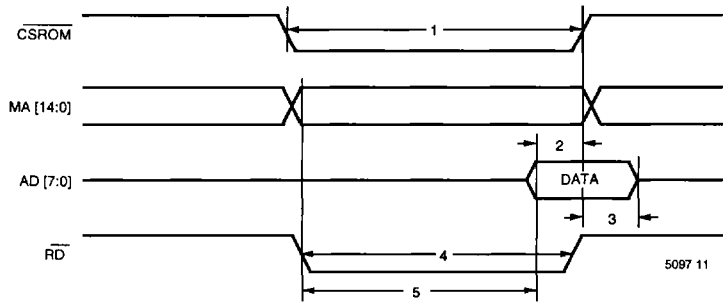
Figure 7. Oscillator, Internal (÷2) Clock and CKOUT Timing



NO.	SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
1	t_{CSRWR}	$\overline{CSRAM}$ low to $\overline{WR}$ low	19.6608 MHz 29.4912 MHz	32 30	0.5		ns
2	t_{RW}	$\overline{WR}$ width	19.6608 MHz 29.4912 MHz			204 136	ns
3	t_{WRADV}	$\overline{WR}$ low to data valid				3.5	ns
4	t_{WRADI}	$\overline{WR}$ high to data invalid			0.5		cp
5	t_{CSRRD}	$\overline{CSRAM}$ low to $\overline{RD}$ low	19.6608 MHz 29.4912 MHz	32 30	0.5		ns
6	t_{RD}	$\overline{RD}$ width	19.6608 MHz 29.4912 MHz			204 136	ns
7	t_{ADVCL}	Read set up time		16			ns
8	t_{CLADI}	Read hold time		0			ns
9	t_{RLDV}	Read low to data valid	19.6608 MHz 29.4912 MHz			188 120	ns

NOTE: CP = 102 ns for 19.6608 MHz XTAL & 68 ns for 29.4912 MHz crystal
Recommended ROM access time: 19.6608 MHz – 220 ns, 29.4912 MHz – 150 ns

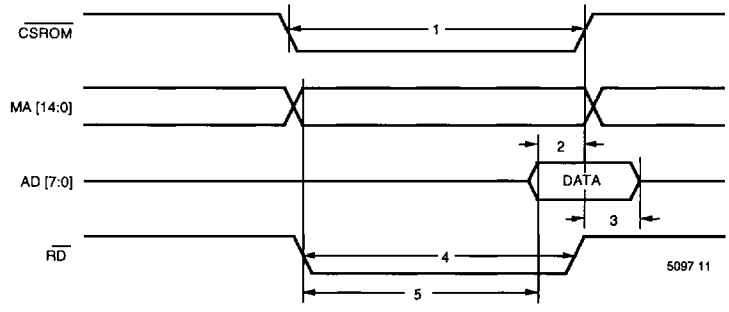
Figure 8. RAM Read or Write Cycle



NO.	SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
1	t_{CSROM}	$\overline{CSROM}$ width	19.6608 MHz 29.4912 MHz			204 136	ns
2	t_{CSRAD}	Read setup time		16			ns
3	t_{CSRDH}	Read hold time		0			ns
4	t_{RD}	$\overline{RD}$ width			2	204 130	ns
5	t_{ADDV}	Address valid to data valid	19.6608 MHz 29.4912 MHz			188 120	ns ns

NOTE: Recommended ROM access time: 19.6608 MHz 170 ns
29.4912 MHz 120 ns

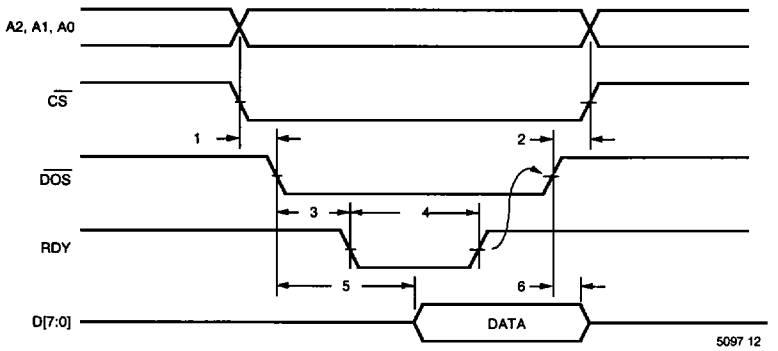
Figure 9a. External Program Storage Read Bus Cycle



NO.	SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
1	t_{CSROM}	$\overline{CSROM}$ width	19.6608 MHz 29.4912 MHz			306 204	ns
2	t_{CSRAD}	Read setup time		16			ns
3	t_{CSRDH}	Read hold time		0			ns
4	t_{RD}	$\overline{RD}$ width			2	306 204	ns
5	t_{ADDV}	Address valid to data valid	19.6608 MHz 29.4912 MHz			188 290	ns ns

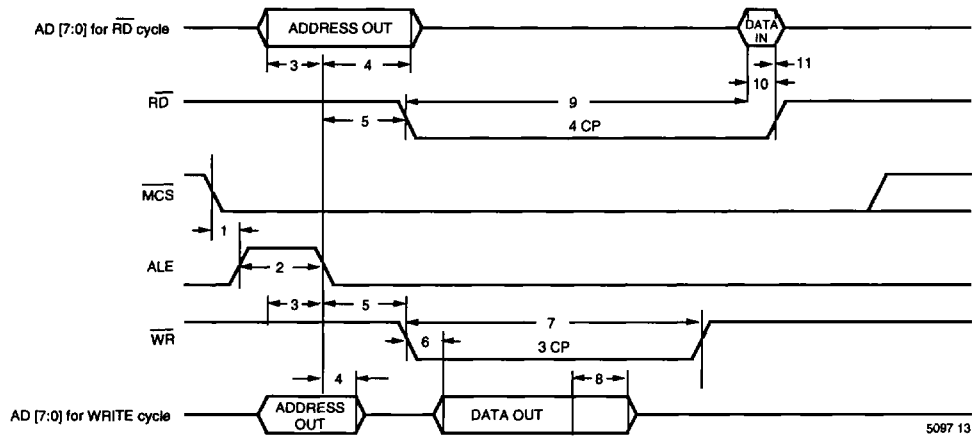
NOTE: Recommended ROM access time: 19.6608 MHz 290 ns
29.4912 MHz 188 ns

Figure 9b. External Program Storage Read Bus Cycle with Wait State



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{CSLDOL}	$\overline{CS}$ low to $\overline{DOS}$ low			0	ns
2	t_{DOHCSH}	$\overline{DOS}$ high to $\overline{CS}$ high			0	ns
3	t_{DOLRDL}	$\overline{DOS}$ low to RDY low			26	ns
4	t_{RDL}	RDY low time (~5–6CP)	5		6	cp
5	t_{DOLDV}	$\overline{DOS}$ low to D valid		2		cp
6	t_{DOHDZ}	$\overline{DOS}$ high to D high-Z	0			ns

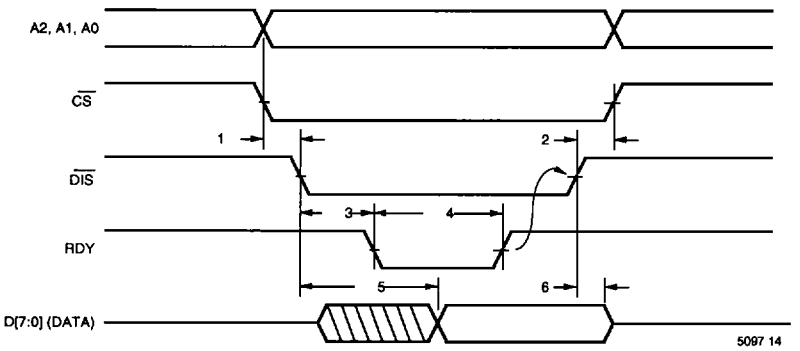
Figure 10. Write Cycle (PC Bus Write Into UART Register)



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{MCAL}	$\overline{MCS}$ low to ALE high		0.5		cp
2	t_{ALE}	ALE pulse width		1		cp
3	t_{AVLE}	Address valid to ALE low		1		cp
4	t_{HAD}	Hold address after ALE low		1		cp
5	t_{ALRD}	Delay from ALE low to $\overline{RD}/\overline{WR}$ low	1		cp	
6	t_{DURL}	Data valid after $\overline{WR}$ low			20	ns
7	t_{WR}	Write pulse width		3		cp
8	t_{DHWR}	Data hold after $\overline{WR}$ high		0.5		cp
9	t_{DVRL}	Data valid after $\overline{RD}$ low 19.6608 MHz 29.4912 MHz			388 272	ns
10	t_{DVRH}	Data valid setup to $\overline{RD}$ high	20			ns
11	t_{DH}	Data hold after $\overline{RD}$ high	0			ns
12	t_{RD}	Read pulse width		4		cp

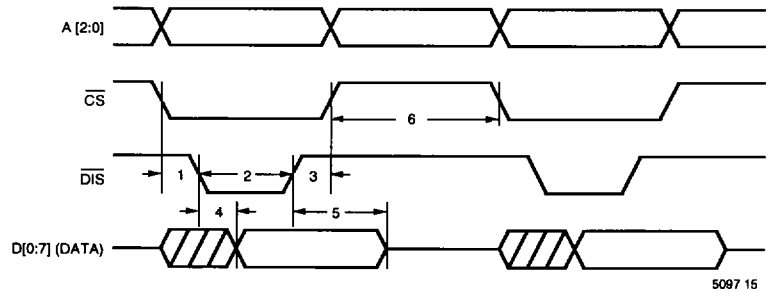
NOTE: CP = 68 ns using 29.4912 MHz crystal

Figure 11. MAP EERAM Read and Write Cycles



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{CSLDIL}	$\overline{CS}$ low to $\overline{DIS}$ low			0	ns
2	t_{DIHCSH}	$\overline{DIS}$ high to $\overline{CS}$ high			0	ns
3	t_{DILRDL}	$\overline{DIS}$ low to RDY low			26	ns
4	t_{RDL}	RDY low time (~5–6CP)	5		6	cp
5	t_{DILDV}	$\overline{DIS}$ low to D valid		2	3	cp
6	t_{DIHDZ}	$\overline{DIS}$ high to D high-Z			20	ns

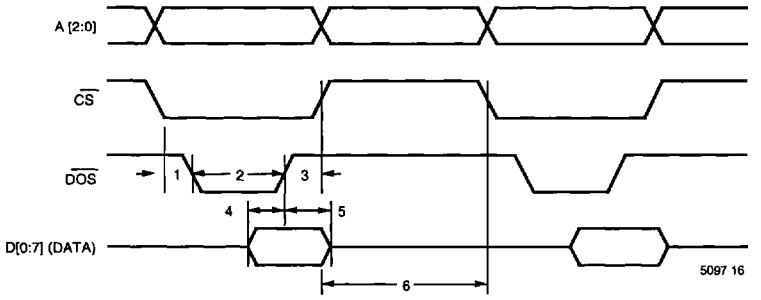
Figure 12. Read Cycle (PC Bus Read From UART Register)



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{CSLDIL}	$\overline{CS}$ low to $\overline{DIS}$ low			0	ns
2	t_{DIS}	$\overline{DIS}$ width	3			cp
3	t_{DIHCSH}	$\overline{DIS}$ high to $\overline{CS}$ high			0	ns
4	t_{DILDV}	$\overline{DIS}$ low to D valid		2		cp
5	t_{DIHDZ}	$\overline{DIS}$ high to high-Z			5	ns
6	t_{CYCRD}	Wait time before next access	2			cp

NOTE: CP is +2 clock

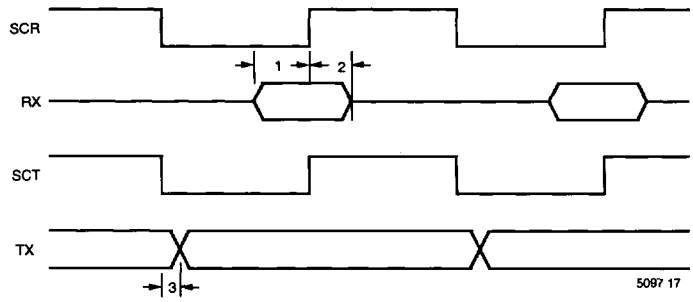
Figure 13. Read Cycle (No RDY pin) (PC Bus Read From UART Register)



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{CSLDOL}	$\overline{CS}$ low to $\overline{DOS}$ low			0	ns
2	t_{DOS}	$\overline{DOS}$ width	3			cp
3	t_{DOHCSH}	$\overline{DOS}$ high to $\overline{CS}$ high			0	ns
4	t_{DSUP}	Data set up time	20			ns
5	t_{DHLD}	Data hold time	10			ns
6	t_{CYCWRD}	Wait time before next access	2			cp

NOTE: CP is internal ÷2 clock

Figure 14. Write Cycle (No RDY pin) (PC Bus Write Into UART Register)



NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{RXSH}	Bit set up time	20			ns
2	t_{RXHD}	Bit hold time	0			ns
3	t_{TXBIT}	XCT low to bit out			30	ns

Figure 15. Single Bit USART Read and Write Timing

TYPICAL APPLICATIONS

The MAC II was designed to perform the DSP and control functions for a wide range of Sierra Modem Advanced Peripherals (MAPs) including Sendfax, Quatro and facsimile data pumps. The SC11043 is specifically aimed at V.42bis applications where the ability to address a full compression dictionary is required. It also provides an expanded ROM address capacity to allow other powerful combinations. As an application specific Controller, the MAC II has several features specific to the Modem functions including hardware echo, V.23 multiplexer and a serial transmit bit register (STBR) to efficiently handle synchronous protocols such as MNP and V.42.

The firmware to support the DSP and Controller functions, including extended AT commands, MNP, V.42bis and T.30 fax handshaking are available from Sierra in modular form for easy maintenance and upgrading. Please contact Sierra for licensing information.

The MAC II interfaces directly with ROM, RAM, EEPROM and MAC. No buffers or latches are required. For send/receive fax and voice applications an external address decoder such as a 74HC139 must be used. 29.4912 MHz crystal operation is a third overtone, parallel resonant type designed for 12pF load and 5.5pF shunt capacitance.

The power on reset circuit is risetime sensitive. In some applications it may be necessary to increase the value of C. With worst case power supply ramp up, the reset signal should rise above the RESET threshold for a minimum of 600µs. During power down mode the LEDs may be shut off by the controller firmware to reduce power.

The bi-directional buffer is required to interface the CMOS controller with standard PC bus. In some applications where the loading is controlled (e.g. Laptops) the buffer may not be needed. Power from the PC should be carefully filtered for optimum performance. Separate digital and analog grounds on the board should be commoned close to the edge connector and decoupling capacitors.

Ferrite beads on the phone line input help to reduce noise input and RF conduction.

Note that the -5V supply is not required with many of Sierra's modem chips. The ±10V supply is for the RS232 drivers.

For optimum performance at low received signal levels with low S/N ratios, it is important to use the recommended power supply decoupling circuit as shown in the figures.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the MAP. A 10Ω, 1/4W resistor in place of, or in series with, the inductor in the MAP power lead has been found to be helpful in computer based products or where the power supply is particularly noisy.

The 10µF capacitors should be a tantalum type while the 0.1µF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the chips as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply.

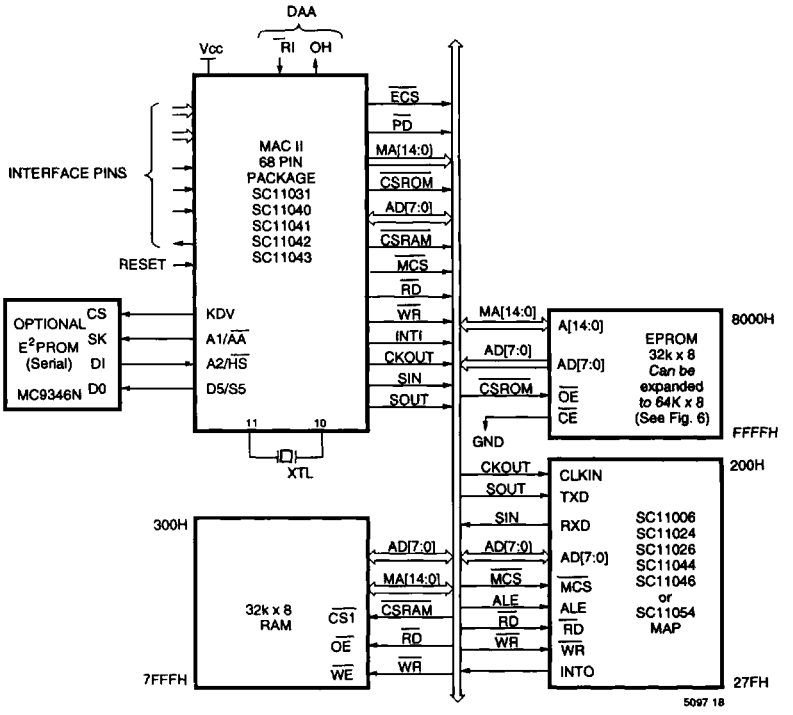


Figure 16. MAC II 68 Pin Package Interfaces to Serial E²PROM, ROM Map for Serial Interface Configurations

THE MAC II AND INTEL 8096 SPEED COMPARISON

The attached is an instruction execution time comparison for the MAC II and Intel 8096. The biggest improvement over 8096 is the 16 bit multiplication; it is 2 μs versus 6.5 μs. The jump instructions are twice as fast. The shift instructions are also about twice faster. The other arithmetic and logic instructions are about the same speed. Indirect addressing instructions in the MAC II is about 20% slower than in the 8096.

The following comparison is for the 8096 with 12 MHz crystal and the MAC II with 29.4912 MHz. The time unit is "μs". The instructions and operands are all from internal storage. Both the MAC II and Intel 8096 will run slower for external storage access.

		DIRECT		IMMEDIATE		INDIRECT	
INSTRUCTION	OPERANDS	MAC II	8096	MAC II	8096	MAC II	8096
ADD	2	.680	1.00	.81	1.25	1.29	1.50
ADD	3	.680	1.25	.81	1.50	1.29	1.75
ADDB	2	.680	1.00	.68	1.00	1.29	1.50
ADDB	3	.680	1.25	.68	1.25	1.29	1.75
AND	2	.680	0.75	.81	1.25	1.29	1.50
AND	3	.680	1.00	.81	1.50	1.29	1.75
ANDB	2	.680	1.00	.68	1.00	1.29	1.50
ANDB	3	.680	1.25	.68	1.25	1.29	1.75
CMP	2	.680	1.00	.81	1.25	1.29	1.50
CMPB	2	.680	1.00	.68	1.00	1.29	1.50
DJNZ		.61/.83	1.25/2.25	(NO JUMP/JUMP)			
EXTB		.47	1.00				
JBC		.68/.88	1.25/2.25				
JBS		.68/.88	1.25/2.25				
JC		.34/.55	1.00/2.00				
JE		.34/.55	1.00/2.00				
JGE		.34/.55	1.00/2.00				
JGT		.34/.55	1.00/2.00				
JH		.34/.55	1.00/2.00				
JLE		.34/.55	1.00/2.00				
JLT		.34/.55	1.00/2.00				
JNC		.34/.55	1.00/2.00				
JNE		.34/.55	1.00/2.00				
JNH		.34/.55	1.00/2.00				
JNV		.34/.55	1.00/2.00				
JV		.34/.55	1.00/2.00				
LCALL		.75	3.25				
LD	2	.68	1.00	.81	1.25	1.29	1.50
LDB	2	.68	1.00	.68	1.00	1.29	1.50
LJMP	1	.61	2.00	.68	1.00	1.29	1.50
MUL	3	2.24	6.50	(BIGGEST IMPROVEMENT)			
NOP		.16	1.00				
OR	2	.68	1.00	.81	1.25	1.29	1.50
ORB	2	.68	1.00	.68	1.00	1.29	1.50
PUSHF		.34	2.00				
POPF		.34	2.25				
RET		.68	3.00				
SHL		.75+0.66N	1.75+0.25N	(N = SHIFT COUNT)			
SHLB		.75+0.66N	1.75+0.25N				
SHLL		1.02+0.66N	1.75+0.25N				
SHR		.75+0.66N	1.75+0.25N				
SHRB		.75+0.66N	1.75+0.25N				
SHRL		1.02+0.66N	1.75+0.25N				
SHRA		.68+0.66N	1.75+0.25N				
SHRAL		1.02+0.66N	1.75+0.25N				
SJMP		.47	2.00				
ST		.88	1.75				
STB		.88	1.75				
SUB	2	.68	1.00	.81	1.25	1.29	1.50
SUBB	2	.68	1.00	.68	1.00	1.29	1.50
SUB	3	.68	1.25	.81	1.50	1.29	1.75
SUBB	3	.68	1.25	.68	1.25	1.29	1.75
XOR	2	.68	1.00	.81	1.25	1.29	1.50
XORB	2	.68	1.00	.68	1.00	1.29	1.50